Self-Powered Isolated Comparator

OBSOLETE PRODUCT
DATA SHEET FOR REFERENCE ONLY
Consult www.linear.com for possible alternate source.

FEATURES

- **UL Recognized File E151738 to UL1577**
- **Self-Powered Across Isolation Barrier**
- **2500V_{RMS} Isolation**
- **2.5V Isolated Reference, I_{LOAD} = 5mA_{MAX}**
- Zero-Cross Output for Line Power
- Dual Differential Input Comparator
- High Input Impedance Comparator

APPLICATIONS

- Self-Powered Isolated Sensing
- Isolated Temperature Control
- Isolated Voltage Monitor
- Isolated Switch Control

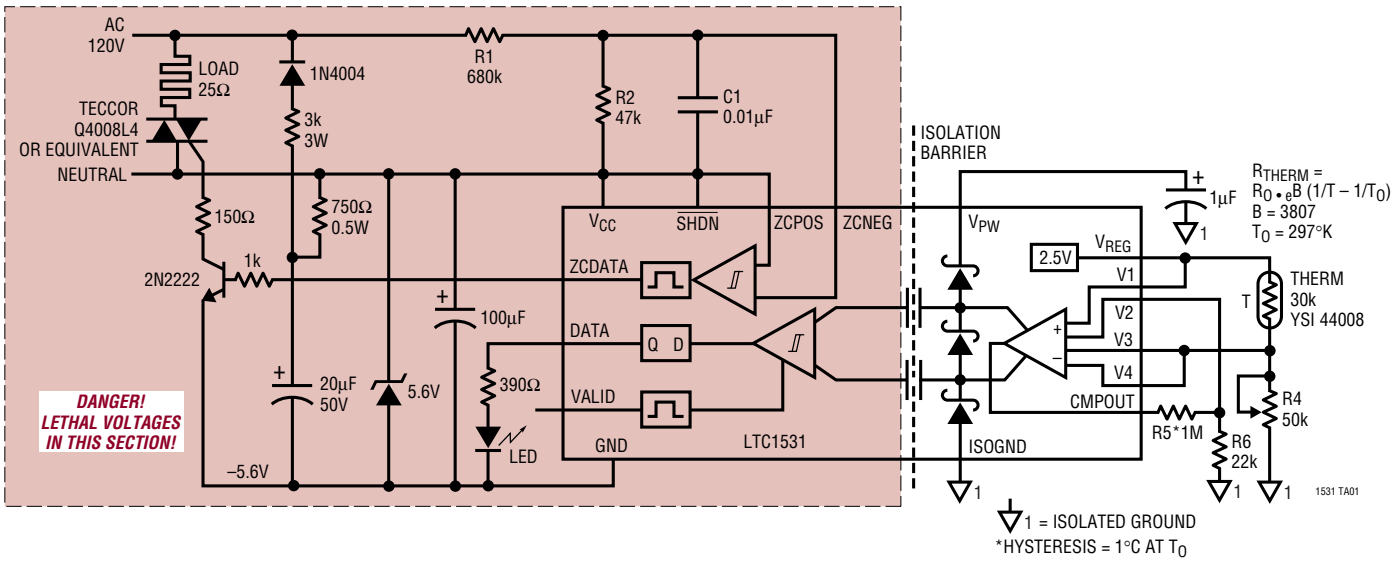
DESCRIPTION

The LTC®1531 is an isolated self-powered dual differential comparator. An internal capacitive isolation barrier provides 2500V_{RMS} of isolation between the comparator and its output. The part provides UL-rated isolated comparisons without the need for an isolated supply since both comparator power and output data are transmitted across the capacitive barrier. The comparator data is transferred differentially across the isolation barrier to provide high common mode voltage and noise immunity.

The isolated side can supply a 2.5V reference output to power external sensor circuits such as a thermistor bridge. The dual differential comparator inputs allow for comparison of two differential voltages as well as single-ended voltages. The powered side provides a latched data output as well as a pulsed zero-cross comparator output for controlling a triac. The part is available in a 28-lead SO package.

TYPICAL APPLICATION

Isolated Thermistor Temperature Controller

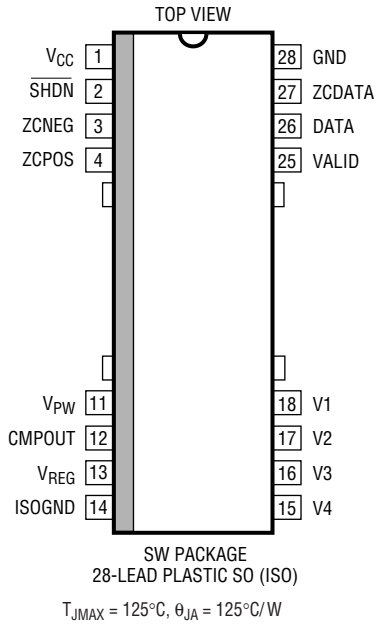


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC} to GND) 7V
Input Voltages
  Isolated Comparator
  (V1 to V4) ..... –0.3V to (V_{PW} + 0.3V)
  $\overline{SHDN}$, ZCPOS, ZCNEG ..... –0.3V to 12V
Current
  Input Pins ..... ±10mA
  ZCDATA, VALID, DATA ..... ±10mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



SW PACKAGE
28-LEAD PLASTIC SO (ISO)

T_{JMAX} = 125°C, θ_{JA} = 125°C/W

ORDER PART NUMBER
LTC1531CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C, V_{CC} = 5V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VCC}	Supply Current	$\overline{SHDN}$ = V_{CC}, No Load $\overline{SHDN}$ = 0V	● ●		10 0.2	14 10	mA µA
V_{ZCOS}	Zero-Cross Offset	V_{CM} = V_{CC}	●		±30	±120	mV
V_{HYS}	Zero-Cross Hysteresis	V_{CM} = V_{CC} (Note 7)	●		200	800	mV
f_{SAMPLE}	Isolated Comparator Sample Rate	V_{REG} Not Loaded (Note 2)			300		Hz
V_{OS}	Isolated Comparator Offset	V1 = V2, V3 = V4 V1 – V3 = 2V, V4 – V2 = 2V	● ●		2.0 2.0	4.0 4.0	mV mV
R_{VIN}	Isolated Comparator Input Impedance	V1 = V3 = 2.5V, V2 = V4 = 0V V1 = V2 = 1.25V, V3 = V4 = 0V			18 300		MΩ MΩ
I_{VIN}	Isolated Comparator Input Current	V1 = V3 – 2.5V, V2 = V4 = 0V f_{SAMPLE} = 700Hz (Note 4)			±1		nA
V_{REG}	V_{REG}	2mA Load V_{PW} = 3.3V (Note 5)	●	2.40	2.50	2.55	V
R_{VREG}	V_{REG} Output Impedance	2mA to 5mA Load	●		4	15	Ω
I_{CMPOUT}	CMPOUT High Impedance Leakage Current	V_{CMPOUT} = 2.5V			1		nA
t_{VREG}	V_{REG} On-Time		●	90	108	130	µs
V_{PWH}	V_{PW}, Power Detect Enable Voltage				3.3		V
I_{VPW}	Current Transfer to V_{PW}	V_{PW} = 0V V_{PW} = 3.3V			45 30		µA µA
V_{ISO}	Isolation Voltage	1 Minute (Note 6) 1 Second	● ●	2500 4500			V_{RMS} V_{DC}

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C, V_{CC} = 5V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	$\overline{SHDN}$ Input High Voltage	V_{CC} = 4.5V	●	2.4			V
V_{IL}	$\overline{SHDN}$ Input Low Voltage	V_{CC} = 5.5V	●			0.8	V
V_{OH}	DATA, VALID, ZCDATA Output High Voltage	V_{CC} = 4.5V, I_O = –400µA	●	3.0	4.3		V
V_{OL}	DATA, VALID, ZCDATA Output Low Voltage	V_{CC} = 4.5V, I_O = 1.6mA	●		0.2	0.4	V
I_{INL}, I_{INH}	$\overline{SHDN}$ Low or High Level Input Current	V_{IN} = 5V, 0V	●			±1	µA
dV/dt	Continuous dV/dt Rejection	(Note 8)	●	50	70		V/µs
C_{ISO}					2		pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The sample rate is not continuous, but depends on V_{PW} charging rate. See Applications Information.

Note 3: See Applications Information for further description of the comparator switched-capacitor input circuit.

Note 4: The sample rate, f_{SAMPLE}, varies with loading on V_{PW} and V_{REG}.

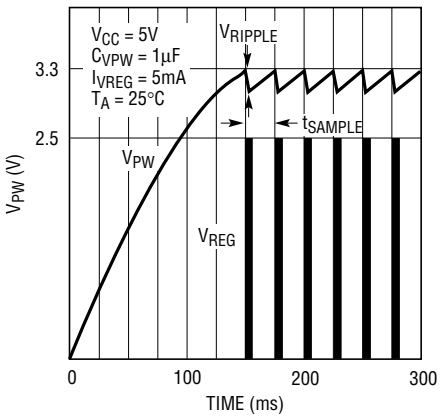
Note 5: Load on CMPOUT pulls current from V_{REG} when CMPOUT is high.

Note 6: Value derived from 1 second test.

Note 7: Zero-cross hysteresis is the minimum amount of signal amplitude above or below 0V differential to retrigger the zero-cross comparator.

Note 8: Parameter not tested but guaranteed by design.

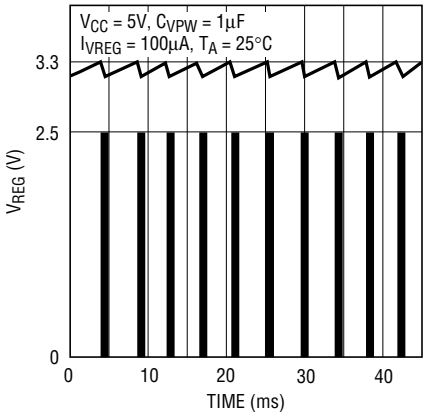
TYPICAL PERFORMANCE CHARACTERISTICS



NOTES: V_{RIPPLE} DEPENDS ON C_{VPW} AND I_{VPW} + I_{VREG}
t_{SAMPLE} DEPENDS ON I_{VPW} + I_{VREG}

1531 F01

Figure 1. V_{PW} Power-Up and V_{REG} Samples vs Time



NOTE: NONPERIODIC SAMPLES DUE TO DEPENDENCE ON V_{PW} > 3.3V AND THE POWER-LISTEN CYCLE SAMPLING

1531 F02

Figure 2. V_{REG} and V_{PW} vs Time (I_{VREG} = 100µA)

TYPICAL PERFORMANCE CHARACTERISTICS

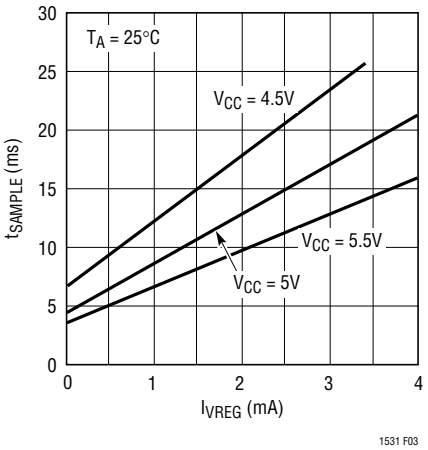


Figure 3. Average t_{SAMPLE} vs I_{VREG}

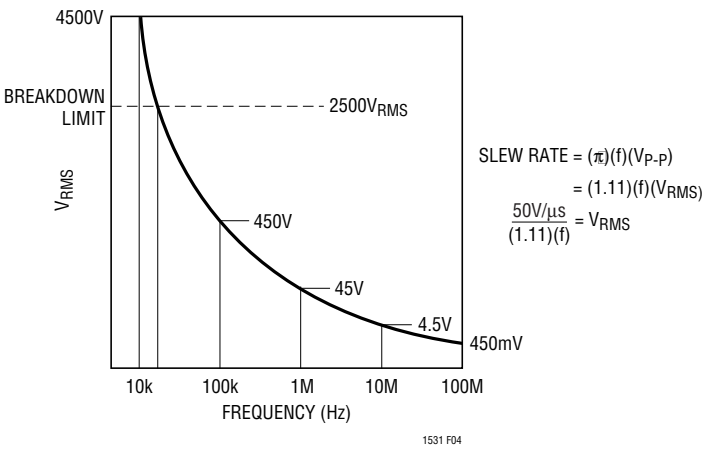


Figure 4. V_{RMS} vs Frequency

PIN FUNCTIONS

V_{CC} (Pin 1): Powered Side Power Supply.

$\overline{SHDN}$ (Pin 2): Active Low Chip Shutdown. A low signal causes the circuitry to power down. DATA logic output level will be reset to zero during power-down.

ZCNEG (Pin 3): Zero-Cross Comparator Negative Input.

ZCPOS (Pin 4): Zero-Cross Comparator Positive Input.

V_{PW} (Pin 11): Isolated Power Supply. Connect to an external storage capacitor.

CMPOUT (Pin 12): Isolated Latched Comparator Data. CMPOUT is active when V_{REG} is on. The CMPOUT output can be used on the isolated side for hysteresis (see applications). The output will contain the result of the previous comparison. When V_{REG} is low, the CMPOUT pin is Hi-Z.

V_{REG} (Pin 13): Isolated 2.5V Regulated Output. Pulsed on for 100µs with a maximum load current of 5mA. V_{REG} also supplies power to the CMPOUT output (Pin 12).

ISOGND (Pin 14): Isolated Side Power Ground.

V4 (Pin 15): Comparator Negative Input. The comparator inputs are summed together with the comparison output equal to (V1 + V2)/2 > (V3 + V4)/2 or equivalently (V1 – V3) > (V4 – V2).

V3 (Pin 16): Comparator Negative Input.

V2 (Pin 17): Comparator Positive Input.

V1 (Pin 18): Comparator Positive Input.

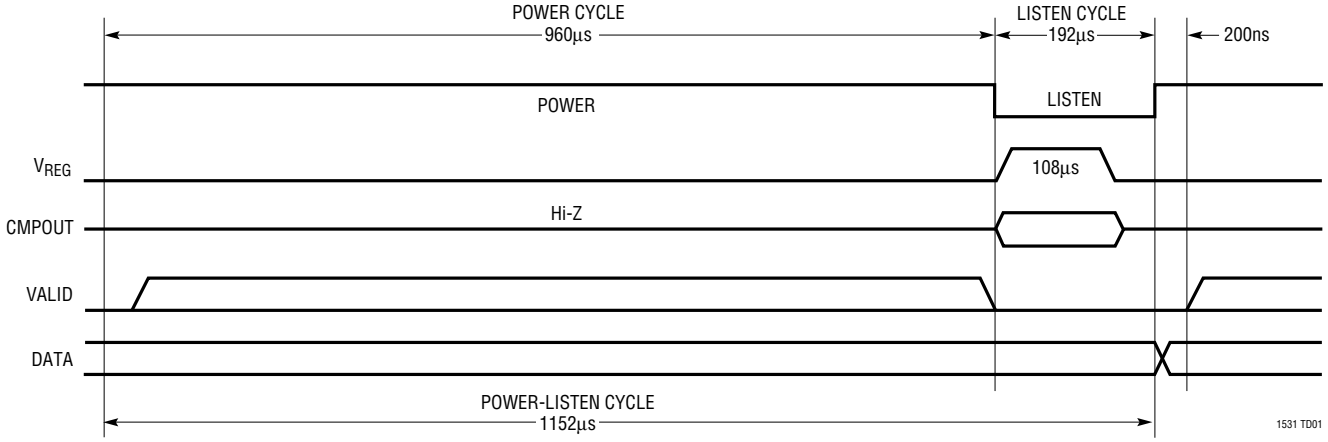
VALID (Pin 25): Pulsed Output. Indicates when valid data was received from the comparator. May be used to clock DATA to external circuitry.

DATA (Pin 26): Latched Comparator Result. DATA holds the value of the last valid comparison result. DATA changes only when a valid comparison was received from the isolated side.

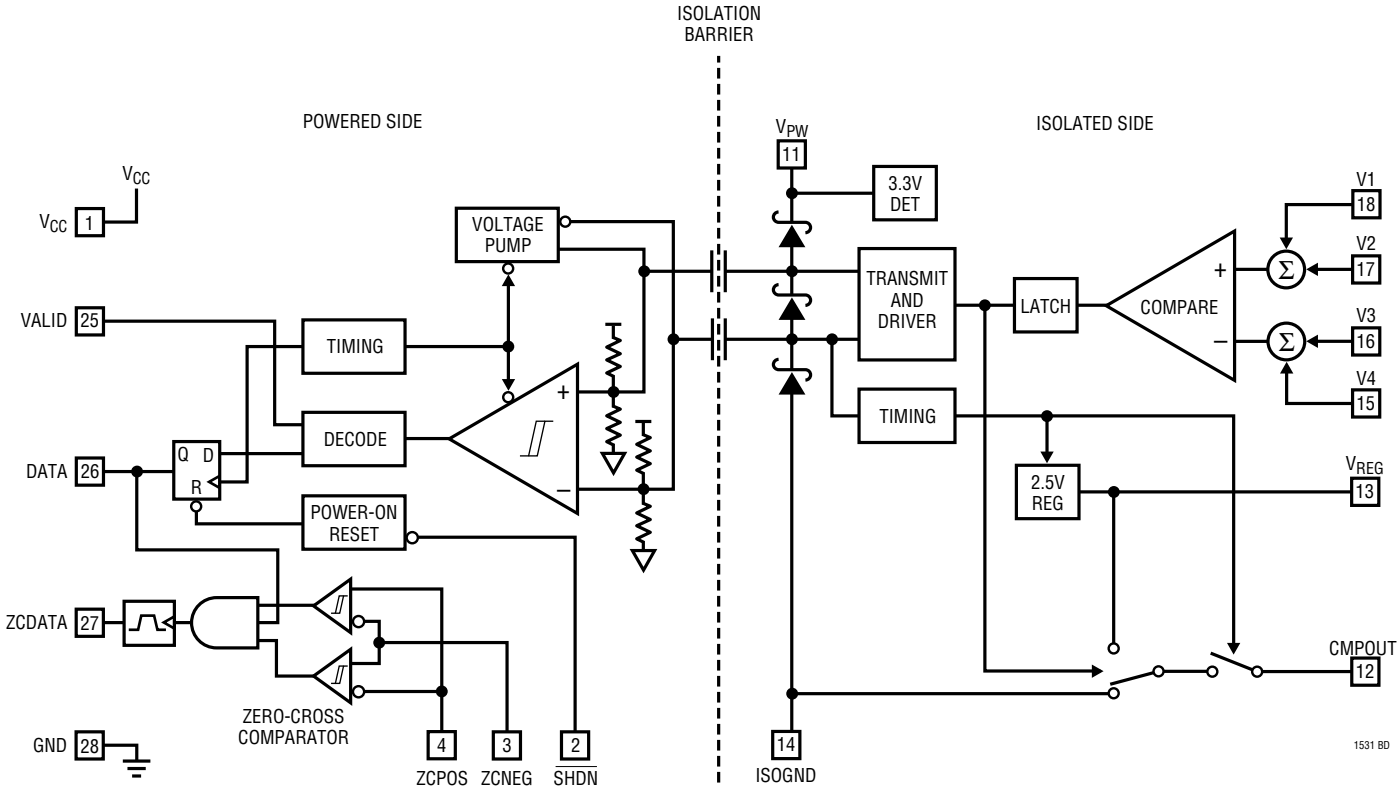
ZCDATA (Pin 27): A 24µs to 30µs Pulsed Output. The pulse occurs when the DATA output is high and the zero-cross comparator inputs (ZCPLS-ZCNEG) cross zero volts differential. Typically the zero-cross input signal is an RC phase shifted AC sine wave. This output is a TTL level pulse that can be used for firing an external triac.

GND (Pin 28): Power Supply Low Impedance Ground Connection.

TIMING DIAGRAM



BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC1531 is an isolated self-powered dual differential comparator. It contains a switched-capacitor comparator that is self-powered through a capacitive isolation barrier. The capacitive isolation barrier provides $2500V_{RMS}$ of isolation. The isolated comparator cycles between storing power and performing sampled comparisons. During the power delivery cycle, the nonisolated powered side delivers power through the internal isolation capacitors and rectifier onto an external storage capacitor. Periodically the isolated comparator makes a comparison if sufficient voltage has been stored on the external supply capacitor. See Timing and Block Diagrams.

During a comparison, the isolated side uses the energy stored on the external capacitor to deliver a regulated 2.5V power source for 108µs followed by a sampled comparison. The result is transmitted back to the nonisolated powered side and latched as the logic level DATA output. A comparison will occur during the listen cycle if sufficient voltage (3.3V) has been stored on the isolated external capacitor. New DATA is latched only if a comparison was actually done. A zero-crossing trigger pulse output for firing a triac, ZCDATA, is available to trigger a triac when the latched DATA output is high. A VALID data output pulse is provided after each power-listen cycle in which a comparison was done to indicate that DATA has been updated. The VALID output can be used to clock external circuitry when a new comparator DATA value occurs.

POWER-LISTEN CYCLE

Self-Powering Through the Isolation Barrier

The LTC1531 comparator powered side toggles between delivering power to the isolated side and listening for a comparison result (see Timing Diagram). During the power cycle, AC power is delivered through the isolation capacitors, formed in the lead frame, to the isolated side. During the listen cycle, the powered side receives pulses from the isolated side and determines if a valid comparison occurred.

The isolated side of the LTC1531 requires an external capacitor connected to V_{PW} whose value must be large enough to sustain less than a 300mV drop for 108µs with the internal + external V_{REG} load current. Power is delivered to this external capacitor through the internal isolation capacitors and rectifiers during the power cycle. When this voltage reaches approximately 3.3V, the compare circuitry is enabled and a comparison will occur during the next listen cycle. With V_{CC} = 5V, this capacitive coupled isolated power source can be modeled as an equivalent 5.3V to 6.5V source with a 100kΩ source impedance. The V_{PW} pin will tend to self-regulate at 3.3V with a ripple determined by the discharge current supplied during the 108µs V_{REG} output pulse and the external capacitor value. The value of the capacitor affects the initial start-up time and the ripple voltage on V_{PW}, but it does not influence the sample rate of the comparator. This is because the sample rate is determined by the rate of power delivered through the isolation barrier and the rate it is consumed in the internal plus external isolated circuits.

Any excessive external DC loading on V_{PW} may prevent the capacitor voltage from reaching the required 3.3V enable voltage. Up to 20µA of continuous loading on V_{PW} can be tolerated based on the 100k, 5.3V model of the power source (see Typical Applications for examples). The quiescent current of the isolated side is approximately 2µA to 3µA.

SAMPLE RATE

The comparator sample rate depends on the charging rate through the isolated capacitors and the external + internal load current . The power-listen cycles at 700Hz to 900Hz, however, a comparison will only occur when V_{PW} exceeds the 3.3V enable voltage. Typical sample rate for light loading is 200Hz to 300Hz. The actual sampling is not uniform, but occurs during the listen period of the power cycle and when $V_{PW} \geq 3.3V$. Typical sample rates for various supply and load conditions are plotted in Figure 3. Continuous micropower loads will also decrease the sample rate.

V_{REG} Reference Output

The V_{REG} reference output pulses on for approximately 108µs at 2.5V. During the off time, V_{REG} does not go high impedance. The V_{REG} output stage is shown in Figure 5. Large capacitance should not be attached to V_{REG} in order to avoid power loss. Charging of the V_{REG} output capaci-

APPLICATIONS INFORMATION

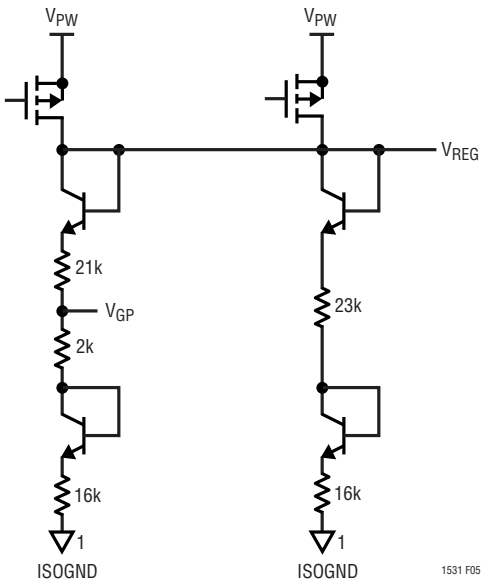


Figure 5. V_{REG} Output Stage

tance, which will subsequently be discharged between samples, will consume power from V_{PW}.

ISOLATED COMPARATOR INPUTS AND CMPOUT

The LTC1531 isolated comparator has a 4-input summing comparator that performs the following comparison:

$(V1 + V2)/2 > (V3 + V4)/2$

By rearranging the equation, for example, a dual differential comparison is performed:

$(V1 – V4) > (V3 – V2)$ or $(V1 – V3) > (V4 – V2)$

The input has a rail-to-rail input and common mode voltage range of V_{PW}-ISOGND. The summing nature of the inputs allows midsupply referencing. For example, connecting V3 to V_{REG} and V4 to ISOGND sums together to provide $V_{REG}/2$ for the negative comparator input. See for example, the Isolated Switch Control.

Charge injection and leakage currents occur at the comparator inputs. The amount depends on how the comparator is used. Minimum leakage currents occur with V1 = V2 and V3 = V4 where the input impedance is from charge injection and is nominally 300MΩ. When V1 ≠ V2 or V3 ≠ V4, the input impedance due to leakage currents is about 15MΩ to 20MΩ. Since the comparator is turned on only for the last 10µs of the 108µs V_{REG} period, the charge injection occurs at about the 98µs point with a coupling capacitance of 2pF per input.

The CMPOUT signal is typically used to provide hysteresis, as in the Isolated Temperature Control application. CMPOUT is the latched result of the previous comparison and is active during the following V_{REG} ON period. CMPOUT is powered by V_{REG}, the internal 2.5V regulated output, and is in high impedance except during the 108µs V_{REG} ON time. When active, CMPOUT is switched low to ISOGND or high to V_{REG} depending on the stored result of the previous comparison. The stored CMPOUT data is reset during power-up. CMPOUT is not necessarily reset by the powered side $\overline{SHDN}$ pin, except when shutdown results in V_{PW} drooping low enough to trigger a power-on reset on the isolated side between 1.5V to 2.5V.

DATA, VALID, ZCDATA

During a power cycle, the VALID signal goes high if a valid comparison was made during the previous listen cycle. VALID goes low at the beginning of the next listen cycle. The low-to-high transition of VALID can be used to clock DATA into external circuitry. VALID is delayed 200ns after the DATA output. In order for a comparison to occur, sufficient power must be stored on the isolated side storage capacitor.

The DATA output holds the last received compare result. DATA is reset to zero on power-up and shutdown. The VALID output is held high for one power cycle following a correctly received compare result. The received DATA value from the isolated side contains redundancy to improve noise immunity.

The ZCDATA is a 25µs output pulse triggered by the zero-cross comparator. In order for a pulse to occur, the DATA output must be at logic 1 and the ZCPOS-ZCNEG zero-cross comparator input crosses 0V after the input has exceeded the ±150mV to 800mV of hysteresis. The zero-cross comparator output is typically used to trigger a triac from a 60Hz RC phase shifted AC line signal. See Typical Applications.

APPLICATIONS INFORMATION

The zero-cross comparator inputs, ZCPOS and ZCNEG, have an input common mode range that allows signal swings near the positive supply rails. The ZCPOS and ZCNEG inputs contain ESD diode protection devices which will clamp input signals that go below GND. The current into the diode should be limited to less than 5mA. The Isolated Thermistor Temperature Controller shows an example phase shift network with attenuation that satisfies these conditions. The positive input voltage should not exceed the 12V maximum rating or the 5mA input current to the ESD diode clamp.

ISOLATION dV/dt

The maximum continuous dV/dt across the isolation barrier that will still allow the isolated comparator to operate is 50V/μs. Continuous rates of dV/dt greater than this cause the isolated side to not detect when its power cycle has stopped and a comparison should begin. Figure 4 shows the maximum continuous rate trade-off of frequency vs voltage of a sine wave:

$$SR = (\pi)(f)(V_{P-P})$$

where SR = slew rate, V_{P-P} = the peak-to-peak voltage and f = frequency. Noise immunity to intermittent dV/dt rates greater than 50V/μs can be rejected by the LTC1531.

AC Noise Rejection and Things to Avoid

Minimizing AC noise pickup at the isolated comparator should follow the following guidelines.

1. Allow the isolated side ground to float. The isolated side should only be common with the isolated circuit.
2. Use hysteresis to decrease sensitivity by using CMPOUT.
3. Use lower impedance circuits if powered by V_{REG}. Avoid large capacitance tied directly to V_{REG} output, since this output does not go Hi-Z (high impedance) during the off time.

PC Board Layout

The PC board layout should not have copper near the lead frame isolation capacitors. The copper reduces the power coupling and power delivery to the isolated side (see Figure 6).

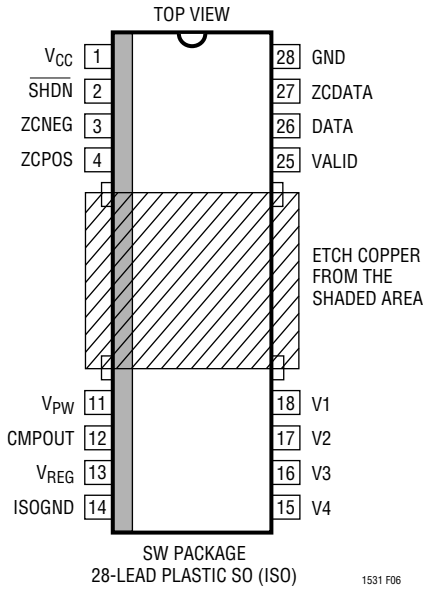


Figure 6. PC Board Layout Consideration

TYPICAL APPLICATIONS DESCRIPTION

The Isolated Thermistor Temperature Controller (front page) uses a simple AC power rectifier and Zener to provide 5.6V of DC power to the LTC1531. To avoid power dissipation in the 3k, 3W resistor, DC power can be provided with a charge pump circuit similar to the Isolated Switch Control. In this circuit, a thermistor half bridge is used with the 4-input comparator connected to provide the other half of the bridge, V4 = 2.5V, V3 = 0V, giving (V4 + V3)/2 = 1.25V. With the 50k pot set to about 30k, the trip point is 25°C with a hysteresis of ±0.5°C. Here, V_{REG} turns on and powers the half-bridge while the comparator samples the result. The zero-cross comparator, ZCPOS and ZCNEG, is used to trigger a triac at the 10° phase point. The circuit, R1, R2 and C1, provides the phase shift, θ, as determined by:

$$R2C1 \cong \tan(\theta)/2\pi 60Hz$$

and where the attenuation ≅ R2/R1. In this example, R1 = 680k, R2 = 47k and C1 = 0.01μF, provide a 7V peak input signal with 10° of phase lag.

APPLICATIONS INFORMATION

The Remote Light-Controlled Switch (Figure 7) is similar to the Isolated Thermistor Temperature Controller. The thermistor is replaced with a Cadmium Light Sensor.

The Isolated Switch Control (Figure 8) is also similar, where a low voltage switch is isolated from the AC power control. Here, a charge pump using the 1µF nonpolar capacitor and diodes are used for powering the LTC1531.

The Isolated Voltage Sense circuit (Figure 9) uses the three-state CMPOUT pin in a delta-sigma configuration. Here, the time constant of R1C1 is increased by the effective duty cycle of CMPOUT ON to OFF time. At a 300Hz sample rate and a typical ON time of 108µs, the time constant is:

$(1M \bullet 0.22\mu F)/(300Hz \bullet 108\mu s) \approx 6.6sec$

The input range is 0V to 2.5V set by the V_{REG} output voltage. The output is recovered using a rail-to-rail op amp, LT1490, averaging circuit with a 10sec time constant. The output range is 0V to V_{CC} output for a 0V to V_{REG} input range.

The Isolated Potentiometer Transducer Sense circuit (Figure 10) uses the same principle as the Isolated Voltage Sense circuit to provide a 0V to V_{CC} output proportional to the potentiometer sensor input.

The Isolated Thermocouple Voltage circuit (Figure 11) again uses the delta-sigma approach to translate a thermocouple temperature into a 0V to V_{CC} output. Additionally, a micropower op amp, the LT1495, is used to provide a continuous voltage amplification of the thermocouple. The LT1389 with the thermistor bridge provides cold junction compensation over a 0°C to 60°C temperature range within ±0.5°C. The op amp gain is set to give the K-type thermocouple a 0°C to 200°C range which translates to a 0V to V_{CC} output signal. Reducing R3 will increase the temperature sensing range.

The Over Temperature Detect circuit (Figure 12) uses the same continuous micropower cold junction compensation circuit as in the Isolated Thermocouple Voltage circuit. In this case, the comparator's minus input is set to 1.25V, which corresponds to 100°C as set by the LT1495 op amp gain. When the thermocouple exceeds 100°C, V_{TRIP} goes high.

The Isolated Battery Cell Monitor circuit (Figure 13) uses LTC1531 isolation to both float the individual grounds on the isolated comparator and isolate the battery from the logic outputs, CELL1, CELL2, ... In this application, R1 and R2 (R3 and R4) divide the 2.5V reference down to 0.89V, while the cell voltage is divided in half by connecting V1 to the cell and V2 to 0V. Hence, when the cell voltage drops below 1.786V, CELL1 goes high. Likewise for additional cells with additional LTC1531s.

The Isolated Window Comparator circuit (Figure 14) uses two LTC1531s and a logic gate to provide isolated window comparisons. In this circuit, the first LTC1531, V_{HIGH}, does the comparison:

$V1 - V3 > V4 - V2$

or

$(0V - X \bullet V_{REG}) > (V_{IN}^- - V_{IN}^+)$

or

$X \bullet V_{REG} < (V_{IN}^+ - V_{IN}^-)$

where $X = R2/(R2 + R1)$.

The second LTC1531, V_{LOW}, does the comparison:

$(-X \bullet V_{REG}) > (V_{IN}^+ - V_{IN}^-)$

When $(V_{IN}^+ - V_{IN}^-)$ is less than $-X \bullet V_{REG}$, V_{LOW} goes high and when $(V_{IN}^+ - V_{IN}^-)$ is greater than $X \bullet V_{REG}$, V_{HIGH} goes high. In between $-X \bullet V_{REG}$ and $+X \bullet V_{REG}$, V_{WINDOW} is high. Therefore, the window width is $2 \bullet X \bullet V_{REG}$.

The AC Line Overcurrent Detect circuit (Figure 15) uses the micropower op amps, the quad LTC1496, to peak detect the voltage across a sense resistor in series with an AC load. The two amplifiers connected to R_{SENSE} act as half-wave rectifiers because their outputs cannot swing below ground. The gain is set to trip when the voltage on R_{SENSE} exceeds 125mV and the minus comparator input is set to 1.25V. The peak detector has a discharge resistor of 1M plus the op amp input bias current.

TYPICAL APPLICATIONS

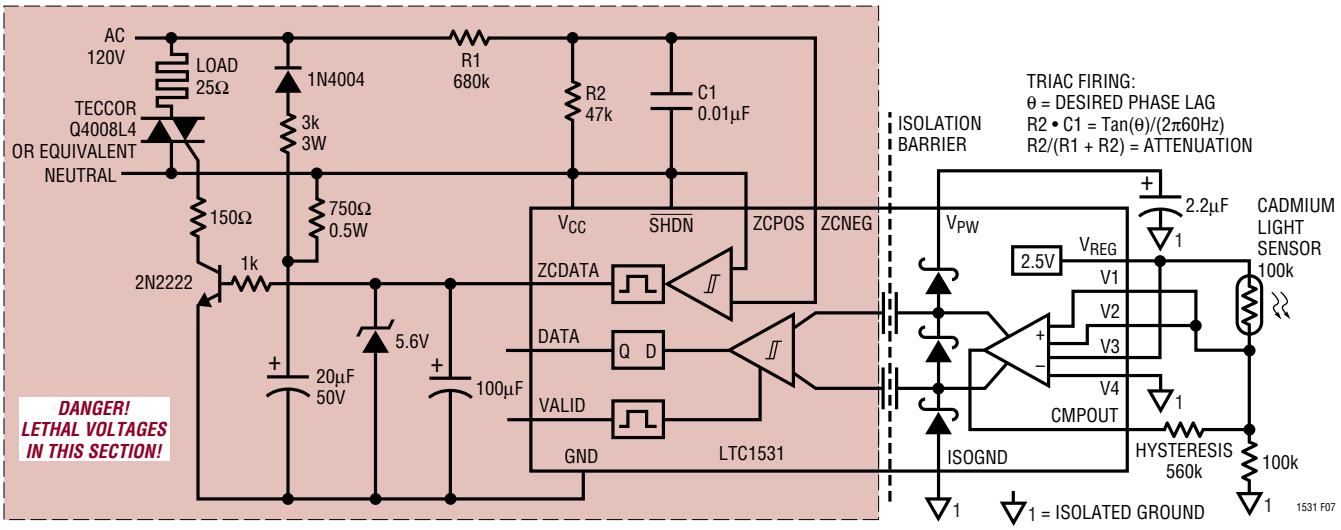


Figure 7. Remote Light-Controlled Switch

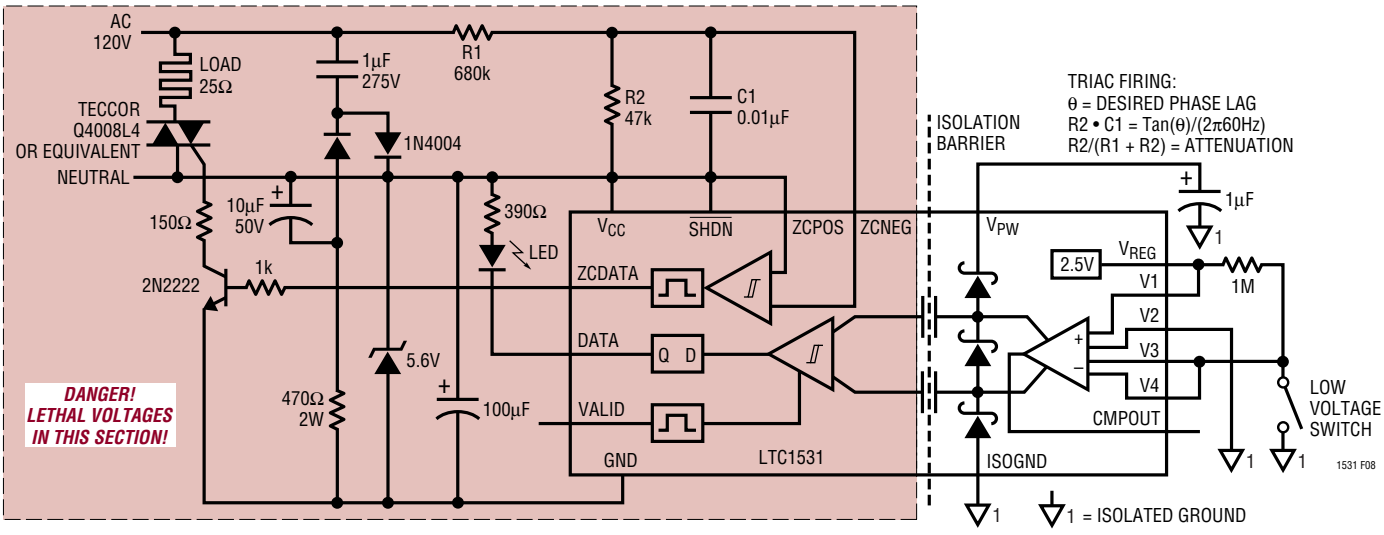


Figure 8. Isolated Switch Control

TYPICAL APPLICATIONS

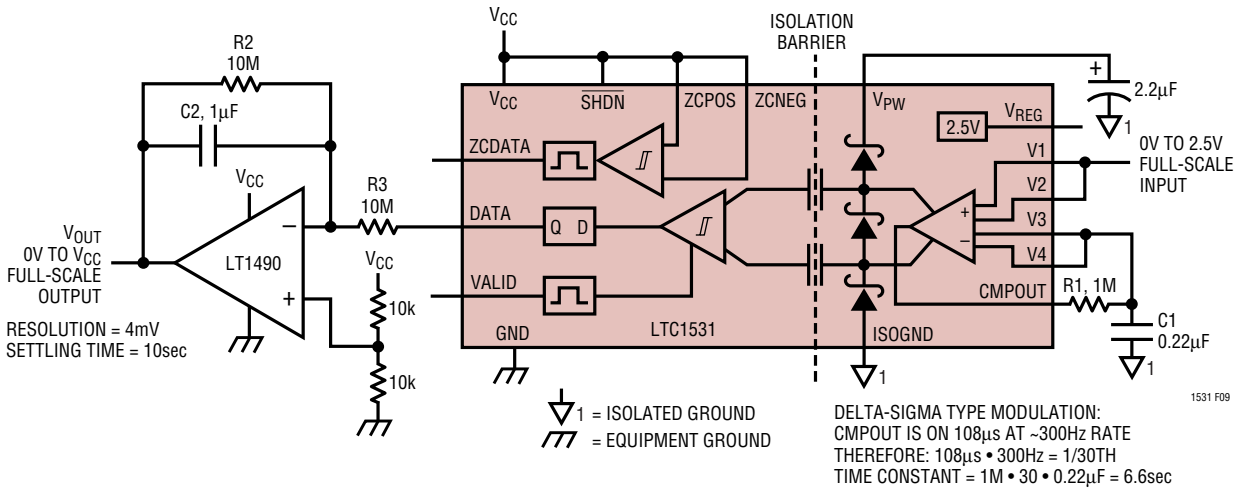


Figure 9. Isolated Voltage Sense

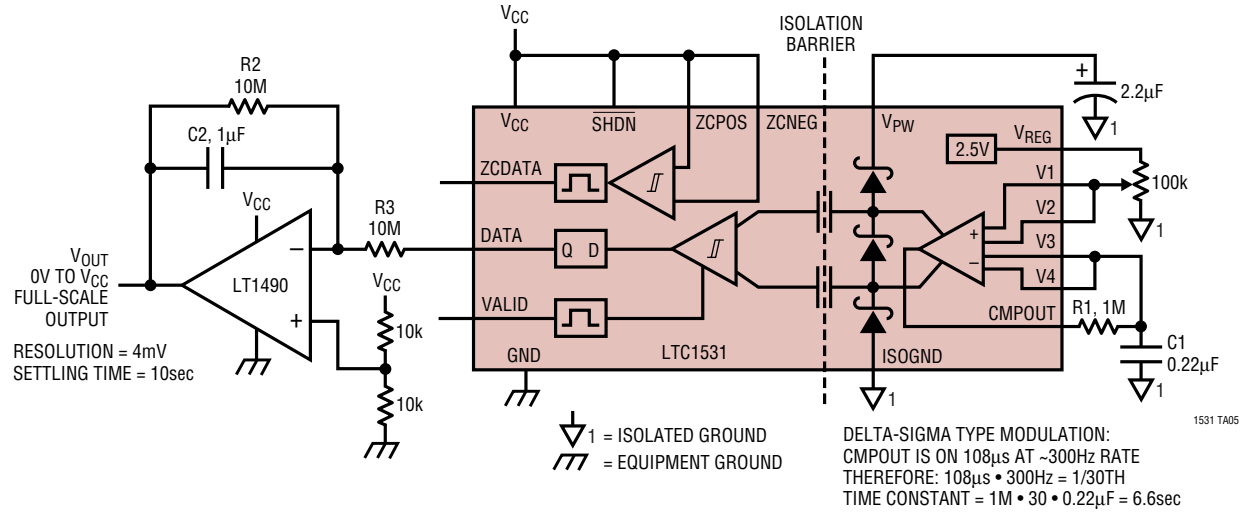


Figure 10. Isolated Potentiometer Transducer Sense

TYPICAL APPLICATIONS

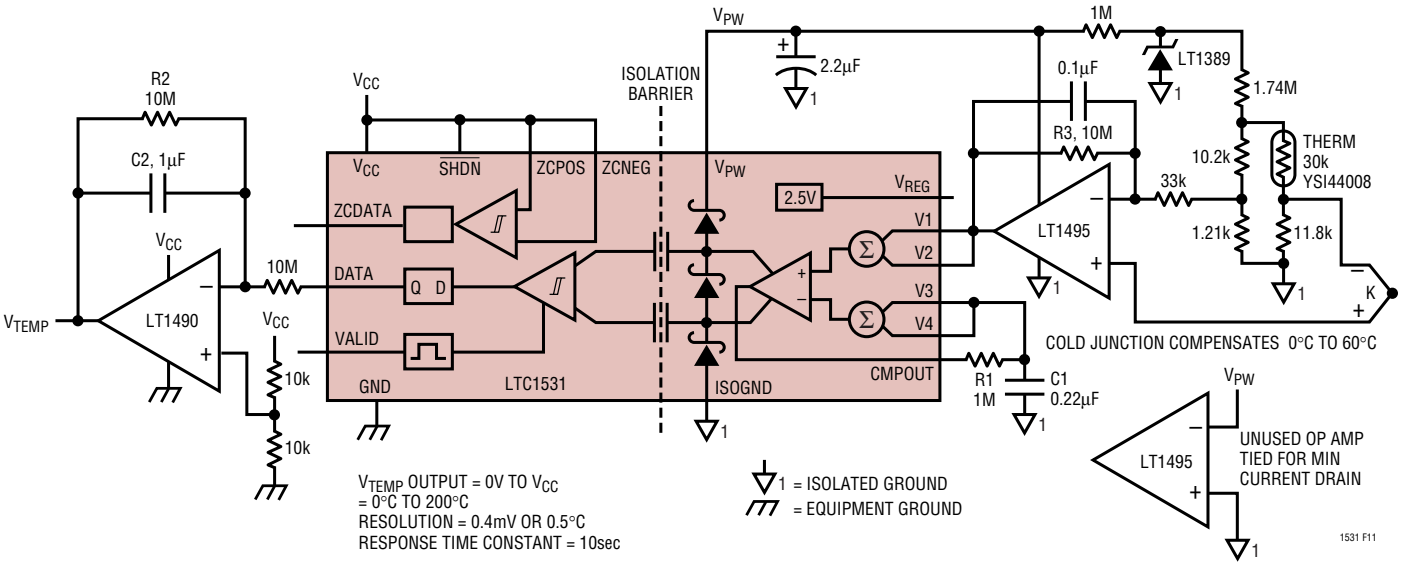


Figure 11. Isolated Thermocouple Voltage

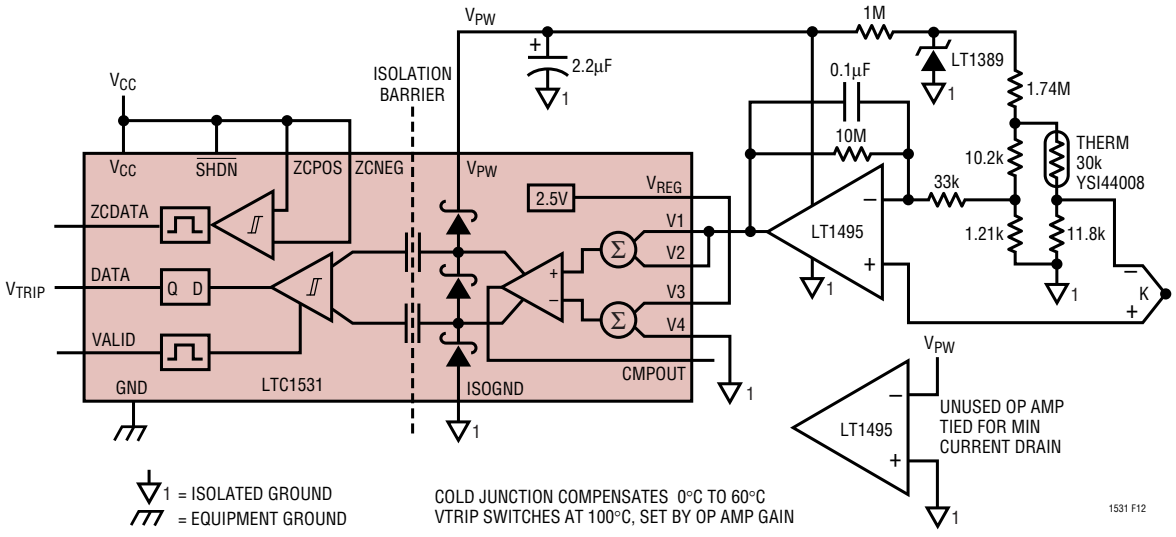


Figure 12. Over Temperature Detect

TYPICAL APPLICATIONS

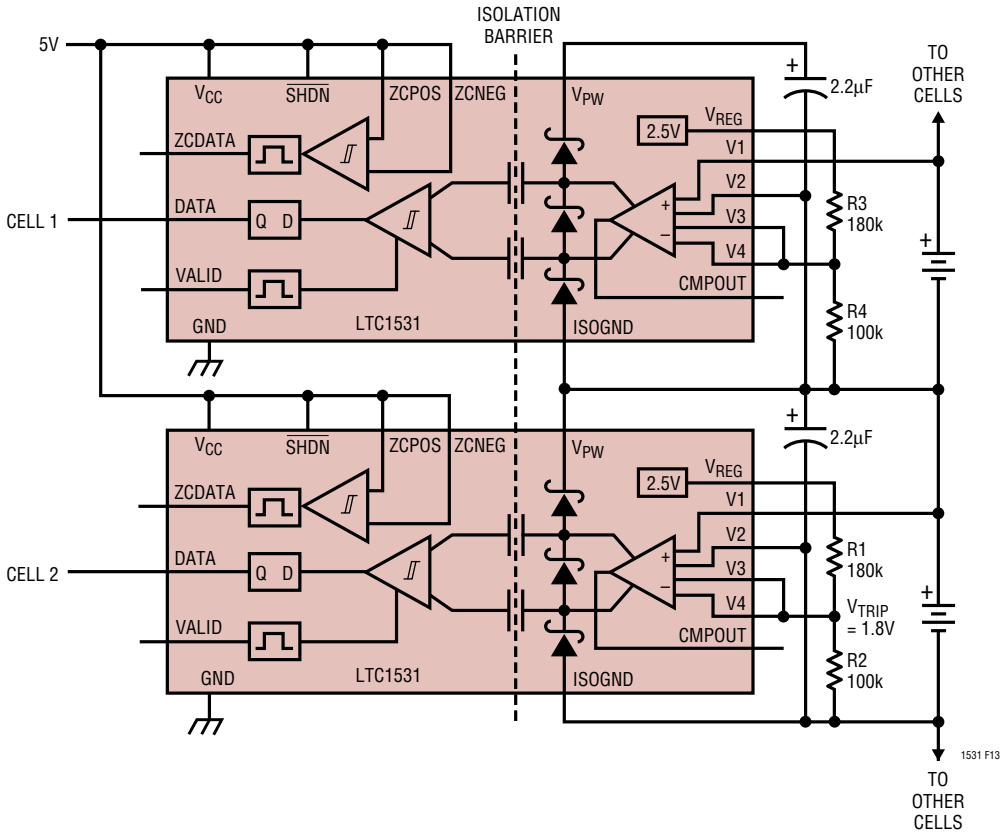


Figure 13. Isolated Battery Cell Monitor

TYPICAL APPLICATIONS

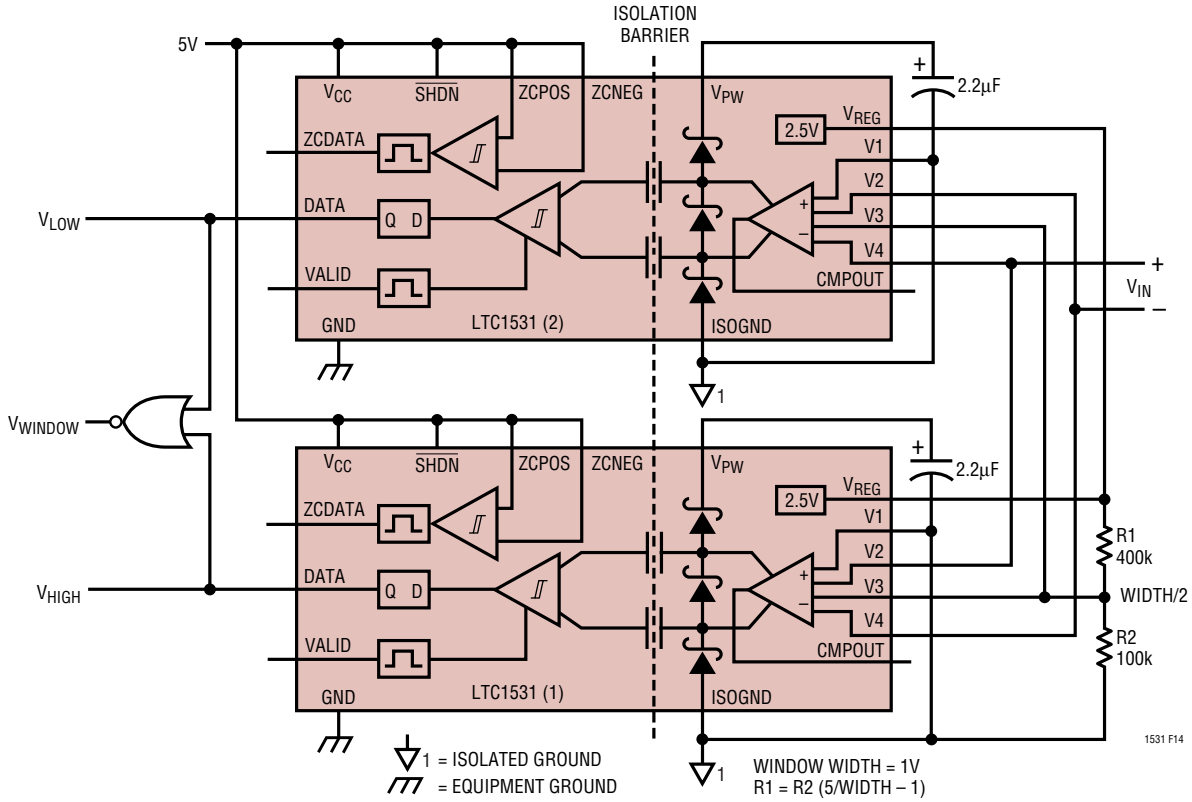
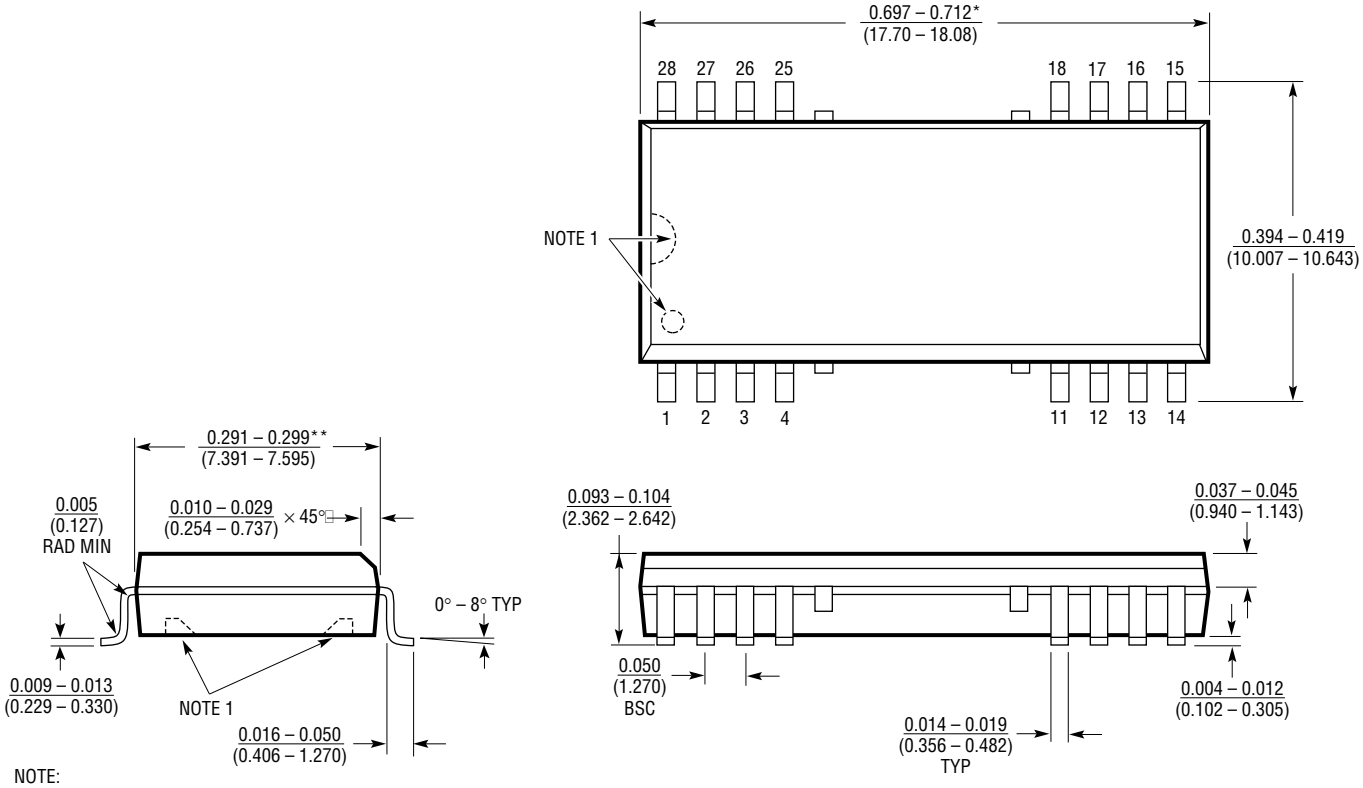


Figure 14. Isolated Window Comparator

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
28-Lead Plastic Small Outline Isolation Barrier (Wide 0.300)
(LTC DWG # 05-08-1690)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
   THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

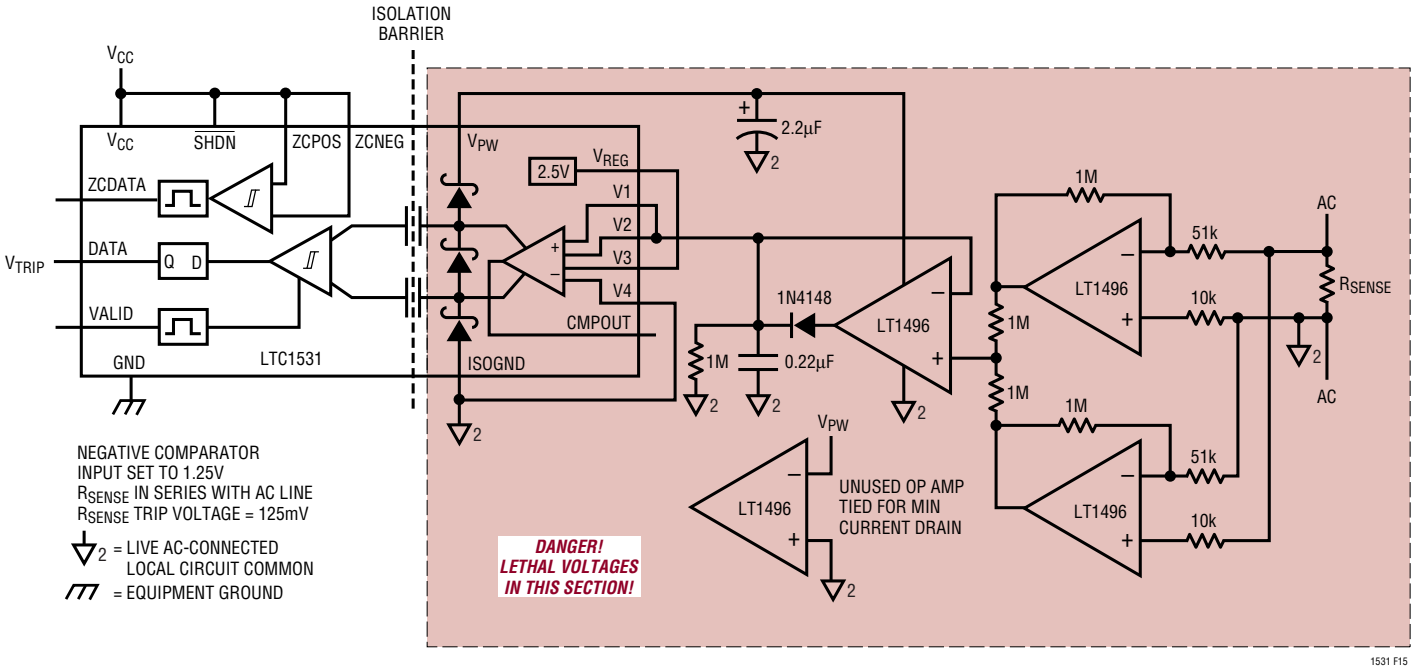


Figure 15. AC Line Overcurrent Detect

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1177	Isolated MOSFET Driver	No Secondary Power Supply, 2500V_{RMS} Isolation
LT1389	Nanopower Reference	800nA, 0.05% Accuracy, 10ppm/°C Max Drift
LTC1440/LTC1441 LTC1442	Ultralow Power Single/Dual Comparators with Reference	2.1µA Typ, 2V to 11V Supply, Adjustable Hysteresis
LT1495/LT1496	1.5µA Max, Dual/Quad Precision Rail-to-Rail Input and Output Op Amps	Low Offset 375µV_{MAX}, 2.2V to 36V Supply
LTC1540	Nanopower Comparator with Reference	0.3µA Typ, Adjustable Hysteresis, 2V to 11V Supply

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
1531f LT 0607 REV A • PRINTED IN USA