

# TC75W70L8X

## 1. Functional Description

- Dual Comparator

## 2. General

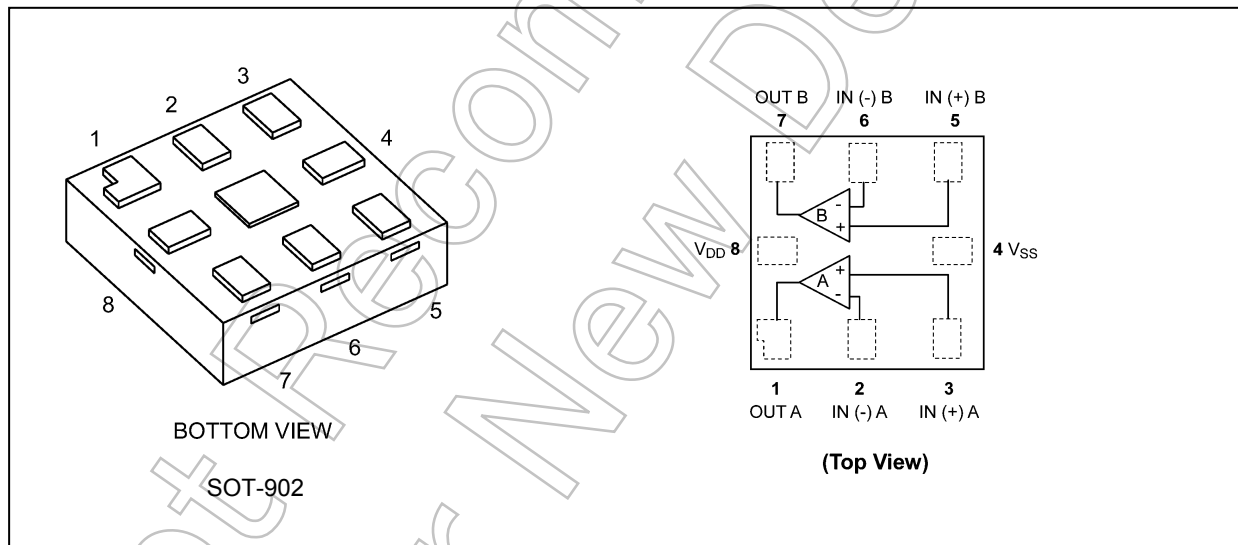
This is a CMOS Input/Output full swing comparator with low operating voltage and low supply current.

The comparator have low operating voltage  $V_{DD} = 1.3\text{ V to }5.5\text{ V}$  and low supply current  $I_{DD} = 26\ \mu\text{A (typ.) @ }V_{DD} = 1.5\text{ V}$ . Output circuit type is push-pull circuit. The package SOT-902 (1.6 mm × 1.6 mm, t: 0.55 mmMAX) is ultra small, so that it is ideal for high-density assembly such as cellular phone.

## 3. Features

- (1) Dual circuit, Input/Output full swing comparator
- (2) Low operating voltage:  $V_{DD} = 1.3\text{ V to }5.5\text{ V}$
- (3) Low supply current:  $I_{DD} = 26\ \mu\text{A (typ.) @ }V_{DD} = 1.5\text{ V}$
- (4) Ultra Small package: SOT-902 (1.6 mm × 1.6 mm, t = 0.55 mmMAX)
- (5) Low input bias current: 1 pA (typ.)
- (6) Push-pull output circuit
- (7) Single power supply operation

## 4. Packaging and Pin Assignment



### 5. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{DD}$		$\pm 3.0$ or $6.0$	V
Differential input voltage	$\Delta V_{IN}$		$\pm 6.0$	V
Input voltage	$V_{IN}$		$V_{SS}$ to $V_{DD}$	V
Output current	$I_{OUT}$		$\pm 35$	mA
Power dissipation	$P_D$	(Note 1)	300	mW
Operating temperature	$T_{opr}$		-40 to 85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to 125	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: Since this device is susceptible to latch-up, a phenomenon inherent to CMOS devices, follow these considerations:

- Don't raise the voltage level of the output pins above  $V_{DD}$  or lower it below  $V_{SS}$ . Consider the power-on timing as well.
- Ensure that any abnormal noise is not introduced into the device.

Note 1: Mounted on an FR4 board.

### 6. Operating Ratings (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{DD}$		1.3 to 5.5	V
Supply voltage	$V_{DD}, V_{SS}$		$\pm 0.65$ to $\pm 2.75$	V

**7. Electrical Characteristics**

**7.1.  $V_{DD} = 3.0\text{ V}$  (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{SS} = \text{GND}$ )**

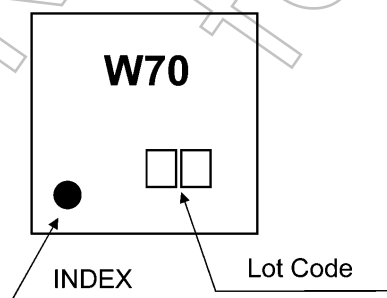
Characteristics	Symbol	Note	Test Condition	Test Circuit	Min	Typ.	Max	Unit
Input offset voltage	$V_{IO}$		—	—	—	$\pm 1$	$\pm 6$	mV
Input offset current	$I_{IO}$		—	—	—	1	—	$\mu\text{A}$
Input bias current	$I_I$		—	—	—	1	—	$\mu\text{A}$
Common-mode input voltage range	$V_{ICM}$		—	—	0	—	3.0	V
Supply current	$I_{DD}$	(Note 1)	—	Fig.10.3	—	27	47	$\mu\text{A}$
Sink current	$I_{SINK}$		$V_{OL} = 0.5\text{ V}$	Fig.10.2	9	18	—	mA
Source current	$I_{SOURCE}$		$V_{OH} = 2.5\text{ V}$	Fig.10.1	7	15	—	mA
Low-level output voltage	$V_{OL}$		$I_{SINK} = 5.0\text{ mA}$	Fig.10.2	—	0.15	0.30	V
High-level output voltage	$V_{OH}$		$I_{SOURCE} = 5.0\text{ mA}$	Fig.10.1	2.70	2.85	—	V
Propagation delay time (L/H)	$t_{PLH}$		Over drive = 100 mV	Fig.10.4	—	400	—	ns
Propagation delay time (H/L)	$t_{PHL}$		Over drive = 100 mV	Fig.10.4	—	800	—	ns
Response time (low-to-high)	$t_{TLH}$		Over drive = 100 mV	Fig.10.4	—	14	—	ns
Response time (high-to-low)	$t_{THL}$		Over drive = 100 mV	Fig.10.4	—	14	—	ns

**7.2.  $V_{DD} = 1.5\text{ V}$  (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{SS} = \text{GND}$ )**

Characteristics	Symbol	Note	Test Condition	Test Circuit	Min	Typ.	Max	Unit
Input offset voltage	$V_{IO}$		—	—	—	$\pm 1$	$\pm 6$	mV
Input offset current	$I_{IO}$		—	—	—	1	—	$\mu\text{A}$
Input bias current	$I_I$		—	—	—	1	—	$\mu\text{A}$
Common-mode input voltage range	$V_{ICM}$		—	—	0	—	1.5	V
Supply current	$I_{DD}$	(Note 1)	—	Fig.10.3	—	26	46	$\mu\text{A}$
Sink current	$I_{SINK}$		$V_{OL} = 0.5\text{ V}$	Fig.10.2	2.5	6.0	—	mA
Source current	$I_{SOURCE}$		$V_{OH} = 1.0\text{ V}$	Fig.10.1	1.5	5.0	—	mA
Low-level output voltage	$V_{OL}$		$I_{SINK} = 1.5\text{ mA}$	Fig.10.2	—	0.10	0.25	V
High-level output voltage	$V_{OH}$		$I_{SOURCE} = 1.5\text{ mA}$	Fig.10.1	1.25	1.40	—	V
Propagation delay time (L/H)	$t_{PLH}$		Over drive = 100 mV	Fig.10.4	—	400	—	ns
Propagation delay time (H/L)	$t_{PHL}$		Over drive = 100 mV	Fig.10.4	—	720	—	ns
Response time (low-to-high)	$t_{TLH}$		Over drive = 100 mV	Fig.10.4	—	20	—	ns
Response time (high-to-low)	$t_{THL}$		Over drive = 100 mV	Fig.10.4	—	33	—	ns

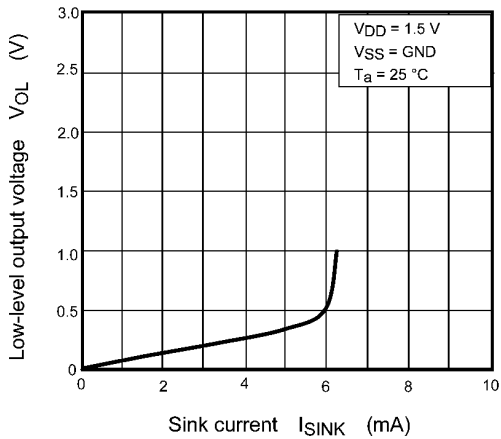
Note 1: The current consumption of the device increases with its operating frequency. Ensure that its power dissipation does not exceed the rated allowable power dissipation.

**8. Marking**

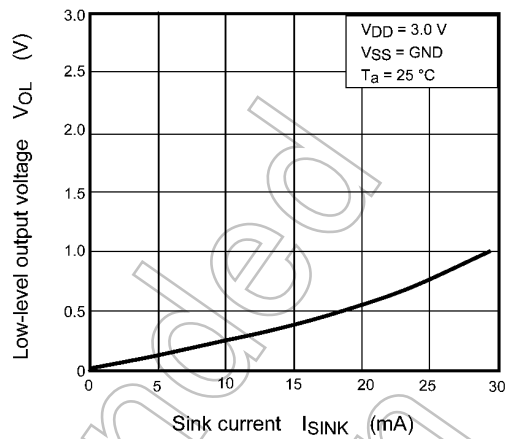


(Top View)

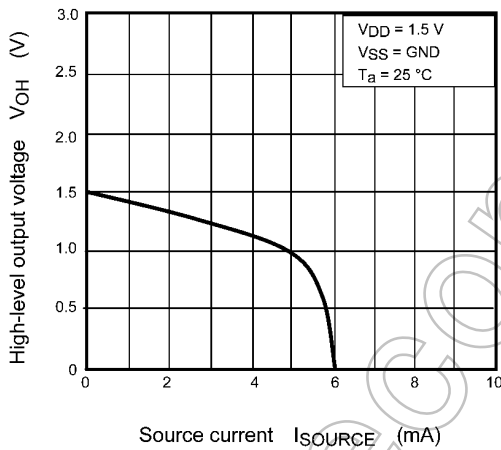
**9. Characteristics Curves (Note)**



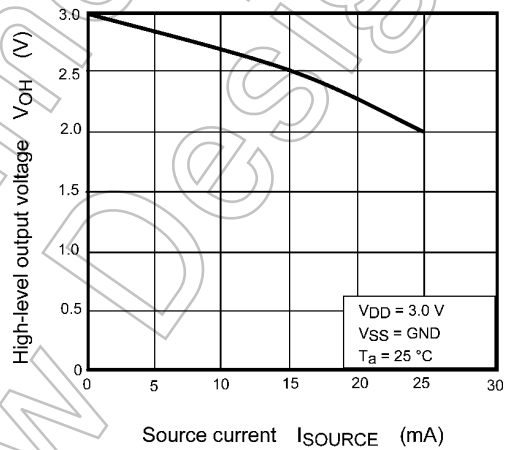
**Fig. 9.1  $V_{OL} - I_{SINK}$**



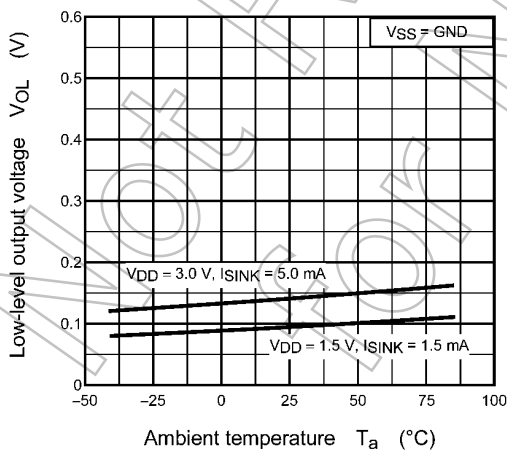
**Fig. 9.2  $V_{OL} - I_{SINK}$**



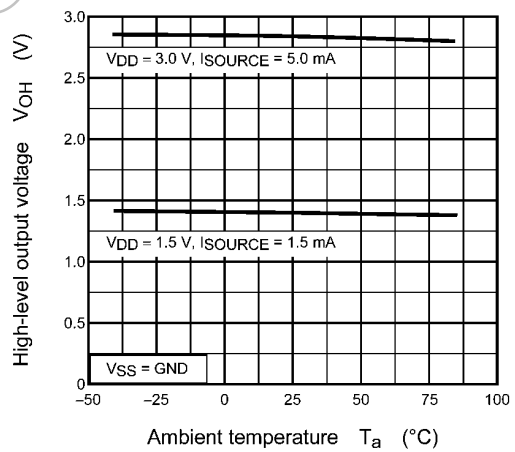
**Fig. 9.3  $V_{OH} - I_{SOURCE}$**



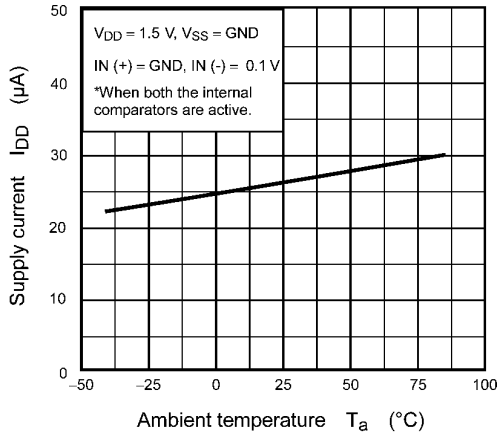
**Fig. 9.4  $V_{OH} - I_{SOURCE}$**



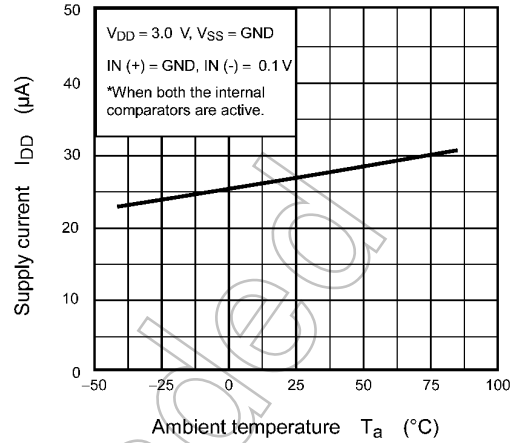
**Fig. 9.5  $V_{OL} - T_a$**



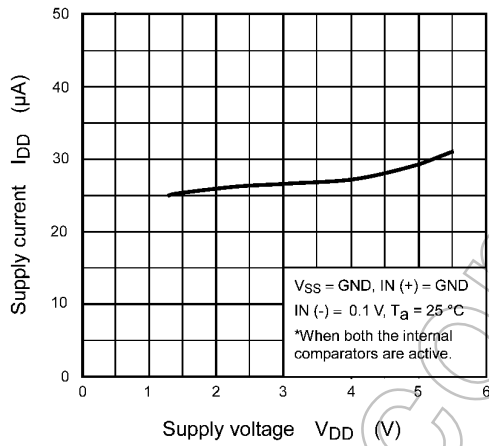
**Fig. 9.6  $V_{OH} - T_a$**



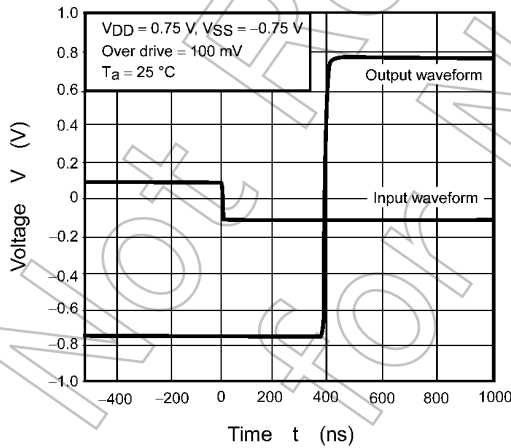
**Fig. 9.7  $I_{DD} - T_a$**



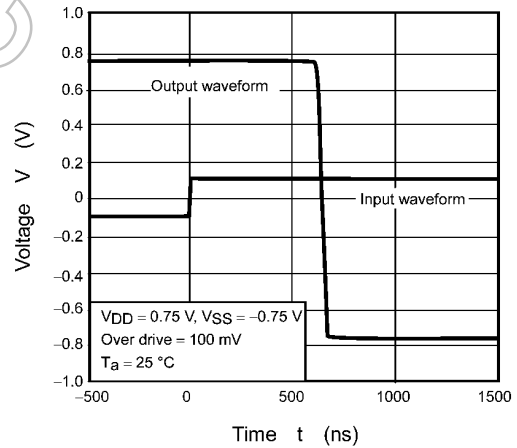
**Fig. 9.8  $I_{DD} - T_a$**



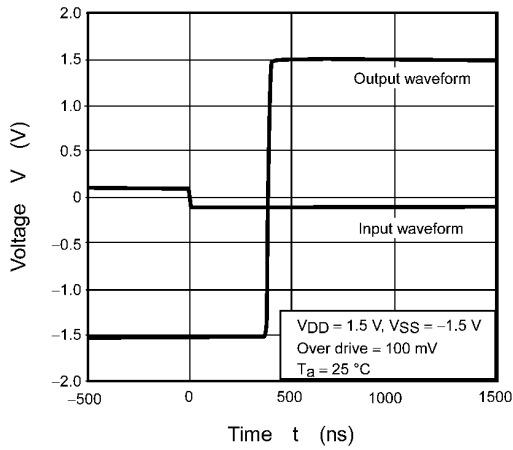
**Fig. 9.9  $I_{DD} - V_{DD}$**



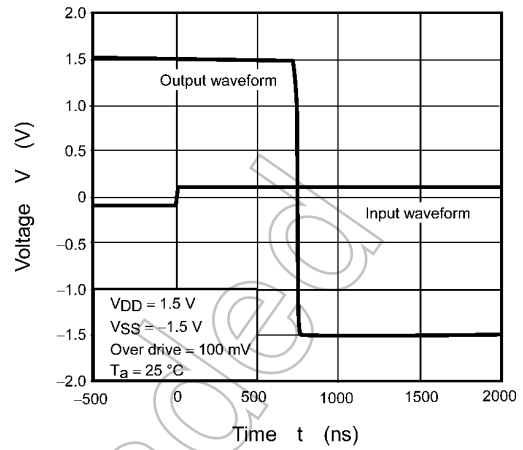
**Fig. 9.10 Propagation delay time (L/H)  $t_{pLH}$**



**Fig. 9.11 Propagation delay time (H/L)  $t_{pHL}$**



**Fig. 9.12 Propagation delay time (L/H)  $t_{PLH}$**



**Fig. 9.13 Propagation delay time (H/L)  $t_{PHL}$**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Not Recommended for New Design

10. Test Circuits

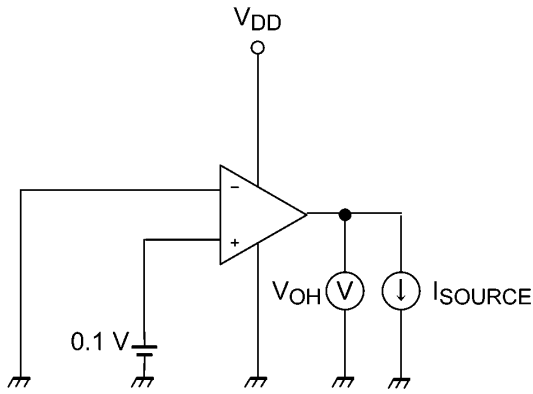


Fig. 10.1  $I_{SOURCE}, V_{OH}$

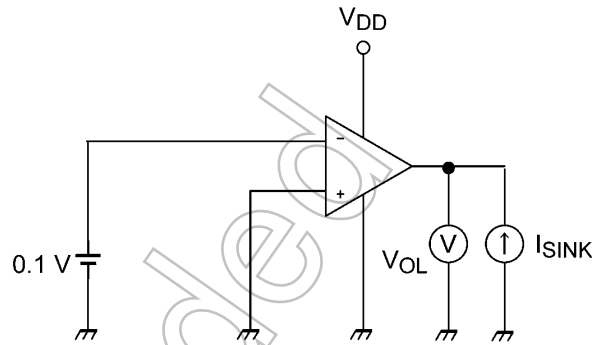


Fig. 10.2  $I_{SINK}, V_{OL}$

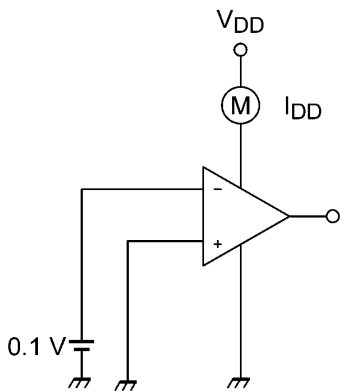


Fig. 10.3  $I_{DD}$

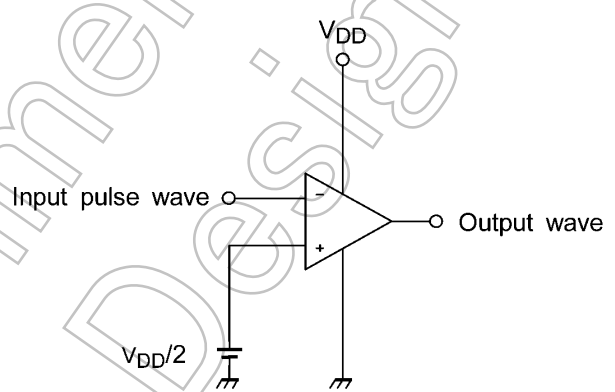


Fig. 10.4 Propagation delay time  $t_{PLH}, t_{PHL}$

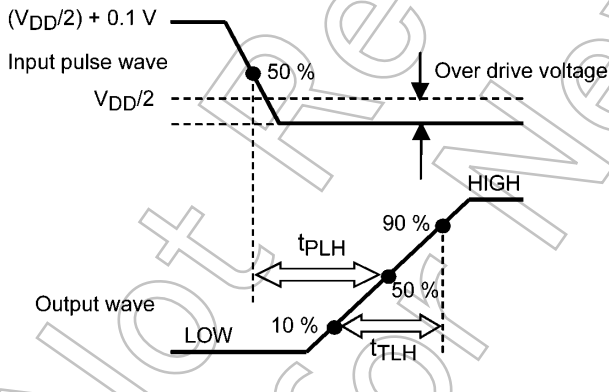


Fig. 10.5 Propagation delay time (L/H)  $t_{PLH}$  wave

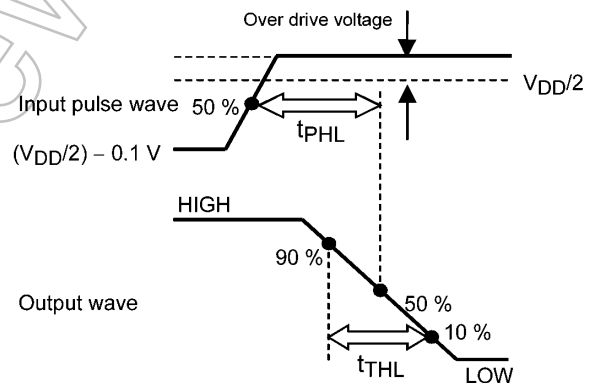
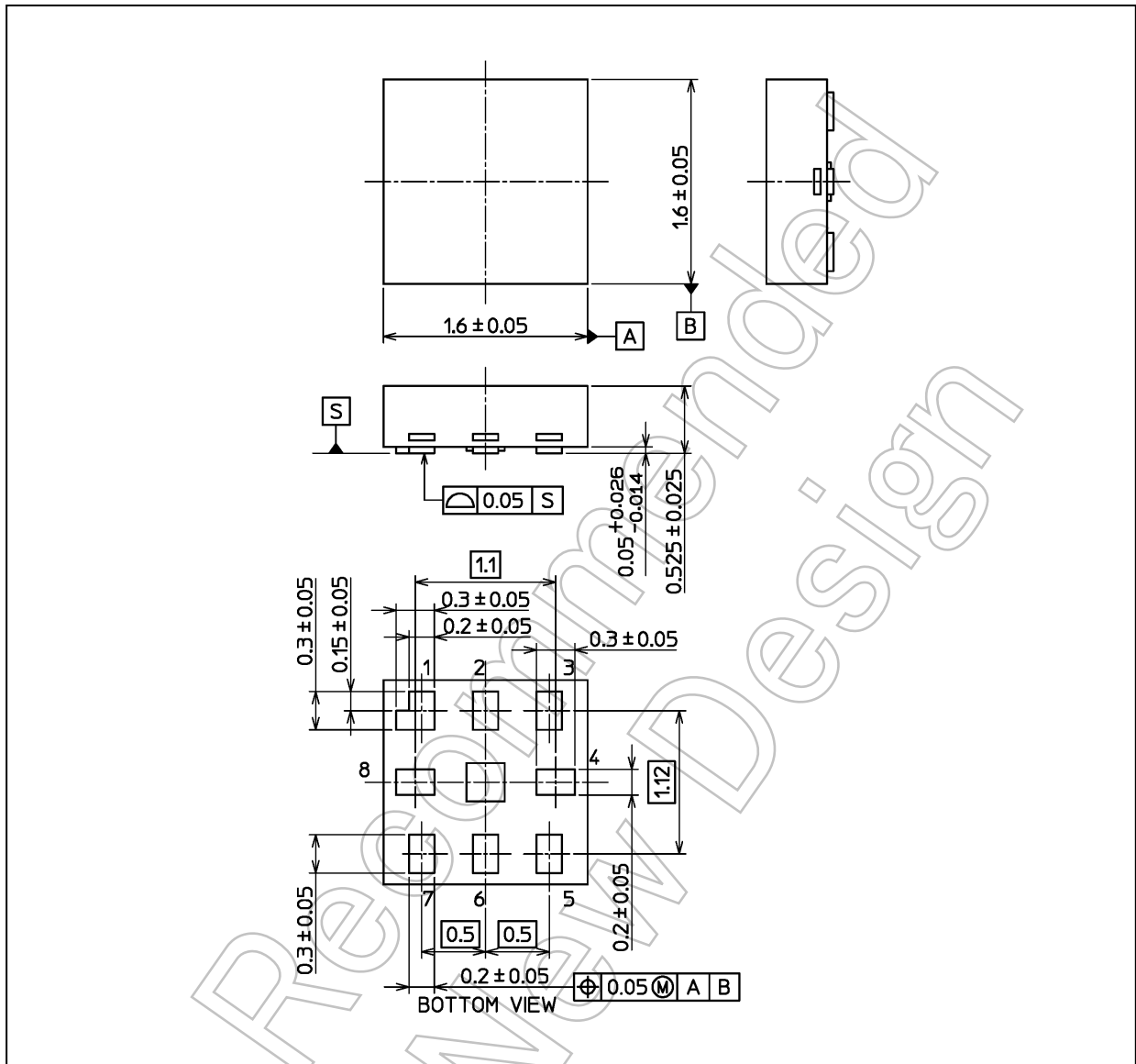


Fig. 10.6 Propagation delay time (H/L)  $t_{PHL}$  wave

Package Dimensions

Unit: mm



Weight: 0.0031 g (typ.)

Package Name(s)
TOSHIBA: P-UFLGA8-0202-0.50-001
Nickname: SOT-902



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