INFORMATION ONLY NOTIFICATION

PCN # 20123503 Revision B

Title Of Change: Part Number Change for 19 duplicate parts

Publish Date: 05/07/12

Revision History of PCN:

Rev	Action Date	User ID	Action Name	Action Comments
B	05/04/2012	CJMKSC	Create PCN	

This is to inform you that a design and/or process change will be made to the following product(s).
This notification is for your information and concurrence.

If you have any questions concerning this change, please contact:

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Change Type: PART NUMBER CHANGE

PROPOSED 1st SHIP DATE

04/16/12

DESCRIPTION OF CHANGE AND PRODUCTS AFFECTED

This Rev B publication corrects the typo for the LM139AJ/PB part number below as well as the customer specific device listing in at the end of this notice.

The purpose of this Product Change Notification (PCN) is to inform you that National Semiconductor will be changing the orderable/manufacturing part number on a select set of products as follows:

Old Part Number	New Part Number
LF347N	LF347N/PB
LP324N	LP324N/PB
LP339N	LP339N/PB
LF347BN	LF347BN/PB
LM124AJ	LM124AJ/PB
LM139AJ	LM139AJ/PB
LM2901N	LM2901N/PB
LM2902N	LM2902N/PB
LM324AN	LM324AN/PB
LM339AN	LM339AN/PB
LP2902N	LP2902N/PB
TL082CP	TL082CP/PB
LM124J	LM124J/PB
LM139J	LM139J/PB
LM148J	LM148J/PB
LM324N	LM324N/PB
LM339N	LM339N/PB
LM348N	LM348N/PB
ADC0820CCN	ADC0820CCN/PB

REASON FOR CHANGE

As part of the integration process resulting from the acquisition of National Semiconductor by Texas Instruments this past September, it was discovered that both National Semiconductor and Texas Instruments have these 19 identical parts in their respective product portfolios. As these identical parts may not be pin to pin compatible, it is necessary for customers to start ordering by the new part numbers to assure receiving the "National Semiconductor" version of the product. Also, while all 19 of the National Semiconductor versions are leaded (Pb), the Texas Instruments versions in most cases are lead free.

Customers can start ordering immediately by the new part number and must transition to the new ordering part number by 30th June 2012.

ANTICIPATED IMPACT ON FORM, FIT, FUNCTION, QUALITY, OR RELIABILITY (POSITIVE / NEGATIVE)

No impact to form, fit, function, quality, or reliability. The design, manufacturing, and testing of all these products remain unchanged. This is a part number change only.

SAMPLE AVAILABILITY DATE SCHEDULE

Not applicable.

CHANGES TO PRODUCT IDENTIFICATION RESULTING FROM THIS PCN

All supporting documentation and package containers will reflect the new part number as described above. Device top marking will remain the same.

RELIABILITY REFERENCE REPORTS

PART NUMBERS AFFECTED

ADC0820CCN	LF347BN	LF347N
LM124AJ	LM124J	LM139AJ
LM139J	LM148J	LM2901N
LM2902N	LM324AN	LM324N
LM339AN	LM339N	LM348N
LP2902N	LP324N	LP339N
TL082CP		

ATTACHMENTS

N/A

National Semiconductor

LP339
Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 µA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

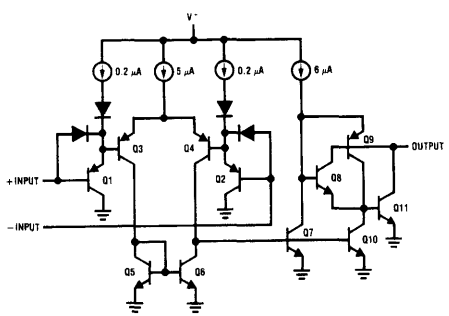
Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

Features

- Ultra-low power supply current drain (60 µA)—independent of the supply voltage (75 µW/comparator at +5 V_{DC})
- Low input biasing current: 3 nA
- Low input offset current: ±0.5 nA
- Low input offset voltage: ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O=2 V_{DC})
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



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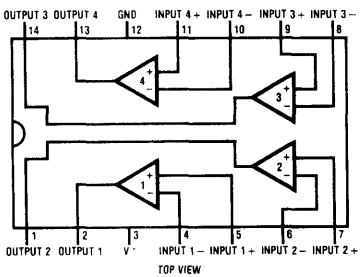

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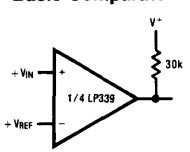
Order Number LP339M for S.O. Package
See NS Package Number M14A
Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

Typical Applications (V^+= 5.0 V_{DC})

Basic Comparator



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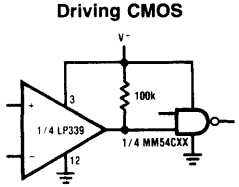
Driving CMOS



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	±36 V_{DC}
Input Voltage	−0.3 V_{DC} to 36 V_{DC}
Power Dissipation (Note 2)	
Molded DIP	570 mW
Output Short Circuit to GND (Note 3)	Continuous
Input Current V_{IN}<−0.3 V_{DC} (Note 4)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65° to +150°C
Soldering Information:	
Dual-In-Line Package (10 sec.)	+260°C
S.O. Package:	
Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

(V+=5 V_{DC}) (Note 5)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	T_A=25°C (Note 10)		±2	±5	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with the Output in the Linear Range, T_A=25°C (Note 6)		2.5	25	nA_{DC}
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$, T_A=25°C		±0.5	±5	nA_{DC}
Input Common Mode Voltage Range	T_A=25°C (Note 7)	0		V+−1.5	V_{DC}
Supply Current	R_L=Infinite on all Comparators, T_A=25°C		60	100	μA_{DC}
Voltage Gain	V_O = 1 V_{DC} to 11 V_{DC}, R_L=15 kΩ, V^+=15 V_{DC}, T_A=25°C		500		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25°C		1.3		µSec
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25°C (Note 8)		8		µSec
Output Sink Current	$V_{IN}(-)$=1 V_{DC}, $V_{IN}(+)$=0, V_O=2 V_{DC}, T_A=25°C (Note 12)	15	30		mA_{DC}
	V_O=0.4 V_{DC}	0.20	0.70		mA_{DC}
Output Leakage Current	$V_{IN}(+)$=1 V_{DC}, $V_{IN}(-)$=0, V_O=5 V_{DC}, T_A=25°C		0.1		nA_{DC}
Input Offset Voltage	(Note 10)			±9	mV_{DC}
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$		±1	±15	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range		4	40	nA_{DC}
Input Common Mode Voltage Range	Single Supply	0		V+−2.0	V_{DC}
Output Sink Current	$V_{IN}(-)$=1 V_{DC}, $V_{IN}(+)$=0, V_O=2 V_{DC}	10			mA_{DC}
Output Leakage Current	$V_{IN}(+)$=1 V_{DC}, $V_{IN}(-)$=0, V_O=30 V_{DC}			1.0	μA_{DC}
Differential Input Voltage	All $V_{IN's}$≥0 V_{DC} (or V^- on split supplies) (Note 9)			36	V_{DC}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For elevated temperature operation, T_j max is 125°C for the LP339. θ_{ja} (junction to ambient) is 175°C/W for the LP339N and 120°C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D ≤ 100 mW), provided the output transistors are allowed to saturate.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} (T_A=25°C).

Note 5: These specifications apply for V^+=5V_{DC} and 0°C≤T_A≤70° C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 7: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5V (T_A=25°C), but either or both inputs can go to 30 V_{DC} without damage.

Note 8: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 µs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics (Continued)

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) at T_A=25°C.

Note 10: At output switch point, V_O=1.4V, R_S=0Ω with V^+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+−1.5 V_{DC}).

Note 11: For input signals that exceed V^+, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Note 12: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 V_{DC} and sink lower currents below this point. (See typical characteristics section and applications section).