

# AMC22C11-Q1 Automotive, Fast Response, Basic Isolated Comparator With Adjustable Threshold and Latch Function

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- Wide high-side supply range: 3 V to 25 V
- Low-side supply range: 2.7 V to 5.5 V
- Adjustable threshold: 20 mV to 2.7 V
- Reference current for threshold adjustment:
  - 100  $\mu\text{A}$ ,  $\pm 1\%$
- Trip threshold error:  $\pm 1\%$  (max) at 250 mV
- Open-drain output with optional latch mode
- Propagation delay: 240 ns (typ)
- High CMTI: 75 V/ns (min)
- Safety-related certifications:
  - 4250- $V_{PK}$  basic isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 3000- $V_{RMS}$  isolation for 1 minute per UL1577

## 2 Applications

- Overcurrent or overvoltage detection in:
  - [HEV/EV charging piles](#)
  - [HEV/EV onboard chargers \(OBC\)](#)
  - [HEV/EV DC/DC converters](#)
  - [HEV/EV traction inverters](#)

## 3 Description

The AMC22C11-Q1 is an isolated comparator with a short response time. The open-drain output is separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide galvanic isolation of up to 3 kV<sub>RMS</sub> according to DIN EN IEC 60747-17 (VDE 0884-17) and UL1577, and supports a working voltage of up to 560 V<sub>RMS</sub>.

The trip threshold is adjustable from 20 mV to 450 mV in low-hysteresis mode and from 600 mV to 2.7 V in high-hysteresis mode through a single external resistor.

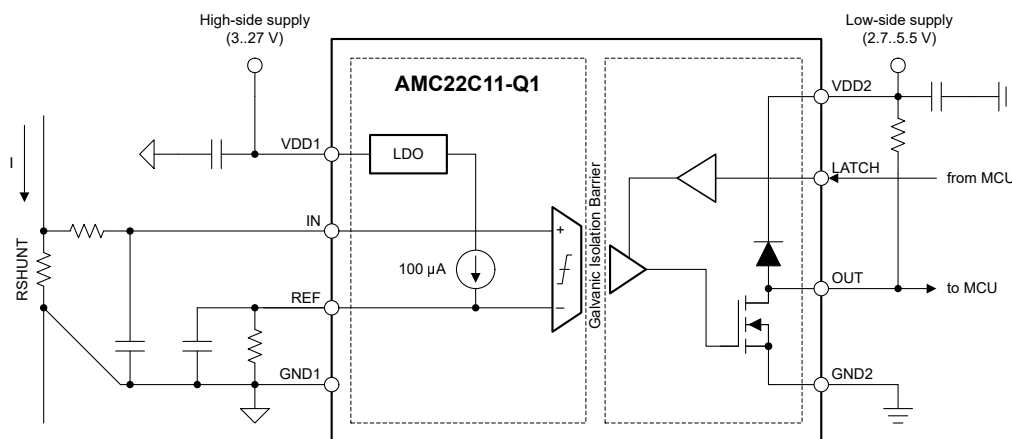
The open-drain output on the device supports transparent mode (LATCH input tied to GND2) where the output follows the input state, or latch mode, where the output is cleared on the falling edge of the latch input signal.

The AMC22C11-Q1 is available in an 8-pin SOIC package and is specified over the full automotive temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Package Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC22C11-Q1	SOIC (8)	4.90 mm × 3.90 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application



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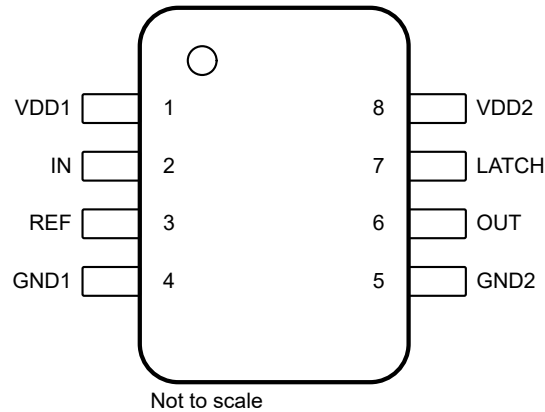
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2022) to Revision A (August 2022)	Page
• Changed document status from <i>advanced information</i> to <i>production data</i> .....	1

## 5 Pin Configuration and Functions



**Figure 5-1. D Package, 8-Pin SOIC (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply. <sup>(1)</sup>
2	IN	Analog input	Analog input pin to the comparator.
3	REF	Analog input	Reference pin that defines the trip threshold. The voltage on this pin also affects the hysteresis of the comparator, as explained in the <a href="#">Reference Input</a> section. This pin is internally connected to a 100- $\mu$ A current source. Connect a resistor from REF to GND1 to define the trip threshold, and a capacitor from REF to GND1 to filter the reference voltage. For best transient noise immunity, place the capacitor as closely to the pin as possible. This pin can also be driven by an external voltage source.
4	GND1	High-side ground	High-side ground.
5	GND2	Low-side ground	Low-side ground.
6	OUT	Digital output	Open-drain output of the comparator. Connect to an external pullup resistor.
7	LATCH	Digital input	Digital input to select latch mode (high) or transparent mode (low) of the open-drain output. Do not leave the input pin unconnected (floating). Connect to GND2 when not used.
8	VDD2	Low-side power	Low-side power supply. <sup>(1)</sup>

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

see<sup>(1)</sup>

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	-0.3	30	V
	VDD2 to GND2	-0.3	6.5	
Analog input voltage	REF to GND1	-0.5	6.5	V
	IN to GND1	-6	5.5	
Digital input voltage	LATCH to GND1	-0.5	VDD2 + 0.5	V
Digital output voltage	OUT to GND2	-0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	-65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> , HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
<b>POWER SUPPLY</b>						
V <sub>VDD1</sub>	High-side power-supply voltage	VDD1 to GND1	3.0	5	25	V
V <sub>VDD2</sub>	Low-side power supply voltage	VDD2 to GND2	2.7	3.3	5.5	V
<b>ANALOG INPUT</b>						
V <sub>IN</sub>	Input voltage	IN to GND1, VDD1 ≤ 4.3 V	-0.4	VDD1 - 0.3		V
		IN to GND1, VDD1 > 4.3 V	-0.4	4		
V <sub>REF</sub>	Reference voltage	Low hysteresis mode	20	450		mV
		High hysteresis mode	600	2700 <sup>(1)</sup>		
	Reference voltage headroom	VDD1 - V <sub>REF</sub>	1.4			V
	Filter capacitance on REF pin		20	100	nF	
<b>DIGITAL I/O</b>						
	Digital input voltage	LATCH pin	GND2	VDD2		V
	Digital output voltage	OUT to GND2	GND2	VDD2		V
	Sink current	OUT	0	4		mA
<b>TEMPERATURE RANGE</b>						
T <sub>A</sub>	Specified ambient temperature		-40	25	125	°C

(1) Reference voltages (V<sub>REF</sub>) > 1.6 V require V<sub>VDD1</sub> > V<sub>VDD1,MIN</sub> to maintain minimum headroom (V<sub>VDD1</sub> - V<sub>REF</sub>) of 1.4 V.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D (SOIC)	UNIT
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	116.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	52.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	58.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	19.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	58.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.5 Power Ratings

PARAMETER	TEST CONDITIONS	VALUE	UNIT
P <sub>D</sub>	VDD1 = 25 V, VDD2 = 5.5 V	95	mW
	VDD1 = VDD2 = 5.5 V	30	
	VDD1 = VDD2 = 3.6 V	20	
P <sub>D1</sub>	VDD1 = 25 V	83	mW
	VDD1 = 5.5 V	18	
	VDD1 = 3.6 V	12	
P <sub>D2</sub>	VDD2 = 5.5 V	12	mW
	VDD2 = 3.6 V	8	

## 6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
<b>GENERAL</b>				
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-III	
<b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At AC voltage	790	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum-rated isolation working voltage	At AC voltage (sine wave)	560	V <sub>RMS</sub>
		At DC voltage	790	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification test)	4250	V <sub>PK</sub>
		V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production test)	5100	
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50-μs waveform per IEC 62368-1	5000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	6500	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method a, after input/output safety test subgroups 2 and 3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.3 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b2, at routine test (100% production), V <sub>ini</sub> = V <sub>IOTM</sub> = V <sub>pd(m)</sub> ; t <sub>ini</sub> = t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 0.5 V <sub>PP</sub> at 1 MHz	~1.5	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 500 V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		55/125/21	
<b>UL1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 3000 V <sub>RMS</sub> or 4250 V <sub>DC</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 3600 V <sub>RMS</sub> , t = 1 s (100% production test)	3000	V <sub>RMS</sub>

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.

## 6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition
Basic insulation	Single protection
Certificate number: pending	File number: E181974

## 6.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 116.5°C/W, VDD1 = VDD2 = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			195	mA
		R <sub>θJA</sub> = 116.5°C/W, VDD1 = VDD2 = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			300	
P <sub>S</sub>	Safety input, output, or total power	R <sub>θJA</sub> = 116.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1070	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum junction temperature.

$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$ , where AVDD<sub>max</sub> is the maximum high-side voltage and DVDD<sub>max</sub> is the maximum controller-side supply voltage.

## 6.9 Electrical Characteristics

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $25\text{ V}$ ,  $V_{DD2} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $V_{REF} = 20\text{ mV}$  to  $2.7\text{ V}$ <sup>(1)</sup>, and  $V_{IN} = -400\text{ mV}$  to  $4\text{ V}$ <sup>(2)</sup>; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ , and  $V_{REF} = 250\text{ mV}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
$R_{IN}$	Input resistance	IN pin, $0 \leq V_{IN} \leq 4\text{ V}$		1		$\text{G}\Omega$
$I_{BIAS}$	Input bias current	IN pin, $0 \leq V_{IN} \leq 4\text{ V}$ <sup>(3)</sup>		0.1	25	nA
		IN pin, $-400\text{ mV} \leq V_{IN} \leq 0\text{ V}$ <sup>(4)</sup>	-310	-0.5		
$C_{IN}$	Input capacitance	IN pin		4		pF
<b>REFERENCE PIN</b>						
$I_{REF}$	Reference current	REF to GND1, $20\text{ mV} < V_{REF} \leq 2.7\text{ V}$	99	100	101	$\mu\text{A}$
$V_{MSEL}$	Mode selection threshold	$V_{REF}$ rising	500	550	600	mV
		$V_{REF}$ falling	450	500	550	
	Mode selection threshold hysteresis			50		mV
<b>COMPARATOR</b>						
$V_{IT+}$	Positive-going trip threshold			$V_{REF} + V_{HYS}$		mV
$E_{IT+}$	Positive-going trip threshold error	$(V_{IT+} - V_{REF} - V_{HYS})$ , $V_{REF} = 20\text{ mV}$ , $V_{HYS} = 4\text{ mV}$	-2		2	mV
		$(V_{IT+} - V_{REF} - V_{HYS})$ , $V_{REF} = 250\text{ mV}$ , $V_{HYS} = 4\text{ mV}$	-2		2	
		$(V_{IT+} - V_{REF} - V_{HYS})$ , $V_{REF} = 2\text{ V}$ , $V_{HYS} = 25\text{ mV}$	-5		5	
$V_{IT-}$	Negative-going trip threshold			$V_{REF}$		mV
$E_{IT-}$	Negative-going trip threshold error	$(V_{IT-} - V_{REF})$ , $V_{REF} = 20\text{ mV}$	-2.5		2.5	mV
		$(V_{IT-} - V_{REF})$ , $V_{REF} = 250\text{ mV}$	-2.5		2.5	
		$(V_{IT-} - V_{REF})$ , $V_{REF} = 2\text{ V}$	-5		5	
$V_{HYS}$	Trip threshold hysteresis	$(V_{IT+} - V_{IT-})$ , $V_{REF} \leq 450\text{ mV}$		4		mV
		$(V_{IT+} - V_{IT-})$ , $V_{REF} \geq 600\text{ mV}$		25		
<b>DIGITAL I/O</b>						
$V_{IH}$	High-level input voltage	LATCH pin	$0.7 \times V_{DD2}$		$V_{DD2} + 0.3$	V
$V_{IL}$	Low-level input voltage	LATCH pin	-0.3		$0.3 \times V_{DD2}$	V
$C_{IN}$	Input capacitance	LATCH pin		4		pF
$V_{OL}$	Low-level output voltage	$I_{SINK} = 4\text{ mA}$		80	250	mV
$I_{LKG}$	Open-drain output leakage current	$V_{DD2} = 5\text{ V}$ , $V_{OUT} = 5\text{ V}$		5	100	nA
CMTI	Common-mode transient immunity	$ V_{IN} - V_{REF}  \geq 4\text{ mV}$ , $R_{PULLUP} = 10\text{ k}\Omega$	75	150		V/ns



## 6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $25\text{ V}$ ,  $V_{DD2} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $V_{REF} = 20\text{ mV}$  to  $2.7\text{ V}$ <sup>(1)</sup>, and  $V_{IN} = -400\text{ mV}$  to  $4\text{ V}$ <sup>(2)</sup>; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ , and  $V_{REF} = 250\text{ mV}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
VDD1 <sub>UV</sub>	VDD1 undervoltage detection threshold	VDD1 rising			3	V
		VDD1 falling			2.9	
VDD1 <sub>POR</sub>	VDD1 power-on reset threshold	VDD1 falling			2.3	V
VDD2 <sub>UV</sub>	VDD2 undervoltage detection threshold	VDD2 rising			2.7	V
		VDD2 falling			2.1	
I <sub>DD1</sub>	High-side supply current			2.7	3.7	mA
I <sub>DD2</sub>	Low-side supply current			1.8	2.2	mA

- (1) Reference voltages  $>1.6\text{ V}$  require  $V_{DD1} > V_{DD1_{MIN}}$ . See the [Recommended Operating Conditions](#) table for details.
- (2) But not exceeding the maximum input voltage specified in the [Recommended Operating Conditions](#) table.
- (3) The typical value is measured at  $V_{IN} = 0.4\text{ V}$ .
- (4) The typical value is measured at  $V_{IN} = -400\text{ mV}$ .

### 6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>LATCH INPUT</b>						
Deglitch time	Falling edge	1.8		3.2	μs	
<b>OPEN-DRAIN OUTPUT</b>						
t <sub>pH</sub>	Propagation delay time,  V <sub>IN</sub>   rising	VDD2 = 3.3 V, V <sub>REF</sub> = 250 mV, V <sub>OVERDRIVE</sub> = 10 mV, C <sub>L</sub> = 15 pF		240	380	ns
		VDD2 = 3.3 V, V <sub>REF</sub> = 2 V, V <sub>OVERDRIVE</sub> = 50 mV, C <sub>L</sub> = 15 pF		210	340	
t <sub>pL</sub>	Propagation delay time,  V <sub>IN</sub>   falling	VDD2 = 3.3 V, V <sub>REF</sub> = 250 mV, V <sub>OVERDRIVE</sub> = 10 mV, C <sub>L</sub> = 15 pF		240	380	ns
		VDD2 = 3.3 V, V <sub>REF</sub> = 2 V, V <sub>OVERDRIVE</sub> = 50 mV, C <sub>L</sub> = 15 pF		210	340	
t <sub>f</sub>	Output signal fall time	R <sub>PULLUP</sub> = 4.7 kΩ, C <sub>L</sub> = 15 pF		2	ns	
<b>MODE SELECTION</b>						
t <sub>HSEL</sub>	Comparator hysteresis selection deglitch time	V <sub>REF</sub> rising or falling		10	μs	
t <sub>DIS13</sub>	Comparator disable deglitch time	V <sub>REF</sub> rising		10	μs	
t <sub>EN13</sub>	Comparator enable deglitch time	V <sub>REF</sub> falling		100	μs	
<b>START-UP TIMING</b>						
t <sub>LS,STA</sub>	Low-side start-up time	VDD2 step to 2.7 V, VDD1 ≥ 3.0 V		40	μs	
t <sub>HS,STA</sub>	High-side start-up time	VDD1 step to 3.0 V, VDD2 ≥ 2.7 V		45	μs	
t <sub>HS,BLK</sub>	High-side blanking time			200	μs	
t <sub>HS,FLT</sub>	High-side-fault detection delay time			100	μs	

### 6.11 Timing Diagrams

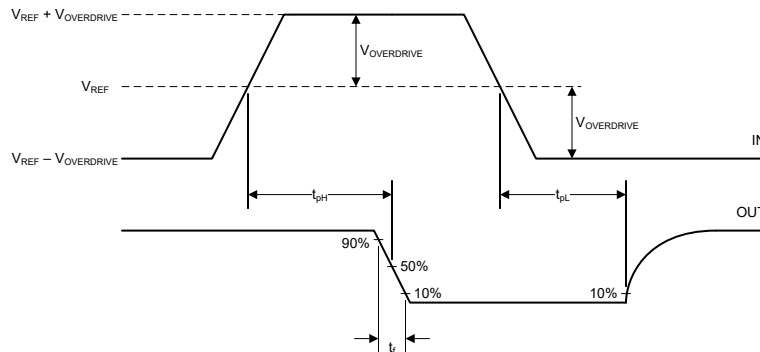


Figure 6-1. Rise, Fall, and Delay Time Definition (LATCH = Low)

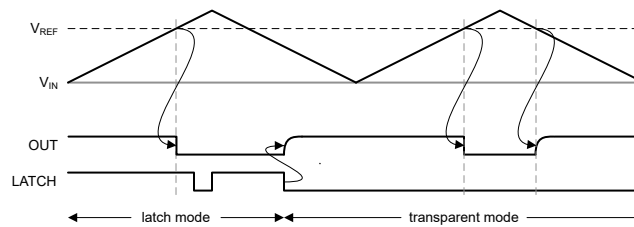
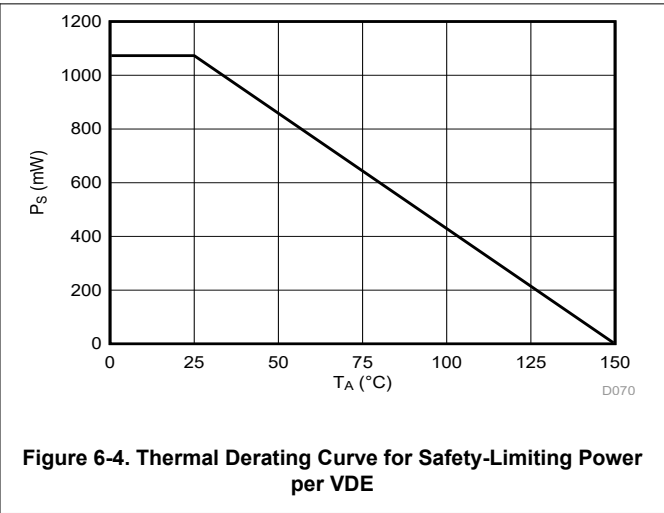
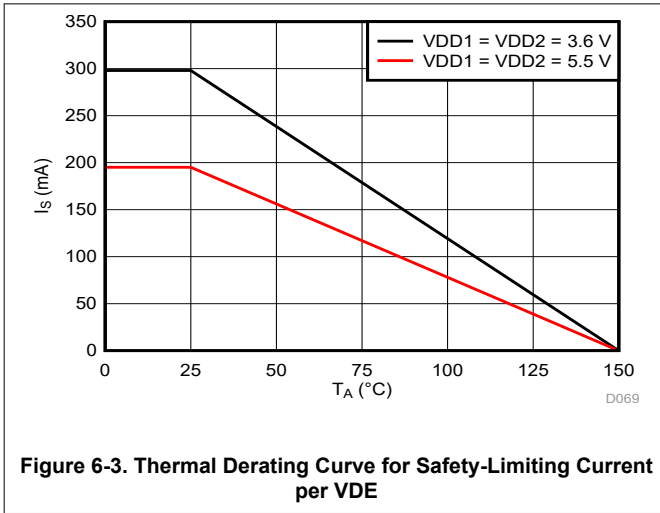


Figure 6-2. Functional Timing Diagram

## 6.12 Insulation Characteristics Curves



### 6.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)

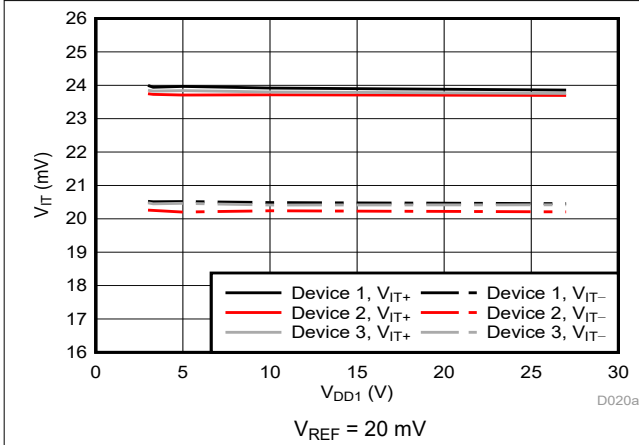


Figure 6-5. Trip Threshold vs Supply Voltage

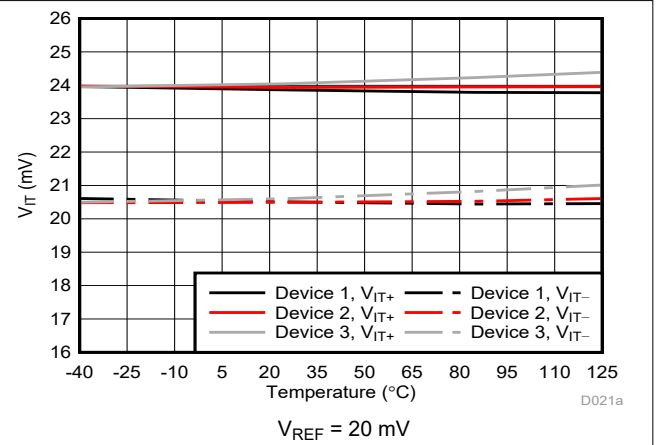


Figure 6-6. Trip Threshold vs Temperature

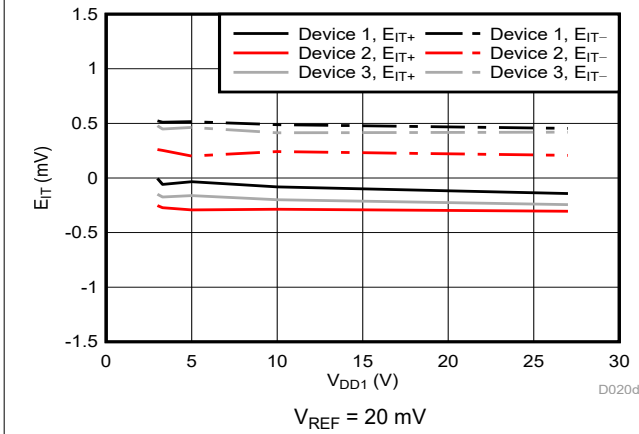


Figure 6-7. Trip Threshold Error vs Supply Voltage

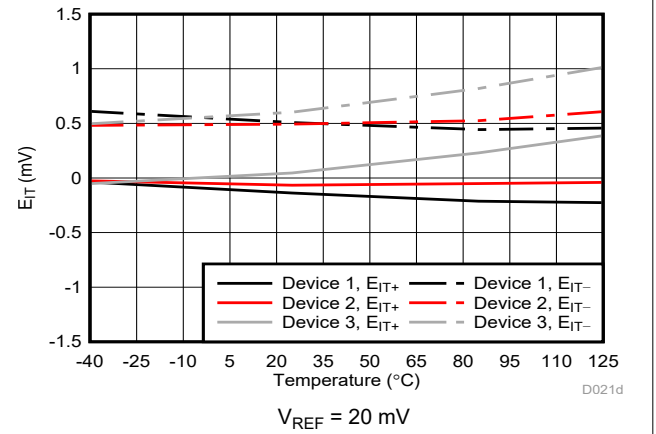


Figure 6-8. Trip Threshold Error vs Temperature

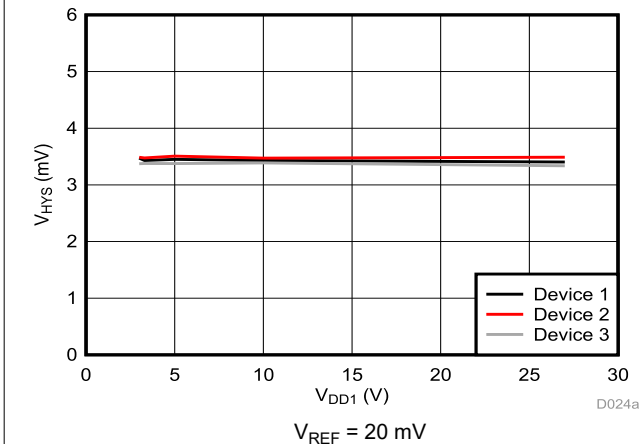


Figure 6-9. Trip Threshold Hysteresis vs Supply Voltage

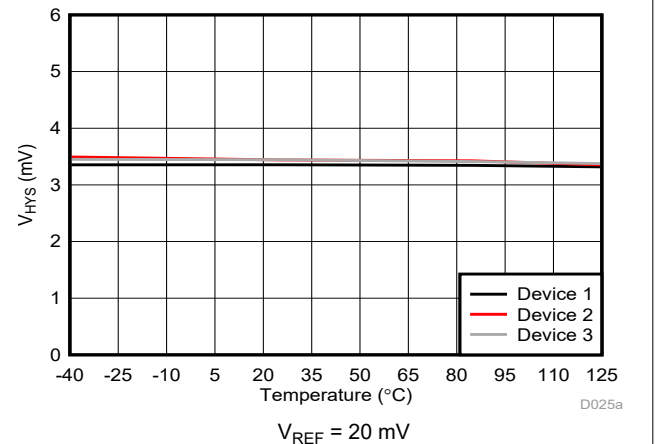
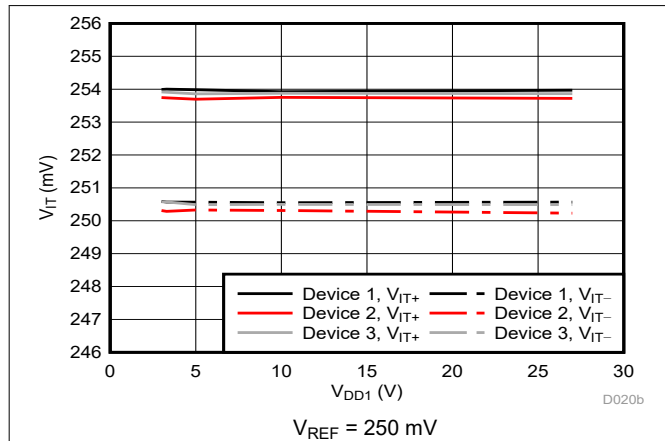


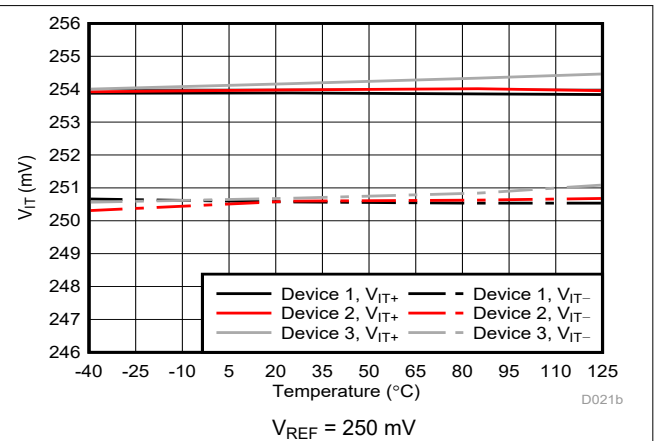
Figure 6-10. Trip Threshold Hysteresis vs Temperature

### 6.13 Typical Characteristics (continued)

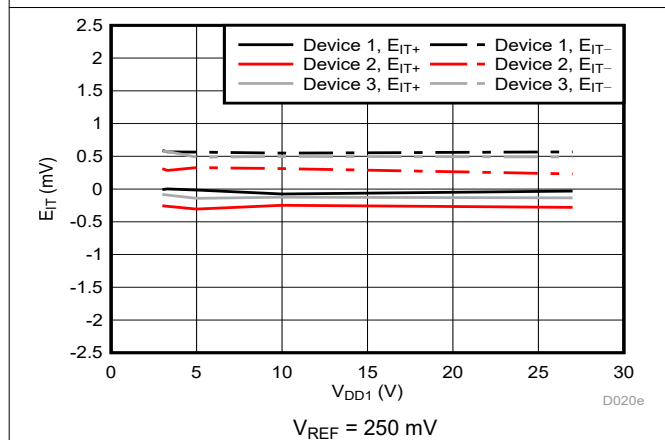
at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)



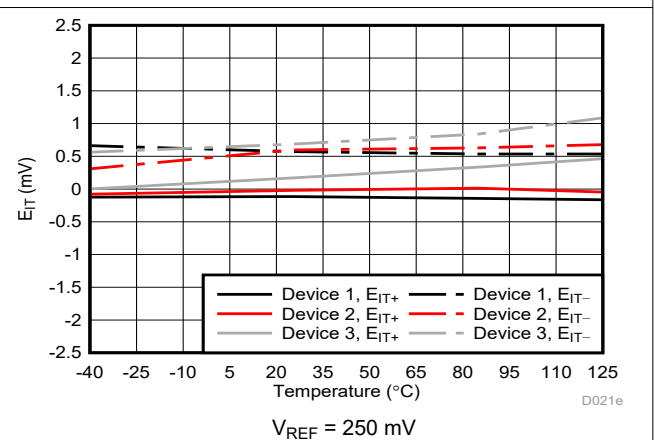
**Figure 6-11. Trip Threshold vs Supply Voltage**



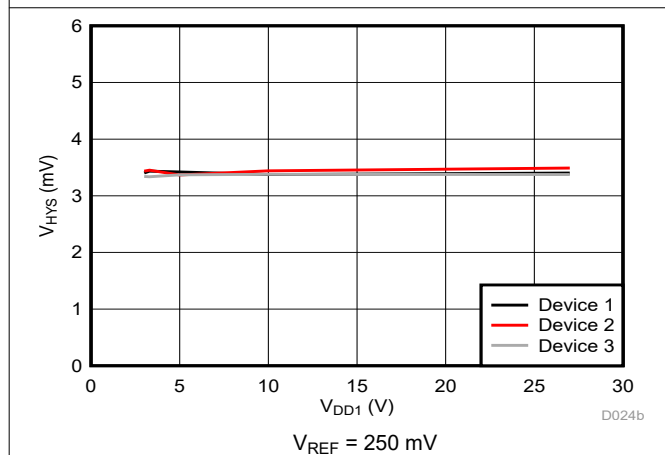
**Figure 6-12. Trip Threshold vs Temperature**



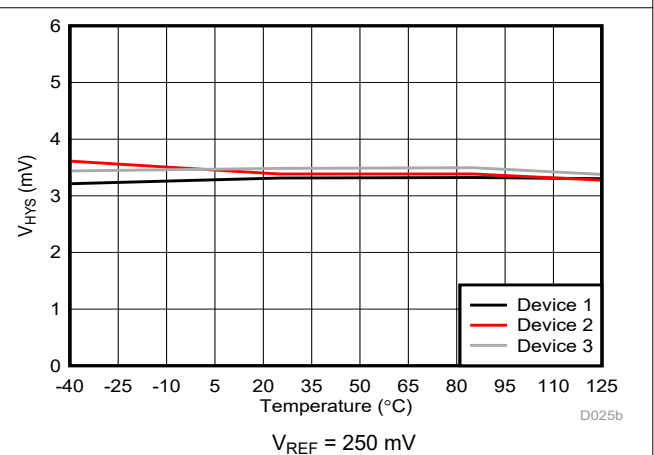
**Figure 6-13. Trip Threshold Error vs Supply Voltage**



**Figure 6-14. Trip Threshold Error vs Temperature**



**Figure 6-15. Trip Threshold Hysteresis vs Supply Voltage**



**Figure 6-16. Trip Threshold Hysteresis vs Temperature**

### 6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)

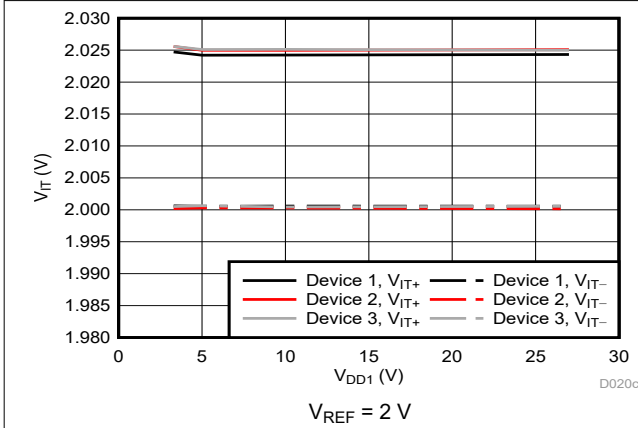


Figure 6-17. Trip Threshold vs Supply Voltage

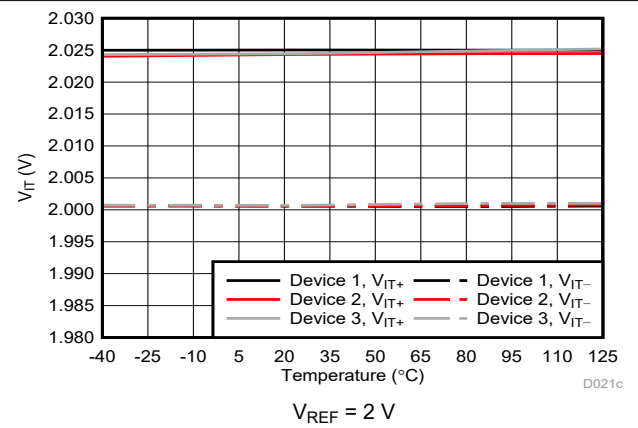


Figure 6-18. Trip Threshold vs Temperature

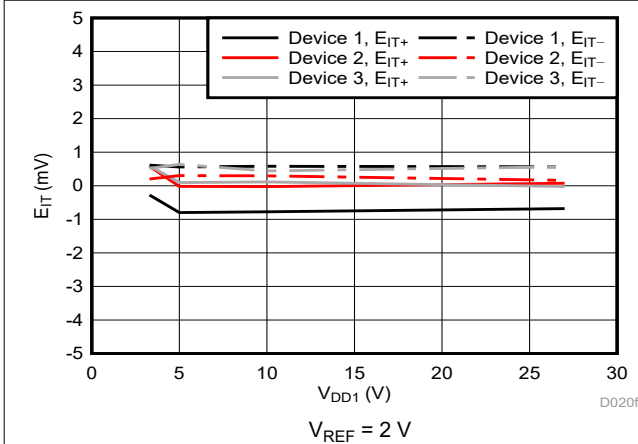


Figure 6-19. Trip Threshold Error vs Supply Voltage

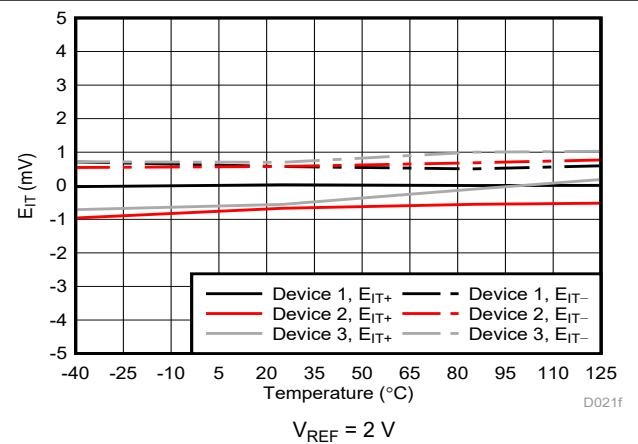


Figure 6-20. Trip Threshold Error vs Temperature

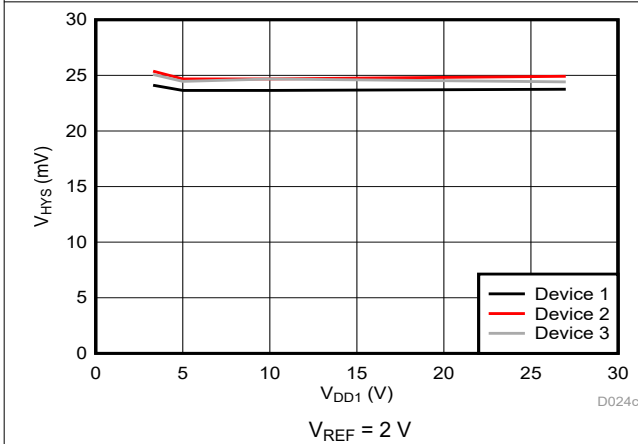


Figure 6-21. Trip Threshold Hysteresis vs Supply Voltage

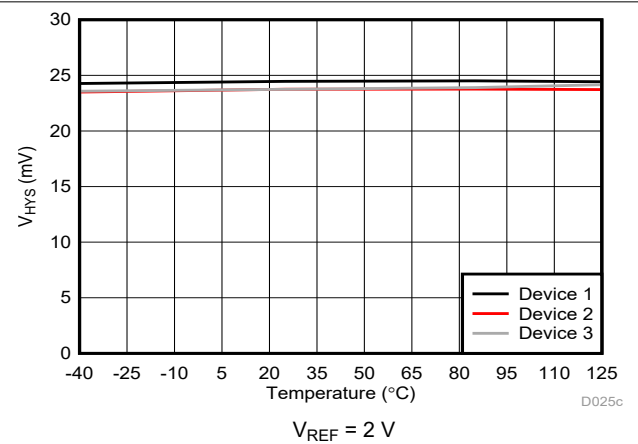


Figure 6-22. Trip Threshold Hysteresis vs Temperature

### 6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)

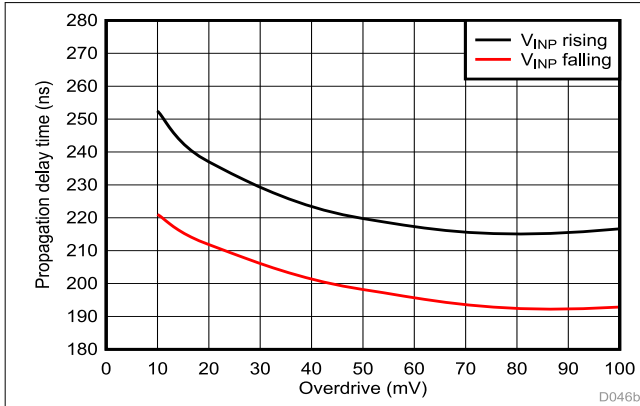


Figure 6-23. Propagation Delay vs Overdrive

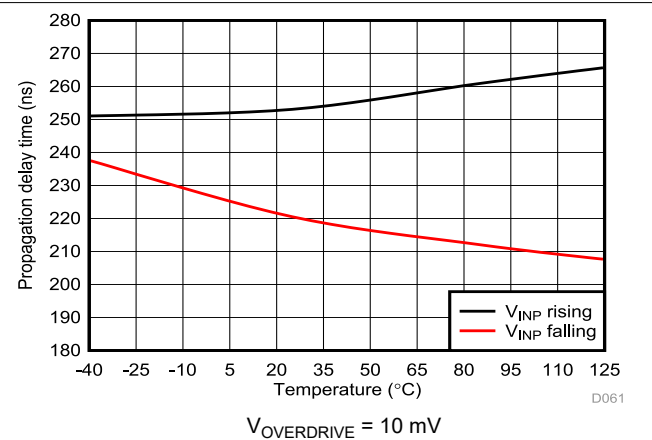


Figure 6-24. Propagation Delay vs Temperature

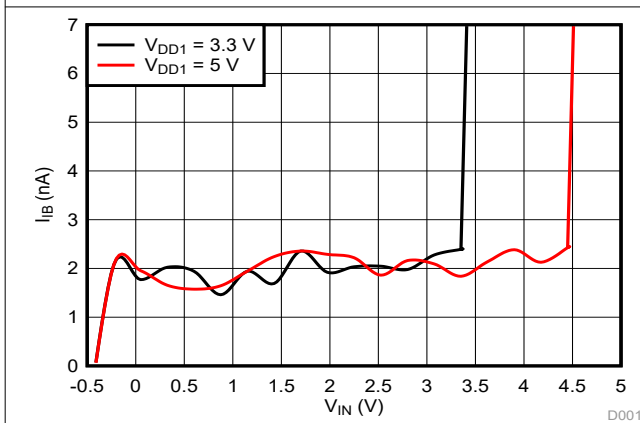


Figure 6-25. Input Bias Current vs Input Voltage

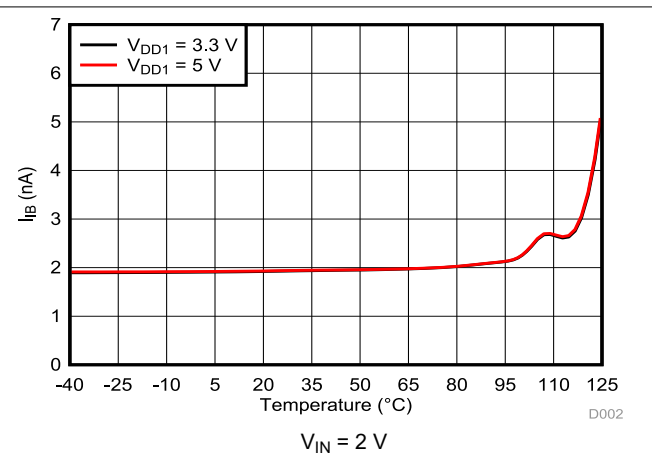


Figure 6-26. Input Bias Current vs Temperature

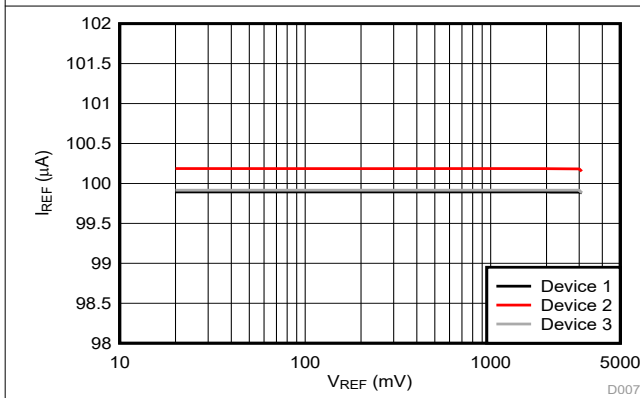


Figure 6-27. Reference Current vs Reference Voltage

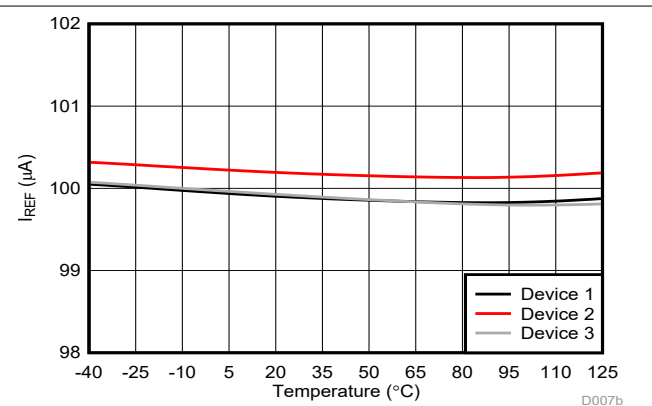


Figure 6-28. Reference Current vs Temperature

### 6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)

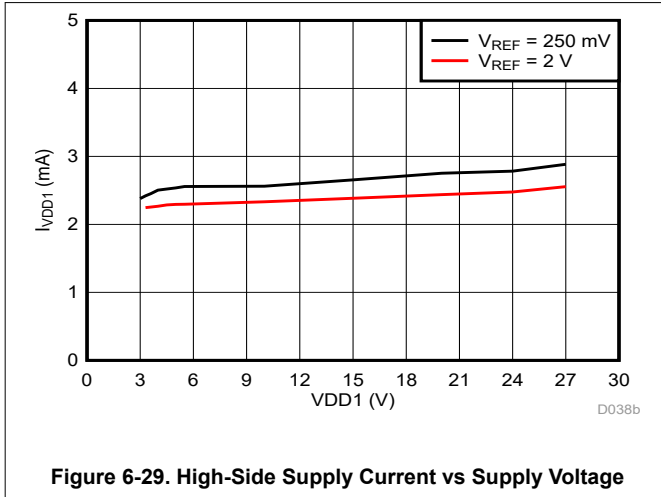


Figure 6-29. High-Side Supply Current vs Supply Voltage

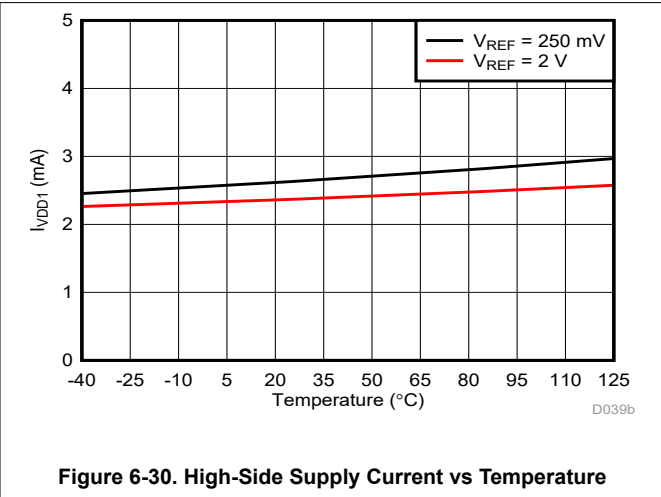


Figure 6-30. High-Side Supply Current vs Temperature

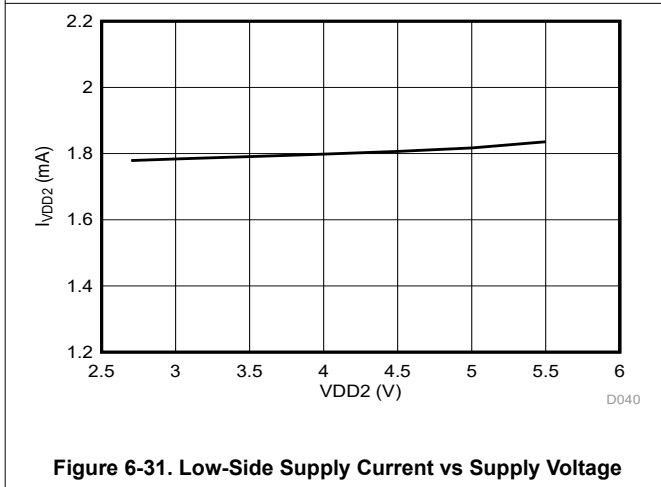


Figure 6-31. Low-Side Supply Current vs Supply Voltage

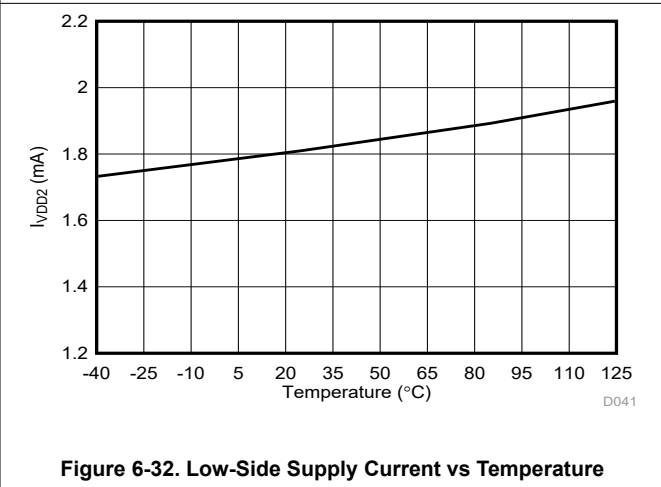


Figure 6-32. Low-Side Supply Current vs Temperature



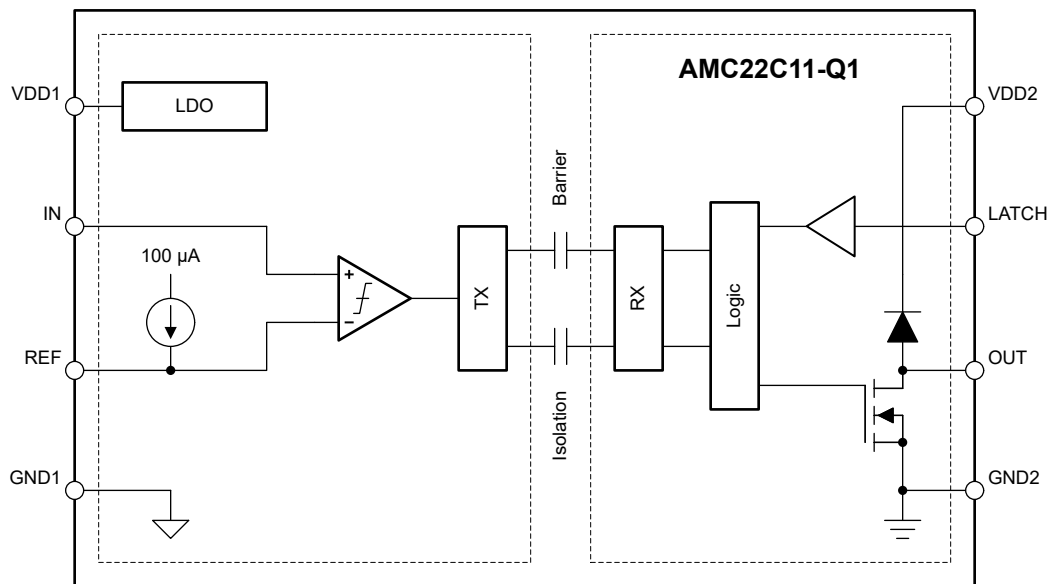
## 7 Detailed Description

### 7.1 Overview

The AMC22C11-Q1 is an isolated comparator with an open-drain output and optional latch function. The comparator compares the input voltage ( $V_{IN}$ ) against the  $V_{IT+}$  threshold that is adjustable from 20 mV to 2.7 V through an internally generated 100- $\mu$ A reference current and a single external resistor. The open-drain output is actively pulled low when the input voltage ( $V_{IN}$ ) is higher than the reference value  $V_{REF}$ . The behavior when  $V_{IN}$  drops below the trip threshold is determined by the LATCH pin, as described in the [Open-Drain Digital Output](#) section.

Galvanic isolation between the high- and low-voltage side of the device is achieved by transmitting the comparator states across a SiO<sub>2</sub>-based, capacitive isolation barrier. This isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application note](#). The digital modulation scheme used in the AMC22C11-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics, result in high reliability and common-mode transient immunity.

### 7.2 Functional Block Diagram



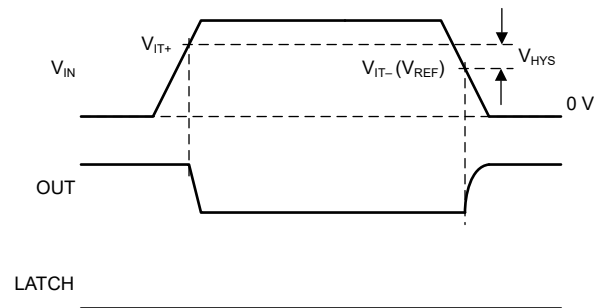
## 7.3 Feature Description

### 7.3.1 Analog Input

The comparator trips when the input voltage ( $V_{IN}$ ) rises above the  $V_{IT+}$  threshold that is defined as the reference value plus the internal hysteresis voltage. The comparator releases when  $V_{IN}$  drops below the  $V_{IT-}$  threshold that equals the reference value.

The difference between  $V_{IT+}$  and  $V_{IT-}$  is referred to as the *comparator hysteresis* and is 4 mV for reference voltages below 450 mV. The integrated hysteresis makes the AMC22C11-Q1 less sensitive to input noise and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis. The hysteresis increases to 25 mV for reference values ( $V_{REF}$ ) greater than 600 mV. See the [Reference Input](#) description for more details.

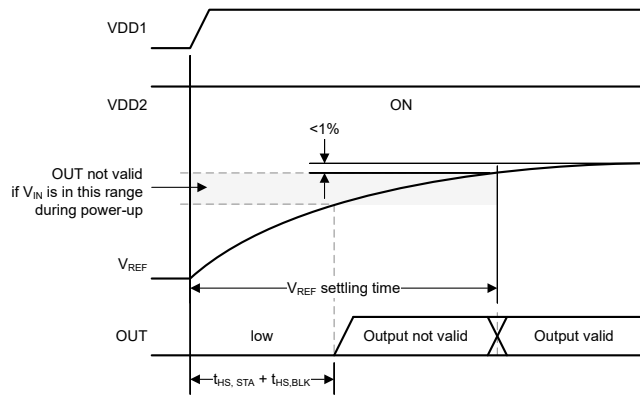
Figure 7-1 shows a timing diagram of the relationship between hysteresis and switching thresholds.



**Figure 7-1. Switching Thresholds and Hysteresis**

### 7.3.2 Reference Input

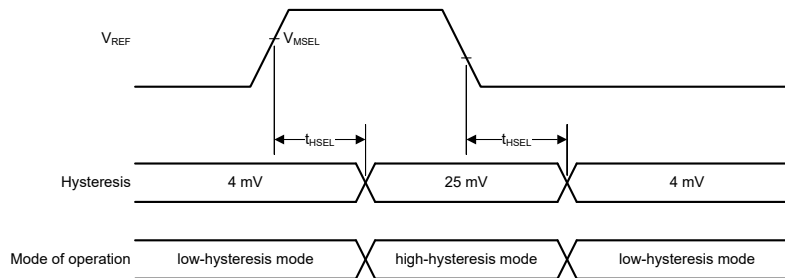
The voltage on the REF pin determines the trip threshold of the comparator. The internal precision current source forces a 100- $\mu$ A current through an external resistor connected from the REF pin to GND1. The resulting voltage across the resistor ( $V_{REF}$ ) equals the trip threshold, see [Figure 7-1](#). Place a 100-nF capacitor parallel to the resistor to filter the reference voltage. This capacitor must be charged by the 100- $\mu$ A current source during power-up and the charging time may exceed the high-side blanking time ( $t_{HS,BLK}$ ). In this case, as shown in [Figure 7-2](#), the comparator may output an incorrect state after the high-side blanking time has expired until  $V_{REF}$  reaches the final value. See the [Power-Up and Power-Down Behavior](#) section for more details on power-up behavior.



**Figure 7-2. Output Behavior for Long Settling Times of the Reference Voltage**

The reference pin can be driven by an external voltage source to change the comparator threshold during operation. However, do not drive  $V_{REF}$  dynamically across the  $V_{MSEL}$  threshold during normal operation because doing so changes the hysteresis of the comparator and can lead to unintentional switching of the output.

[Figure 7-3](#) shows a mode selection timing diagram.

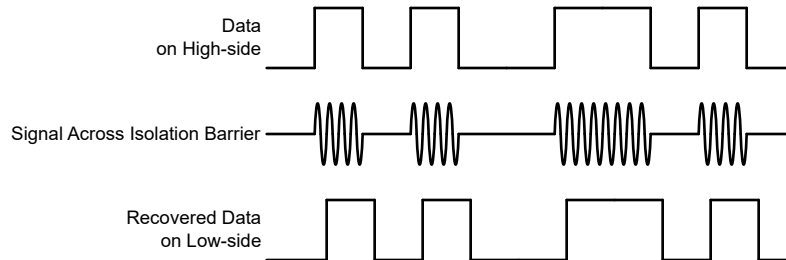


**Figure 7-3. Mode Selection**

### 7.3.3 Isolation Channel Signal Transmission

The AMC22C11-Q1 uses an on-off keying (OOK) modulation scheme, as shown in [Figure 7-4](#), to transmit the comparator output states across the SiO<sub>2</sub>-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the data for the logic that drives the open-drain output buffer. The AMC22C11-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.



**Figure 7-4. OOK-Based Modulation Scheme**

### 7.3.4 Open-Drain Digital Output

The AMC22C11-Q1 provides an open-drain output with optional latching function. The output is actively pulled low when  $V_{IN}$  exceeds the threshold value defined by the voltage on the REF pin, see [Figure 7-1](#).

The open-drain output is diode-connected to the VDD2 supply (see the [Functional Block Diagram](#)), meaning that the output cannot be pulled more than 500 mV above the VDD2 supply before significant current begins to flow into the OUT pin. In particular, the open-drain output is clamped to one diode voltage above ground if VDD2 is at the GND2 level. This behavior is indicated by the gray shadings in [Figure 7-5](#) through [Figure 7-10](#).

On a system level, the CMTI performance of an open-drain signal line depends on the value of the pullup resistor. During a common-mode transient event with a high slew rate (high  $dV/dt$ ), the open-drain signal line may be pulled low due to parasitic capacitive coupling between the high-side and the low-side of the printed circuit board (PCB). The effect of the parasitic coupling on the signal level is a function of the pullup strength and a lower value pullup resistor results in better CMTI performance. The AMC22C11-Q1 has been characterized with a relatively weak pullup resistor value of 10 k $\Omega$  to ensure that the specified CMTI performance is met in a typical application with a 4.7 k $\Omega$  or lower pullup resistor.

#### 7.3.4.1 Transparent Output Mode

The device is set to transparent mode when the LATCH pin is pulled low, thus allowing the output state to change and follow the input signal with respect to the programmed trip threshold. For example, when the input signal rises above the trip threshold, the OUT pin is pulled low. When the input signal drops below the trip threshold, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the OUT pin to a hardware interrupt input on a controller. As soon as an out-of-range condition is detected by the device and the OUT pin is pulled low, the controller interrupt terminal detects the output state change and can begin making changes to the system operation needed to address the out-of-range condition.

#### 7.3.4.2 Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the OUT pin to detect an overcurrent condition. A typical example of this application is a system that is only able to poll the OUT terminal state periodically to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, a change in the state of the OUT pin can be missed if the out-of-range condition does not appear during one of these periodic polling events.

Latch mode is specifically intended to accommodate these applications. The device is placed in latch mode by setting the voltage on the LATCH terminal to a logic high level. The difference between latch mode and transparent mode is how the output responds when an out-of-range event ends. In transparent mode, when the input signal drops below the trip threshold, the output state returns to the default high setting to indicate that the out-of-range event has ended.

In latch mode, when an out-of-range condition is detected and the OUT pin is pulled low, the OUT pin does not return to the default high level when the input signal drops below the trip threshold level. To clear the event, the LATCH terminal must be pulled low for at least 4  $\mu$ s. Pulling the LATCH pin low allows the OUT pin to return to the default high level, provided that the input signal has dropped below the trip threshold. If the input signal is still above the threshold when the LATCH pin is pulled low, the OUT terminal remains low. When the out-of-range event is detected by the system controller, the LATCH pin can be set back to high in order to place the device back into latch mode.

### 7.3.5 Power-Up and Power-Down Behavior

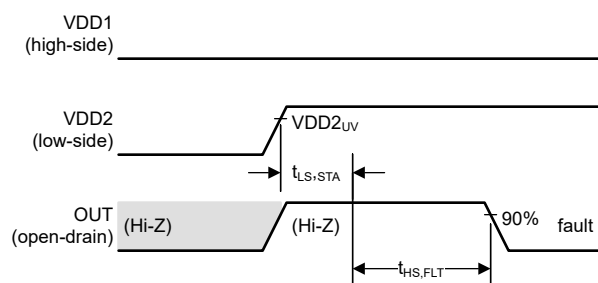
The open-drain output powers up in a high-impedance (Hi-Z) state when the low-side supply (VDD2) turns on. After power-up, if the high-side is not functional yet, the output is actively pulled low. This condition happens after the low-side start-up time plus the high-side fault detection delay time ( $t_{LS,STA} + t_{HS,FLT}$ ), as shown in Figure 7-5. Similarly, if the high-side supply drops below the undervoltage threshold (VDD1<sub>UV</sub>) for more than the high-side fault detection delay time during normal operation, the open-drain output is pulled low, as shown in Figure 7-8. This delay allows the system to shut down reliably when the high-side supply is missing.

Communication start between the high-side and low-side of the comparator is delayed by the high-side blanking time ( $t_{HS,BLK}$ , a time constant implemented on the high-voltage side) to allow the voltage on the REF pin to settle, and to avoid unintentional switching of the comparator output during power-up.

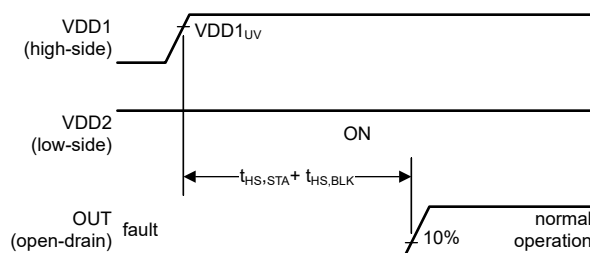
Figure 7-5 through Figure 7-10 depict typical power-up and power-down scenarios.

In Figure 7-5, the low-side supply (VDD2) turns on but the high-side supply (VDD1) remains off. The output powers up in a Hi-Z state. After  $t_{HS,FLT}$ , OUT is pulled low indicating a no-power fault on the high-side.

In Figure 7-6, the high-side supply (VDD1) turns on long after the low-side supply (VDD2) turns on. The output is initially in an active-low state, see case (1). After the high-side supply is enabled, there is a duration of  $t_{HS,STA} + t_{HS,BLK}$  before the device assumes normal operation and the output reflects the current state of the comparator.



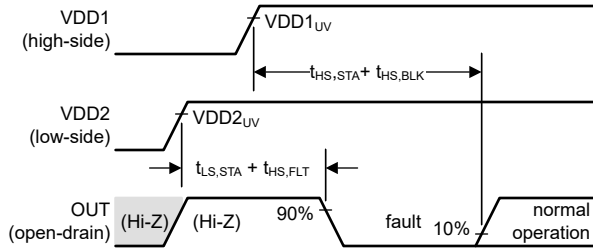
**Figure 7-5. VDD2 Turns On, VDD1 Stays Off**



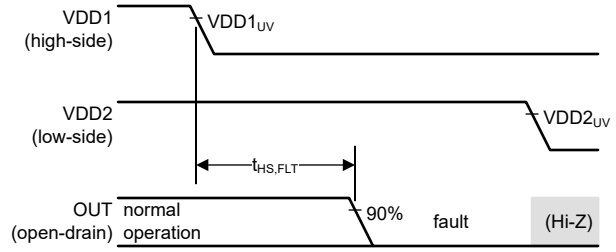
**Figure 7-6. VDD2 is On; VDD1 Turns On (Long Delay)**

In Figure 7-7, the low-side supply (VDD2) turns on, followed by the high-side supply (VDD1) with only a short delay. The output is initially in a Hi-Z state. The high-side fault detection delay ( $t_{HS,FLT}$ ) is shorter than the high-side blanking time ( $t_{HS,BLK}$ ), and therefore the output is pulled low after  $t_{HS,FLT}$ , indicating that the high-side is not operational yet. After the high-side blanking time ( $t_{HS,BLK}$ ) elapses, the device assumes normal operation and the output reflects the current state of the comparator.

In Figure 7-8, the high-side supply (VDD1) turns off, followed by the low-side supply (VDD2). After the high-side fault detection delay time ( $t_{HS,FLT}$ ), the output is actively pulled low. As soon as VDD2 drops below the VDD2<sub>UV</sub> threshold, the output enters a Hi-Z state.



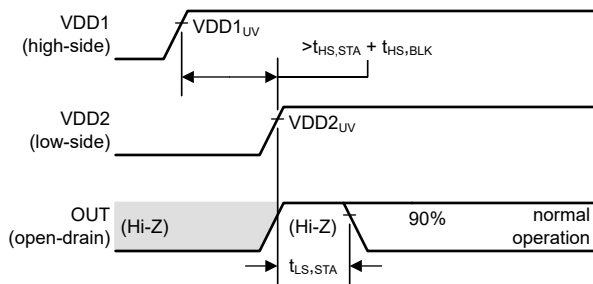
**Figure 7-7. VDD2 Turns On, Followed by VDD1 (Short Delay)**



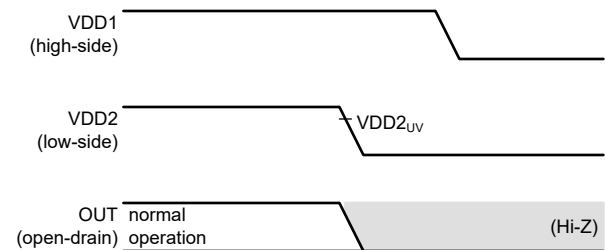
**Figure 7-8. VDD1 Turns Off, Followed by VDD2**

In [Figure 7-9](#), the low-side supply (VDD2) turns on after the high-side is fully powered up (the delay between VDD1 and VDD2 is greater than  $(t_{HS,STA} + t_{HS,BLK})$ ). After the low-side start-up time ( $t_{LS,STA}$ ), the device enters normal operation.

In [Figure 7-10](#), the low-side supply (VDD2) turns off, followed by the high-side supply (VDD1). As soon as VDD2 drops below the  $VDD2_{UV}$  threshold, the output enters a Hi-Z state.



**Figure 7-9. VDD1 Turns On, Followed by VDD2 (Long Delay)**



**Figure 7-10. VDD2 Turns Off, Followed by VDD1**

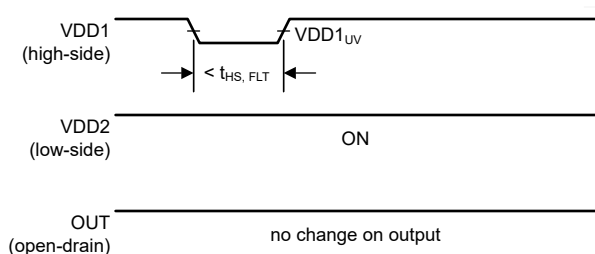
### 7.3.6 VDD1 Brownout and Power-Loss Behavior

Brownout is a condition where the VDD1 supply droops below the specified operating voltage range but the device remains functional. Power-loss is a condition where the VDD1 supply drops below a level where the device stops being functional. Depending on the duration and the voltage level, a brownout condition may or may not be noticeable at the output of the device. A power-loss condition is always signaled on the output of the isolated comparator.

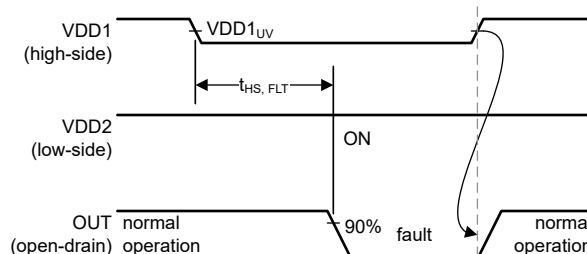
Figure 7-11 through Figure 7-13 show typical brownout and power-loss scenarios.

In Figure 7-11, VDD1 droops below the undervoltage detection threshold ( $VDD1_{UV}$ ) but recovers before the high-side-fault detection delay time ( $t_{HS,FLT}$ ) expires. The brownout event has no effect on the comparator output.

In Figure 7-12, VDD1 droops below the undervoltage detection threshold ( $VDD1_{UV}$ ) for more than the high-side-fault detection delay time ( $t_{HS,FLT}$ ). The brownout condition is detected as a fault and the output is pulled low after a delay equal to  $t_{HS,FLT}$ . The device resumes normal operation as soon as VDD1 recovers above the  $VDD1_{UV}$  threshold.

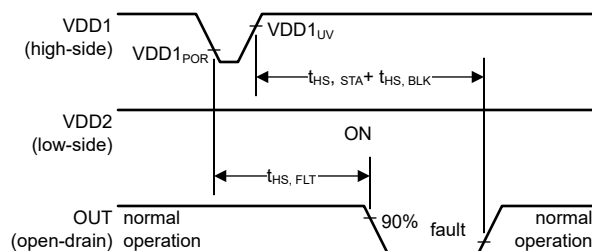


**Figure 7-11. Output Response to a Short Brownout Event on VDD1**



**Figure 7-12. Output Response to a Long Brownout Event on VDD1**

In Figure 7-13, VDD1 droops below the power-on-reset (POR) threshold ( $VDD1_{POR}$ ). The power-loss condition is detected as a fault and the output is pulled low after a delay equal to  $t_{HS,FLT}$ . The device resumes normal operation after a delay equal to  $t_{HS,STA} + t_{HS,BLK}$  after VDD1 recovers above the  $VDD1_{UV}$  threshold.



**Figure 7-13. Output Response to a Power-Loss Event on VDD1**



## 7.4 Device Functional Modes

The AMC22C11-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the [Recommended Operating Conditions](#) table.

The voltage on the REF pin affects the threshold of the comparator. For reference voltages below the  $V_{MSEL}$  threshold, the comparator operates in low-hysteresis mode. For reference voltages above the  $V_{MSEL}$  threshold, the comparator operates in high-hysteresis mode as described in the [Reference Input](#) section.

The device has two output operating modes that are selected based on the LATCH input pin setting: transparent mode and latch mode. These modes affect how the OUT pin responds to the changing input signal conditions. See the [Open-Drain Digital Output](#) section for details.

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

---

### 8.1 Application Information

With the device low response time, high common-mode transient immunity (CMTI), and basic-certified isolation barrier, the AMC22C11-Q1 is designed to provide fast and reliable overcurrent and overvoltage detection for high-voltage applications in harsh and noisy environments.

### 8.2 Typical Application

#### 8.2.1 DC Link Overcurrent Detection

DC link overcurrent detection is a common requirement in DC/DC converter and motor-drive designs. Although the inductor current of a DC/DC converter or the phase currents of a motor drive are typically sensed for control purposes, phase current monitoring alone is not sufficient to detect all possible overcurrent conditions (such as shoot-through in the power stage). The most comprehensive way of implementing DC link overcurrent detection is to monitor the current in the DC+ and DC– lines. This detection, as illustrated in [Figure 8-1](#), can be achieved by monitoring the voltage drop across two shunt resistors.

The DC+ load current flowing through the shunt resistor R10 produces a positive voltage in respect to GND1 that is monitored by the AMC22C11-Q1. When the voltage drop across R10 exceeds the reference value set by the external resistor R11, the comparator trips and signals the overcurrent event on the open-drain output OUT.

The DC– load current flowing through the shunt resistor R20 produces a negative voltage in respect to GND1 that is monitored by a [AMC22C12-Q1](#). When the voltage drop across R20 exceeds the reference value set by the external resistor R21, the comparator trips and signals the overcurrent event on the open-drain output OUT.

The open-drain outputs from both isolated comparators are shorted together to form a single alert signal to the microcontroller unit (MCU). Similarly, both LATCH signals are tied together and can be controlled by a single GPIO pin from the MCU.

The isolated comparator on the DC+ side requires a high-side power supply that is referenced to the DC+ potential. A low-cost solution is based on the push-pull driver [SN6501-Q1](#) and a transformer that supports the desired isolation voltage ratings. The integrated low-dropout (LDO) regulator on the high-side of the AMC22C11-Q1 allows direct connection of the VDD1 pin to the transformer output and no further preregulation of the transformer output voltage is required.

The isolated comparator on the DC– side requires a high-side power supply that is referenced to the DC– potential. A common solution is to power the isolated comparator from the low-side gate driver supply, as illustrated in [Figure 8-1](#), or any other voltage supply referenced to DC–. The integrated low-dropout (LDO) regulator on the high-side of the AMC22C12-Q1 supports a wide range of input voltages and greatly simplifies the power-supply design.

The fast response time and high common-mode transient immunity (CMTI) of the AMC22C11-Q1 ensure reliable and accurate operation even in high-noise environments.

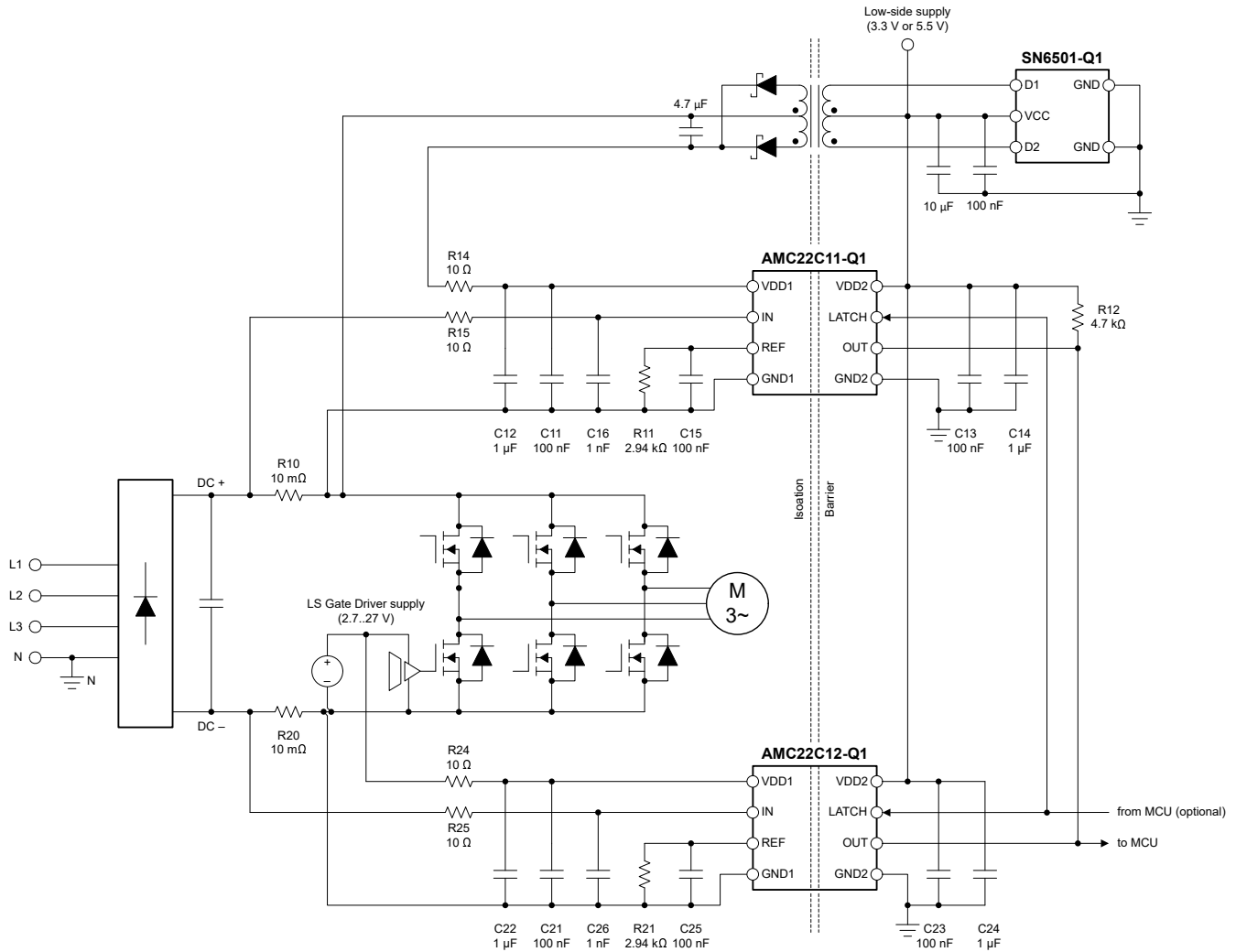


Figure 8-1. Using the AMC22C11-Q1 for DC+ Overcurrent Detection

### 8.2.1.1 Design Requirements

Table 8-1 lists the parameters for the application example in Figure 8-1.

Table 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3 V to 27 V
Low-side supply voltage	2.7 V to 5.5 V
Shunt-resistor value	10 mΩ
Overcurrent detection threshold	30 A

### 8.2.1.2 Detailed Design Procedure

The value of the shunt resistors (R10 and R20) in this example is 10 mΩ. At the desired 30-A overcurrent detection level, the voltage drop across the shunt resistor is  $10 \text{ m}\Omega \times 30 \text{ A} = 300 \text{ mV}$ . The positive-going trip threshold of the comparator is  $V_{\text{REF}} + V_{\text{HYS}}$ , where  $V_{\text{HYS}}$  is 4 mV (as specified in the [Electrical Characteristics](#) table) and  $V_{\text{REF}}$  is the voltage across R11 (R12, respectively) that is connected between the REF and GND1 pins. R11 and R12 are calculated as  $(V_{\text{TRIP}} - V_{\text{HYS}}) / I_{\text{REF}} = (300 \text{ mV} - 4 \text{ mV}) / 100 \mu\text{A} = 2.96 \text{ k}\Omega$ . The next lower value from the E96 series (1% accuracy) is 2.94 kΩ, resulting in an overcurrent trip threshold (rising) of 29.8 A.

A 10-Ω, 1-nF RC filter (R15, C16 and R25, C26, respectively) is placed at the input of the comparator to filter the input signal and reduce noise sensitivity. This filter adds  $10 \Omega \times 1 \text{ nF} = 10 \text{ ns}$  of propagation delay that must be considered when calculating the overall response time of the protection circuit. Larger filter constants are preferable to increase noise immunity if the system can tolerate the additional delay.

Table 8-2 summarizes the key parameters of the design.

**Table 8-2. Overcurrent Detection Design Example**

PARAMETER	VALUE
Reference resistor value (R11, R21)	2.94 kΩ
Reference capacitor value (C15, C25)	100 nF
Reference voltage	296 mV
Reference voltage settling time (to 90% of final value)	690 μs
Overcurrent trip threshold (rising)	298 mV / 29.8 A
Overcurrent trip threshold (falling)	294 mV / 29.4 A

### 8.3 Application Curves

Figure 8-2 shows the typical response of the AMC22C11-Q1 to a triangular input waveform with an amplitude of 310 mV<sub>PP</sub>. The output (OUT) switches when VIN crosses the 250-mV level determined by the REF pin voltage that is biased to 250 mV in this example.

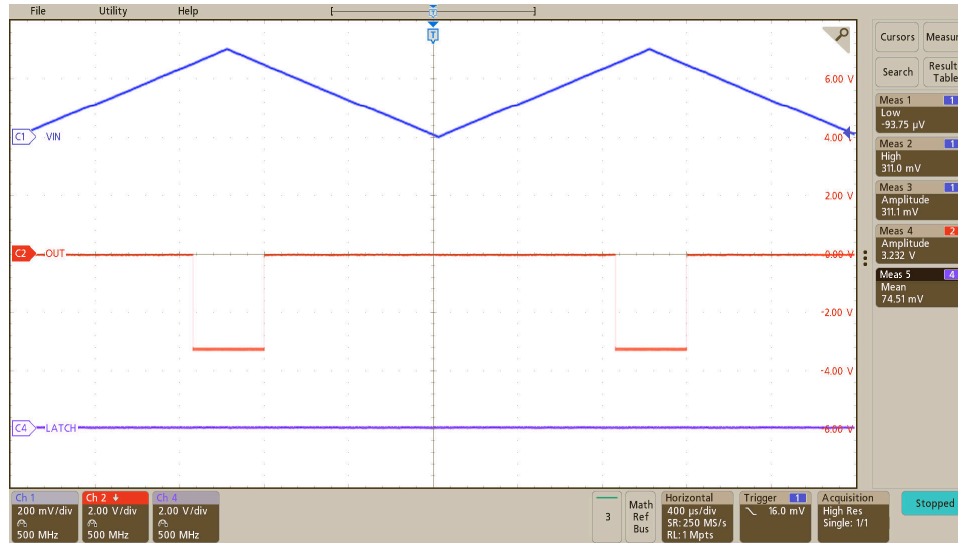


Figure 8-2. Output Response of the AMC22C11-Q1 to a Triangular Input Waveform

The integrated LDO of the AMC22C11-Q1 greatly relaxes the power-supply requirements on the high-voltage side and allows powering the device from non-regulated transformer, charge pump, and bootstrap supplies. As given by the following image, the internal LDO provides a stable operating voltage to the internal circuitry, allowing the trip thresholds to remain mostly undisturbed even at ripple voltages of 2 V<sub>PP</sub> and higher.

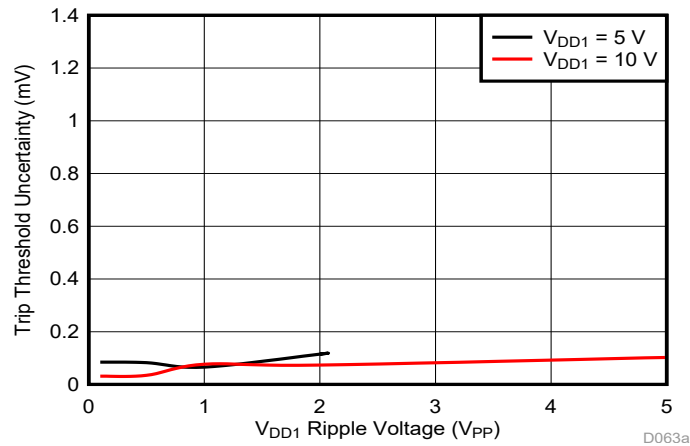


Figure 8-3. Trip Threshold Sensitivity to VDD1 Ripple Voltage ( $f_{\text{RIPPLE}} = 10 \text{ kHz}$ )

## 8.4 Best Design Practices

Keep the connection between the low-side of the sense resistor and the GND1 pin of the AMC22C11-Q1 short and low impedance. Any voltage drop in the ground line adds error to the voltage sensed at the input of the comparator and leads to inaccuracies in the trip thresholds.

For best common-mode transient immunity, place the filter capacitor C5 as closely to the REF pin as possible as illustrated in [Figure 8-5](#). Use a low value pullup resistor (<10 k $\Omega$ ) on the open-drain output, as explained in the [Open-Drain Digital Output](#) section, to minimize the effect of capacitive coupling on the open-drain signal line during a common-mode transient event.

Do not operate the device with the REF pin biased close to the  $V_{MSEL}$  threshold (450-mV to 600-mV range) to avoid dynamic switching of the comparator hysteresis as explained in the [Reference Input](#) section.

The AMC22C11-Q1 provides a limited 200- $\mu$ s blanking time ( $t_{HS,BLK}$ ) to allow the reference voltage ( $V_{REF}$ ) to settle during start up. For many applications, the reference voltage takes longer to settle than the 200- $\mu$ s blanking time and the output of the comparator can possibly glitch during system start up as described in [Figure 7-2](#). Consider the reference voltage settling time in the overall system start-up design.

## 8.5 Power Supply Recommendations

The AMC22C11-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1- $\mu$ F capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1- $\mu$ F capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 8-4 shows a decoupling schematic for the AMC22C11-Q1.

For high VDD1 supply voltages (>5.5 V) place a 10- $\Omega$  resistor (R4) in series with the VDD1 power supply for additional filtering.

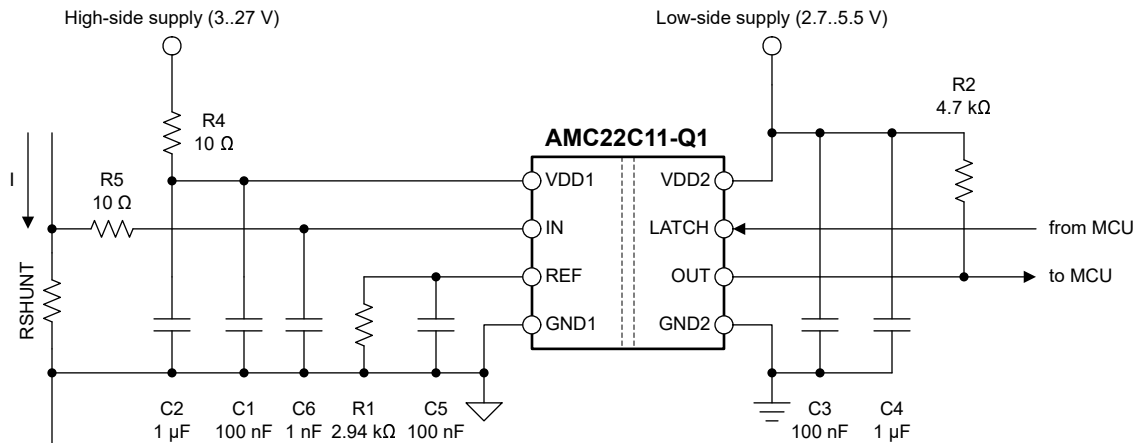


Figure 8-4. Decoupling of the AMC22C11-Q1

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

## 8.6 Layout

### 8.6.1 Layout Guidelines

Figure 8-5 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC22C11-Q1 supply pins) and placement of the other components required by the device.

### 8.6.2 Layout Example

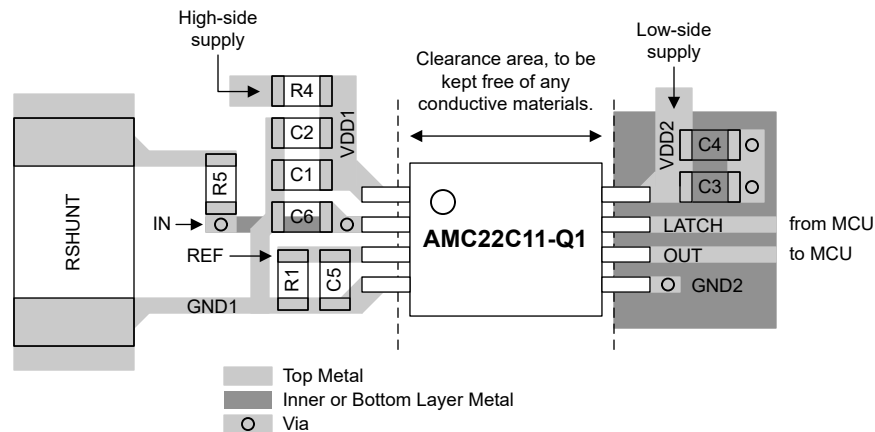


Figure 8-5. Recommended Layout of the AMC22C11-Q1

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary application note](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application note](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application note](#)
- Texas Instrument, [SN6501-Q1 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator design tool](#)

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on [Subscribe to updates](#) to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 9.4 Trademarks

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#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



### 10.1 Mechanical Data

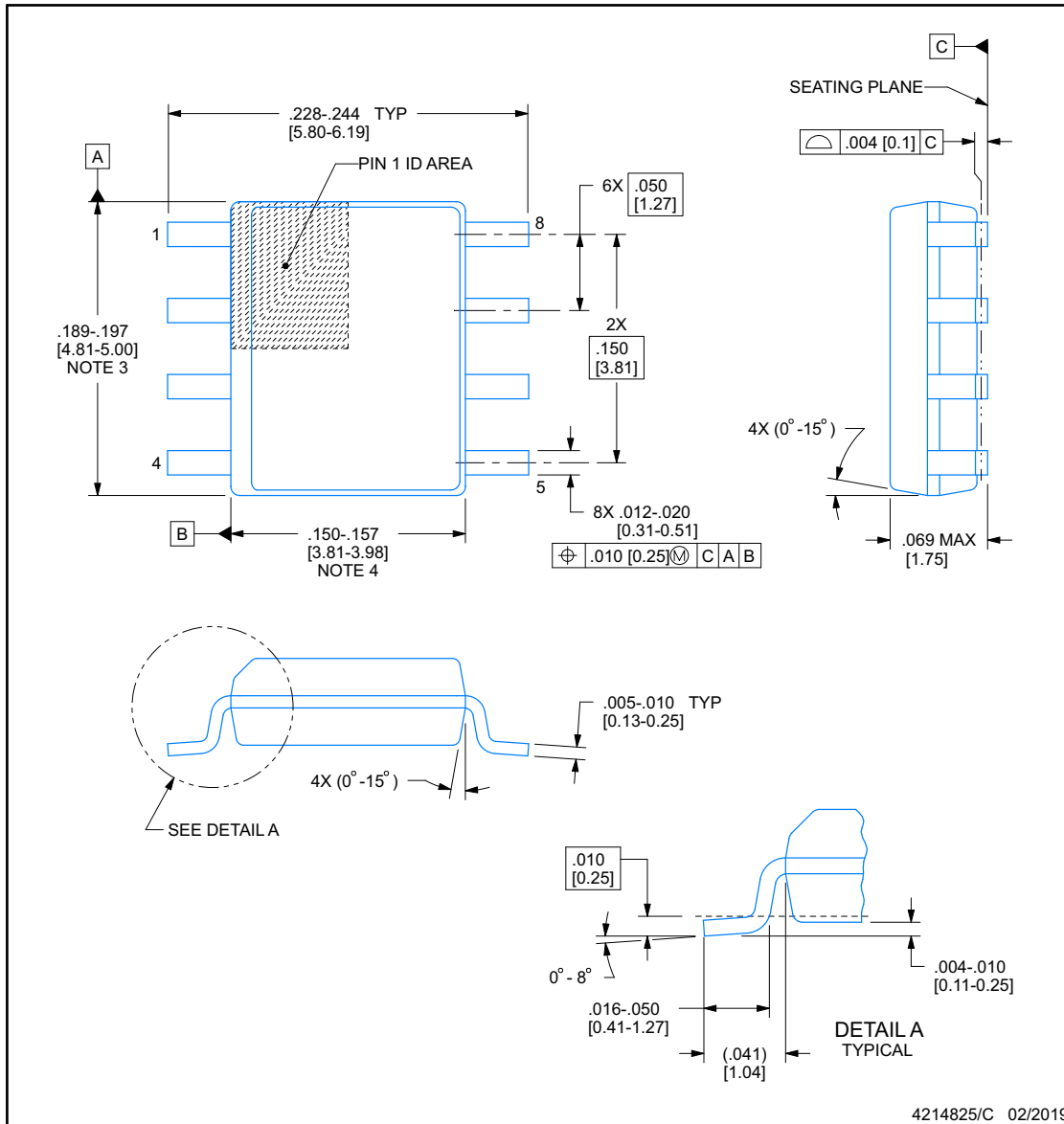


## PACKAGE OUTLINE

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



**NOTES:**

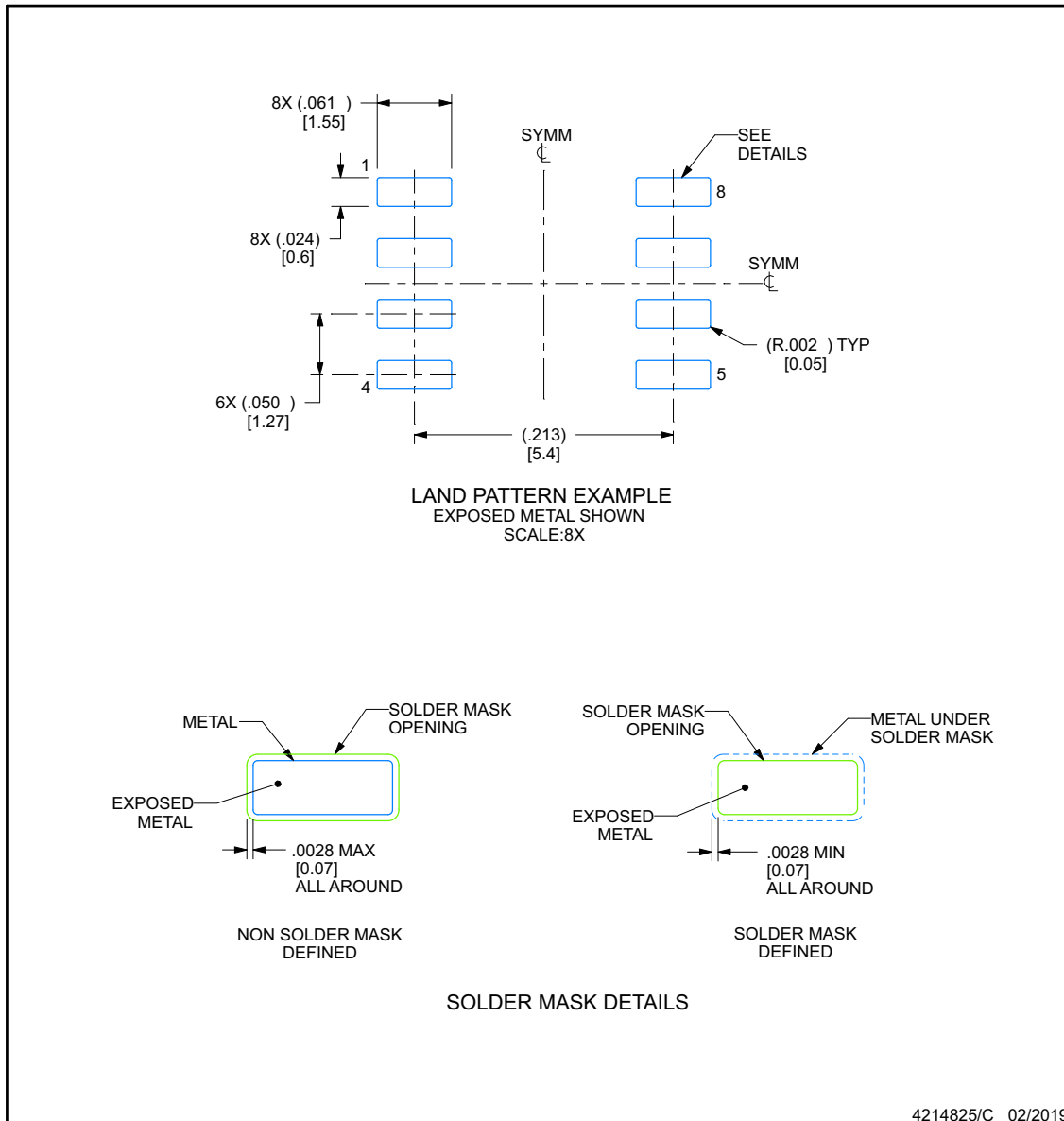
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

## EXAMPLE BOARD LAYOUT

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

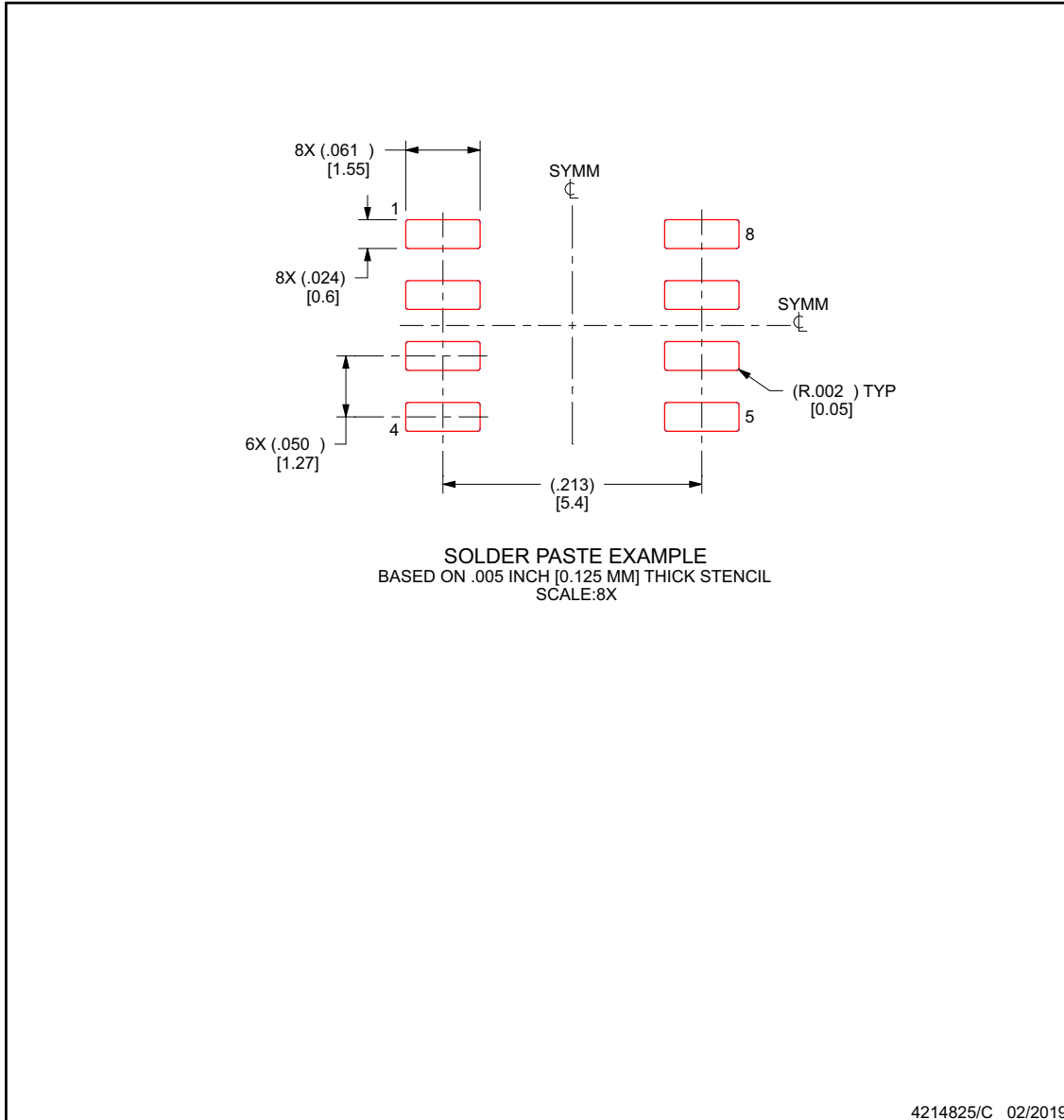
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC22C11QDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22C11Q	<a href="#">Samples</a>
PAMC22C11QDRQ1	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF AMC22C11-Q1 :**

- Catalog : [AMC22C11](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC22C11QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC22C11QDRQ1	SOIC	D	8	3000	356.0	356.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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