Low Noise, Dimmable EL Lamp Driver

Features

- Adjustable output regulation for dimming
- 220V_{PP} output voltage for higher brightness
- Single cell lithium ion compatible
- 150nA shutdown current
- Separately adjustable lamp and converter frequencies
- 3x3mm 12-Lead QFN package
- Split supply capability

Applications

- Mobile cellular phone keypads
- PDAs
- Handheld wireless communication products
- Global Positioning Systems (GPS)

General Description

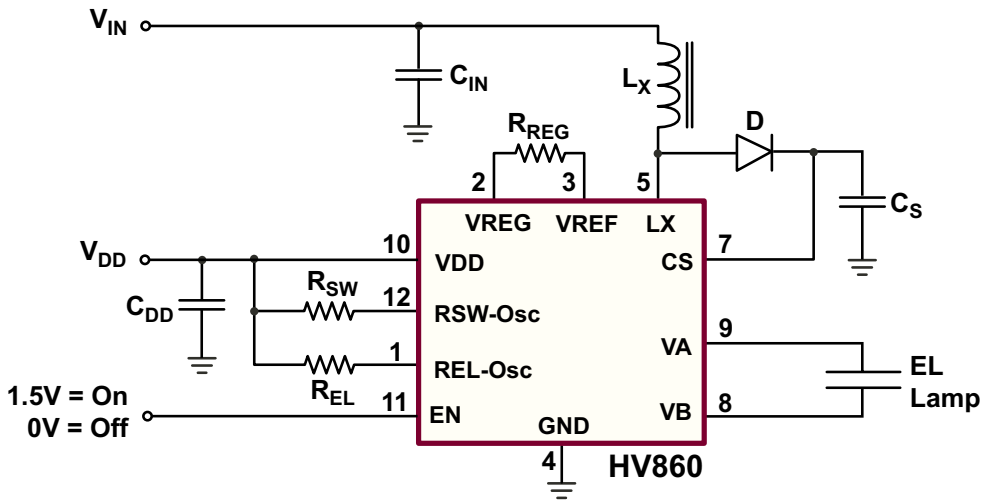
The Supertex HV860 is a high voltage driver designed for driving Electroluminescent, (EL), lamps of up to 5 square inches. The input supply voltage range is from 2.5 to 4.5V. The device uses a single inductor and a minimum number of passive components. Using the internal reference voltage, the regulated output voltage is at a nominal voltage of 110V. The EL lamp will therefore see ±110V. An enable pin, (EN), is available to turn the device on and off via a logic signal.

The HV860 has two internal oscillators, a switching MOSFET, and a high voltage EL lamp driver H-bridge. The frequency for the switching MOSFET is set by an external resistor connected between the RSW-Osc pin and the supply pin VDD. The EL lamp driver frequency is set by an external resistor connected between REL-Osc pin and VDD pin. An external inductor is connected between the LX and VDD pins or VIN for split supply applications. A 3.0nF capacitor is connected between CS and ground. The EL lamp is connected between VA and VB.

The switching MOSFET charges the external inductor and discharges it into the capacitor at CS. The voltage at CS will start to increase. Once the voltage at CS reaches a nominal value of 110V, the switching MOSFET is turned OFF to conserve power. The outputs VA and VB are configured as an H bridge and are switching in opposite states to achieve ±110V across the EL lamp.

EL lamp dimming can be accomplished by changing the input voltage to the VREG pin. The VREG pin allows an external voltage source to control the VCS amplitude. The VCS voltage is approximately 87 times the voltage seen on VREG.

Typical Application Circuit

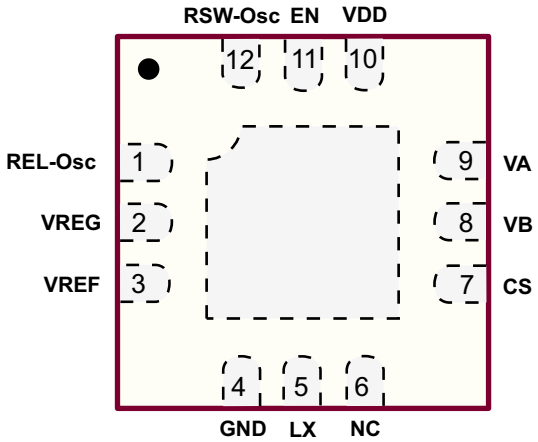


Ordering Information

Device	12-Lead QFN *3.00x3.00mm body* *0.80mm height (max)* *0.50mm pitch*
HV860	HV860K7-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



12-Lead QFN (K7)

(top view)

Note:

Pads are at the bottom of the package. Center heat slug is at ground potential.

Absolute Maximum Ratings

Parameter	Value
V_{DD}, Supply voltage	-0.5V to 6.0V
Operating temperature	-40°C to +85°C
Storage temperature	-65°C to +150°C
Power dissipation:	1.6W
V_{CS}, Output voltage	-0.5V to +120V
V_{REG} External input voltage	1.33V

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
——— = "Green" Packaging

Package may or may not include the following marks: Si or

12-Lead QFN (K7)

Thermal Resistance

Package	θ_{ja}
12-Lead QFN (K7)	60 °C/W

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	2.5	-	4.5	V	---
f_{SW}	Switching frequency	40	-	200	kHz	---
f_{EL}	EL output frequency	150	-	500	Hz	---
C_{LOAD}	EL lamp capacitance load	0	-	20	nF	---
T_A	Operating temperature	-40	-	+85	°C	---

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{DS(ON)}$	On-resistance of switching transistor	-	-	6.0	Ω	I = 100mA
V_{CS}	Maximum output regulation voltage	90	-	120	V	V_{DD} = 2.5V to 4.5V

Electrical Characteristics *(cont.)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{CS}	Output regulation voltage	-	95	-	V	V_{DD} = 2.5 to 4.5V, V_{REG} = 1.092V
		-	75	-		V_{DD} = 2.5 to 4.5V, V_{REG} = 0.862V
		-	55	-		V_{DD} = 2.5 to 4.5V, V_{REG} = 0.632V
V_{REG}	External input voltage range	0	-	1.33	V	V_{DD} = 2.5 to 4.5V
V_{REFH}	V_{REF} output high voltage	1.18	1.26	1.33	V	V_{DD} = 2.5 to 4.5V
I_{DDQ}	Quiescent V_{DD} supply current	-	-	150	nA	EN = Low
I_{DD}	Input current going into the VDD pin	-	-	250	µA	V_{DD} = 2.5 to 4.5V, R_{EL} = 2.0MΩ, R_{SW} = 1.0MΩ
I_{IN}	Input current including inductor current	-	16	30	mA	V_{IN} = 3.0V. See Figure 1.
I_{INQ}	Quiescent V_{IN} supply current	-	-	200	nA	V_{IN} = 4.2V. EN = Low. See Figure 1.
f_{EL}	EL lamp frequency	160	200	240	Hz	R_{EL} = 2.0MΩ
f_{SW}	Switching transistor frequency	76	90	104	kHz	R_{SW} = 1.0MΩ
D	Switching transistor duty cycle	-	-	88	%	---
V_{IH}	Enable input logic high voltage	1.5	-	V_{DD}	V	V_{DD} = 2.5 to 4.5V
V_{IL}	Enable input logic low voltage	0	-	0.2	V	V_{DD} = 2.5 to 4.5V
I_{IH}	Enable input logic high current	-	-	100	µA	V_{IH} = V_{DD} = 2.5 to 4.5V
I_{IL}	Enable input logic low current	-	-	-1.0	µA	V_{IL} = 0V, V_{DD} = 2.5 to 4.5V
C_{IN}	Enable input capacitance	-	-	15	pF	---

Block Diagram

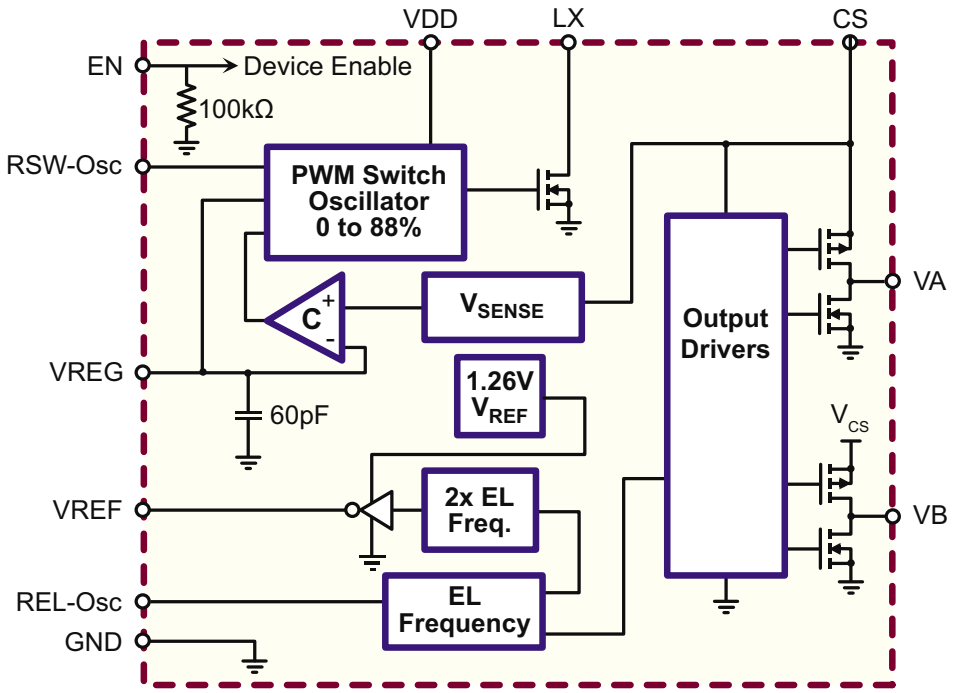
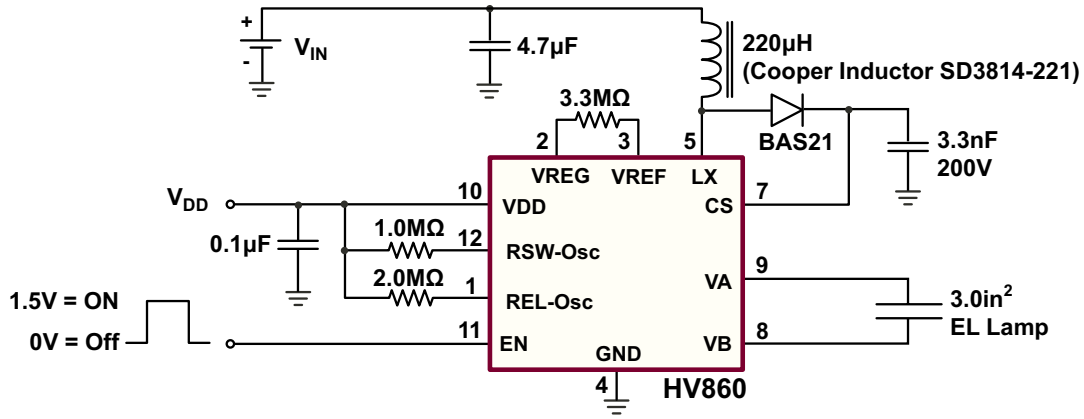


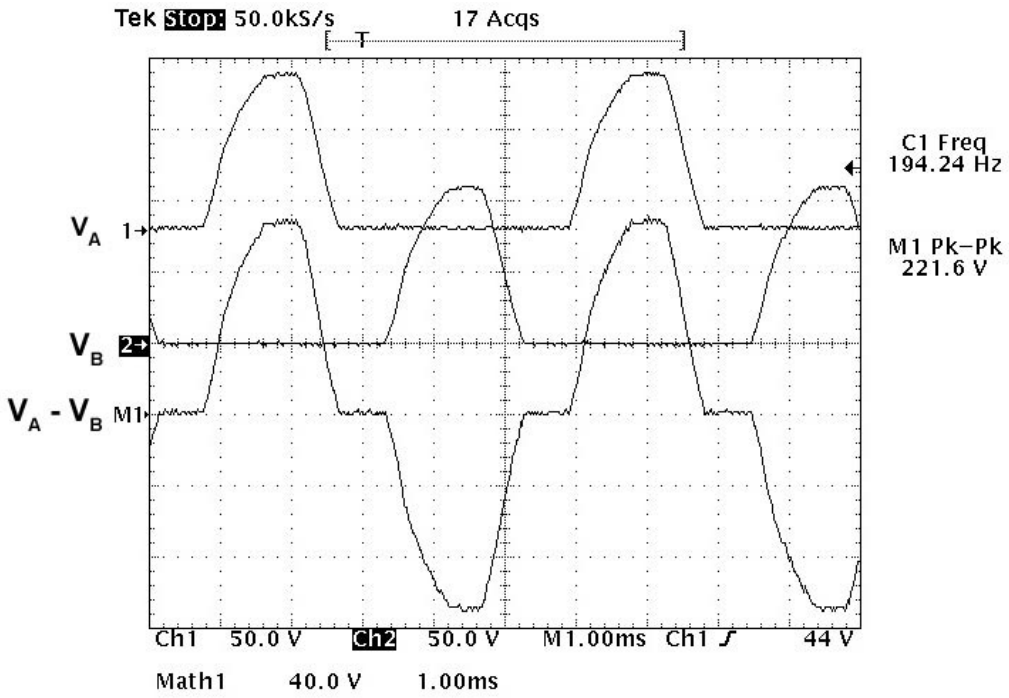
Figure 1: Typical Application / Test Circuit



Typical Performance

V_{DD}	Lamp Size	V_{IN}	I_{IN}	V_{CS}	f_{EL}	Brightness
3.0V	3.0in²	3.3V	19.42mA	110V	194Hz	20.32cd/m²
		3.7V	17.95mA			21.40cd/m²
		4.2V	16.02mA			21.81cd/m²

Typical Waveform on V_A, V_B, and Differential Waveform V_A - V_B



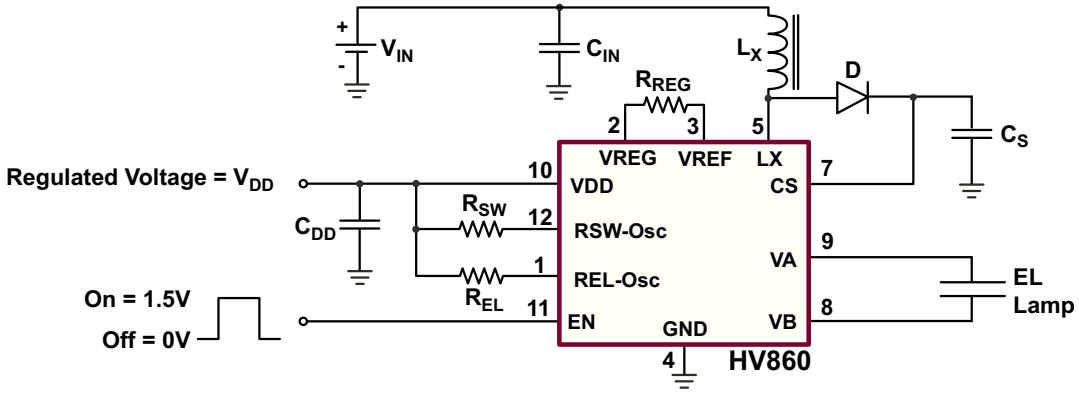
Split Supply Configuration

The HV860 can also be used for handheld devices operating from a battery where a regulated voltage is available. This is shown in Figure 2. The regulated voltage can be used to run the internal logic of the HV860. The amount of current necessary to run the internal logic is 250µA max. Therefore, the regulated voltage could easily provide the current without being loaded down.

Enable/Disable Configuration

The HV860 can be easily enabled and disabled via a logic control signal on the EN pin as shown in Figure 2. The control signal can be from a microprocessor. When the microprocessor signal is high the device is enabled, and when the signal is low, it is disabled.

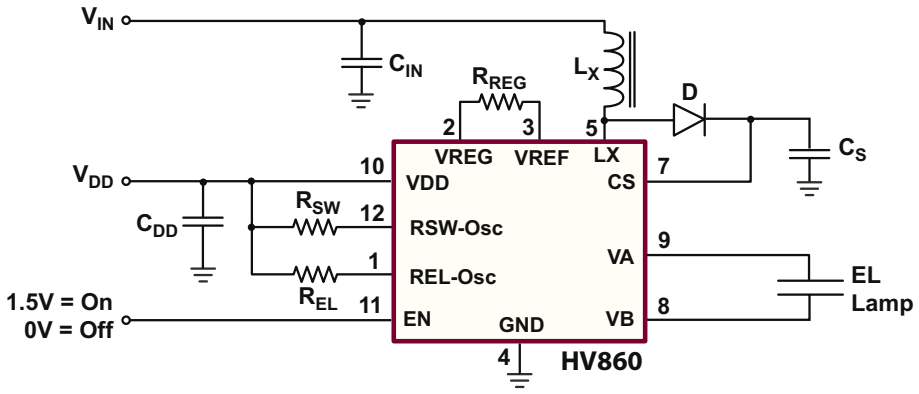
Figure 2: Split Supply and Enable/Disable Configuration



Audible Noise Reduction

The EL lamp, when lit, emits an audible noise. This is due to EL lamp construction. The audible noise generated by the EL lamp can be a major problem for applications where the EL lamp is held close to the ear, such as cellular phones. The HV860 employs a proprietary circuit to help minimize the EL lamp's audible noise by using a single resistor, R_{REG}, as shown in Figure 3.

Figure 3: Typical Application Circuit for Audible Noise Reduction



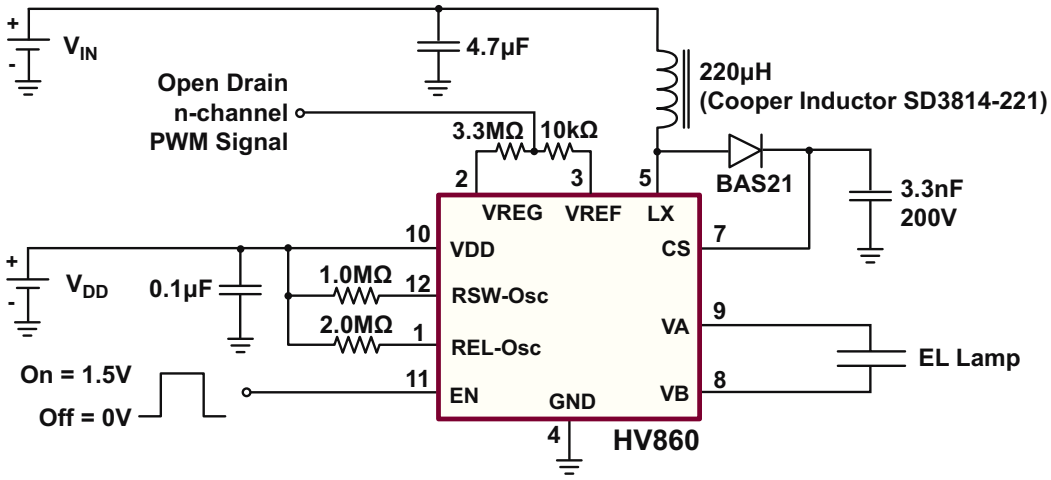
How to Minimize EL Lamp Audible Noise

The audible noise from the EL lamp can be minimized with the proper selection of R_{REG}. R_{REG} is connected between the VREF and VREG pins. VREG has an internal 60pF capacitor to ground. EL lamp noise can be minimized without much loss in brightness by setting the RC time constant to be approximately 1/12 of the EL frequency's period.

EL Lamp Dimming using PWM

This section describes the method of dimming the EL lamp. Reducing the voltage amplitude at the VREG pin will reduce the voltage on the CS pin, which will effectively reduce the peak to peak voltage the EL lamp sees. Figure 4 shows a circuit to dim the lamp by changing the duty cycle of a PWM signal. A 10kΩ resistor is connected in series with a 3.3MΩ resistor. An N-channel open drain PWM signal is used to pull the 10kΩ resistor to ground. The effective voltage on the VREG pin will be proportional to the duty cycle of the PWM signal. The PWM operating frequency can be anywhere between 20kHz to 100kHz.

Figure 4: PWM Dimming Circuit

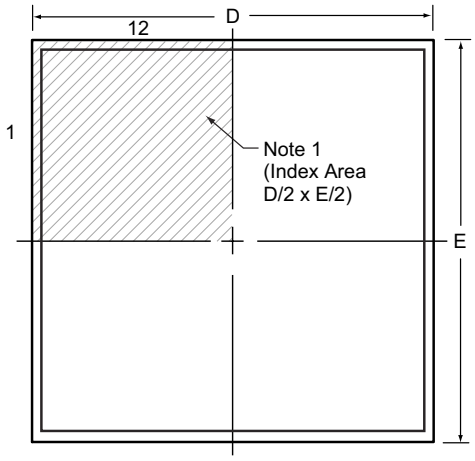


Pin Configuration and External Component Description

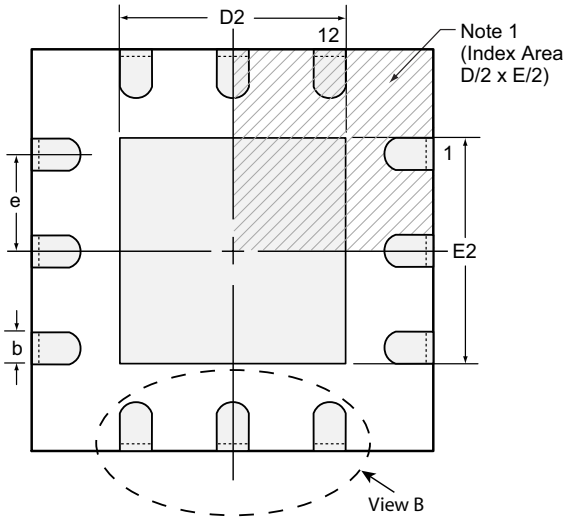
Pin #	Name	Description
1	REL-Osc	External resistor from REL-Osc to VDD sets the EL frequency. The EL frequency is inversely proportional to the external R_{EL} resistor value. Reducing the resistor value by a factor of two will result in increasing the EL frequency by two.
2	VREG	Input voltage to set V_{CS} regulation voltage. This pin allows an external voltage source to control the V_{CS} amplitude. EL lamp dimming can be accomplished by varying the input voltage at VREG. The V_{CS} voltage is approximately 87 times the voltage seen on VREG. External resistor R_{REG}, connected between VREG and VREF pins controls the V_{CS} charging rate. The charging rate is inversely proportional to the R_{REG} resistor value.
3	VREF	Switched internal reference voltage.
4	GND	Device ground.
5	LX	Drain of internal switching MOSFET. Connection for an external inductor. The inductor L_X is used to boost the low input voltage by inductive flyback. When the internal switch is on, the inductor is being charged. When the internal switch is off, the charge stored in the inductor will be transferred to the high voltage capacitor C_S. The energy stored in the capacitor is transferred to the internal H-bridge, and therefore to the EL lamp. In general, smaller value inductors, which can handle more current, are more suitable to drive larger size lamps. As the inductor value decreases, the switching frequency of the inductor (controlled by R_{SW}) should be increased to avoid saturation. A 220µH Cooper (SD3814-221) inductor with 5.5Ω series DC resistance is typically recommended. For inductors with the same inductance value, but with lower series DC resistance, lower R_{SW} resistor value is needed to prevent high current draw and inductor saturation.
6	NC	No internal connections to the device.
7	CS	High voltage regulated output. Connection for an external high voltage capacitor to ground
8	VB	V_B side of the EL lamp driver H-bridge. Connection for one of the EL lamp terminals.
9	VA	V_A side of the EL lamp driver H-bridge. Connection for one of the EL lamp terminals.
10	VDD	Low voltage input supply pin.
11	EN	Logic input pin. Logic high will enable the device. This pin has an 100kΩ internal pull-down resistor connected to GND.
12	RSW-Osc	External resistor from RSW-Osc to VDD sets the switch converter frequency. The switch converter frequency is inversely proportional to the external R_{SW} resistor value. Reducing the resistor value by a factor of two will result in increasing the switch converter frequency by two.

12-Lead QFN Package Outline (K7)

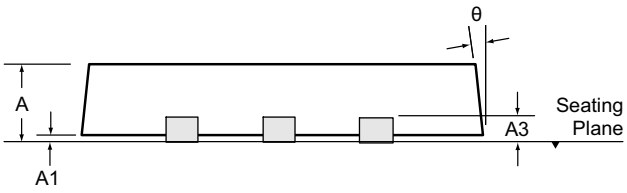
3.00x3.00mm body, 0.80mm height (max), 0.50mm pitch



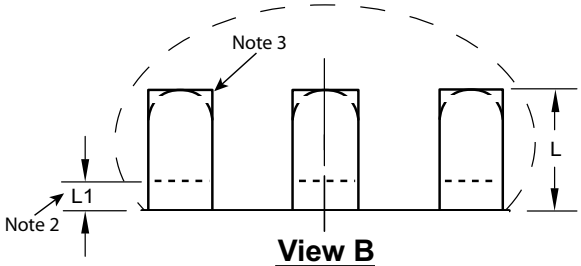
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	2.85*	1.25	2.85*	1.25	0.50 BSC	0.30	0.00	0°
	NOM	0.75	0.02		0.25	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.30	3.15*	1.65	3.15*	1.65		0.50	0.15	14°

JEDEC Registration MO-220, Variation WEED-5, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
Supertex Doc. #: *DSPD-12QFNK73X3P050, Version B041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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