AM29841DM

High Performance Bus Interface Latches

The Am29640 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide versions of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buttered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) - ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g.,$\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29600 high perlormance interface family products are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

Am29841 – 46

High Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - Noninverting transparent t_{PD} = 5.25ns typ
  - Inverting transparent t_{PD} = 6.0ns typ
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch-free during power-up and down. Outputs have Schottky clamp to ground

- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- Low input/output capacitance
  - 6pF inputs (typical)
  - 8pF outputs (typical)
- I_{OH} specified 2.0V and 2.4V

GENERAL DESCRIPTION

The Am29840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide versions of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$)

to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family products are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM

Am29843

BD001050
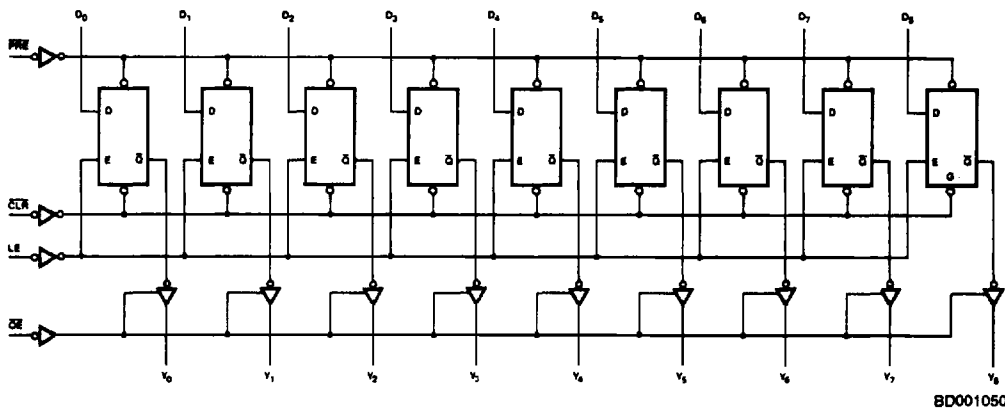
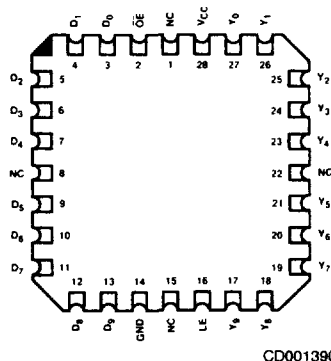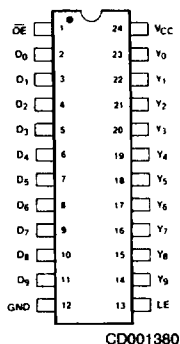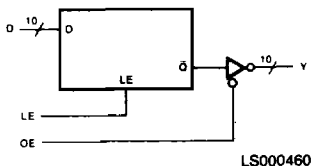## PRODUCT SELECTOR GUIDE

	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29841	Am29843	Am29845
Inverting	Am29842	Am29844	Am29846

01972C

Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

Am29841/Am29842 10-BIT LATCHES

DIP pinout:

Pin		Pin	
OE	1	24	V_CC
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
D_9	11	14	Y_9
GND	12	13	LE

CD001380

PLCC pinout:

Top pins: D_1, D_0, $\overline{OE}$, NC, V_{CC}, Y_0, Y_1

Left pins: D_2 (5), D_3 (6), D_4 (7), NC (8), D_5 (9), D_6 (10), D_7 (11)

Right pins: Y_2 (25), Y_3 (24), Y_4 (23), NC (22), Y_5 (21), Y_6 (20), Y_7 (19)

Bottom pins: D_8, D_9, GND, NC, LE, Y_8, Y_9

CD001390

LOGIC SYMBOL

LS000460

METALLIZATION AND PAD LAYOUT
Am29841*
10-Bit Latches

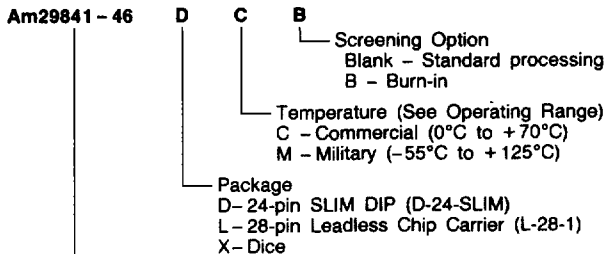|			
OE	1	24	V_CC
D_0	2	23	Y_0
D_1	3	22	Y_1
D_2	4	21	Y_2
D_3	5	20	Y_3
D_4	6	19	Y_4
D_5	7	18	Y_5
D_6	8	17	Y_6
D_7	9	16	Y_7
D_8	10	15	Y_8
D_9	11	14	Y_9
GND	12	13	LE
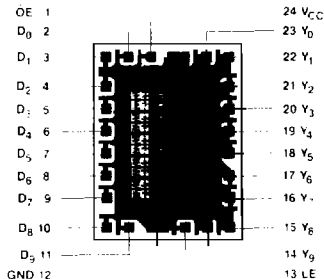
DIE SIZE 0.084" x 0.064"
Note: the Am29842 is inverted

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ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29841 – 46 D C B

— Screening Option
  Blank – Standard processing
  B – Burn-in

— Temperature (See Operating Range)
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)

— Package
  D – 24-pin SLIM DIP (D-24-SLIM)
  L – 28-pin Leadless Chip Carrier (L-28-1)
  X – Dice

— Device type
  High Performance Bus Interface Latches

Valid Combinations	
Am29841 Am29842 Am29843 Am29844 Am29845 Am29846	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations
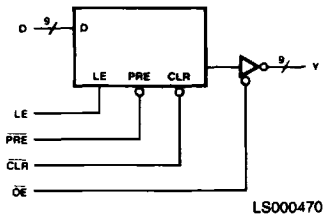
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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CONNECTION DIAGRAM
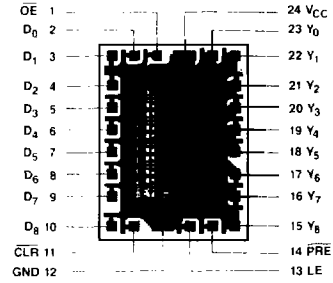### Top View

Am29843/Am29844 9-BIT LATCHES

```
OE   [ 1      24 ]  Vcc
D0   [ 2      23 ]  Y0
D1   [ 3      22 ]  Y1
D2   [ 4      21 ]  Y2
D3   [ 5      20 ]  Y3
D4   [ 6      19 ]  Y4
D5   [ 7      18 ]  Y5
D6   [ 8      17 ]  Y6
D7   [ 9      16 ]  Y7
D8   [ 10     15 ]  Y8
CLR  [ 11     14 ]  PRE
GND  [ 12     13 ]  LE
```

CD001400

```
         D1  D0  OE  NC  Vcc  Y0  Y1
          4   3   2   1   28  27  26
D2   5                            25  Y2
D3   6                            24  Y3
D4   7                            23  Y4
NC   8                            22  NC
D5   9                            21  Y5
D6   10                           20  Y6
D7   11                           19  Y7
         12  13  14  15  16  17  18
         D8  CLR GND NC  LE  PRE Y8
```

CD001410

LOGIC SYMBOL

LS000470
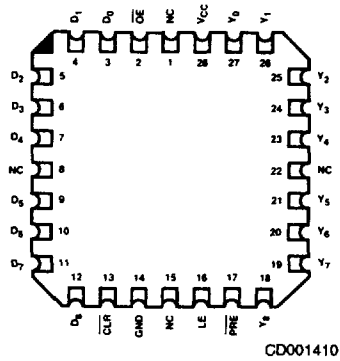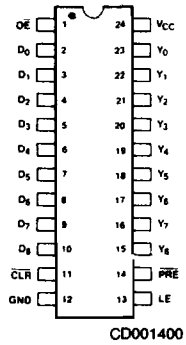
METALLIZATION AND PAD LAYOUT
Am29843*
9-Bit Latches

```
OE   1                    24  Vcc
D0   2                    23  Y0
D1   3                    22  Y1
D2   4                    21  Y2
D3   5                    20  Y3
D4   6                    19  Y4
D5   7                    18  Y5
D6   8                    17  Y6
D7   9                    16  Y7
D8   10                   15  Y8
CLR  11                   14  PRE
GND  12                   13  LE
```

DIE SIZE 0.084" x 0.064"
Note: the Am29844 is inverted

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CONNECTION DIAGRAM
Top View

Am29845/Am29846 8-BIT LATCHES

CD001340

CD001350

LOGIC SYMBOL

LS000440
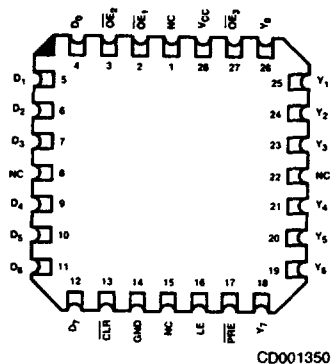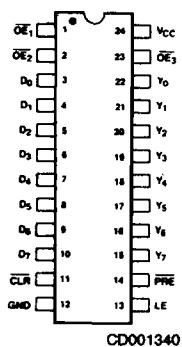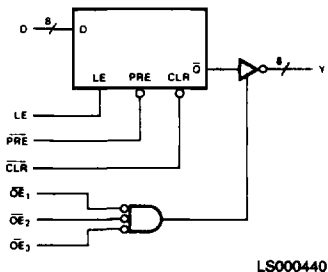
METALLIZATION AND PAD LAYOUT
Am29845*
8-Bit Latches
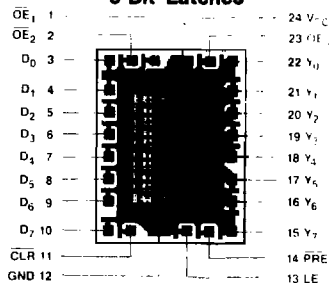
DIE SIZE 0.064″ x 0.064″
Note: the Am29846 is inverted

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Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Am29841/43/45 (Noninverting)			
11	$\overline{CLR}$	I	When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
	D_i	I	The latch data inputs.
13	LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
	Y_i	O	The 3-state latch outputs.
1	$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When OE is HIGH, the outputs Y_i are in the high-impedance (off) state.
14	$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
Am29842/44/46 (Inverting)			
11	$\overline{CLR}$	I	When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
	D_i	I	The latch inverting data inputs.
13	LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
	Y_i	O	The 3-state latch outputs.
1	$\overline{OE}$	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Y_i are in the high-impedance (off) state.
14	$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES

29841/43/45 (Noninverting)

Inputs					Internal Outputs		
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

29842/44/46 (Inverting)

Inputs					Internal Outputs		
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

01972C

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
Ambient Temperature with
  Power Applied .... −55°C to +125°C
Supply Voltage to Ground Potential
  Continuous .... −0.5V to +7.0V
DC Voltage Applied to Outputs
  for High Output State .... −0.5V to V_{CC} max
DC input voltage .... −0.5V to +5.5V
DC Output Current, into Outputs 100mA
DC input Current .... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature .... 0°C to +70°C
  Supply Voltage .... +4.75V to +5.25V

Military (M) Devices
  Temperature .... −55°C to +125°C
  Supply Voltage .... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

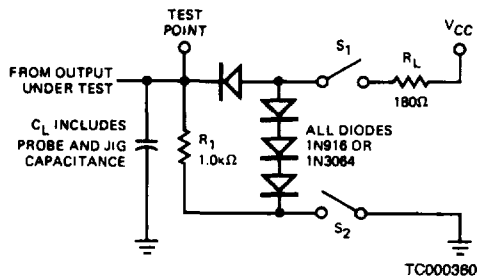## DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2.4	3.3		Volts
			I_{OH} = −24mA	2.0	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA			0.5	Volts
			COM'L, I_{OL} = 48mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−1.0.	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Output Off-State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current[3]	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply Current	V_{CC} = MAX Outputs Open	Over Temperature Range			120	mA
			+70			110	
			+125°C			100	

Notes: 1. All typical values are T_A = 25°C, V_{CC} = 5.0V.
2. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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SWITCHING TEST CIRCUIT

TC000360

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| Parameters	Description		Test Conditions (Note 4)	COMMERCIAL		MILITARY		Units
				Min	Max	Min	Max	
t_{PLH} (Am29841, 3, 5)	Data (D_i) to Output Y_i (LE = HIGH)		$C_L = 50pF$	3.5	9.5	3.5	11	ns
t_{PHL}				3.5	9.5	3.5	11	ns
t_{PLH}			$C_L = 300pF$		12.5		14	ns
t_{PHL}					13		15	ns
t_s	Data to LE Setup Time		$C_L = 50pF$	2.5		2.5		ns
t_H	Data to LE Hold Time			2.5		3		ns
t_{PLH} (Am29842, 4, 6)	Data (D_i) to Output ($\overline{Y}_i$) (LE = HIGH)		$C_L = 50pF$	3.5	10		12	ns
t_{PHL}				3.5	10		12	ns
t_{PLH}			$C_L = 300pF$		12.5		14	ns
t_{PHL}					13		15	ns
t_{PLH}	Data to LE Setup Time		$C_L = 50pF$	2.5		2.5		ns
t_{PHL}	Data to LE Hold Time			2.5		3		ns
t_{PLH}	Latch Enable (LE) to Y_i		$C_L = 50pF$		12		16	ns
t_{PHL}					12		16	ns
t_{PLH}			$C_L = 300pF$		16		20	ns
t_{PHL}					16		20	ns
								ns
								ns
t_{PLH}	Propagation Delay, Preset to Y_i		$C_L = 50pF$		12		14	ns
t_S	Preset Recovery (PRE ⌐) Time				14		17	ns
t_{PHL}	Propagation Delay, Clear to Y_i				21		23	ns
t_S	Clear Recovery (CLR ⌐) Time				14		17	ns
t_{PWH}	LE Pulse Width	HIGH	$C_L = 50pF$	6		6		ns
t_{PWL}	Preset Pulse Width	LOW		8		9		ns
t_{PWL}	Clear Pulse Width	LOW		8		9		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌐ to Y_i		$C_L = 300pF$		20		22	ns
t_{ZL}					23		25	ns
t_{ZH}			$C_L = 50pF$		14		15	ns
t_{ZL}					14		15	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i		$C_L = 50pF$		15		15	ns
t_{LZ}					12		12	ns
t_{HZ}			$C_L = 5pF$		9		10	ns
t_{LZ}					9		10	ns

Note: 4. See test circuit and waveforms.

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SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions (Note 4)		Min	Typ	Max	Units
t_{PLH} (Am29841, 3, 5)		C_L = 50pF		3.5	5.7	8	ns
t_{PHL}	Data (D_i) to Output Y_i (LE = HIGH)			3.5	6.2	8	ns
t_{PLH}		C_L = 300pF			10	13	ns
t_{PHL}					10	13	ns
t_s	Data to LE Setup Time	C_L = 50pF		2.0	−0.2		ns
t_H	Data to LE Hold Time			2.5	0.7		ns
t_{PLH} (Am29842, 4, 6)		C_L = 50pF		3.5	6.2	8.5	ns
t_{PHL}	Data (D_i) to Output ($\overline{Y}_i$) (LE = HIGH)			3.5	6.5	8.5	ns
t_{PLH}		C_L = 300pF			10	13	ns
t_{PHL}					10	13	ns
t_S	Data to LE Setup Time	C_L = 50pF		2.5	0.3		ns
t_H	Data to LE Hold Time			2.5	0.2		ns
t_{PLH}		C_L = 50pF			8	10.5	ns
t_{PHL}	Latch Enable (LE) to Y_i				7.5	10	ns
t_{PLH}		C_L = 300pF				15	ns
t_{PHL}						15	ns
							ns
							ns
t_{PLH}	Propagation Delay, Preset to Y_i	C_L = 50pF			6.5	9	ns
t_S	Preset Recovery (PRE ⌐) Time				7.3	12	ns
t_{PHL}	Propagation Delay, Clear to Y_i				15	18	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐) Time				7.8	12	ns
t_{PWH}	LE Pulse Width	HIGH		4	2.5		ns
t_{PWL}	Preset Pulse Width	LOW	C_L = 50pF	5			ns
t_{PWL}	Clear Pulse Width .	LOW		6			ns
t_{ZH}		C_L = 300pF				17	ns
t_{ZL}	Output Enable Time $\overline{OE}$ ⌐ to Y_i					21	ns
t_{ZH}		C_L = 50pF			7.3	12	ns
t_{ZL}					9.7	12	ns
t_{HZ}		C_L = 50pF			10.4	14	ns
t_{LZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i				4.7	11	ns
t_{HZ}		C_L = 5pF (Note 5)			3.4	6	ns
t_{LZ}					3.8	6	ns

Note: 4. See test circuit and waveforms.
5. Not tested.

SWITCHING WAVEFORMS

SET UP, HOLD, AND RELEASE TIMES

DATA INPUT — 3V / 1.5V / 0V

t_s t_h

LATCH ENABLE — 3V / 1.5V / 0V

WF001400
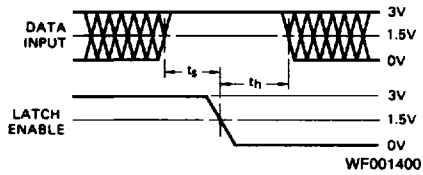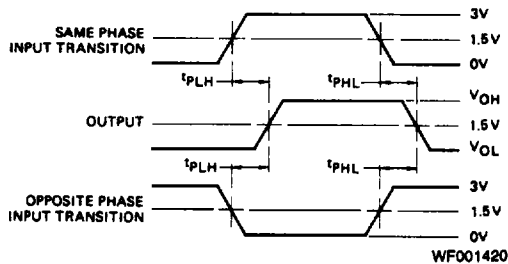
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.
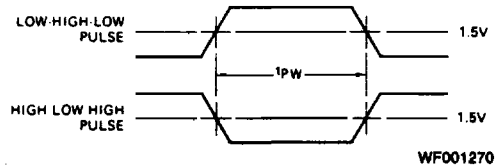
ENABLE AND DISABLE TIMES
Enable   Disable

CONTROL INPUT — 3.0V / 1.5V / 0V

t_{ZL} t_{LZ}

OUTPUT NORMALLY LOW S_2 OPEN   ~4.5V / 1.5V   0.5V   ~1.5V V_{OL}

t_{ZH} t_{HZ}

OUTPUT NORMALLY HIGH S_1 OPEN   1.5V / ~0V V_{OH} ~1.5V   0.5V

WF001410
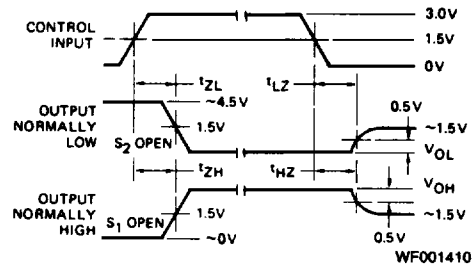
Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

PROPAGATION DELAY

SAME PHASE INPUT TRANSITION — 3V / 1.5V / 0V

t_{PLH} t_{PHL}

OUTPUT — V_{OH} / 1.5V / V_{OL}

t_{PLH} t_{PHL}

OPPOSITE PHASE INPUT TRANSITION — 3V / 1.5V / 0V

WF001420

PULSE WIDTH

LOW-HIGH-LOW PULSE — 1.5V

t_{PW}

HIGH LOW HIGH PULSE — 1.5V

WF001270

Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

V_{CC} INPUTS   OUTPUTS

7.5kΩ   3kΩ I_{OH}

INPUT I_L I_H

OUTPUT I_{OL}

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