

December 1996

Fast CMOS Octal Transparent Latches

Features

- Advanced 0.8 micron CMOS Technology
- Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2373T, CD74FCT2573T Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Description

These devices are 8-bit wide octal transparent latches designed with three-state outputs and are intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When \overline{OE} is HIGH, the bus output is in the high impedance state.

The CD74FCT2XXX device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT373ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT373CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT373DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT373TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT533ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT533ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT533CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT533CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT533TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT533TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2373ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2373ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2373CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2373CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2373TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2373TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2573ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2573ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2573CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2573CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2573TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2573TQM	-40 to 85	20 Ld QSOP	M20.15-P

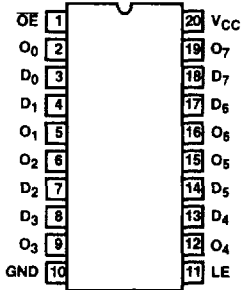
NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

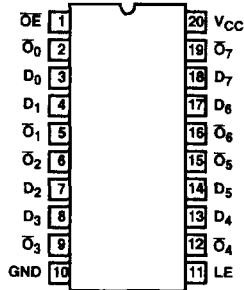
CD74FCT373T, CD74FCT533T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T

Pinouts

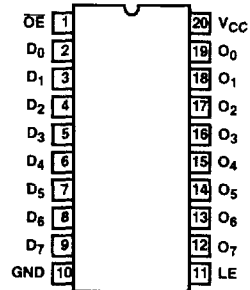
CD74FCT373T, CD74FCT2373T
(QSOP, SOIC)
TOP VIEW



CD74FCT533T
(QSOP, SOIC)
TOP VIEW

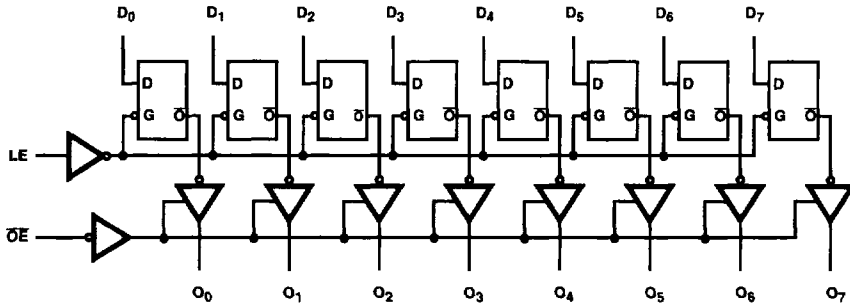


CD74FCT573T, CD74FCT2573T
(QSOP, SOIC)
TOP VIEW

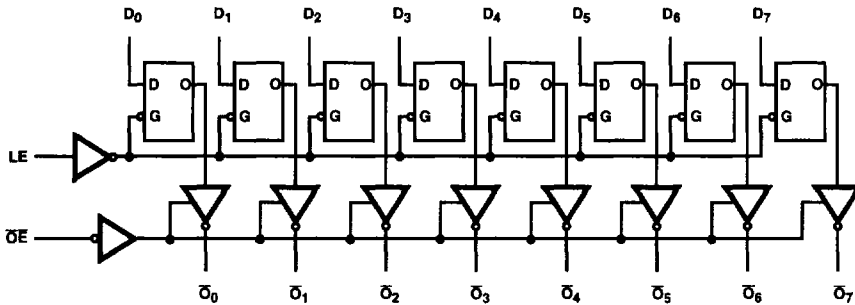


Functional Block Diagrams

CD74FCT373T, CD74FCT2373T, CD74FCT573, CD74FCT2573T



CD74FCT533T



4

**OCTAL 5V FCT
5V FCT 25Ω**

CD74FCT373T, CD74FCT533T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T

TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D_N	LE	\overline{OE}	\overline{O}_N
CD74FCT533T			
H	H	L	L
L	H	L	H
X	X	H	Z

TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D_N	LE	\overline{OE}	O_N
CD74FCT373T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T			
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
\overline{OE}	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D_0 - D_7	Data Inputs
O_0 - O_7	Three-State Outputs
\overline{O}_0 - \overline{O}_7	Complementary Three-State Outputs
GND	Ground
V_{CC}	Power

CD74FCT373T, CD74FCT533T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4)	MAX	UNITS
					TYP		
Total Power Supply Current (Note 10)	I _C	V _{CC} = Max, Outputs Open f _I = 10MHz, 50% Duty Cycle OE = GND; LE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	1.5	3.0 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	1.8	4.5 (Note 9)	mA
		V _{CC} = Max, Outputs Open f _I = 2.5MHz, 50% Duty Cycle OE = GND; LE = V _{CC} Eight Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	3.0	6.0 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	5.0	14.0 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		DT CD74FCT373T ONLY		UNITS
			(NOTE 12)		(NOTE 12)		(NOTE 12)		(NOTE 12)		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
CD74FCT373T, CD74FCT2373T											
Propagation Delay D _N to O _N	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
Propagation Delay LE to O _N	t _{PLH} , t _{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.9	ns
Output Enable Time OE to O _N	t _{PZH} , t _{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
Output Disable Time (Note 13) OE to O _N	t _{PHZ} , t _{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
Setup Time HIGH or LOW, D _N to LE	t _{SU}		2.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D _N to LE	t _H		1.5	-	1.5	-	1.5	-	1.5	-	ns
LE Pulse Width (Note 13) HIGH	t _W		6.0	-	5.0	-	5.0	-	4.0	-	ns
CD74FCT533T											
Propagation Delay D _N to O _N	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	5.2	1.5	4.2	-	-	ns
Propagation Delay LE to O _N	t _{PLH} , t _{PHL}		2.0	13.0	2.0	8.5	2.0	5.5			ns
Output Enable Time OE to O _N	t _{PZH} , t _{PZL}		1.5	11.0	1.5	6.5	1.5	5.5	-	-	ns
Output Disable Time (Note 13) OE to O _N	t _{PHZ} , t _{PLZ}		1.5	7.0	1.5	5.5	1.5	5.0			ns
Setup Time HIGH or LOW, D _N to LE	t _{SU}		2.0	-	2.0	-	2.0	-	-	-	ns
Hold Time HIGH or LOW, D _N to LE	t _H		1.5	-	1.5	-	1.5	-			ns
LE Pulse Width (Note 13) HIGH	t _W		6.0	-	5.0	-	5.0	-	-	-	ns

Switching Specifications Over Operating Range (Continued)

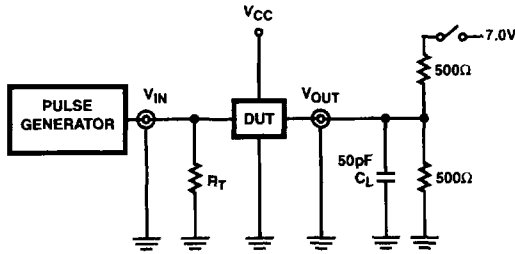
PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		DT CD74FCT373T ONLY		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
			CD74FCT573T, CD2573T								
Propagation Delay D _N to \bar{O}_N	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	-	-	ns
Propagation Delay LE to \bar{O}_N	t _{PLH} , t _{PHL}		2.0	12.0	2.0	8.5	2.0	5.5	-	-	ns
Output Enable Time $\bar{O}\bar{E}$ to O _N	t _{PZH} , t _{PZL}		1.5	9.5	1.5	6.5	1.5	5.5	-	-	ns
Output Disable Time (Note 13) $\bar{O}\bar{E}$ to O _N	t _{PHZ} , t _{PLZ}		1.5	6.5	1.5	5.5	1.5	5.0	-	-	ns
Setup Time HIGH or LOW, D _N to LE	t _{SU}		2.0	-	2.0	-	2.0	-	-	-	ns
Hold Time HIGH or LOW, D _N to LE	t _H		1.5	-	1.5	-	1.5	-	-	-	ns
LE Pulse Width (Note 13) HIGH	t _W		6.0	-	5.0	-	5.0	-	-	-	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.

4
OCTAL 5V FCT
5V FCT 25Ω

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

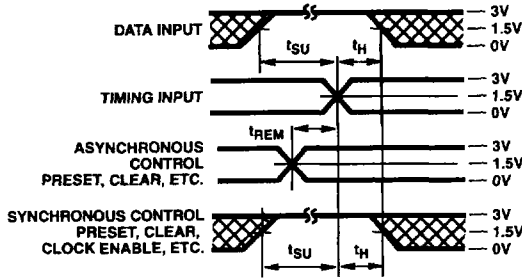


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

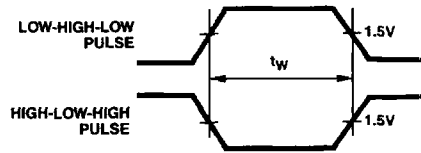


FIGURE 3. PULSE WIDTH

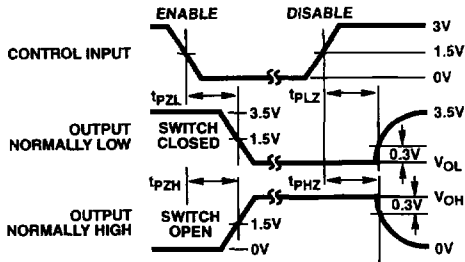


FIGURE 4. ENABLE AND DISABLE TIMING

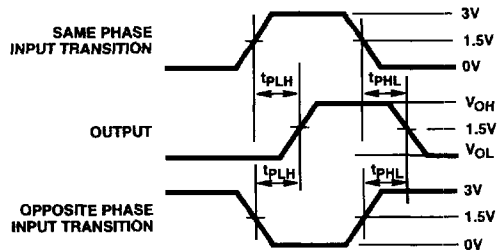


FIGURE 5. PROPAGATION DELAY