

December 1996

## Fast CMOS 3.3V 8-Bit Transparent Latch

### Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**

### Description

The CD74LPT573 is an 8-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When OE is HIGH, the bus output is in the high impedance state.

The CD74LPT573 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

### Ordering Information

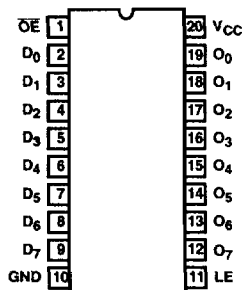
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT573AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT573AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT573CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT573CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT573M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT573QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

### Pinout

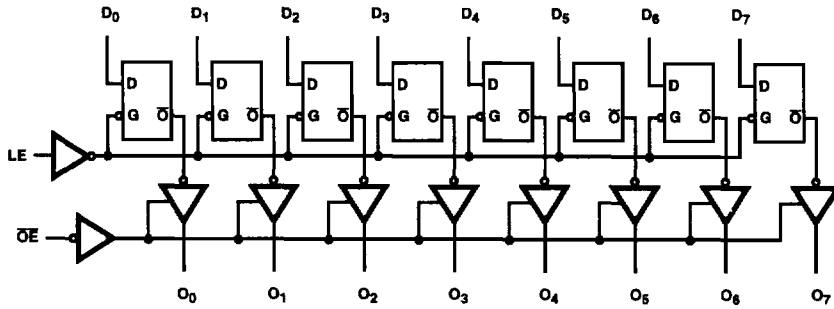
CD74LPT573  
(QSOP, SOIC)  
TOP VIEW



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3.3V LPT

**Functional Block Diagram**



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D <sub>N</sub>	LE	OE	O <sub>N</sub>
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance

**Pin Descriptions**

PIN NAME	DESCRIPTION
OE	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D <sub>7</sub> -D <sub>0</sub>	Data Inputs
O <sub>7</sub> -O <sub>0</sub>	Three-State Outputs
GND	Ground
V <sub>CC</sub>	Power

**Absolute Maximum Ratings**

DC Input Voltage ..... -0.5V to 7.0V  
 DC Output Current ..... 120mA

**Operating Conditions**

Operating Temperature Range ..... -40°C to 85°C  
 Supply Voltage to Ground Potential  
 Inputs and V<sub>CC</sub> Only ..... -0.5V to 7.0V  
 Supply Voltage to Ground Potential  
 Outputs and D/O Only ..... -0.5V to 7.0V

**Thermal Information**

Thermal Resistance (Typical, Note 2)                    θ<sub>JA</sub> (°C/W)  
 SOIC Package ..... 87  
 QSOP Package ..... 110  
 Maximum Junction Temperature ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
 (Lead Tips Only)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

2. θ<sub>JA</sub> is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
				DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T <sub>A</sub> = -40°C to 85°C, V <sub>CC</sub> = 2.7V to 3.6V			
Input HIGH Voltage (Input Pins)	V <sub>IH</sub>	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V <sub>IH</sub>	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V <sub>IL</sub>	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I <sub>IH</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I <sub>IH</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = V <sub>CC</sub>	-	-	±1	µA
Input LOW Current (Input Pins)	I <sub>IL</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I <sub>IL</sub>	V <sub>CC</sub> = Max	V <sub>IN</sub> = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I <sub>OZH</sub>	V <sub>CC</sub> = Max	V <sub>OUT</sub> = 5.5V	-	-	±1	µA
	I <sub>OZL</sub>	V <sub>CC</sub> = Max	V <sub>OUT</sub> = GND	-	-	±1	µA
Clamp Diode Voltage	V <sub>IK</sub>	V <sub>CC</sub> = Min, I <sub>IN</sub> = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I <sub>ODH</sub>	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I <sub>ODL</sub>	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V <sub>OH</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	-	-	V
			I <sub>OH</sub> = -3mA	2.4	3.0	-	V
		V <sub>CC</sub> = 3.0V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -8mA	2.4 (Note 7)	3.0	-	V
			I <sub>OH</sub> = -24mA	2.0	-	-	V
Output LOW Voltage	V <sub>OL</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 0.1mA	-	-	0.2	V
			I <sub>OL</sub> = 16mA	-	0.2	0.4	V
			I <sub>OL</sub> = 24mA	-	0.3	0.5	V

## Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS	
Short Circuit Current (Note 6)	$I_{OS}$	$V_{CC} = \text{Max (Note 5)}, V_{OUT} = \text{GND}$	-60	-85	-240	mA	
Power Down Disable	$I_{OFF}$	$V_{CC} = 0V, V_{IN} \text{ or } V_{OUT} \leq 4.5V$	-	-	$\pm 100$	$\mu A$	
Input Hysteresis	$V_H$		-	150	-	mV	
<b>CAPACITANCE</b> $T_A = 25^\circ C, f = 1\text{MHz}$							
Input Capacitance (Note 8)	$C_{IN}$	$V_{IN} = 0V$	-	4.5	6	pF	
Output Capacitance (Note 8)	$C_{OUT}$	$V_{OUT} = 0V$	-	5.5	8	pF	
<b>POWER SUPPLY SPECIFICATIONS</b>							
Quiescent Power Supply Current	$I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or $V_{CC}$	-	0.1	10	$\mu A$
Quiescent Power Supply Current TTL Inputs HIGH	$\Delta I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC} - 0.6V$ (Note 9)	-	2.0	30	$\mu A$
Dynamic Power Supply Current (Note 10)	$I_{CCD}$	$V_{CC} = \text{Max}, \text{Outputs Open}$ $\overline{OE} = \text{GND}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	50	75	$\mu A/\text{MHz}$
Total Power Supply Current (Note 12)	$I_C$	$V_{CC} = \text{Max}, \text{Outputs Open}$ $f_1 = 10\text{MHz}, 50\% \text{ Duty Cycle}$ $\overline{OE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	-	0.6	2.3	mA
		$V_{CC} = \text{Max}, \text{Outputs Open}$ $f_1 = 2.5\text{MHz}, 50\% \text{ Duty Cycle}$ $\overline{OE} = \text{GND}$ 8 Bits Toggling	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	-	2.1	4.7 (Note 11)	mA

## CD74LPT573

### Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT573		CD74LPT573A		CD74LPT573C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay D <sub>X</sub> to O <sub>X</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
Propagation Delay LE to O <sub>X</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>		2.0	12.0	2.0	8.5	2.0	5.5	ns
Output Enable Time OE to O <sub>X</sub>	t <sub>PZH</sub> , t <sub>PZL</sub>		1.5	9.5	1.5	6.5	1.5	5.5	ns
Output Disable Time (Note 16) OE to O <sub>X</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>		1.5	6.5	1.5	5.5	1.5	5.0	ns
Setup Time HIGH or LOW, D <sub>X</sub> to LE	t <sub>SU</sub>		2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D <sub>X</sub> to LE	t <sub>H</sub>		1.5	-	1.5	-	1.5	-	ns
LE Pulse Width HIGH (Note 16)	t <sub>W</sub>		6.0	-	5.0	-	5.0	-	ns
Output Skew (Note 17)	t <sub>SK(O)</sub>		-	0.5	-	0.5	-	0.5	ns

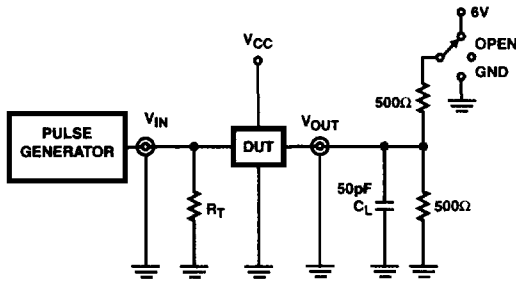
#### NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V<sub>CC</sub> = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. V<sub>OH</sub> = V<sub>CC</sub> - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
12. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>I</sub> = Input Frequency  
 N<sub>I</sub> = Number of Inputs at f<sub>I</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V<sub>CC</sub> = 3.3V ±0.3V, normal range. For V<sub>CC</sub> = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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3.3V LPT

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}$ , $t_{PZL}$ , Open Drain	6V
$t_{PHZ}$ , $t_{PZH}$	GND
$t_{PLH}$ , $t_{PHL}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_r$ ,  $t_f \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

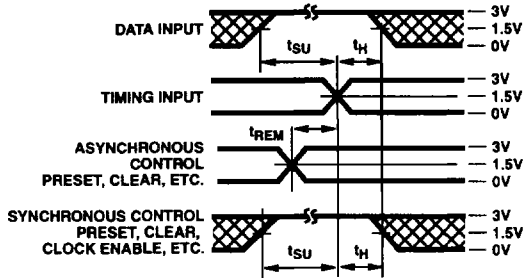


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

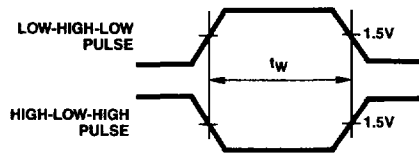


FIGURE 3. PULSE WIDTH

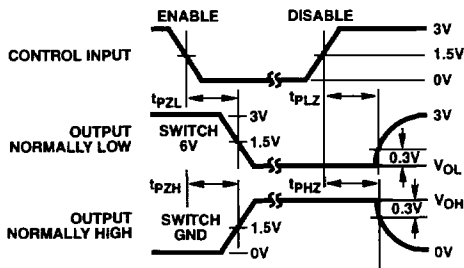


FIGURE 4. ENABLE AND DISABLE TIMING

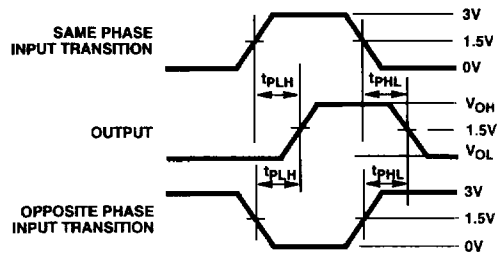


FIGURE 5. PROPAGATION DELAY