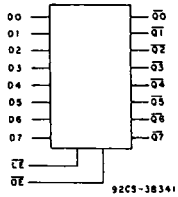


**CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563**

File Number 1599

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 0017825 6 HAS

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

**Octal Inverting Transparent Latch,
3-State Outputs**

Type Features:

- Common latch-enable control
- Common 3-state output-enable control
- Buffered inputs
- 3-State outputs
- Bus line driving capacity
- Typical propagation delay = 13 ns @ $V_{CC} = 5 V, C_L = 15 pF, T_A = 25^\circ C$ (Data to Output)

The RCA CD54/74HC/HCT533/563 are high-speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices.

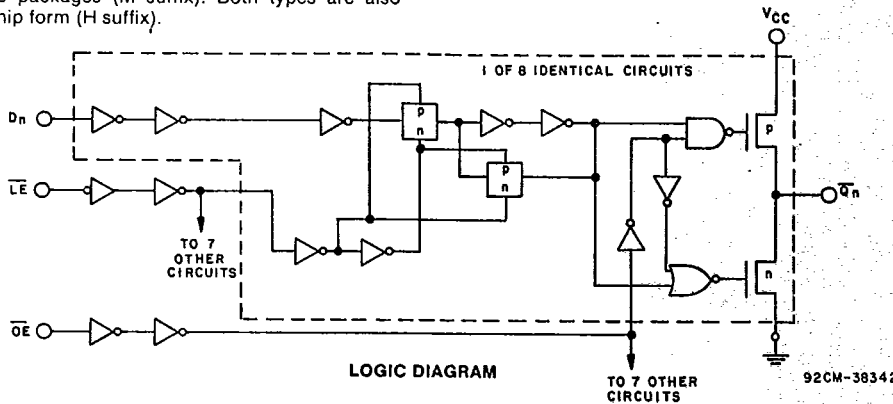
The outputs are transparent to the inputs when the latch enable (\overline{LE}) is high. When the latch enable (\overline{LE}) goes low the data is latched. The output enable (\overline{OE}) controls the 3-state outputs. When the output enable (\overline{OE}) is high the outputs will be in the high impedance state. The latch operation is independent of the state of the output enable.

The CD54/74HC533 and CD54/74HCT533 are identical in function to the CD54/74HC563 and CD54/74HCT563 but have different pinouts. The CD54/74HC533 and CD54/74HCT533 are similar to the CD54/74HC373 and CD54/74HCT373; the latter are non-inverting types.

The CD54HC/HCT533/563 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT533/563 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features

- Fanout (Over Temperature Range):
Standard Outputs — 10 LSTTL Loads
Bus Driver Outputs — 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ C$
- Balanced Propagation and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Phillips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%, N_{IH} = 30\%$ of V_{CC} ;
@ $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 V$ Max., $V_{IH} = 2 V$ Min.
CMOS Input Compatibility
 $I_I \leq 1 \mu A$ @ V_{OL}, V_{OH}



CD54/74HC533, CD54/74HCT533 CD54/74HC563, CD54/74HCT563

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):

(Voltages referenced to ground)

| | | |
|--|-------|--------------|
| DC INPUT DIODE CURRENT, I _{IK} (FOR V _I < -0.5 V OR V _I > V _{CC} + 0.5 V) | | -0.5 to +7 V |
| DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _O < -0.5 V OR V _O > V _{CC} + 0.5 V) | | ± 20 mA |
| DC DRAIN CURRENT, PER OUTPUT (I _O) (FOR -0.5 V < V _O < V _{CC} + 0.5 V) | | ± 20 mA |
| DC V _{CC} OR GROUND CURRENT (I _{CC}): | | ± 35 mA |
| DC V _{CC} OR GROUND CURRENT (I _{CC}): | | ± 70 mA |

POWER DISSIPATION PER PACKAGE (P_O):

| | | |
|---|-------|--------------------------------------|
| For T _A = -40 to +60°C (PACKAGE TYPE E) | | 500 mW |
| For T _A = +60 to +85°C (PACKAGE TYPE E) | | Derate Linearly at 8 mW/°C to 300 mW |
| For T _A = -55 to +100°C (PACKAGE TYPE F, H) | | 500 mW |
| For T _A = +100 to +125°C (PACKAGE TYPE F, H) | | Derate Linearly at 8 mW/°C to 300 mW |
| For T _A = -40 to +70°C (PACKAGE TYPE M) | | 400 mW |
| For T _A = +70 to +125°C (PACKAGE TYPE M) | | Derate Linearly at 6 mW/°C to 70 mW |

OPERATING-TEMPERATURE RANGE (T_A):

| | | |
|---|-------|---------------|
| PACKAGE TYPE F, H | | -55 to +125°C |
| PACKAGE TYPE E, M | | -40 to +85°C |
| STORAGE TEMPERATURE (T _{STG}) | | -65 to +150°C |

LEAD TEMPERATURE (DURING SOLDERING):

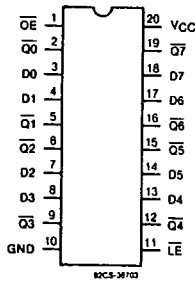
| | | |
|--|-------|--------|
| At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. | | +265°C |
| Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only | | +300°C |

RECOMMENDED OPERATING CONDITIONS:

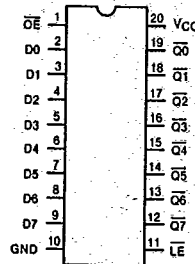
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|-----------------|-------|
| | MIN. | MAX. | |
| Supply-Voltage Range (For T _A = Full Package Temperature Range) V _{CC} .* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage V _{IN} , V _{OUT} | 0 | V _{CC} | V |
| Operating Temperature T _A : | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times, t _r , t _f | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.



CD54/74HC533, CD54/74HCT533
TERMINAL ASSIGNMENT



CD54/74HC563, CD54/74HCT563
TERMINAL ASSIGNMENT

HARRIS SEMICONDUCTOR 27E D 430227J 0017826 8 HAS

**CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563**

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CD74HC533/CD54HC533 CD74HC563/CD54HC563 | | | | | | | | | | CD74HCT533/CD54HCT533 CD74HCT563/CD54HCT563 | | | | | | | | | | UNITS | | | | |
|---|--|--|--|----------------|-----|------|---------------|------|------|----------------|--|--|---------------------|----------------------|-------|------------------|------|---------------|------------|-----|-------|----------------|----|---|--|
| | TEST CONDITIONS | | | 74HC/54HC TYPE | | | 74HC TYPE | | | 54HC TYPE | | | TEST CONDITIONS | | | 74HCT/54HCT TYPE | | | 74HCT TYPE | | | 54HCT TYPE | | | |
| | V _I V | I _O mA | V _{CC} V | +25°C | | | -40/ +85°C | | | -55/ +125°C | | | V _I V | V _{CC} V | +25°C | | | -40/ +85°C | | | | -55/ +125°C | | | |
| | | | | Min | Typ | Max | Min | Max | Min | Max | Min | Max | | | Min | Typ | Max | Min | Max | Min | | Max | | | |
| High-Level Input Voltage V _{IH} | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | to | 2 | — | — | 2 | — | 2 | — | — | — | V | | |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | — | 5.5 | | 2 | — | — | 2 | — | 2 | — | — | — | — | V | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | — | 5.5 | | 2 | — | — | 2 | — | 2 | — | — | — | — | V | |
| Low-Level Input Voltage V _{IL} | | | 2 | — | — | 0.5 | — | 0.5 | — | 0.5 | — | 4.5 | to | — | — | 0.8 | — | 0.8 | — | 0.8 | — | 0.8 | V | | |
| | | | 4.5 | — | — | 1.35 | — | 1.35 | — | 1.35 | — | 5.5 | | — | — | 0.8 | — | 0.8 | — | 0.8 | — | 0.8 | V | | |
| | | | 6 | — | — | 1.8 | — | 1.8 | — | 1.8 | — | 5.5 | | — | — | 0.8 | — | 0.8 | — | 0.8 | — | 0.8 | V | | |
| High-Level Output Voltage V _{OH} | V _{IL} or -0.02 | | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | V _{IL} | or | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | 4.4 | — | V | | |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V _{IL} | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | 4.4 | V | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | V _{IH} | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | 4.4 | V | | | |
| TTL Loads (Bus Driver) | V _{IL} or -6 V _{IH} | | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V _{IL} | or | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | 3.7 | — | V | | |
| | | | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | V _{IH} | | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | 3.7 | V | | | |
| | | | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | V _{IH} | | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | 3.7 | V | | | |
| Low-Level Output Voltage V _{OL} | V _{IL} or 0.02 | | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | V _{IL} | or | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | — | 0.1 | V | | |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | — | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | — | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V | | | | |
| TTL Loads (Bus Driver) | V _{IL} or 6 V _{IH} | | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V _{IL} | or | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | — | 0.4 | V | | |
| | | | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | — | | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V | | | | |
| | | | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | — | | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V | | | | |
| Input Leakage Current | I _I | V _{CC} or Gnd | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | Any Voltage Between V _{CC} & Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | — | ±1 | μA | | | |
| Quiescent Device Current | I _{CC} | V _{CC} or Gnd | 0 | 6 | — | — | 8 | — | 80 | — | 160 | V _{CC} or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | — | 160 | μA | | |
| Additional Quiescent Device Current per input pin. 1 unit load ΔI _{CC} * | | | | | | | | | | | V _{CC} -2.1 | 4.5 to 5.5 | — | 100 | 360 | — | 450 | — | 490 | — | 490 | μA | | | |
| 3-State Leakage Current | I _{OZ} | V _{IL} or V _{IH} | V _O =V _{CC} or Gnd | 6 | — | — | ±0.5 | — | ±5.0 | — | ±10 | V _{IL} or V _{IH} | 5.5 | — | — | ±0.5 | — | ±5.0 | — | ±10 | — | ±10 | μA | | |

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

| Input | Unit Loads* |
|---------|-------------|
| DO — D7 | 0.15 |
| LE | 0.30 |
| OE | 0.55 |

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

HARRIS SEMICONDUCTOR 27E D 430227J 0017827 T HAS

**CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563**

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_A=25^\circ C$, Input $t_r=6ns$)

| CHARACTERISTIC | C_L (pF) | TYPICAL VALUES | | | | UNITS | |
|--|------------------------|----------------|-----|-----|-----|-------|----|
| | | HC | | HCT | | | |
| | | 533 | 563 | 533 | 563 | | |
| Propagation Delay Data to Qn Output Fig. 3 | t_{PLH} t_{PHL} | 15 | 13 | 12 | 14 | 12 | ns |
| Propagation Delay \overline{LE} to Qn Output Fig. 4 | t_{PLH} t_{PHL} | 15 | 14 | 13 | 16 | 14 | |
| Output High Z to High Level, Fig. 6 | t_{PZH} | 15 | 12 | 12 | 14 | 14 | |
| Output High Z to Low Level, Fig. 7 | t_{PZL} | 15 | 12 | 12 | 14 | 14 | |
| Output High Level to High Z, Fig. 6 | t_{PHZ} | 15 | 12 | 12 | 12 | 14 | |
| Output Low Level to High Z, Fig. 7 | t_{PLZ} | 15 | 12 | 12 | 12 | 14 | |
| Power Dissipation Capacitance | C_{PD}^* | — | 42 | 42 | 42 | 42 | pF |

* C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship:
 P_D (total power per latch) = $C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where
 f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

| CHARACTERISTIC | TEST CONDITION V_{CC} V | LIMITS | | | | | | | | | | | | UNITS | |
|--|------------------------------------|--------|------|------|------|----------------|------|-------|------|----------------|------|-------|------|-------|----|
| | | 25°C | | | | -40°C to +85°C | | | | -55° to +125°C | | | | | |
| | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| \overline{LE} Pulse Width (Fig. 4) | t_w | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | 4.5 | 16 | — | 16 | — | 20 | — | 20 | — | 24 | — | 24 | — | | |
| | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | | |
| Set-up Time Data to \overline{LE} (Fig. 5) | t_{su} | 2 | 50 | — | — | — | 65 | — | — | — | 75 | — | — | ns | |
| | 4.5 | 10 | — | 10 | — | 13 | — | 13 | — | 15 | — | 15 | — | | |
| | 6 | 9 | — | — | — | 11 | — | — | — | 13 | — | — | — | | |
| Hold Time Data to \overline{LE} (Fig. 5) | t_H | 2 | 35 | — | — | — | 45 | — | — | — | 55 | — | — | ns | |
| | 4.5 | 7 | — | 8 | — | 9 | — | 10 | — | 11 | — | 12 | — | | |
| | 6 | 6 | — | — | — | 8 | — | — | — | 7 | — | — | — | | |
| | | 2 | 4 | — | — | — | 4 | — | — | — | 4 | — | — | ns | |
| | 4.5 | 4 | — | 5 | — | 4 | — | 5 | — | 4 | — | 5 | — | | |
| | 6 | 4 | — | — | — | 4 | — | — | — | 4 | — | — | — | | |

TRUTH TABLE

| Output Enable | Latch Enable | Data | Q Output |
|------------------|-----------------|------|-------------|
| L | H | H | L |
| L | H | L | H |
| L | L | I | H |
| L | L | h | L |
| H | X | X | Z |

Note:

L = Low voltage level

H = High voltage level

I = Low voltage level one set-up time
prior to the high to low latch enable transition.

h = High voltage level one set-up time

prior to the high to low latch enable transition

X = Don't care

Z = High impedance state

4302271 0017828 J HAS

27E D

HARRIS SEMICONDUCTOR

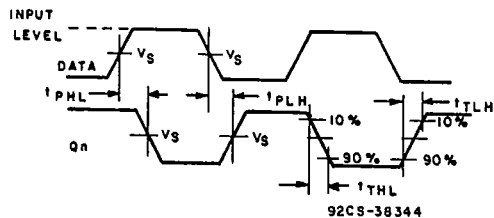
**CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563**

SWITCHING CHARACTERISTICS (C_L = 50 pF, input t_r, t_f = 6 ns)

| CHARACTERISTIC | TEST CONDITIONS V _{CC} (V) | LIMITS | | | | | | | | | | UNITS | | | |
|---------------------------------|--|--------|------|----------------|------|------|------|-----------------|------|------|------|-------|-------|----|----|
| | | +25°C | | -40°C to +85°C | | | | -55°C to +125°C | | | | | | | |
| | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | | 54HCT | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Propagation Delay Data to Qn | t _{PLH} | 2 | — | 165 | — | — | — | 205 | — | — | — | 250 | — | — | ns |
| | t _{PHL} | 4.5 | — | 33 | — | 34 | — | 41 | — | 43 | — | 50 | — | 51 | |
| | 533 | 6 | — | 28 | — | — | — | 35 | — | — | — | 43 | — | — | |
| t _E to Qn | t _{PLH} | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | t _{PHL} | 4.5 | — | 35 | — | 38 | — | 44 | — | 48 | — | 53 | — | 57 | |
| | 533 | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Enable Times | t _{PZH} | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | t _{PZL} | 4.5 | — | 30 | — | 35 | — | 38 | — | 44 | — | 45 | — | 53 | |
| | 533 | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Disable Times | t _{PHZ} | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | t _{PLZ} | 4.5 | — | 30 | — | 30 | — | 38 | — | 38 | — | 45 | — | 45 | |
| | 533 | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Propagation Delay Data to Qn | t _{PLH} | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | t _{PHL} | 4.5 | — | 30 | — | 30 | — | 38 | — | 38 | — | 45 | — | 45 | |
| | 563 | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| t _E to Qn | t _{PLH} | 2 | — | 165 | — | — | — | 205 | — | — | — | 250 | — | — | ns |
| | t _{PHL} | 4.5 | — | 33 | — | 35 | — | 41 | — | 44 | — | 50 | — | 53 | |
| | 563 | 6 | — | 28 | — | — | — | 35 | — | — | — | 43 | — | — | |
| Enable and Disable Times | t _{PZH} , t _{PZL} | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | t _{PHZ} , t _{PLZ} | 4.5 | — | 30 | — | 35 | — | 38 | — | 44 | — | 45 | — | 53 | |
| | 563 | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Input Capacitance | C _i | | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C _o | | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | pF |

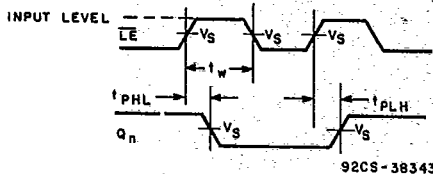
HARRIS SEMICONDUCTOR SECTOR 27E D 4302271 0017829 3 HAS

**CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563**



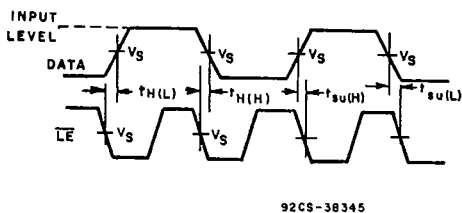
| | 54/74HC | 54/74HCT |
|----------------|---------------------|----------|
| Input Level | V _{CC} | 3 V |
| V _s | 50% V _{CC} | 1.3 V |

Fig. 3 — Data to Q_n output propagation delays and output transition times.



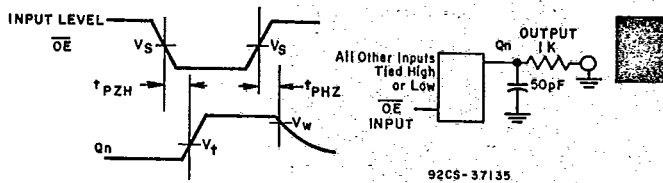
| | 54/74HC | 54/74HCT |
|----------------|---------------------|----------|
| Input Level | V _{CC} | 3 V |
| V _s | 50% V _{CC} | 1.3 V |

Fig. 4 — Latch enable propagation delays.



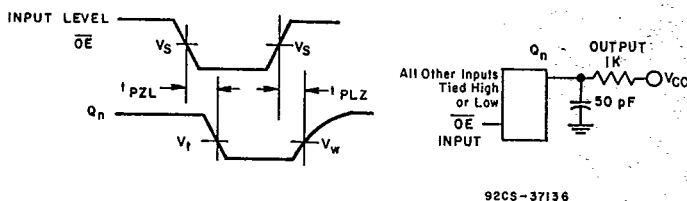
| | 54/74HC | 54/74HCT |
|----------------|---------------------|----------|
| Input Level | V _{CC} | 3 V |
| V _s | 50% V _{CC} | 1.3 V |

Fig. 5 — Latch enable pre-requisite times.



| | 54/74HC | 54/74HCT |
|----------------|---------------------|----------|
| Input Level | V _{CC} | 3 V |
| V _s | 50% V _{CC} | 1.3 V |
| V _i | 50% V _{CC} | 1.3 V |
| V _w | 90% V _{CC} | 4.15 V |

Fig. 6 — 3-state propagation delays.



| | 54/74HC | 54/74HCT |
|----------------|---------------------|----------|
| Input Level | V _{CC} | 3 V |
| V _s | 50% V _{CC} | 1.3 V |
| V _i | 50% V _{CC} | 1.3 V |
| V _w | 10% V _{CC} | 0.45 V |

Fig. 7 — 3-state propagation delays.

HARRIS SEMICONDUCTOR 27E D 430227J 0017830 T HAS