

**Fast CMOS Octal
Transparent Latches**

Product Features:

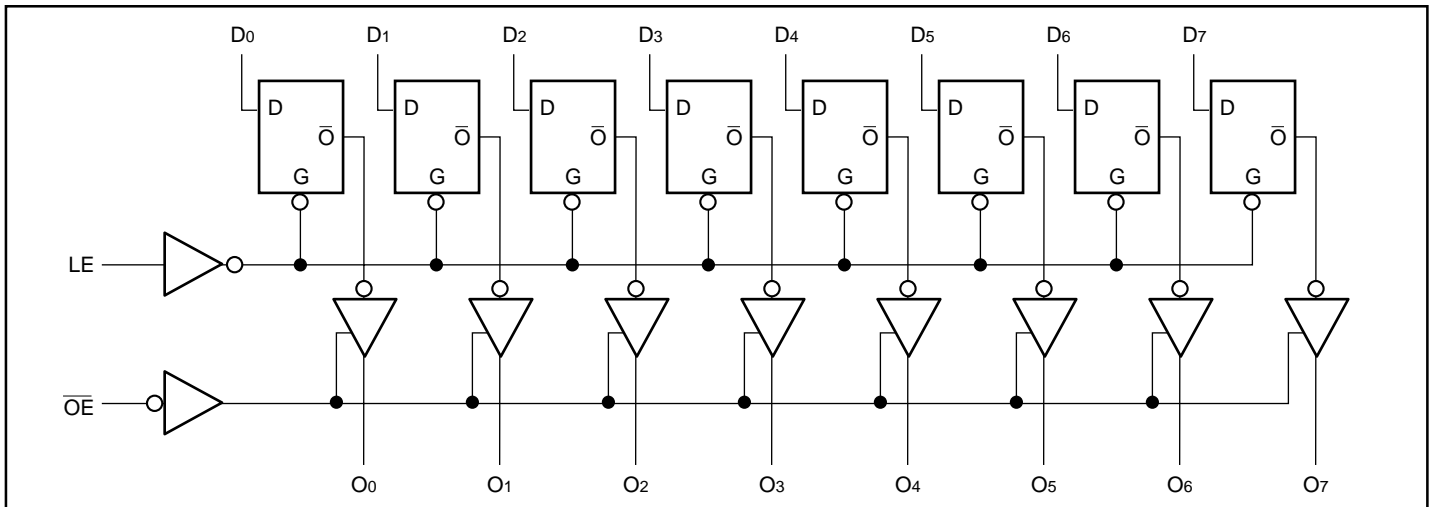
- PI74FCT373/533/573/2373/2573T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 20-pin 173 mil wide plastic TSSOP (L)
 - 20-pin 300 mil wide plastic DIP (P)
 - 20-pin 150 mil wide plastic QSOP (Q)
 - 20-pin 150 mil wide plastic TQSOP (R)
 - 20-pin 300 mil wide plastic SOIC (S)
- Device models available upon request

Product Description:

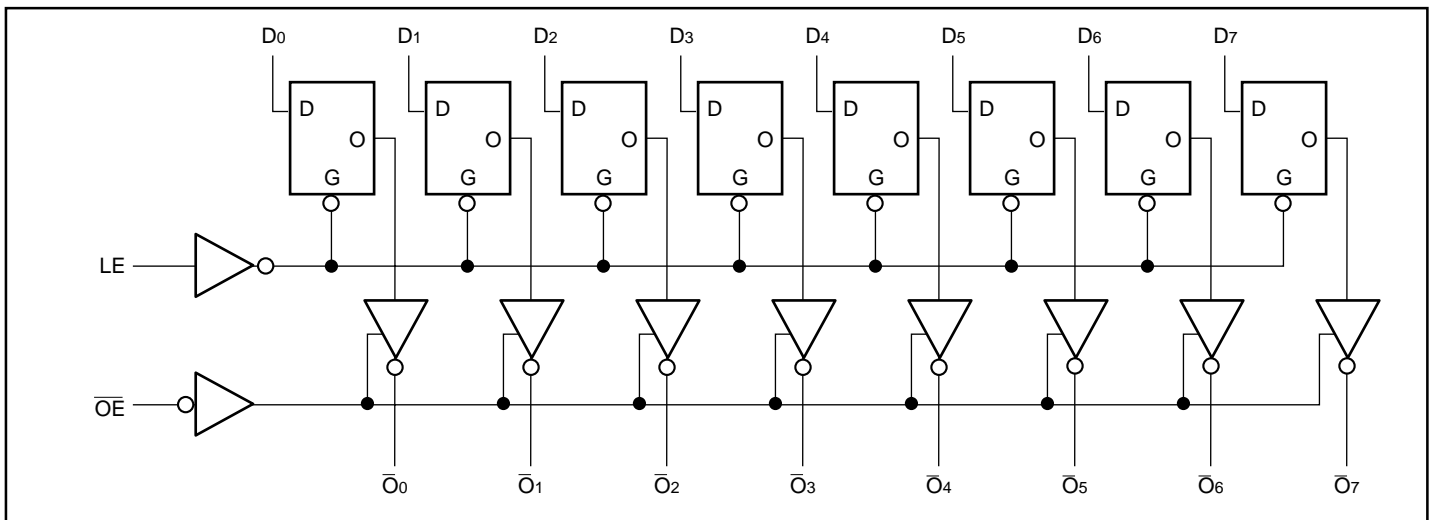
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6/0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise resulting from reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT373T/533T/573T and P174FCT2373T/2573T are 8-bit wide octal transparent latches designed with 3-state outputs and are intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When OE is HIGH, the bus output is in the high impedance state.

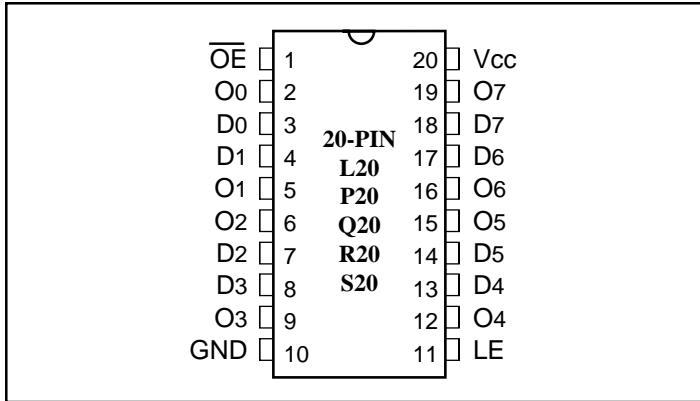
PI74FCT373/2373T and PI74FCT573/2573T Logic Block Diagram



PI74FCT533T Logic Block Diagram



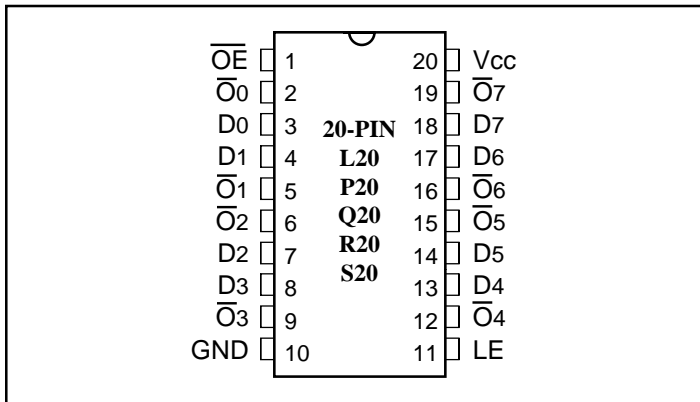
PI74FCT373/2373T Product Pin Configuration



Product Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D0-D7	Data Inputs
O0-O7	3-State Outputs
$\overline{O0-\overline{O7}}$	Complementary 3-State Outputs
GND	Ground
Vcc	Power

PI74FCT533T Product Pin Configuration



PI74FCT533T Truth Table⁽¹⁾

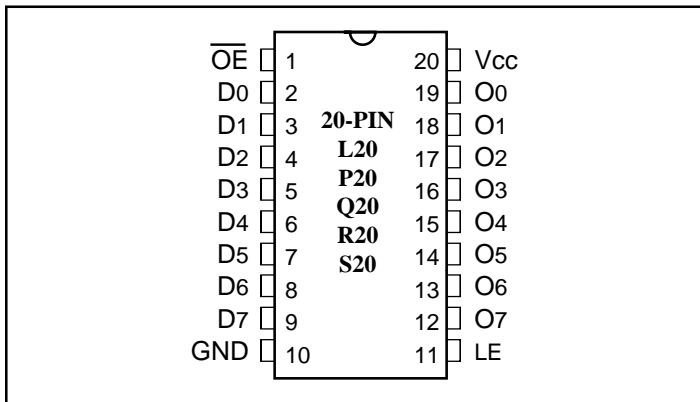
Inputs			Outputs
D _N	LE	\overline{OE}	$\overline{O_N}$
H	H	L	L
L	H	L	H
X	X	H	Z

PI74FCT373/573/2373/2573T Truth Table⁽¹⁾

Inputs			Outputs
D _N	LE	\overline{OE}	O _N
H	H	L	H
L	H	L	L
X	X	H	Z

- H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance

PI74FCT573/2573T Product Pin Configuration





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -15.0 mA	2.4	3.0		V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 64 mA		0.3	0.55	V
VOL	Output LOW Current	VCC = Min., VIN = VIH or VIL	IOL = 12 mA (25Ω Series)		0.3	0.50	V
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
IiH	Input HIGH Current	VCC = Max.	VIN = VCC			1	μA
IiL	Input LOW Current	VCC = Max.	VIN = GND			-1	μA
IOZH	High Impedance	VCC = MAX.	VOUT = 2.7V			1	μA
IOZL	Output Current		VOUT = 0.5V			-1	μA
Vik	Clamp Diode Voltage	VCC = Min., IIN = -18 mA			-0.7	-1.2	V
IOFF	Power Down Disable	VCC = GND, VOUT = 4.5V		—	—	100	μA
Ios	Short Circuit Current	VCC = Max. ⁽³⁾ , VOUT = GND		-60	-120		mA
VH	Input Hysteresis				200		mV

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.,	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open \overline{OE} = GND LE = V _{CC} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle \overline{OE} = GND LE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.5	3.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.8	4.5 ⁽⁵⁾	
			V _{IN} = V _{CC} V _{IN} = GND		3.0	6.0 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.0	14.0 ⁽⁵⁾	

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.



PI74FCT373/2373T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	373T/2373T		373AT/2373AT		373CT/2373CT		373DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay DN to ON	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.9	ns
tpZH tpZL	Output Enable Time OE to ON		1.5	12.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ OE to ON		1.5	7.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
tsu	Setup Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width ⁽³⁾ HIGH		6.0	—	5.0	—	5.0	—	4.0	—	ns

PI74FCT533T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	533T		533AT		533CT		Unit
			Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay DN to ON	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	8.5	2.0	5.5	ns
tpZH tpZL	Output Enable Time OE to ON		1.5	11.0	1.5	6.5	1.5	5.5	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ OE to ON		1.5	7.0	1.5	5.5	1.5	5.0	ns
tsu	Setup Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width ⁽³⁾ HIGH		6.0	—	5.0	—	5.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.



PI74FCT573/2573T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	573T/2573T		573AT/2573AT		573CT		573DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay DN to ON	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	12.0	2.0	8.5	2.0	5.5	2.0	4.9	ns
tpZH tpZL	Output Enable Time OE to ON		1.5	9.5	1.5	6.5	1.5	5.5	1.5	5.5	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ OE to ON		1.5	6.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
tsu	Setup Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	1.5	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.0	—	ns
tw	LE Pulse Width ⁽³⁾ HIGH		6.0	—	5.0	—	5.0	—	3.0	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.