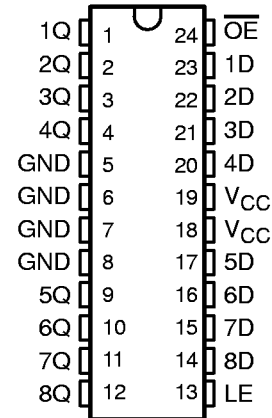


74ACT11373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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- Eight Latches in a Single Package
- 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Buffered Input and Output-Enable Pins
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (NT)

DB, DW, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit latch features 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 74ACT11373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the enable is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 74ACT11373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z



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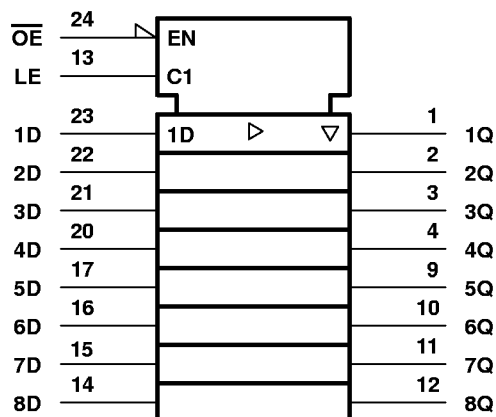
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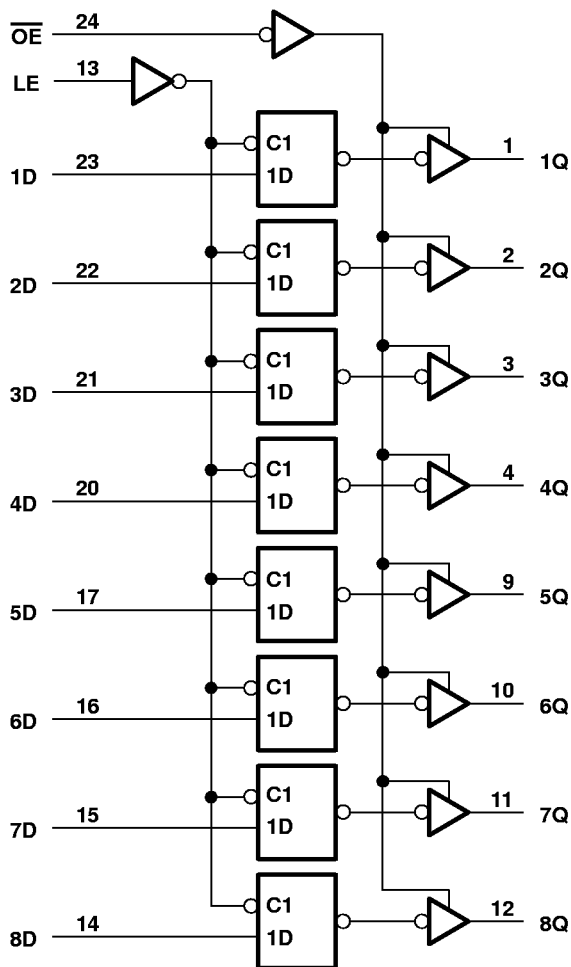
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



74ACT11373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCAS015B – JUNE 1987 – REVISED APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6 V	
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V	
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA	
Continuous current through V_{CC} or GND	±200 mA	
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	DB package	0.65 W
	DW package	1.7 W
	NT package	1.3 W
Storage temperature range, T_{stg}	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	V
I_{OH} High-level output current		–24	mA
I_{OL} Low-level output current		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	ns/V
T_A Operating free-air temperature	–40	85	°C



74ACT11373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCAS015B – JUNE 1987 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX				
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		V	
		5.5 V	5.4			5.4			
	I _{OH} = -24 mA	4.5 V	3.94			3.8			
		5.5 V	4.94			4.8			
I _{OH} = -75 mA [†]	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V				0.1		V	
		5.5 V				0.1			
	I _{OL} = 24 mA	4.5 V				0.44			
		5.5 V				0.44			
	I _{OL} = 75 mA [†]	5.5 V				1.65			
I _{OZ}	V _O = V _{CC} or GND	5.5 V				±0.5		μA	
I _I	V _I = V _{CC} or GND	5.5 V				±0.1		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				8		80	μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V				0.9		1	mA
C _i	V _I = V _{CC} or GND	5 V				4			pF
C _o	V _O = V _{CC} or GND	5 V				10			pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration, LE high	5		5		ns
t _{su}	Setup time, data before LE↓	3.5		3.5		ns
t _h	Hold time, data LE↓	3.5		3.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	D	Q	1.5	7.5	10.3	1.5	11.8	ns
t _{PHL}			1.5	6.5	9.3	1.5	10	
t _{PLH}	LE	Any Q	1.5	8.5	11.3	1.5	13	ns
t _{PHL}			1.5	8.5	10.9	1.5	12.2	
t _{PZH}	$\overline{\text{OE}}$	Any Q	1.5	7	10.7	1.5	12.5	ns
t _{PZL}			1.5	7.5	10.9	1.5	12	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	1.5	10	12.1	1.5	12.2	ns
t _{PLZ}			1.5	7.5	9.5	1.5	10.1	



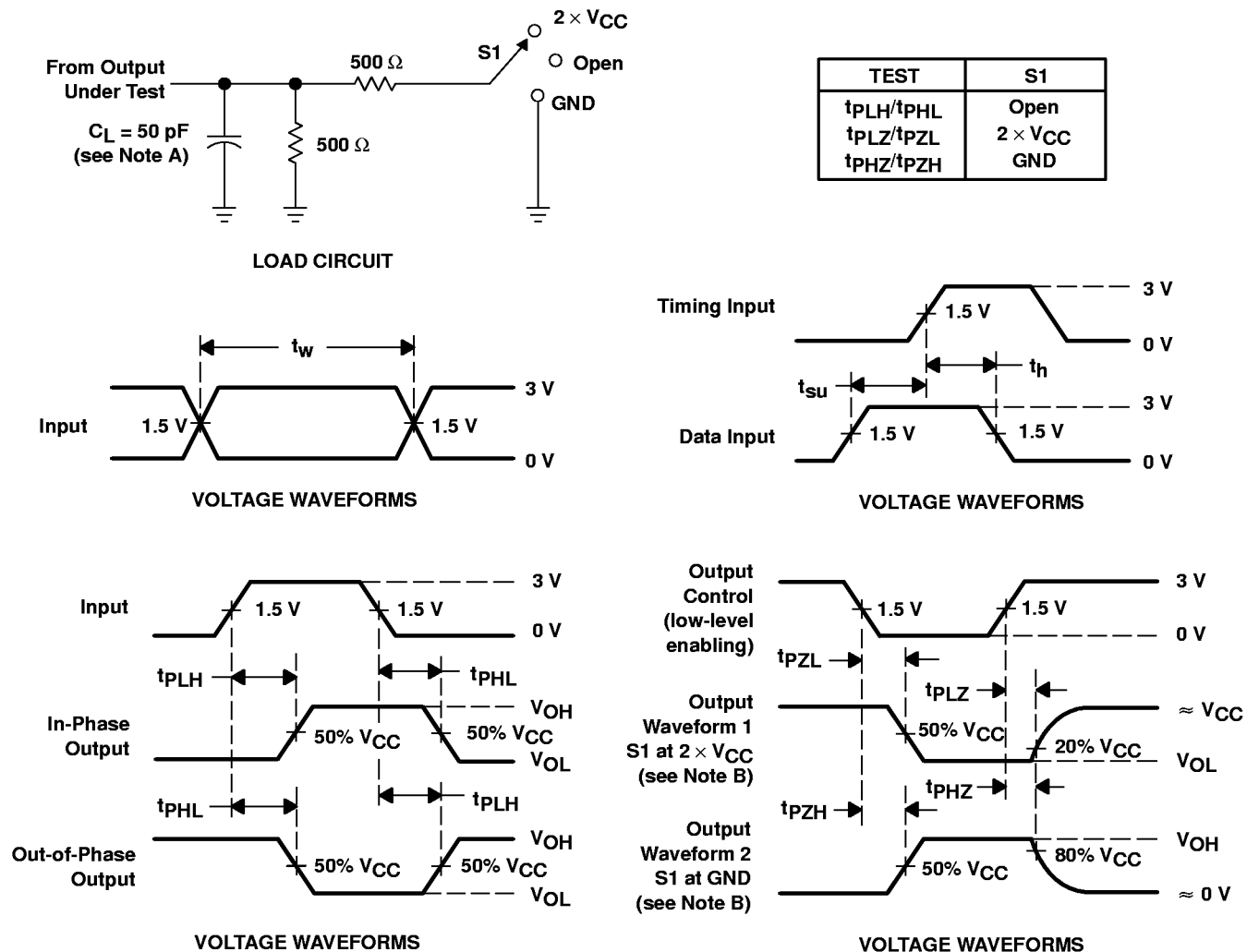
74ACT11373
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WITH 3-STATE OUTPUTS

SCAS015B – JUNE 1987 – REVISED APRIL 1996

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	65	pF
			54	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms