

100355

Low Power Quad Multiplexer/Latch

General Description

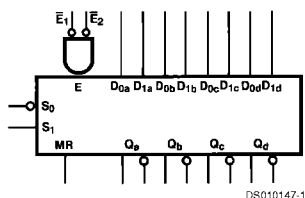
The 100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable (\bar{E}_n) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1 , the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1 . A positive-going signal on either Enable input latches the out-

puts. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 k Ω pulldown resistors.

Features

- Greater than 40% power reduction of the 100155
- 2000V ESD protection
- Pin/function compatible with 100155
- Voltage compensated operating range = -4.2V to -5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

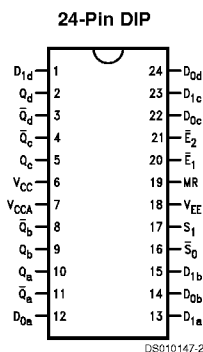
Ordering Code: Logic Symbol



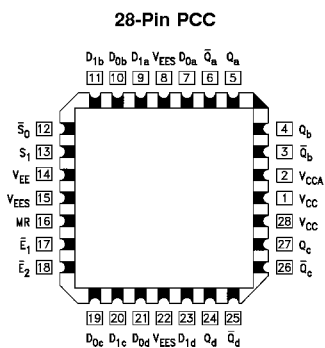
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Pin Names	Description
\bar{E}_1, \bar{E}_2	Enable Inputs (Active LOW)
\bar{S}_0, S_1	Select Inputs
MR	Master Reset
$D_{na}-D_{nd}$	Data Inputs
Q_a-Q_d	Data Outputs
$\bar{Q}_a-\bar{Q}_d$	Complementary Data Outputs

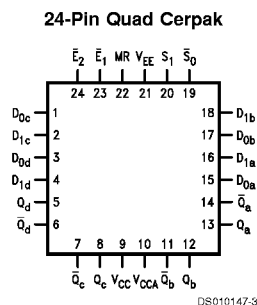
Connection Diagrams



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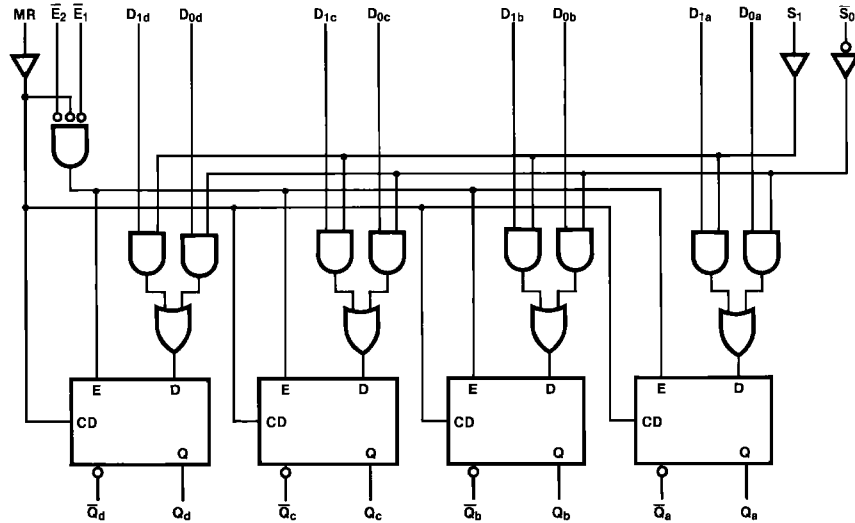


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Logic Diagram



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Operating Mode Table

Controls				Outputs
\bar{E}_1	\bar{E}_2	S_1	\bar{S}_0	Q_n
H	X	X	X	Latched (Note 1)
X	H	X	X	Latched (Note 1)
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Note 1: Stores data present before \bar{E} went HIGH

Truth Table

Inputs						Outputs		
MR	\bar{E}_1	\bar{E}_2	S_1	\bar{S}_0	D_{1x}	D_{0x}	\bar{Q}_x	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched (Note 1)	
L	X	H	X	X	X	X	Latched (Note 1)	

Absolute Maximum Ratings (Note 2)

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610	mV		
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL (Min)}$	
I_{IH}	Input HIGH Current					$V_{IN} = V_{IH (Max)}$	
	\bar{S}_0, S_1			220	μA		
	\bar{E}_1, \bar{E}_2			350			
	$D_{na} - D_{nd}$ MR			340 430			
I_{EE}	Power Supply Current	-87		-40		mA	Inputs Open

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version DIP AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $D_{na} - D_{nd}$ to Output (Transparent Mode)	0.60	1.90	0.60	1.90	0.70	2.00	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	1.00	2.60	1.00	2.60	1.20	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	0.80	2.00	0.80	2.00	0.80	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.30	0.80	2.30	0.80	2.30	ns	Figures 1, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.40	0.60	1.40	0.60	1.40	ns	Figures 1, 2

**Commercial Version
DIP AC Electrical Characteristics** (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_S	Setup Time							ns	Figure 4
	$D_{na}-D_{nd}$	0.90		0.90		0.90			
	\bar{S}_0, S_1	1.70		1.70		1.70			
	MR (Release Time)	1.50		1.50		1.50			Figure 3
t_H	Hold Time							ns	Figure 4
	$D_{na}-D_{nd}$	0.40		0.40		0.40			
	\bar{S}_0, S_1	0.00		0.00		0.00			
$t_{pw} (L)$	Pulse Width LOW \bar{E}_1, \bar{E}_2	2.00		2.00		2.00		ns	Figure 2
$t_{pw} (H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3

**Commercial Version
PCC and Cerpak AC Electrical Characteristics**

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode)	0.60	1.70	0.60	1.70	0.70	1.80	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	1.00	2.40	1.00	2.40	1.20	2.50		
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	0.80	1.80	0.80	1.80	0.80	1.90		
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.10	0.80	2.10	0.80	2.10	ns	Figures 1, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.30	0.60	1.30	0.60	1.30	ns	Figures 1, 2
t_S	Setup Time							ns	Figure 4
	$D_{na}-D_{nd}$	0.80		0.80		0.80			
	\bar{S}_0, S_1	1.60		1.60		1.60			
	MR (Release Time)	1.40		1.40		1.40			Figure 3
t_H	Hold Time							ns	Figure 4
	$D_{na}-D_{nd}$	0.30		0.30		0.30			
	\bar{S}_0, S_1	-0.10		-0.10		-0.10			
$t_{pw} (L)$	Pulse Width LOW \bar{E}_1, \bar{E}_2	2.00		2.00		2.00		ns	Figure 2
$t_{pw} (H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PCC only (Note 5)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		370		370		370	ps	PCC only (Note 5)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		370		370		370	ps	PCC only (Note 5)

Commercial Version PCC and Cerpak AC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
tps	Maximum Skew Pin (Signal) Transition Variation Data to Output Path	270		270		270		ps	PCC only (Note 5)

Note 5: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and tps guaranteed by design.

Industrial Version PCC DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$ (Note 6)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620	mV		
V_{OHc}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to -2.0V
V_{OLc}	Output LOW Voltage	-1565		-1610		mV		
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for ALL Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	1830	1475	mV	Guaranteed LOW Signal for ALL Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL (Min)}$	
I_{IH}	Input HIGH Current					μA	$V_{IN} = V_{IH (Max)}$	
	\bar{S}_0, S_1	300		220				
	\bar{E}_1, \bar{E}_2	350		350				
	$D_{na} - D_{nd}$	340		340				
	MR	430		430				
I_{EE}	Power Supply Current	-87	-40	-87	-40	mA	Inputs Open	

Note 6: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version PCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $D_{na} - D_{nd}$ to Output (Transparent Mode)	0.60	1.70	0.60	1.70	0.70	1.80	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	1.00	2.40	1.00	2.40	1.20	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	0.80	1.80	0.80	1.80	0.80	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.10	0.80	2.10	0.80	2.10	ns	Figures 1, 3

Industrial Version
PCC AC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{TLH}t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.60	1.30	0.60	1.30	ns	Figures 1, 2
t_S	Setup Time							ns	Figure 4
	$D_{na}-D_{nd}$	0.90		0.80		0.80			
	\bar{S}_0, S_1	2.40		1.60		1.60			
	MR (Release Time)	1.50		1.40		1.40			Figure 3
t_H	Hold Time							ns	Figure 4
	$D_{na}-D_{nd}$	0.40		0.30		0.30			
	\bar{S}_0, S_1	0.00		-0.10		-0.10			
$t_{pw}(L)$	Pulse Width LOW \bar{E}_1, \bar{E}_2	2.00		2.00		2.00		ns	Figure 2
$t_{pw}(H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3

Military Version
DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to $-2.0V$	(Notes 7, 8, 9)
		-1085	-870	mV	$-55^\circ C$			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to $-2.0V$	(Notes 7, 8, 9)
		-1830	-1555	mV	$-55^\circ C$			
V_{OHC}	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to $-2.0V$	(Notes 7, 8, 9)
		-1085		mV	$-55^\circ C$			
V_{OLC}	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to $-2.0V$	(Notes 7, 8, 9)
			-1555	mV	$-55^\circ C$			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for ALL Inputs	(Notes 7, 8, 9, 10)	
V_{IL}	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for ALL Inputs	(Notes 7, 8, 9, 10)	
I_{IL}	Input LOW Current	0.50		μA	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL (Min)}$	(Notes 7, 8, 9)	
I_{IH}	Input HIGH Current		220	μA	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH (Max)}$	(Notes 7, 8, 9)	
			\bar{S}_0, S_1					350
			\bar{E}_1, \bar{E}_2					340
			$D_{na}-D_{nd}$					430
			320	μA	$-55^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH (Max)}$	(Notes 7, 8, 9)	
			\bar{S}_0, S_1					500
			\bar{E}_1, \bar{E}_2					490
			$D_{na}-D_{nd}$					630
	MR							
I_{EE}	Power Supply Current	-95	-32	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open	(Notes 7, 8, 9)	

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$ Temp., Subgroups 1, 2, 3, 7, and 8.

Note 9: Sample tested (Method 5005, Table 1) on each Mfg. lot at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ Temp., Subgroups 1, 2, 3, 7, and 8.

Note 10: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version AC Electrical Characteristics

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

Symbol	Parameter	T _C = -55° C		T _C = +25° C		T _C = +125° C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t _{PLH} t _{PHL}	Propagation Delay D _{na} -D _{nd} to Output (Transparent Mode)	0.40	2.30	0.50	2.20	0.50	2.60	ns	Figures 1, 2	(Notes 11, 12, 13)
t _{PLH} t _{PHL}	Propagation Delay S ₀ , S ₁ to Output (Transparent Mode)	0.60	3.00	0.80	2.70	0.80	3.20	ns		
t _{PLH} t _{PHL}	Propagation Delay E ₁ , E ₂ to Output	0.50	2.60	0.60	2.30	0.70	2.70	ns		
t _{PLH} t _{PHL}	Propagation Delay MR to Output	0.60	2.80	0.70	2.60	0.70	2.90	ns	Figures 1, 3	(Notes 11, 12, 13)
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.40	1.90	0.40	1.90	ns	Figures 1, 2	(Note 14)
t _S	Setup Time D _{na} -D _{nd}	0.90		0.90		0.90		ns	Figure 4	(Note 14)
	S ₀ , S ₁	2.40		2.40		2.40			Figure 3	
	MR (Release Time)	1.50		1.50		1.50				
t _H	Hold Time D _{na} -D _{nd}	0.40		0.40		0.40		ns	Figure 4	(Note 14)
	S ₀ , S ₁	0.00		0.00		0.00				
t _{pw} (L)	Pulse Width LOW E ₁ , E ₂	2.00		2.00		2.00		ns	Figure 2	(Note 14)
t _{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3	(Note 14)

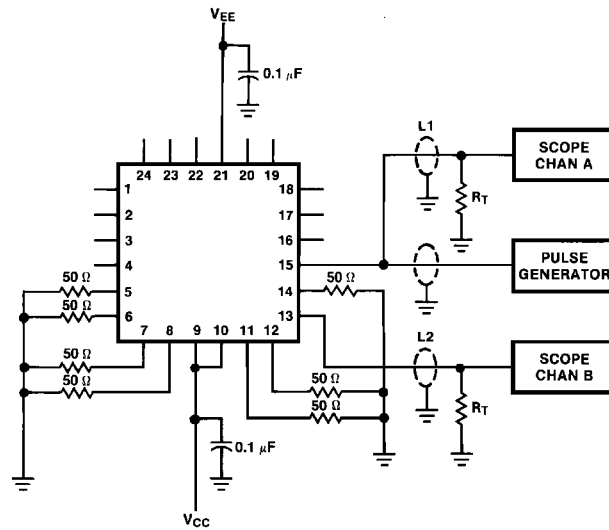
Note 11: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55° C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 12: Screen tested 100% on each device at +25° C, Temperature only, Subgroup A9.

Note 13: Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°, Subgroup A9, and at +125° C, and -55° C Temp., Subgroups A10 & A11.

Note 14: Not tested at +25° C, +125° C and -55° C Temperature (design characterization data).

Test Circuit



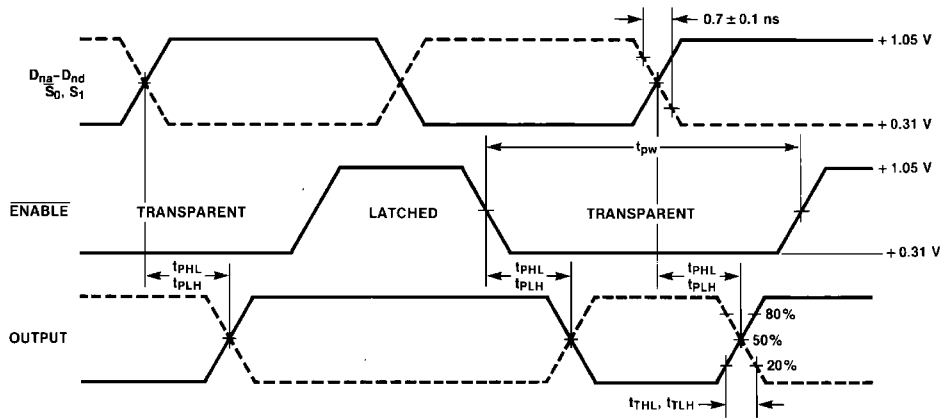
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Notes:

- V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$
- L1 and L2 = equal length 50 Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50 Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit
(Using Quad Cerpak)

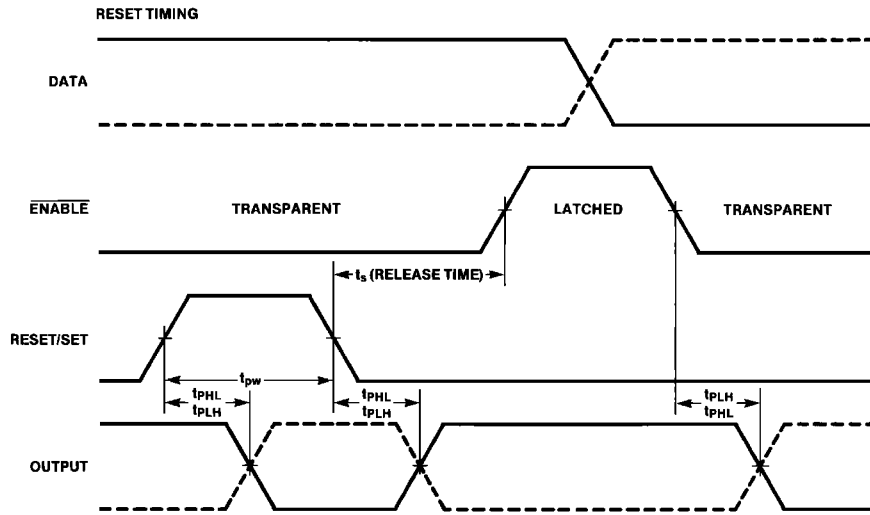
Switching Waveforms



DS010147-7

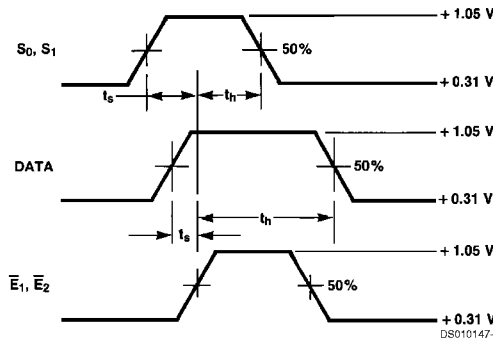
FIGURE 2. Enable Timing

Switching Waveforms (Continued)



DS010147-8

FIGURE 3. Reset Timing



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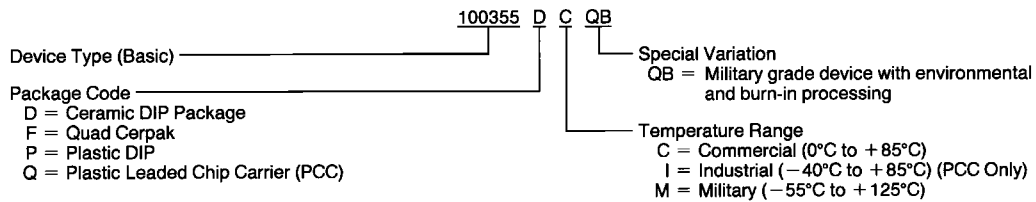
Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.
 t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Times

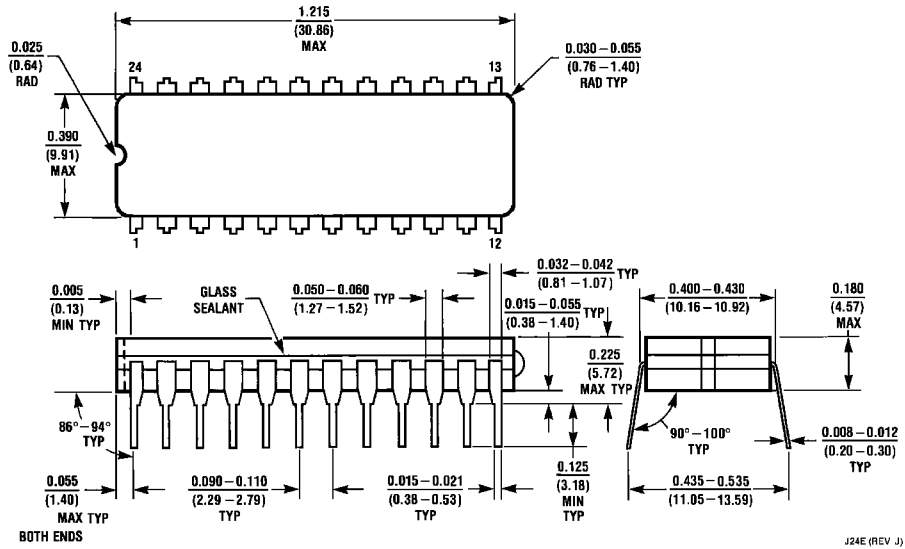
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

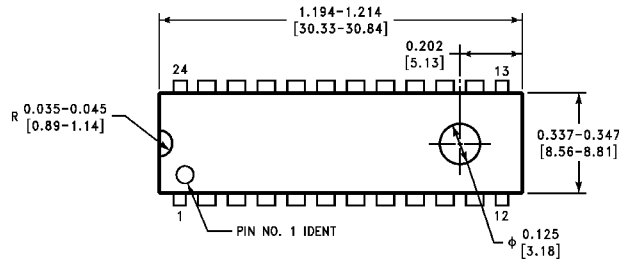


DS010147-11

Physical Dimensions inches (millimeters) unless otherwise noted

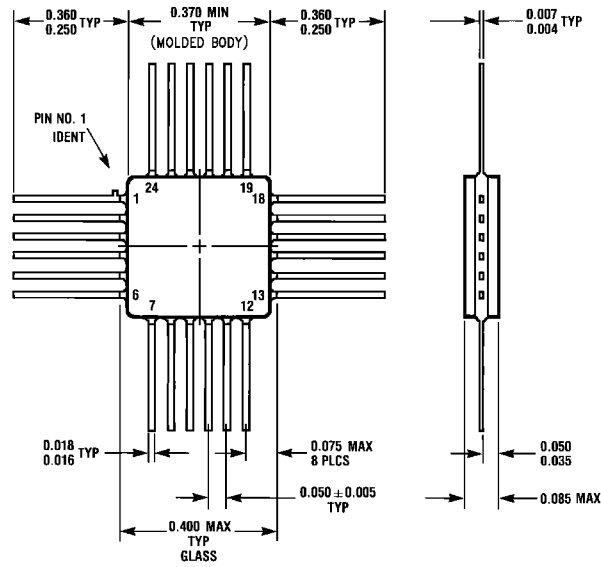


**24-Lead Ceramic Dual-In-Line Package (D)
Package Number J24E**



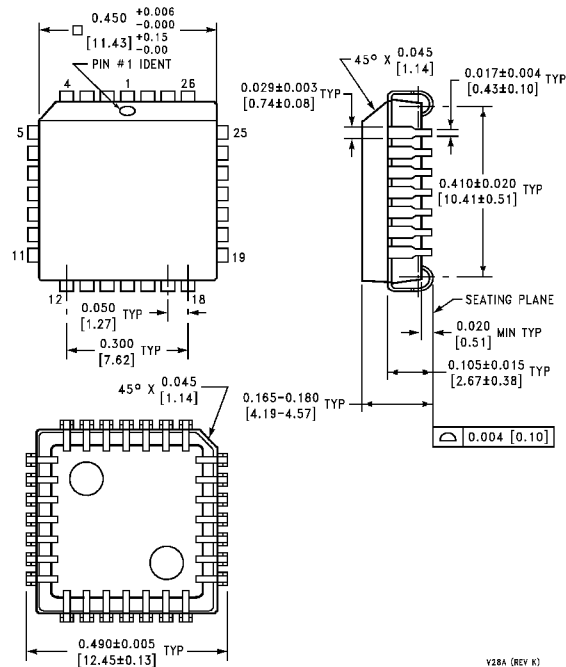
**24-Lead Plastic Dual-In-Line Package (P)
Package Number N24E**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



W24B (REV D)

**24-Lead Ceramic Flatpak (F)
Package Number W24C**



V28A (REV K)

**28-Lead Plastic Chip Carrier (Q)
Package Number V28A**

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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