

# 74F841

## 10-Bit Transparent Latch

### General Description

The 74F841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 74F841 is a 10-bit transparent latch, a 10-bit version of the 74F373.

### Features

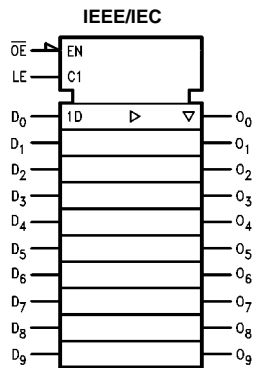
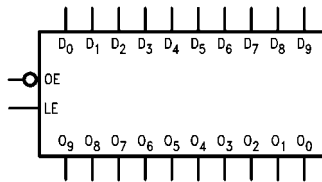
- 3-STATE output

### Ordering Code:

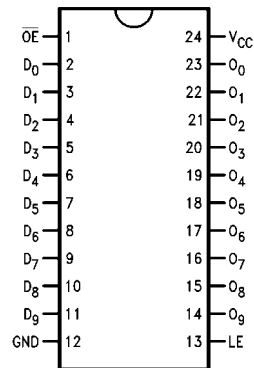
Order Number	Package Number	Package Description
74F841SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F841SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> –D <sub>9</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
O <sub>0</sub> –O <sub>9</sub>	3-STATE Outputs	150/40	–3 mA/24 mA
$\overline{OE}$	Output Enable Input	1.0/1.0	20 $\mu$ A/–0.6 mA
LE	Latch Enable	1.0/1.0	20 $\mu$ A/–0.6 mA

## Functional Description

The 74F841 device consists of ten D-type latches with 3-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

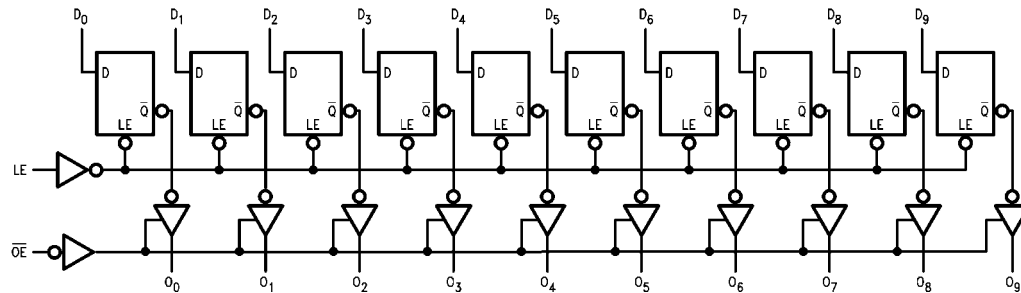
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

## Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched
L	X	X	H	H	Preset
L	X	X	L	L	Clear
L	X	X	H	H	Preset
H	L	X	L	Z	Latched
H	L	X	H	Z	Latched

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = HIGH Impedance  
NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

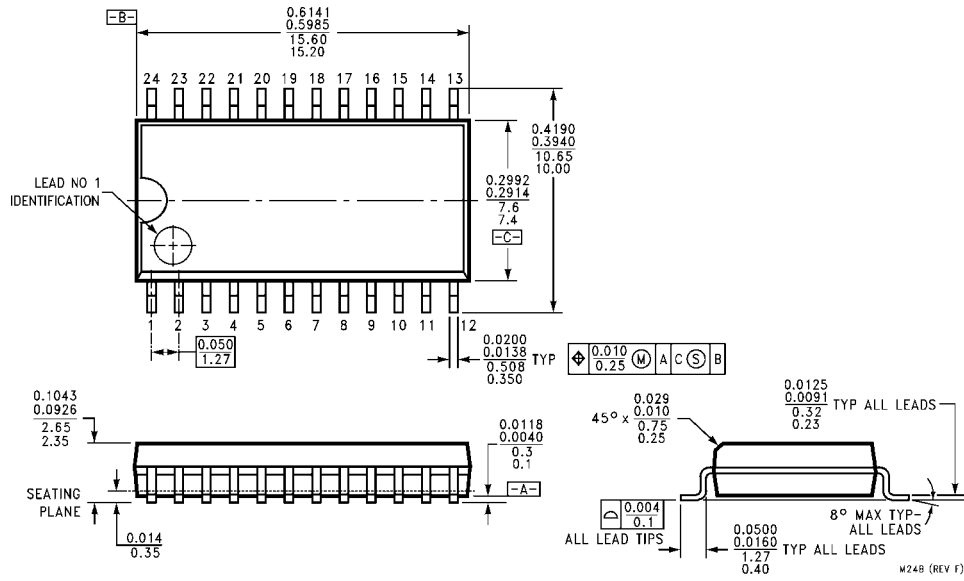
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		69	92	mA	Max	V <sub>O</sub> = HIGH Z

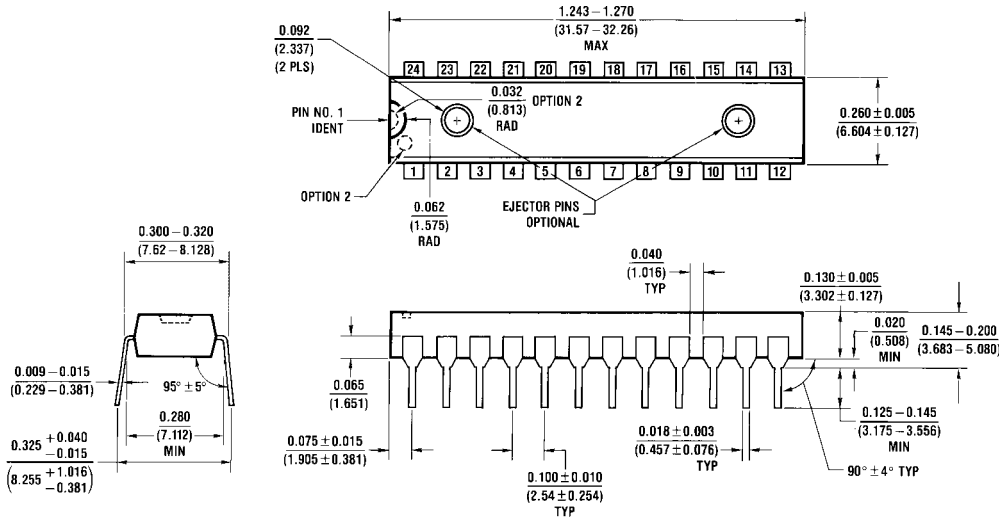
AC Electrical Characteristics							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
$t_{PLH}$	Propagation Delay	2.5		8.0	2.0	9.0	ns
$t_{PHL}$	$D_n$ to $O_n$	1.5		6.5	1.5	7.0	
$t_{PLH}$	Propagation Delay	5.0		12.0	4.5	13.5	ns
$t_{PHL}$	LE to $O_n$	2.0		7.5	2.0	8.0	
$t_{PZH}$	Output Enable Time	2.5		8.5	2.0	9.5	ns
$t_{PZL}$	$\overline{OE}$ to $O_n$	2.5		9.0	2.0	10.0	
$t_{PHZ}$	Output Disable Time	1.0		6.5	1.0	7.5	ns
$t_{PLZ}$	$\overline{OE}$ to $O_n$	1.0		6.5	1.0	7.5	
AC Operating Requirements							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	2.0		2.5		ns	
$t_S(L)$	$D_n$ to LE	2.0		2.5			
$t_H(H)$	Hold Time, HIGH or LOW	2.5		3.0		ns	
$t_H(L)$	$D_n$ to LE	3.0		3.5			
$t_W(H)$	LE Pulse Width, HIGH	4.0		4.0		ns	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N24C (REV F)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C**

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