FAIRCHILD SEMICONDUCTOR™

June 1998
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NC7SZ373
TinyLogic™ UHS D-Type Latch with 3-STATE Output

General Description

The NC7SZ373 is a single positive edge-triggered D-type CMOS Latch with 3-STATE output from Fairchild's Ultra High Speed Series of TinyLogic™ in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.8V to 5.5V range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage. The latch appears transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. The output tolerates voltages above V_{CC} in the 3-STATE condition.

Features

- Space saving SC70 6-lead package
- Ultra High Speed; t_{PD} 2.6 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive; ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.8V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7SZ373P6	MAA06A	Z73	6-Lead SC70, EIAJ SC88, 1.25mm Wide	250 Units on Tape and Reel
NC7SZ373P6X	MAA06A	Z73	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel

Pin Descriptions

Pin Names	Description
D	Data Input
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
Q	Latch Output

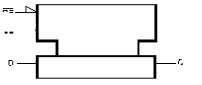
Function Table

Inputs			Output
LE	D	$\overline{OE}$	Q
H	L	L	L
H	H	L	H
L	X	L	Q_{n-1}
X	X	H	Z

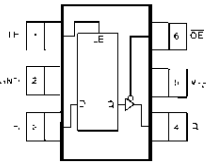
H = HIGH Logic Level X = Immaterial
L = LOW Logic Level Z = HIGH Impedance
Q_{n-1} = Previous state prior to HIGH-to-LOW transition of latch enable

Logic Symbol

IEEE/IEC

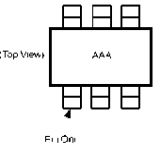


Connection Diagrams



(Top View)

Pin One Orientation Diagram



AAA = Package Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top package mark left to right. Pin One is the lower left pin (see diagram)

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_{IN} < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_{OUT} < 0V	−50 mA
DC Output (I_{OUT}) Source/Sink Current	±50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temp. (T_L)	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @+85°C	180 mW

Recommended Operating Conditions

Power Supply	
Operating (V_{CC})	1.8V to 5.5V
Data Retention	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	
Active State	0V to V_{CC}
3-STATE	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 1.8V, 2.5V ±0.2V	0 to 20 ns/V
V_{CC} = 3.3V ±0.3V	0 to 10 ns/V
V_{CC} = 5.5V ±0.5V	0 to 5 ns/V
Operating Temperature (T_A)	−40°C to +85°C
Thermal Resistance (θ_{JA})	350° C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Min	T_A = +25°C Typ	T_A = +25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Unit	Conditions	
V_{IH}	HIGH Level Control Input Voltage	1.8	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Control Input Voltage	1.8			0.25 V_{CC}		0.25 V_{CC}	V		
		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Control Output Voltage	1.8	1.7	1.8		1.7		V	V_{IN} = V_{IH}	I_{OH} = −100 µA
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		2.3	1.9	2.15		1.9				I_{OH} = −8 mA
		3.0	2.4	2.8		2.4				I_{OH} = −16 mA
		3.0	2.3	2.68		2.3				I_{OH} = −24 mA
		4.5	3.8	4.2		3.8				I_{OH} = −32 mA
V_{OL}	LOW Level Control Output Voltage	1.8		0.0	0.1		0.1	V	V_{IN} = V_{IL}	I_{OL} = 100 µA
		2.3		0.0	0.1		0.1			
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		2.3		0.10	0.3		0.3	V		I_{OL} = 8 mA
		3.0		0.15	0.4		0.4			I_{OL} = 16 mA
		3.0		0.22	0.55		0.55			I_{OL} = 24 mA
		4.5		0.22	0.55		0.55			I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	µA	0 ≤ V_{IN} ≤ 5.5V	
I_{OZ}	3-STATE Output Leakage	1.8 to 5.5			±0.5		±5.0	µA	V_{IN} = V_{IL} or V_{IH} 0 ≤ V_{OUT} ≤ 5.5V	
I_{OFF}	Power-Off Leakage Current	0.0			1.0		10	µA	V_{IN} or V_{OUT} = 5.5V	
I_{CC}	Quiescent Supply Current	1.8 to 5.5			1.0		10	µA	V_{IN} = 5.5V, GND	

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay	1.8	2.0	6.1	10.0	2.0	10.5	ns		Figure 1
t_{PHL}	D to Q	2.5 ± 0.2	1.5	3.6	6.5	1.6	6.8		C_L = 15 pF	Figure 3
		3.3 ± 0.3	1.0	2.7	4.6	1.2	5.0		R_L = 1 MΩ	
		5.0 ± 0.5	1.0	2.0	3.4	1.0	3.7		S_1 = Open	
		3.3 ± 0.3	1.5	3.3	5.5	1.5	6.2		C_L = 50 pF	Figure 1
		5.0 ± 0.5	1.0	2.6	4.3	1.3	4.8		R_L = 500Ω, S_1 = Open	Figure 3
t_{PLH}	Propagation Delay	1.8	2.0	6.0	9.6	2.0	10.0	ns		Figure 1
t_{PHL}	LE to Q	2.5 ± 0.2	1.8	3.5	6.1	1.5	6.6		C_L = 15 pF	Figure 3
		3.3 ± 0.3	1.3	2.6	4.4	1.0	4.8		R_L = 1 MΩ	
		5.0 ± 0.5	1.0	2.0	3.2	0.8	3.5		S_1 = Open	
		3.3 ± 0.3	1.5	3.3	5.3	1.5	6.2		C_L = 50 pF	Figure 1
		5.0 ± 0.5	1.3	2.6	4.2	1.2	4.6		R_L = 500Ω, S_1 = Open	Figure 4
t_{PZL}	Output Enable Time	1.8	2.0	6.0	9.0	2.0	9.5	ns	C_L = 50 pF, V_1 = 2x V_{CC}	Figure 1
t_{PZH}		2.5 ± 0.2	2.0	3.7	6.0	1.8	6.6		R_U, R_D = 500Ω	Figure 4
		3.3 ± 0.3	1.5	2.8	5.0	1.4	5.3		S1 = GND for t_{PZH}	
		5.0 ± 0.5	1.0	2.2	3.7	1.0	3.9		S1 = V_1 for t_{PZL}	
t_{PLZ}	Output Disable Time	1.8	2.0	5.1	8.0	2.0	8.5	ns	C_L = 50 pF, V_1 = 2x V_{CC}	Figure 1
t_{PHZ}		2.5 ± 0.2	2.0	3.5	6.0	1.8	6.3		R_U, R_D = 500Ω	Figure 4
		3.3 ± 0.3	1.5	2.8	4.5	1.4	4.7		S_1 = GND for t_{PHZ}	
		5.0 ± 0.5	1.0	2.3	3.7	1.0	3.9		S_1 = V_1 for t_{PLZ}	
t_S	Setup Time,	2.5 ± 0.2				2.0		ns	C_L = 50 pF	Figure 1
	D to LE	3.3 ± 0.3				1.5			R_L = 500 Ω, S_1 = Open	Figure 5
		5.0 ± 0.5				1.5				
t_H	Hold Time,	2.5 ± 0.2				1.5		ns	C_L = 50 pF	Figure 1
	D to LE	3.3 ± 0.3				1.5			R_L = 500 Ω, S_1 = Open	Figure 5
		5.0 ± 0.5				1.5				
t_W	Pulse Width, LE	2.5 ± 0.2				3.0		ns		Figure 1
		3.3 ± 0.3				3.0			C_L = 50 pF	Figure 5
		5.0 ± 0.5				3.0			R_L = 500 Ω, S_1 = Open	

Capacitance (Note 2)

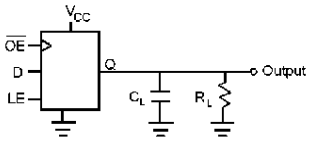
Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	3		pF	V_{CC} = Open, V_{IN} = 0V or V_{CC}
C_{OUT}	Output Capacitance	4		pF	V_{CC} = 3.3V, V_{IN} = 0V or V_{CC}
C_{PD}	Power Dissipation Capacitance	14		pF	V_{CC} = 3.3V
	(Note 3)	17			V_{CC} = 5.0V

Note 2: $T_A = +25C$ f = 1 MHz

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle (See Figure 2) C_{PD} is related to I_{CCD} dynamic operating current by the expression

$I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$

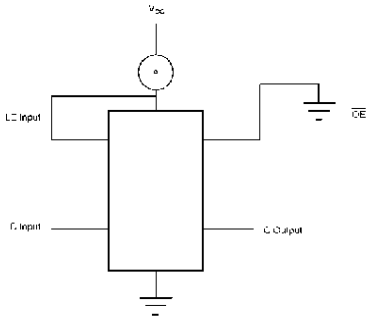
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz t_w = 500 ns

FIGURE 1. AC Test Circuit



D Input = AC Waveform, $t_r = t_f = 1.8$ ns,

D Input PRR = 10 MHz, Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

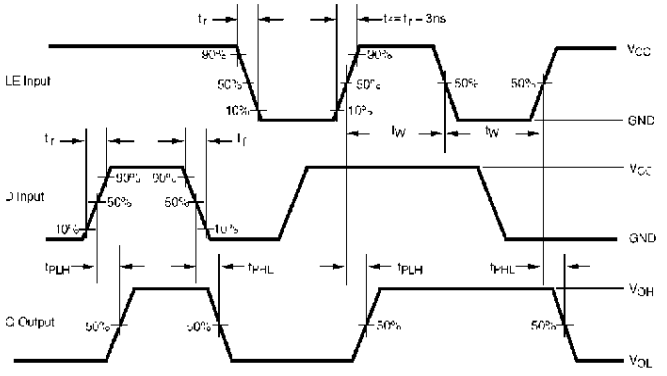


FIGURE 3. AC Waveforms

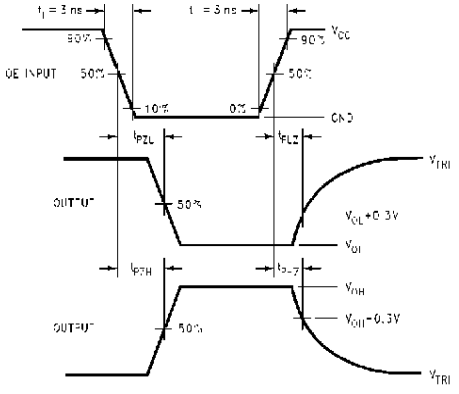


FIGURE 4. AC Waveforms

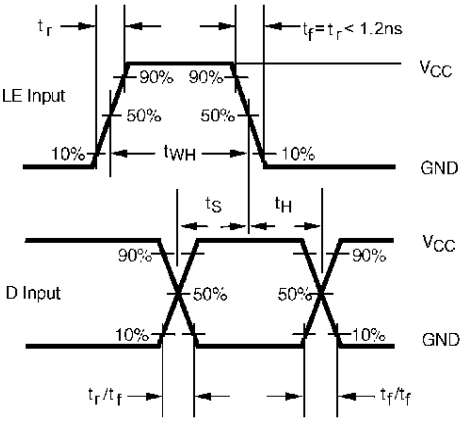


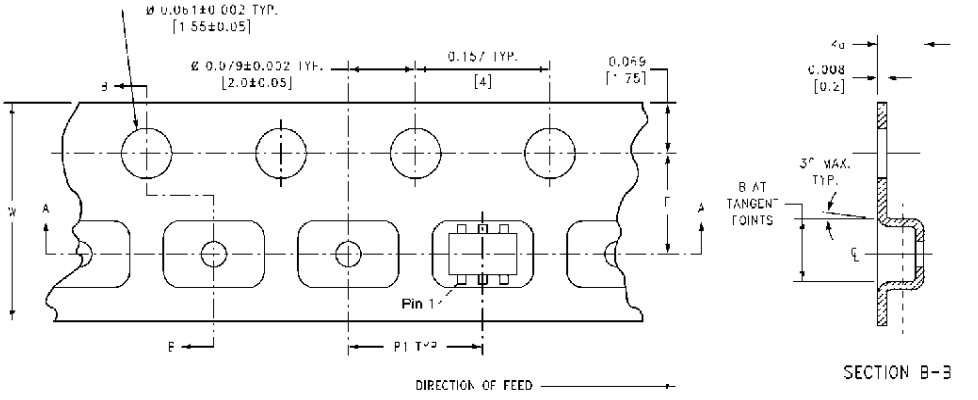
FIGURE 5. AC Waveforms

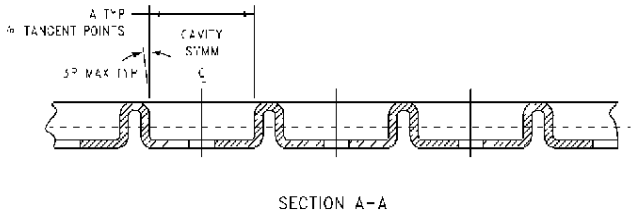
Tape and Reel Specification

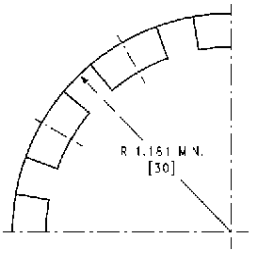
TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

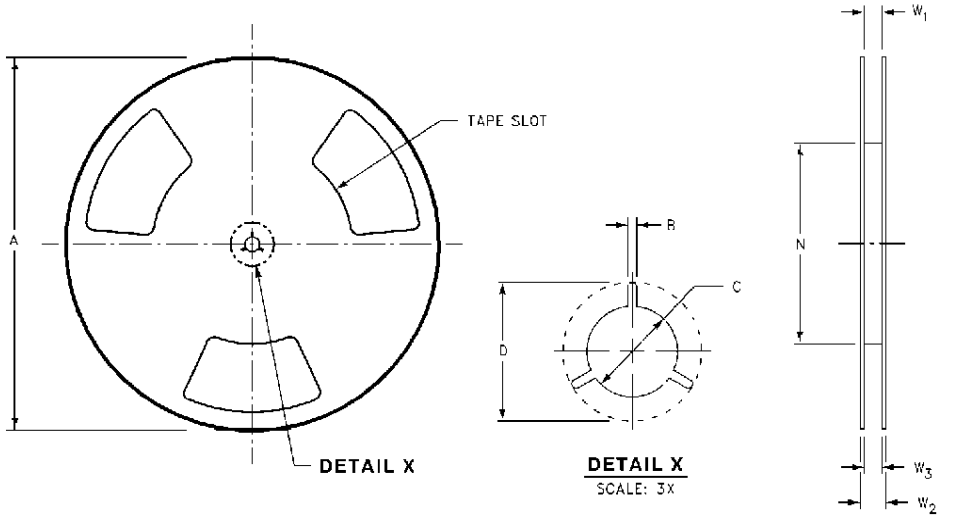






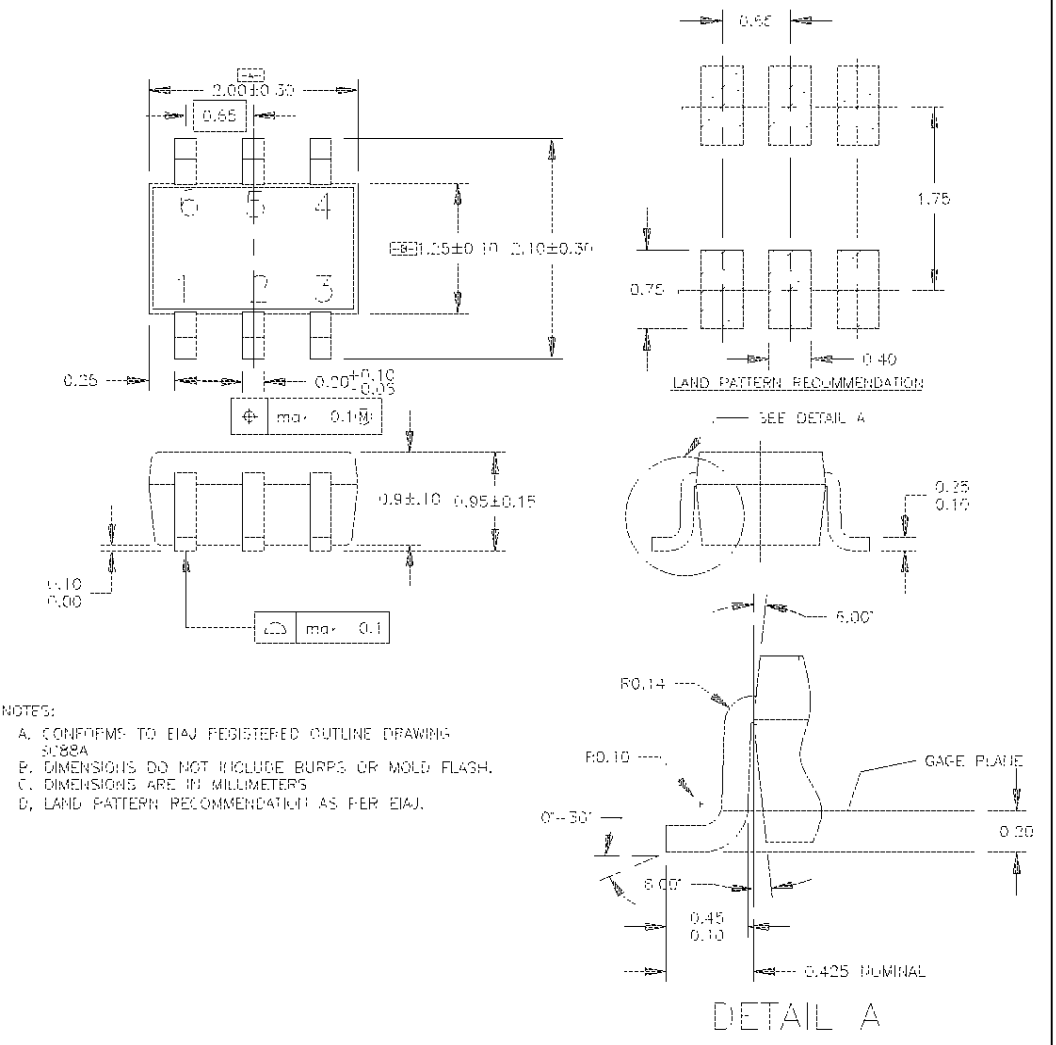
Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.
D. LAND PATTERN RECOMMENDATION AS PER EIAJ.

6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A