FAIRCHILD SEMICONDUCTOR®

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# DM74ALS563A
# Octal D-Type Transparent Latch with 3-STATE Output

## Features

- Switching specifications at 50pF
- Switching specifications guaranteed over full temperature and $V_{CC}$ range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly

## General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the DM74ALS563A are transparent D-type latches. While the enable (G) is HIGH the Q outputs will follow the data (D) inputs. When the enable is taken LOW the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

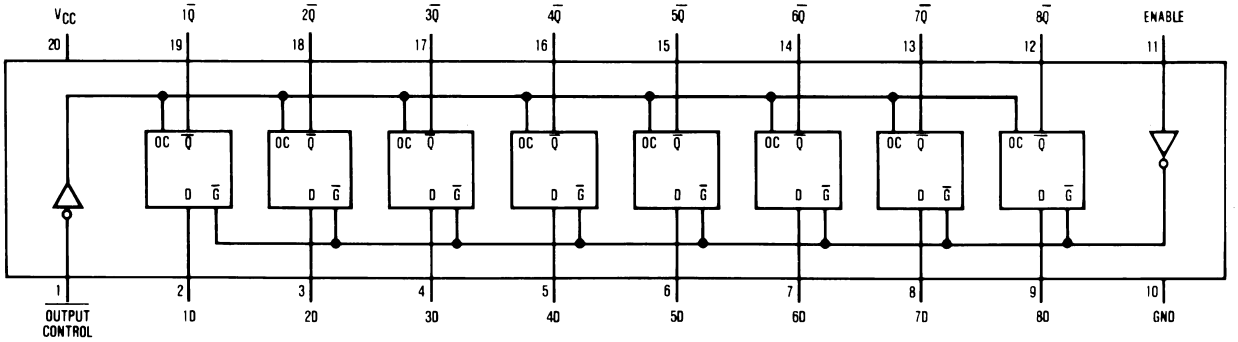
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

## Ordering Information

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74ALS563AWM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

## Connection Diagram




## Function Table

| $\overline{\text{Output Control}}$ | Enable G | D | Output $\overline{Q}$ |
|---|---|---|---|
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q}_0$ |
| H | X | X | Z |

L = LOW State

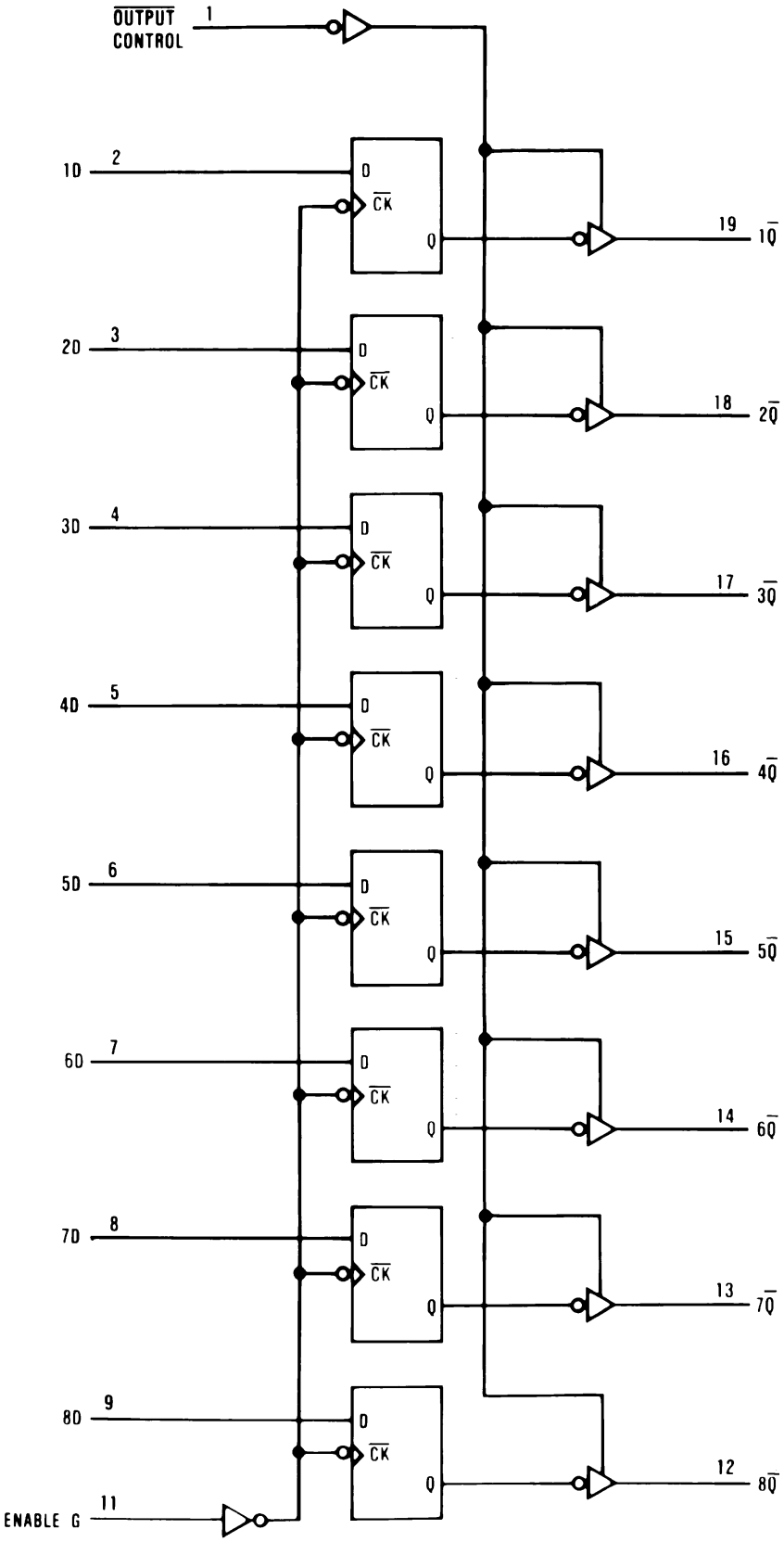
H = HIGH State

X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

## Logic Diagram



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Supply Voltage | 7V |
| $V_I$ | Input Voltage | 7V |
| | Voltage Applied to Disabled Output | 5.5V |
| $T_A$ | Operating Free Air Temperature Range | 0°C to +70°C |
| $T_{STG}$ | Storage Temperature Range | –65°C to +150°C |
| $\theta_{JA}$ | Typical Thermal Resistance | 75.0°C/W |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Nom. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | HIGH Level Input Voltage | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | –2.6 | mA |
| $I_{OL}$ | LOW Level Output Current | | | 24 | mA |
| $t_W$ | Width of Enable Pulse, HIGH or LOW | 15 | | | ns |
| $t_{SU}$ | Data Setup Time(1) | 10↓ | | | ns |
| $t_H$ | Data Hold Time(1) | 10↓ | | | ns |
| $T_A$ | Free Air Operating Temperature | 0 | | 70 | °C |

**Note:**

1. The (↓) arrow indicates the negative edge of the enable is used for reference.

## Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at $V_{CC}$ = 5V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = 4.5V, $I_I$ = –18 mA | | | | –1.2 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = 4.5V, $V_{IL}$ = $V_{IL}$ Max., $I_{OH}$ = Max. | | 2.4 | 3.2 | | V |
| | | $V_{CC}$ = 4.5V to 5.5V, $I_{OH}$ = –400µA | | $V_{CC}$ – 2 | | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = 4.5V, $V_{IH}$ = 2V | $I_{OL}$ = 12mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24mA | | 0.35 | 0.5 | |
| $I_I$ | Input Current @ Maximum Input Voltage | $V_{CC}$ = 5.5V, $V_{IH}$ = 7V | | | | 0.1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = 5.5V, $V_{IH}$ = 2.7V | | | | 20 | µA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = 5.5V, $V_{IL}$ = 0.4V | | | | –0.1 | mA |
| $I_O$ | Output Drive Current | $V_{CC}$ = 5.5V, $V_O$ = 2.25V | | –30 | | –112 | mA |
| $I_{OZH}$ | OFF-State Output Current HIGH Level Voltage Applied | $V_{CC}$ = 5.5V, $V_{IH}$ = 2V, $V_O$ = 2.7V | | | | 20 | µA |
| $I_{OZL}$ | OFF-State Output Current LOW Level Voltage Applied | $V_{CC}$ = 5.5V, $V_{IH}$ = 2V, $V_O$ = 0.4V | | | | –20 | µA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5.5V, Outputs OPEN | Outputs HIGH | | 10 | 17 | mA |
| | | | Outputs LOW | | 16 | 26 | |
| | | | Outputs Disabled | | 17 | 29 | |

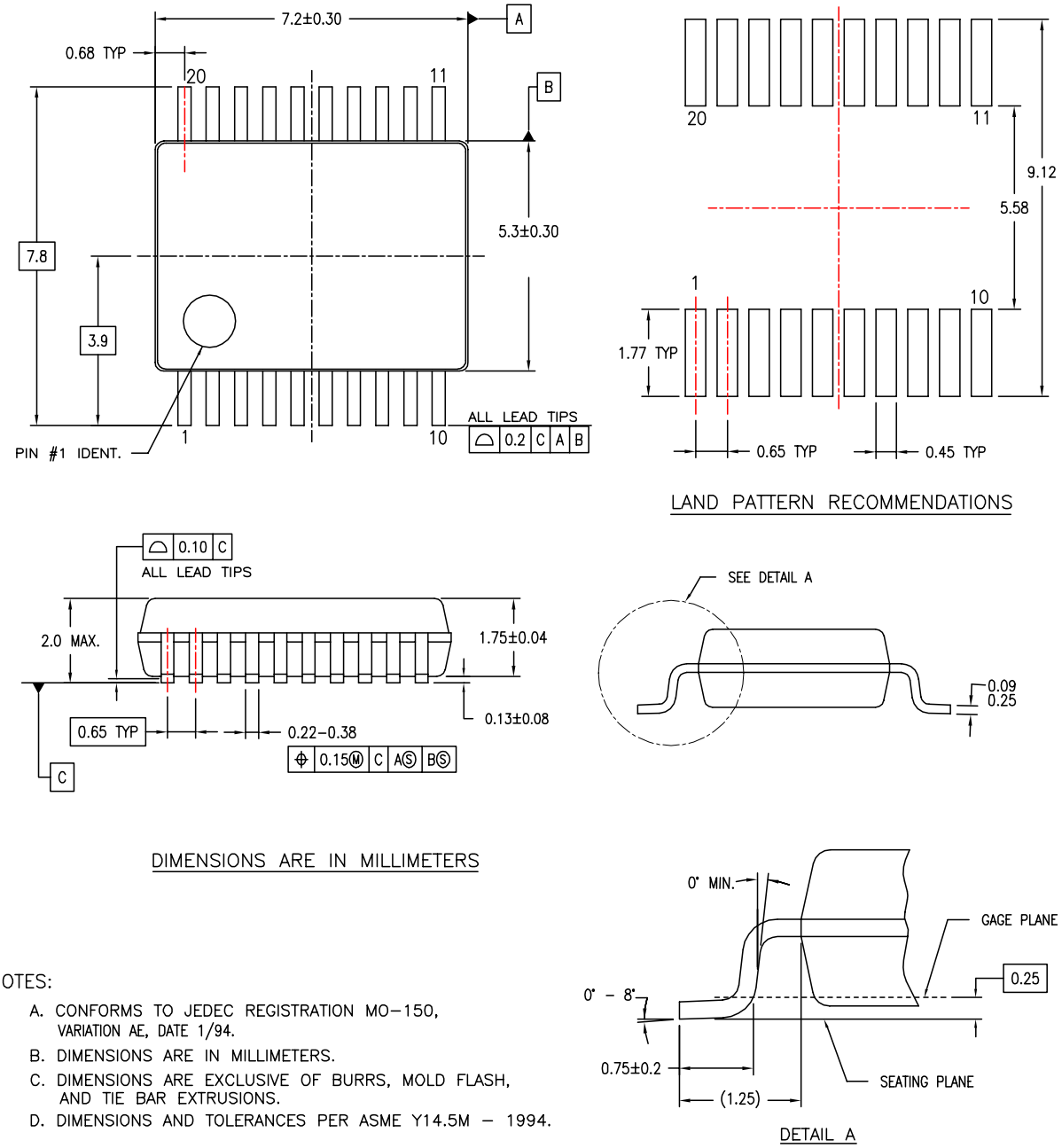
## Switching Characteristics

Over recommended operating free air temperature range.

| Symbol | Parameter | Conditions | From | To | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, LOW-to-HIGH Level Output | $V_{CC}$ = 4.5V to 5.5V, $R_L$ = 500Ω, $C_L$ = 50pF | Data | Any $\overline{Q}$ | 3 | 18 | ns |
| $t_{PHL}$ | Propagation Delay Time, HIGH-to-LOW Level Output | | Data | Any $\overline{Q}$ | 3 | 14 | ns |
| $t_{PLH}$ | Propagation Delay Time, LOW-to-HIGH Level Output | | Enable | Any $\overline{Q}$ | 8 | 22 | ns |
| $t_{PHL}$ | Propagation Delay Time, HIGH-to-LOW Level Output | | Enable | Any $\overline{Q}$ | 8 | 21 | ns |
| $t_{PZH}$ | Output Enable Time to HIGH Level Output | | Output Control | Any $\overline{Q}$ | 4 | 18 | ns |
| $t_{PZL}$ | Output Enable Time to LOW Level Output | | Output Control | Any $\overline{Q}$ | 4 | 18 | ns |
| $t_{PHZ}$ | Output Disable Time from HIGH Level Output | | Output Control | Any $\overline{Q}$ | 2 | 10 | ns |
| $t_{PLZ}$ | Output Disable Time from LOW Level Output | | Output Control | Any $\overline{Q}$ | 3 | 15 | ns |

## Physical Dimensions

Dimensions are in millimeters unless otherwise noted.




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

**Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**
**Package Number M20B**

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