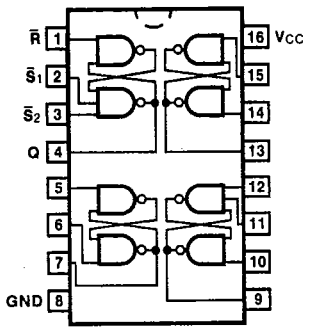
54/74279
54LS/74LS279
QUAD SET-RESET LATCH

CONNECTION DIAGRAM
PINOUT A



4

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74279PC, 74LS279PC		9B
Ceramic DIP (D)	A	74279DC, 74LS279DC	54279DM, 54LS279DM	6B
Flatpak (F)	A	74279FC, 74LS279FC	54279FM, 54LS279FM	4L

TRUTH TABLE

INPUTS $\bar{S}_1$	INPUTS $\bar{S}_2$	INPUTS $\bar{R}$	OUTPUT Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	20/10	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		30		7.0	mA	V_{CC} = Max, $\bar{R}$ = Gnd
t_{PLH} t_{PHL}	Propagation Delay $\bar{S}$ to Q		22 15		22 15	ns	Figs. 3-1, 3-10
t_{PHL}	Propagation Delay $\bar{R}$ to Q		27		27	ns	Figs. 3-1, 3-10

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.