

# DATA SHEET

**74F373**

Octal transparent latch (3-State)

**74F374**

Octal D flip-flop (3-State)

Product data  
Supersedes data of 1994 Dec 05

2002 Nov 20

# Latch/flip-flop

# 74F373/74F374

*74F373 Octal transparent latch (3-State)*  
*74F374 Octal D-type flip-flop (3-State)*

## FEATURES

- 8-bit transparent latch — 74F373
- 8-bit positive edge triggered register — 74F374
- 3-State outputs glitch free during power-up and power-down
- Common 3-State output register
- Independent register and 3-State buffer operation
- SSOP Type II Package

## DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ( $\overline{OE}$ ) control gates.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is HIGH. The latch remains transparent to the data input while E is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-LOW output enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the latch operation. When  $\overline{OE}$  is LOW, latched or transparent data appears at the output.

When  $\overline{OE}$  is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F374 is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ( $\overline{OE}$ ) control gates.

The register is fully edge triggered. The state of the D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-LOW output enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the register operation. When  $\overline{OE}$  is LOW, the data in the register appears at the outputs. When  $\overline{OE}$  is HIGH, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5 ns	35 mA

TYPE	TYPICAL $f_{max}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F374	165 MHz	55 mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5 V \pm 10\%$ , $T_{amb} = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$	
20-pin plastic DIP	N74F373N, N74F374N	SOT146-1
20-pin plastic SOL	N74F373D, N74F374D	SOT163-1
20-pin plastic SSOP type II	N74F373DB, N74F374DB	SOT339-1

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

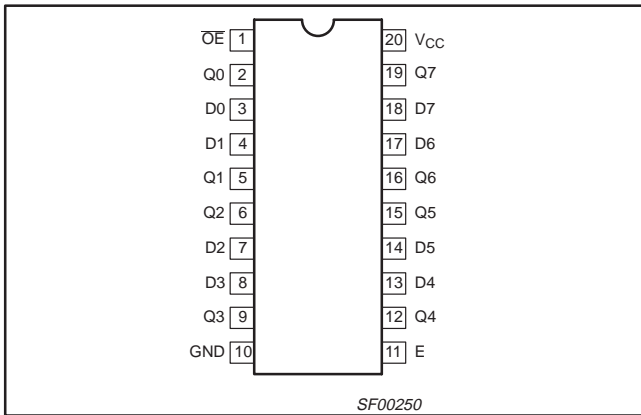
PINS	DESCRIPTION	74F (U.L.) HIGH / LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0 / 1.0	20 $\mu\text{A}$ / 0.6 mA
E (74F373)	Enable input (active-HIGH)	1.0 / 1.0	20 $\mu\text{A}$ / 0.6 mA
$\overline{OE}$	Output enable inputs (active-LOW)	1.0 / 1.0	20 $\mu\text{A}$ / 0.6 mA
CP (74F374)	Clock pulse input (active rising edge)	1.0 / 1.0	20 $\mu\text{A}$ / 0.6 mA
Q0 - Q7	3-State outputs	150 / 40	3.0 mA / 24 mA

**NOTE:** One (1.0) FAST unit load is defined as: 20  $\mu\text{A}$  in the HIGH state and 0.6 mA in the LOW state.

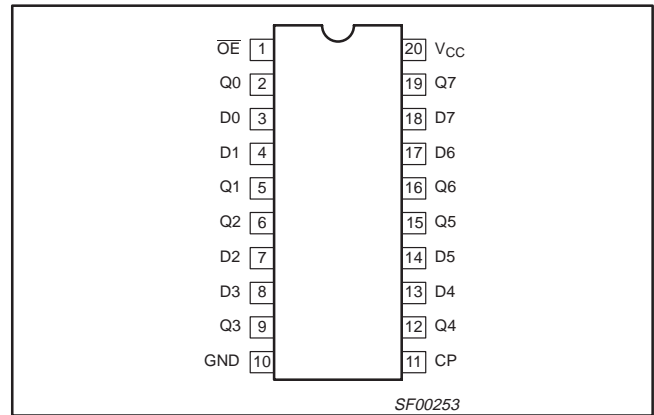
# Latch/flip-flop

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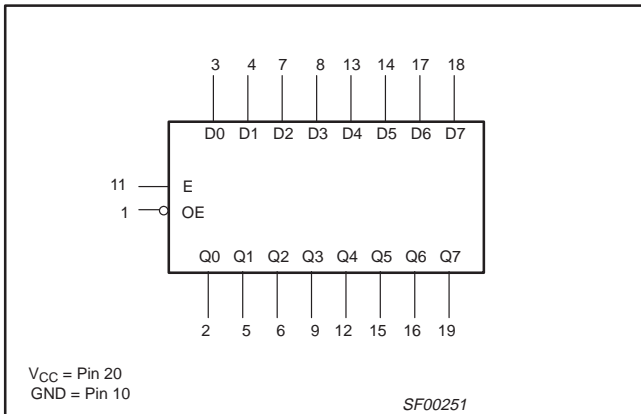
## PIN CONFIGURATION – 74F373



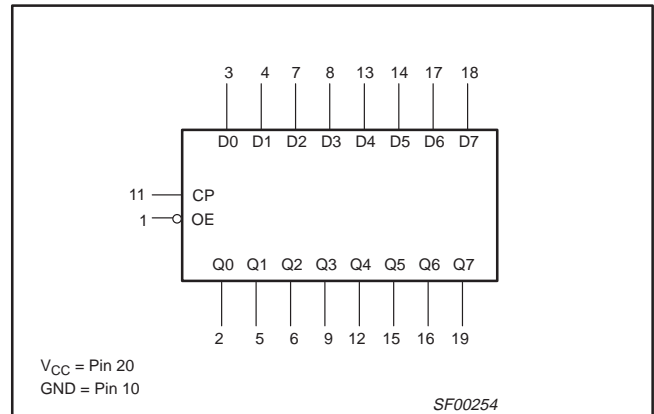
## PIN CONFIGURATION – 74F374



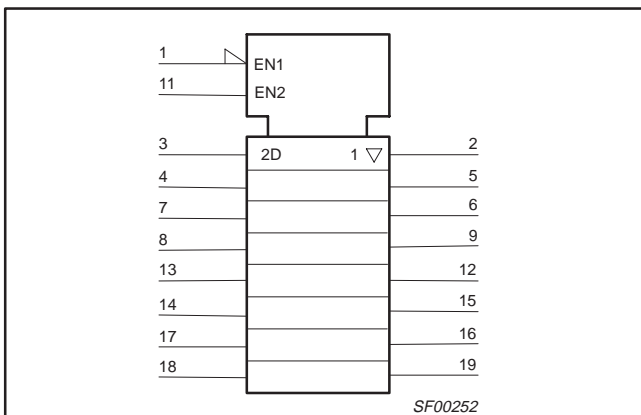
## LOGIC SYMBOL – 74F373



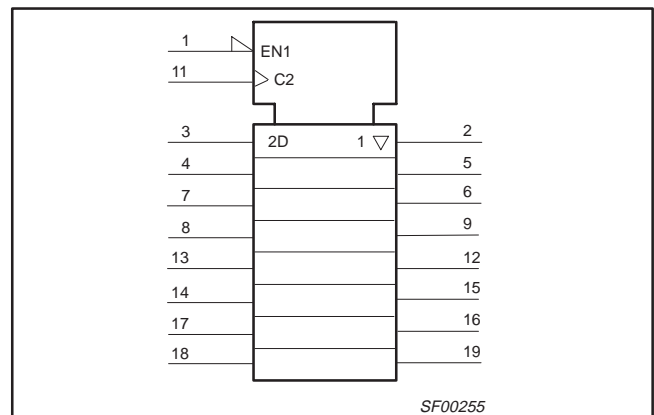
## IEC/IEE SYMBOL – 74F374



## IEC/IEEE SYMBOL – 74F373



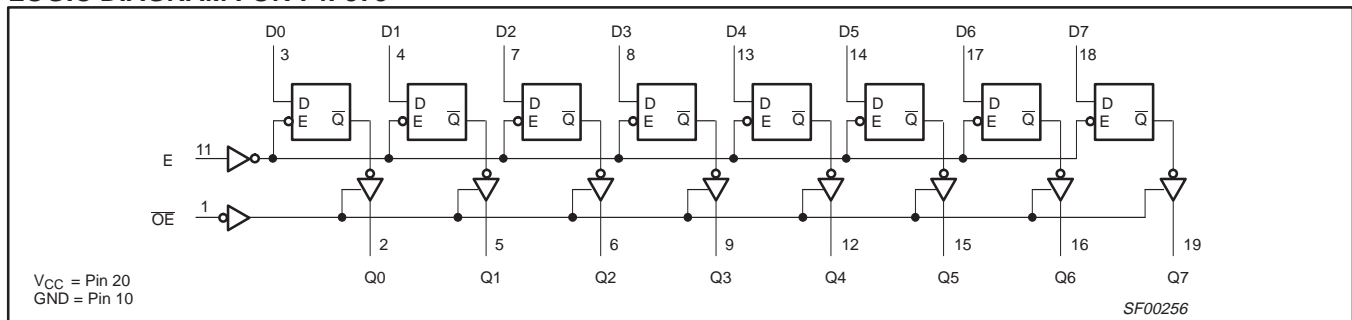
## IEC/IEEE SYMBOL – 74F374



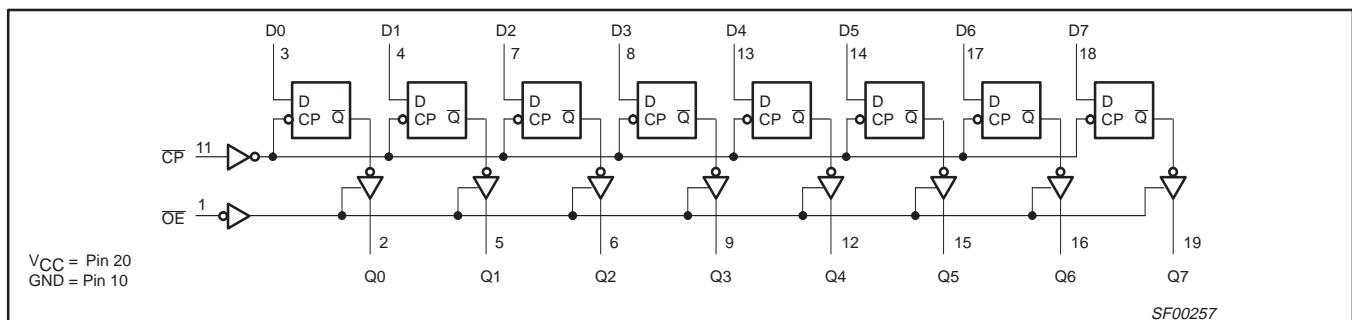
# Latch/flip-flop

# 74F373/74F374

## LOGIC DIAGRAM FOR 74F373



## LOGIC DIAGRAM FOR 74F374



## FUNCTION TABLE FOR 74F373

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
OE	E	D <sub>n</sub>		Q0 - Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D <sub>n</sub>	D <sub>n</sub>	Z	

### NOTES:

- H = High-voltage level
- h = HIGH state must be present one set-up time before the HIGH-to-LOW enable transition
- L = Low-voltage level
- l = LOW state must be present one set-up time before the HIGH-to-LOW enable transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = HIGH-to-LOW enable transition

## Latch/flip-flop

## 74F373/74F374

## FUNCTION TABLE FOR 74F374

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↑	X	NC	NC	Hold
H	↑	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

## NOTES:

- H = High-voltage level  
 h = HIGH state must be present one set-up time before the LOW-to-HIGH clock transition  
 L = Low-voltage level  
 l = LOW state must be present one set-up time before the LOW-to-HIGH clock transition  
 NC = No change  
 X = Don't care  
 Z = High impedance "off" state  
 ↑ = LOW-to-HIGH clock transition  
 ↑ = Not LOW-to-HIGH clock transition

## ABSOLUTE MAXIMUM RATINGS

Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in HIGH output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in LOW output state	48	mA
T <sub>amb</sub>	Operating free air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	HIGH-level input voltage	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	-	-	0.8	V
I <sub>Ik</sub>	Input clamp current	-	-	-18	mA
I <sub>OH</sub>	HIGH-level output current	-	-	-3	mA
I <sub>OL</sub>	LOW-level output current	-	-	24	mA
T <sub>amb</sub>	Operating free air temperature range	0	-	+70	°C

## Latch/flip-flop

## 74F373/74F374

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
			MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.4		V
			±5%V <sub>CC</sub>	2.7	3.4	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.35 0.50	V
			±5%V <sub>CC</sub>		0.35 0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0 V			100	μA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V			-0.6	mA
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V			50	μA
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5 V			-50	μA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-60	-150	mA
I <sub>CC</sub>	Supply current (total)	74F373			35 60	mA
		74F374			57 86	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**AC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω			T <sub>amb</sub> = 0 °C to +70 °C V <sub>CC</sub> = +5.0 V ± 10% C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to Qn	Waveform 3	3.0	5.3	7.0	3.0	8.0	ns
			2.0	3.7	5.0	2.0	6.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay E to Qn	Waveform 2	5.0	9.0	11.5	5.0	12.0	ns
			3.0	4.0	7.0	3.0	8.0	
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to HIGH or LOW level	Waveform 6 Waveform 7	2.0	5.0	11.0	2.0	11.5	ns
			2.0	5.6	7.5	2.0	8.5	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from HIGH or LOW level	Waveform 6 Waveform 7	2.0	4.5	6.5	2.0	7.0	ns
			2.0	3.8	5.0	2.0	6.0	
f <sub>max</sub>	Maximum clock frequency	Waveform 1	150	165		140		ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn	Waveform 1	3.5	5.0	7.5	3.0	8.5	ns
				3.5	5.0	7.5	3.0	
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to HIGH or LOW level	Waveform 6 Waveform 7	2.0	9.0	11.0	2.0	12.0	ns
			2.0	5.3	7.5	2.0	8.5	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from HIGH or LOW level	Waveform 6 Waveform 7	2.0	5.3	6.0	2.0	7.0	ns
			2.0	4.3	5.5	2.0	6.5	

# Latch/flip-flop

# 74F373/74F374

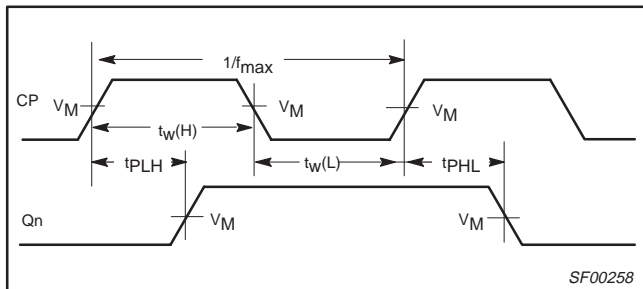
## AC SET-UP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω			T <sub>amb</sub> = 0 °C to +70 °C V <sub>CC</sub> = +5.0 V ± 10% C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>su</sub> (H) t <sub>su</sub> (L)	Set-up time, HIGH or LOW level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, HIGH or LOW level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		
t <sub>w</sub> (H)	E Pulse width, HIGH		Waveform 1	3.5			4.0		
t <sub>su</sub> (H) t <sub>su</sub> (L)	Set-up time, HIGH or LOW level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, HIGH or LOW level Dn to CP		Waveform 5	0 0			0 0		
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse width, HIGH or LOW		Waveform 5	3.5 4.0			3.5 4.0		

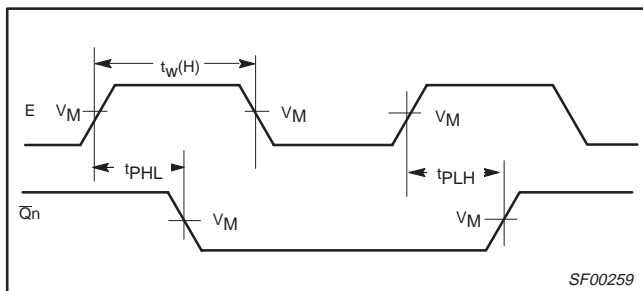
## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5 V.

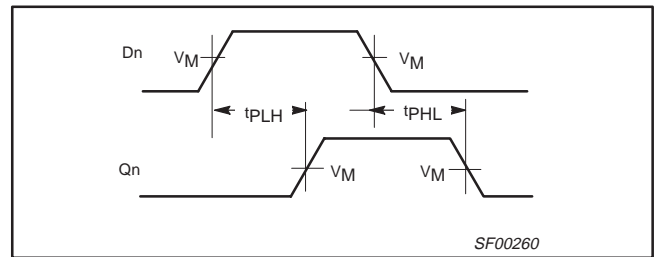
The shaded areas indicate when the input is permitted to change for predictable output performance.



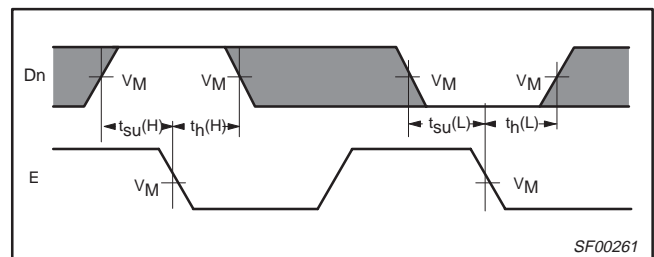
**Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency**



**Waveform 2. Propagation delay for enable to output and enable pulse width**



**Waveform 3. Propagation delay for data to output**



**Waveform 4. Data set-up time and hold times**

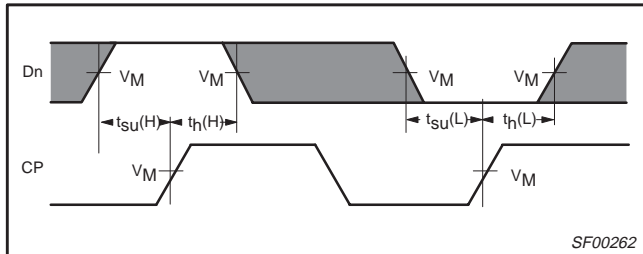
# Latch/flip-flop

# 74F373/74F374

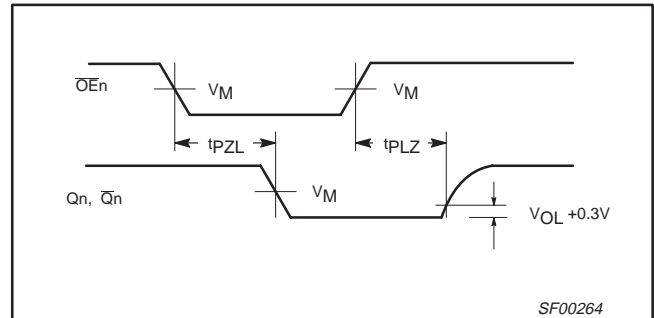
## AC WAVEFORMS (continued)

For all waveforms,  $V_M = 1.5\text{ V}$ .

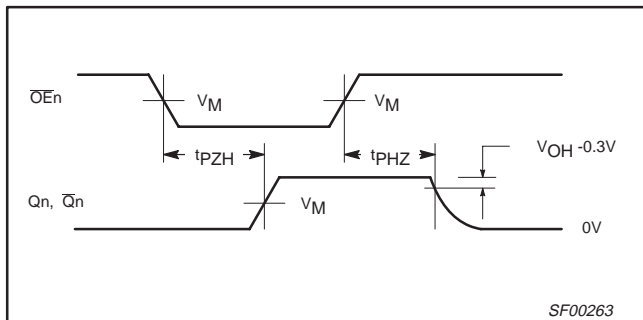
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 5. Data set-up time and hold times



Waveform 7. 3-State output enable time to LOW level and output disable time from LOW level



Waveform 6. 3-State output enable time to HIGH level and output disable time from HIGH level

## TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION	
TEST	SWITCH
$t_{pLZ}, t_{pZL}$	closed
All other	open

Test circuit for 3-state outputs

Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

SF00265

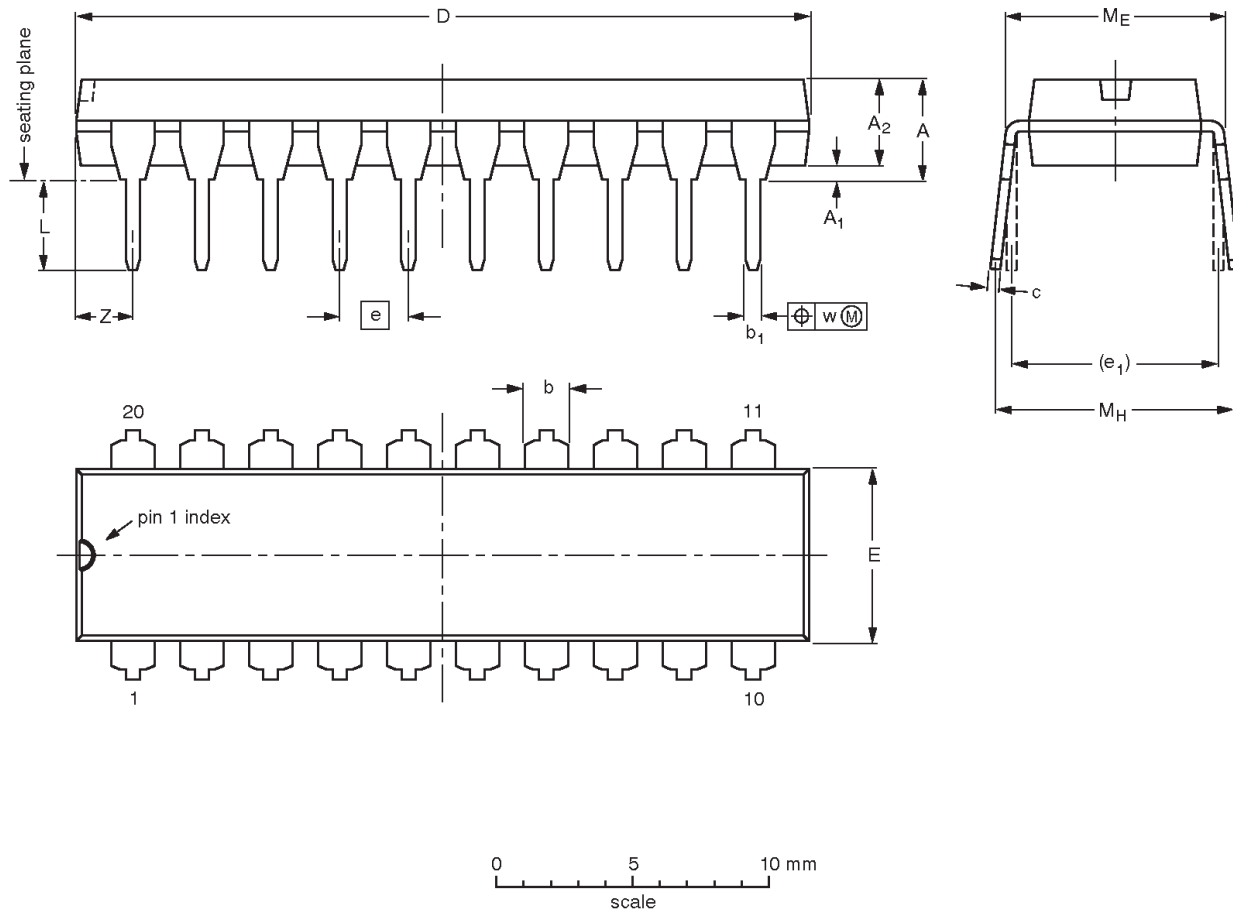


# Latch/flip-flop

# 74F373/74F374

**DIP20: plastic dual in-line package; 20 leads (300 mil)**

**SOT146-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

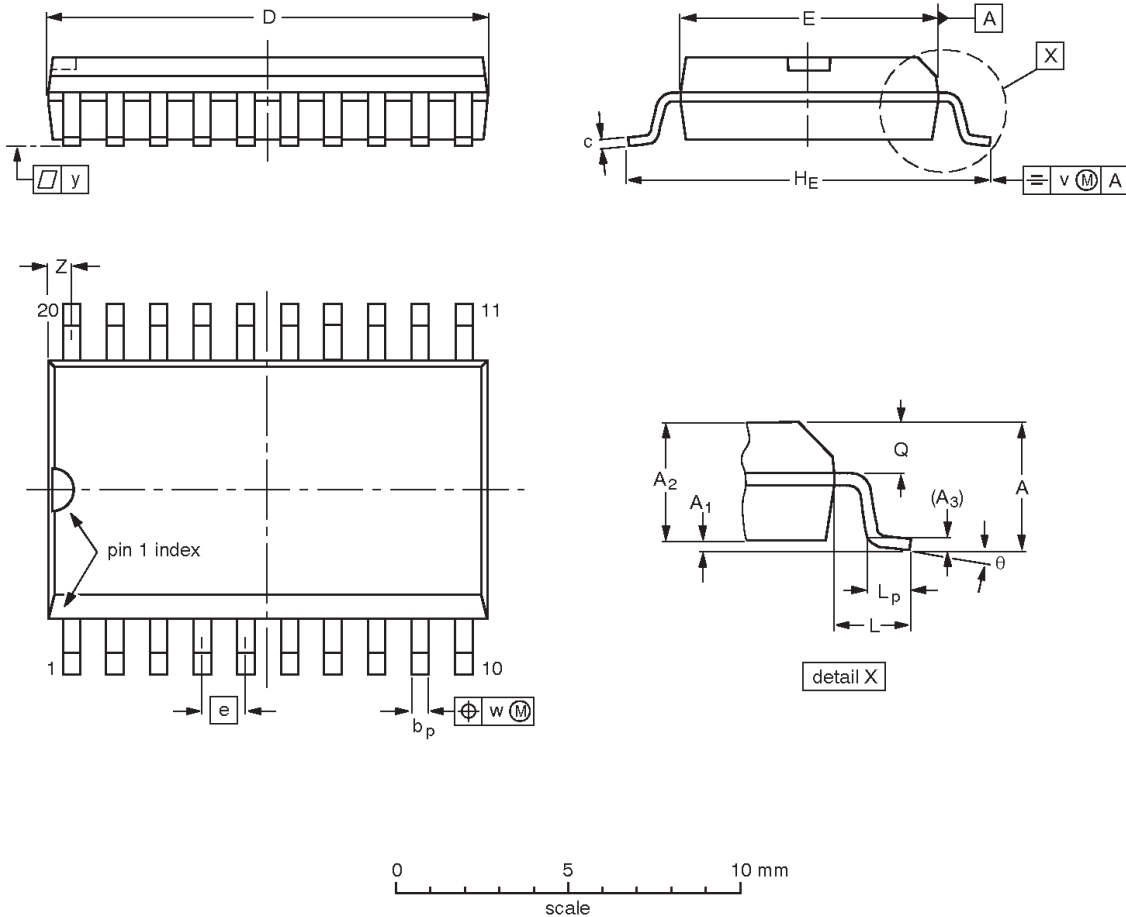
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			-95-05-24 99-12-27

# Latch/flip-flop

# 74F373/74F374

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

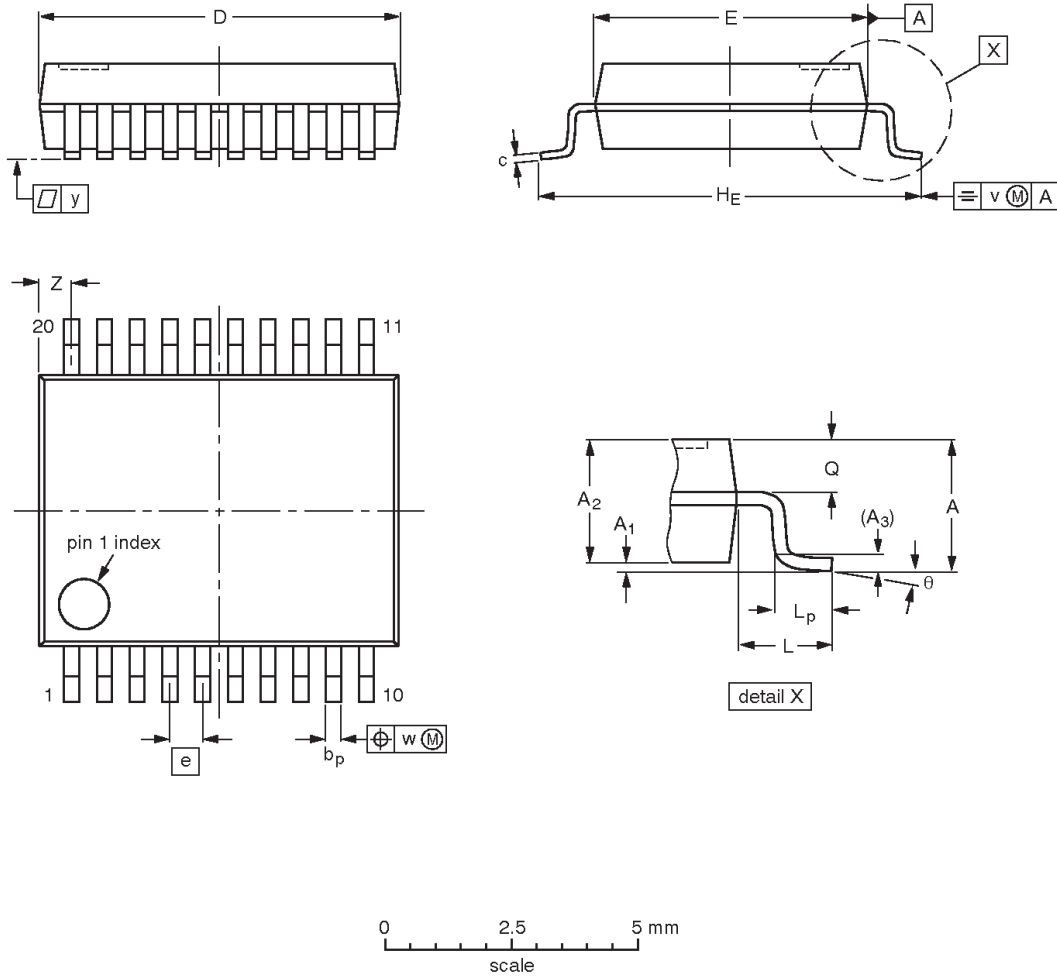
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				97-05-22 99-12-27

# Latch/flip-flop

# 74F373/74F374

**SSOP20:** plastic shrink small outline package; 20 leads; body width 5.3 mm

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150				95-02-04 99-12-27

## Latch/flip-flop

74F373/74F374

## REVISION HISTORY

Rev	Date	Description
_3	20021120	<b>Product data; third version (9397 750 10758). Supersedes 74F373_374_2 dated 1994 Dec 05 (9397 750 05119).</b> Engineering Change Notice 853-0369 29206 (date: 20021115). <b>Modifications:</b> <ul style="list-style-type: none"><li>• Corrected ordering information table (from 'N74374DB' to '74F374DB').</li><li>• Add SSOP20 (SOT339-1) package outline drawing.</li></ul>
_2	19941205	<b>Product data; second version (9397 750 05119).</b> Engineering Change Notice 853-0369 14383 (date: 19941205).

## Latch/flip-flop

74F373/74F374

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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