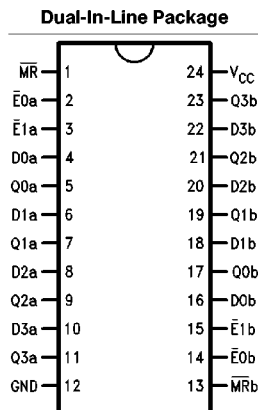


## 9308/DM9308 Dual 4-Bit Latch

### General Description

The 9308 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input and an active LOW Enable inputs. The 74116 is a pin for pin equivalent of the 9308.

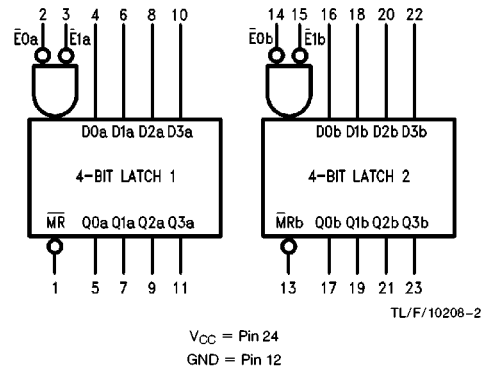
### Connection Diagram



TL/F/10208-1

Order Number 9308DMQB, 9308FMQB or DM9308N  
See NS Package Number J24A, N24A or W24C

### Logic Symbol



Pin Names	Description
$D_{0a}-D_{3a}$ } $D_{0b}-D_{3b}$ }	Parallel Latch Inputs
$\overline{E}0a, \overline{E}1a, \overline{E}0b, \overline{E}1b$	AND Enable Inputs (Active LOW)
$\overline{MR}a, \overline{MR}b$	Master Reset Inputs (Active LOW)
$Q_{0a}-Q_{3a}$ } $Q_{0b}-Q_{3b}$ }	Parallel Latch Outputs

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	–55°C to +125°C
COM	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			–0.8			–0.8	mA
I <sub>OL</sub>	Low Level Output Current			16			16	mA
T <sub>A</sub>	Free Air Operating Temperature	–55		125	0		70	°C
t <sub>s</sub> (H)	Setup Time HIGH, D <sub>n</sub> to $\overline{E}_n$	6			10			ns
t <sub>h</sub> (H)	Hold Time HIGH, D <sub>n</sub> to $\overline{E}_n$	4			–2.0			ns
t <sub>s</sub> (L)	Setup Time LOW, D <sub>n</sub> to $\overline{E}_n$	10			12			ns
t <sub>h</sub> (L)	Hold Time LOW, D <sub>n</sub> to $\overline{E}_n$	4			8			ns
t <sub>w</sub> (L)	$\overline{E}_n$ Pulse Width LOW	18			18			ns
t <sub>w</sub> (L)	$\overline{MR}$ Pulse Width LOW	18			18			ns
t <sub>rec</sub>	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	10			8			ns

## Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –18 mA			–1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4			V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			–1.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	MIL	–20	–70	mA
			COM	–20	–57	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)			100	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I<sub>CC</sub> is measured with all outputs open and all inputs grounded.

## Functional Description

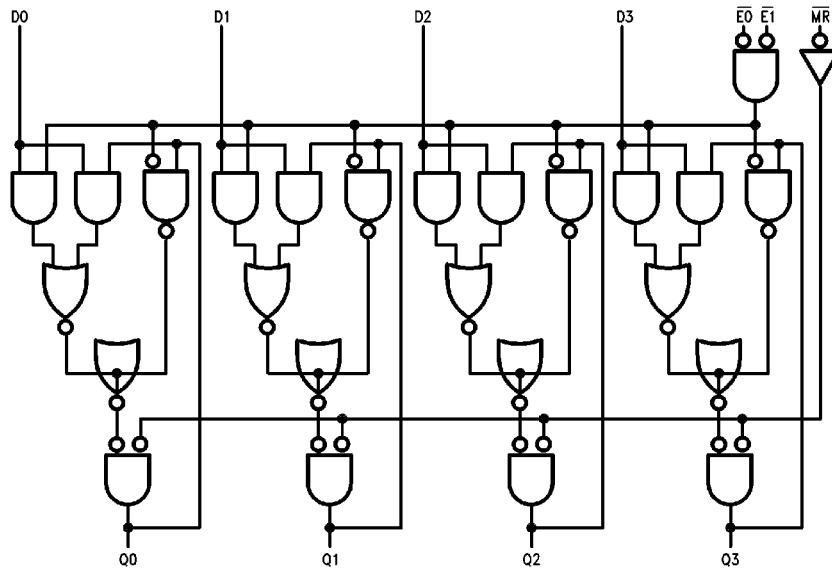
Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

## Truth Table

$\overline{MR}$	$\overline{E}0$	$\overline{E}1$	D	$Q_n$	Operation
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	$Q_{n-1}$	Hold
H	H	L	X	$Q_{n-1}$	Hold
H	H	H	X	$Q_{n-1}$	Hold
L	X	X	X	L	Reset

$Q_{n-1}$  = Previous Output State  
 $Q_n$  = Present Output State  
 H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

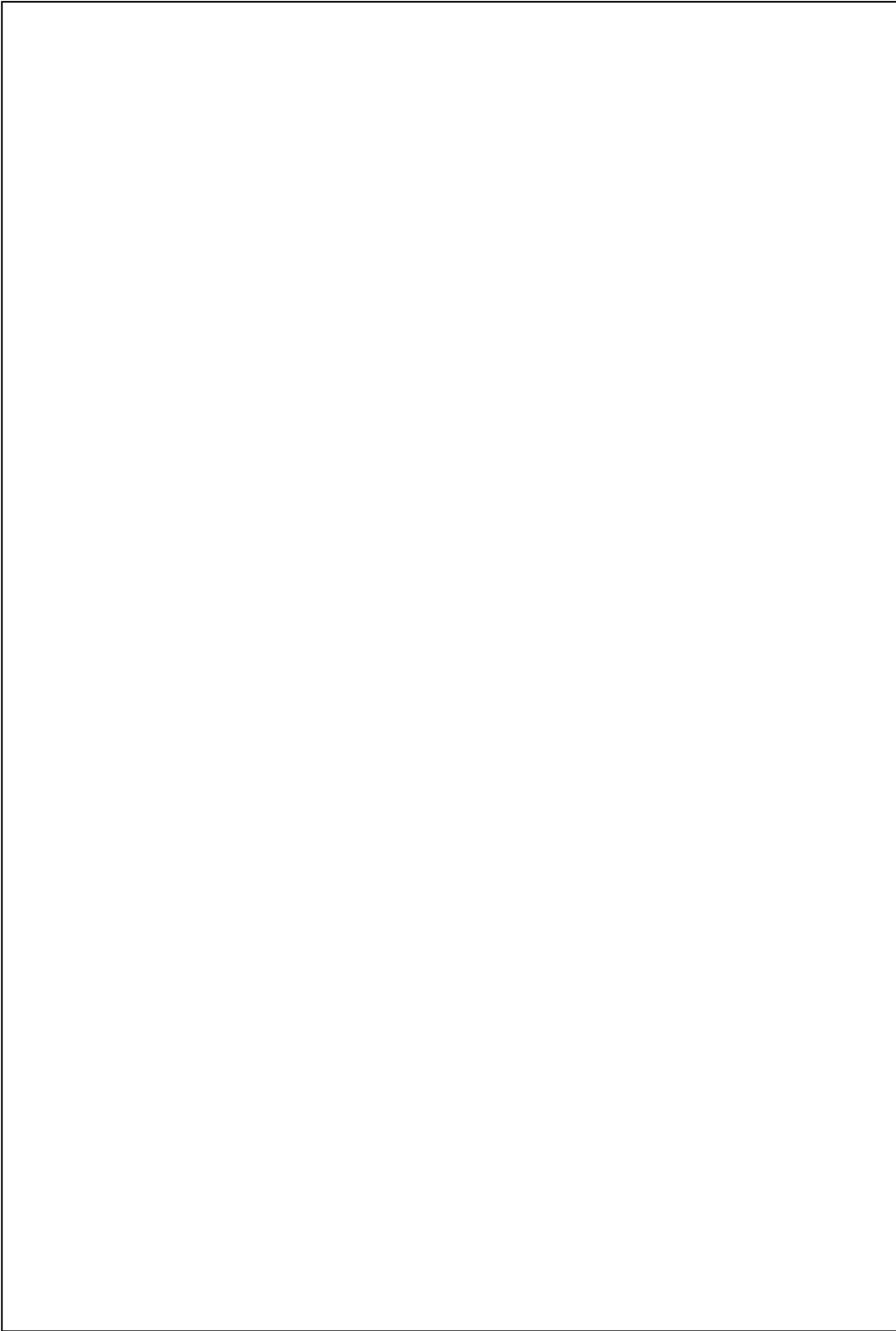
## Logic Diagram



TL/F/10208-3

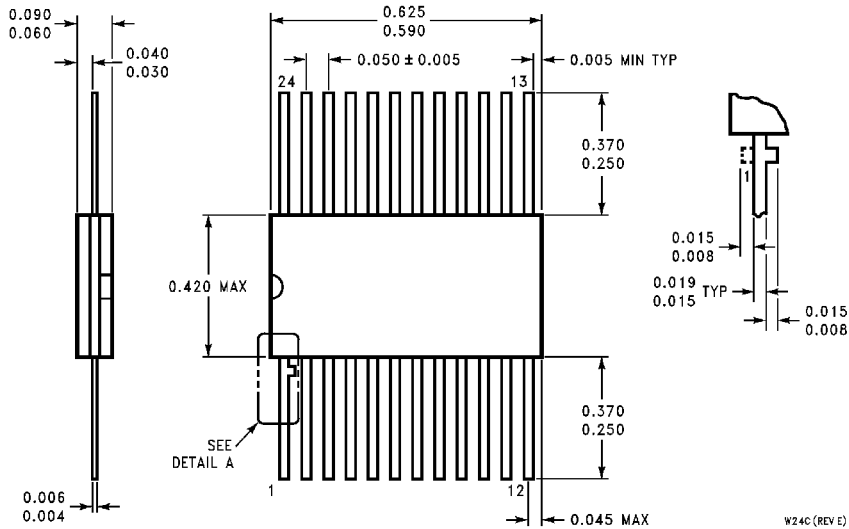
## Switching Characteristics $V_{CC} = +5.0V, T_A = +25^\circ C$ (See Section 5 for test waveforms and output load.)

Symbol	Parameter	9308		Units
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		
		Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{E}n$ to $Q_n$		30 22	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $Q_n$		15 18	ns
$t_{PHL}$	Propagation Delay $\overline{MR}$ to $Q_n$		22	ns





**Physical Dimensions** inches (millimeters) (Continued)



**24-Lead Ceramic Flat Package (W)**  
**Order Number 9308FMQB**  
**NS Package Number W24C**

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