# 10Gbps Active Back-match, Differential Laser Diode Driver

Preliminary Technical Data

# ADN2525

## FEATURES

**Up to 10.7Gbps operation**
**Very low power: Icc=157mA**
**Typical 24 ps rise/fall times**
**PECL/CML compatible data inputs**
**Bias current range: 10mA to 100mA**
**Differential modulation current range: 10mA to 80mA**
**Automatic Laser Shutdown (ALS)**
**3.3V operation**
**Compact 3x3mm LFCSP package**
**Voltage–input control for bias and modulation currents**
**XFP compliant bias current monitor**

## APPLICATIONS

**SONET OC-192 optical transceivers**
**SDH STM-64 optical transceivers**
**10Gb Ethernet optical transceivers**
**XFP/X2/XENPAK/MSA 300 optical modules**

## GENERAL DESCRIPTION

The ADN2525 laser diode driver is designed for direct modulation of packaged laser diodes having a differential impedance ranging from 5Ω to 50Ω. The active back-termination technique provides excellent matching with the output transmission lines while reducing the power dissipation in the output stage. The small package provide the optimum solution for compact modules where laser diodes are packaged in low pin-count optical sub-assemblies.

The differential data inputs are PECL/CML compatible and terminated with an internal 100Ω differential resistor to minimize signal reflections to the data signal source.

The modulation and bias currents are programmable via MSET and BSET control pins. By driving these pins with control voltages, the user has the flexibility to implement various average power and extinction ratio control schemes, including closed loop control, and look-up tables.

The automatic laser shutdown feature allows the user to turn the bias and modulation currents on/off by driving the ALS pin with the proper logic levels.

The product is available in a space saving 3mm ×3mm LFCSP package specified from –40°C to 85°C.

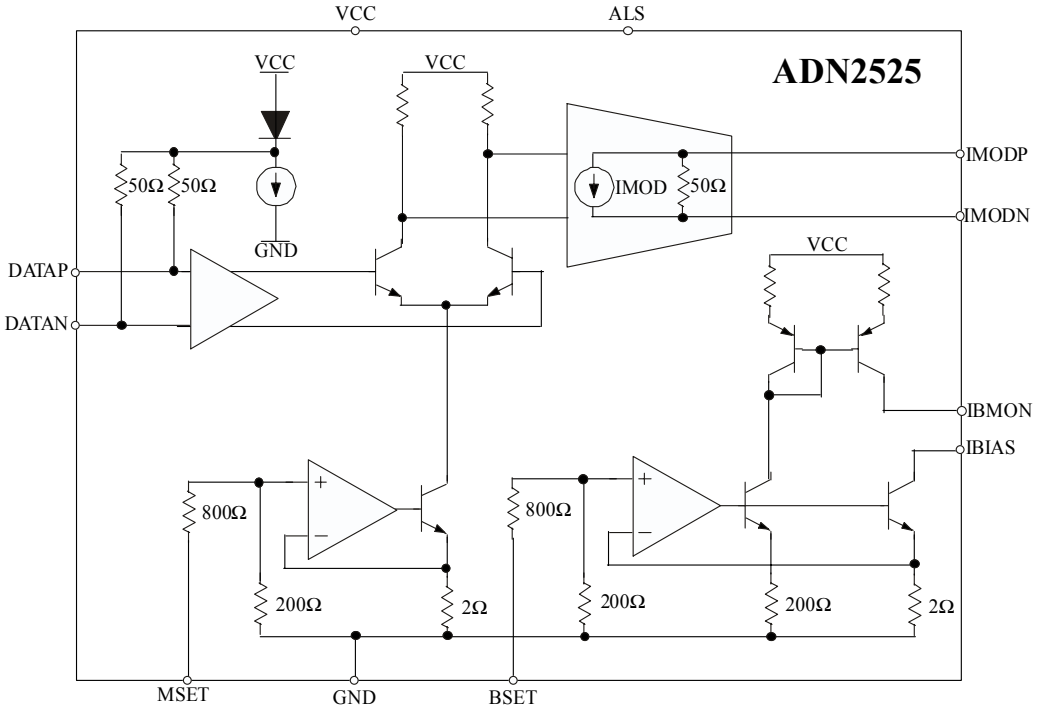


**Figure 1. Functional block diagram**

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# ADN2525-SPECIFICATIONS

(VCC= $VCC_{MIN}$ to $VCC_{MAX}$, $T_A$ = -40$^0$C to 85$^0$C, 50Ω differential load impedance, unless otherwise noted. Typical values are specified at 25$^0$C, IMOD=40mA)

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| **BIAS CURRENT(IBIAS)** | | | | | |
| Bias current range | 10 | | 100 | mA | |
| Bias current while ALS asserted | | | 100 | μA | ALS='HIGH' |
| Compliance voltage – see note 1 | 0.6 | | VCC-0.8 | V | IBIAS=100mA |
| | 0.6 | | VCC-1.2 | V | IBIAS=10mA |
| **MODULATION CURRENT (IMODP, IMODN)** | | | | | |
| Modulation current range | 10 | | 80 | mA diff. | $R_{LOAD}$= 5Ω to 50Ω differential |
| Modulation current while ALS asserted | | | 0.5 | mA diff | ALS='HIGH' |
| Rise time (20% to 80%) – see notes 2, 6 | | 24 | 34 | ps | |
| Fall time (20% to 80%) – see notes 2, 6 | | 24 | 34 | ps | |
| Pulse width distortion – see note 6 | TBD | TBD | TBD | ps | |
| Overshoot – see notes 2, 6 | TBD | | TBD | % | |
| Undershoot – see notes 2, 6 | TBD | | TBD | % | |
| Random jitter – see notes 2 ,6 | | 0.4 | TBD | ps RMS | |
| Deterministic jitter – see notes 3, 6 | | 7.2 | TBD | $ps_{p-p}$ | |
| Differential $\|S_{22}\|$ | | –10 | | dB | F<10GHz, $Z_0$=50Ω differential |
| Compliance voltage – see note 1 | VCC-1.1 | | VCC+1.1 | V | |
| **DATA INPUTS (DATAP, DATAN)** | | | | | |
| Input data rate | | | 10.7 | Gbps | NRZ |
| Differential input swing | 0.4 | | 1.6 | $V_{p-p}$ diff. | Differential AC coupled |
| Differential $\|S_{11}\|$ | | -10 | | dB | F<10GHz, $Z_0$=100Ω differential |
| Input termination resistance | 85 | 100 | 115 | Ω | Differential |
| **BIAS CONTROL INPUT (BSET)** | | | | | |
| BSET voltage to IBIAS gain | 80 | 100 | 120 | mA/V | |
| BSET input resistance | 800 | 1000 | 1200 | Ω | |
| **MODULATION CONTROL INPUT (MSET)** | | | | | |
| MSET voltage to IMOD gain | 70 | 88 | 110 | mA/V | |
| MSET input resistance | 800 | 1000 | 1200 | Ω | |
| **BIAS MONITOR (IBMON)** | | | | | |
| IBMON to IBIAS ratio | | 10 | | μA/mA | |
| Accuracy of IBIAS to IBMON ratio | -3.5 | | +3.5 | % | 10mA ≤IBIAS< 40mA, $R_{IBMON}$=1KΩ |
| | -2.5 | | +2.5 | % | 40mA ≤IBIAS< 70mA, $R_{IBMON}$=1KΩ |
| | -2 | | +2 | % | 70mA ≤IBIAS< 100mA, $R_{IBMON}$=1KΩ |
| **AUTOMATIC LASER SHUTDOWN (ALS)** | | | | | |
| $V_{IH}$ | 2.4 | | | V | |
| $V_{IL}$ | | | 0.8 | V | |
| $I_{IL}$ | -20 | | 20 | μA | |
| $I_{IH}$ | 0 | | 200 | μA | |
| ALS assert time – see figure 2 | | | 10 | μs | Rising edge of ALS to fall of IBIAS and IMOD below 10% of nominal |
| ALS negate time – see figure 2 | | | 10 | μs | Falling edge of ALS to rise of IBIAS and IMOD above 90% of nominal |
| **POWER SUPPLY** | | | | | |
| $V_{CC}$ | 3.07 | 3.3 | 3.53 | V | |
| $I_{CC}$ – see note 4 | | 31 | 38 | mA | $V_{BSET}$=$V_{MSET}$=0V |
| Isupply – see note 5 | | 157 | 176 | mA | $V_{BSET}$=$V_{MSET}$=0V |

Notes:
1. Refers to the voltage between the pin for which the compliance voltage is specified and GND.
2. The pattern used is composed by a repetitive sequence of 8 ones followed by 8 zeros at 10.7Gbps rate.
3 The pattern used is K28.5 (00111110101100000101) at 10.7Gbps rate.
4.Only includes current in ADN2525 VCC pins.
5. Includes current in ADN2525 VCC pins and DC current in IMODP and IMODN pull-up inductors. See section on "Power Consumption" for total supply current calculation.
6. Measured using the high-speed characterization circuit shown in figure 3.

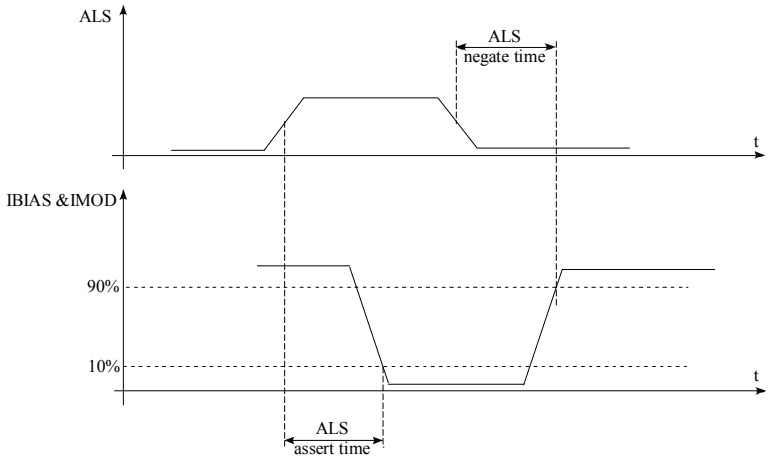


**Figure 2. ALS timing diagram**

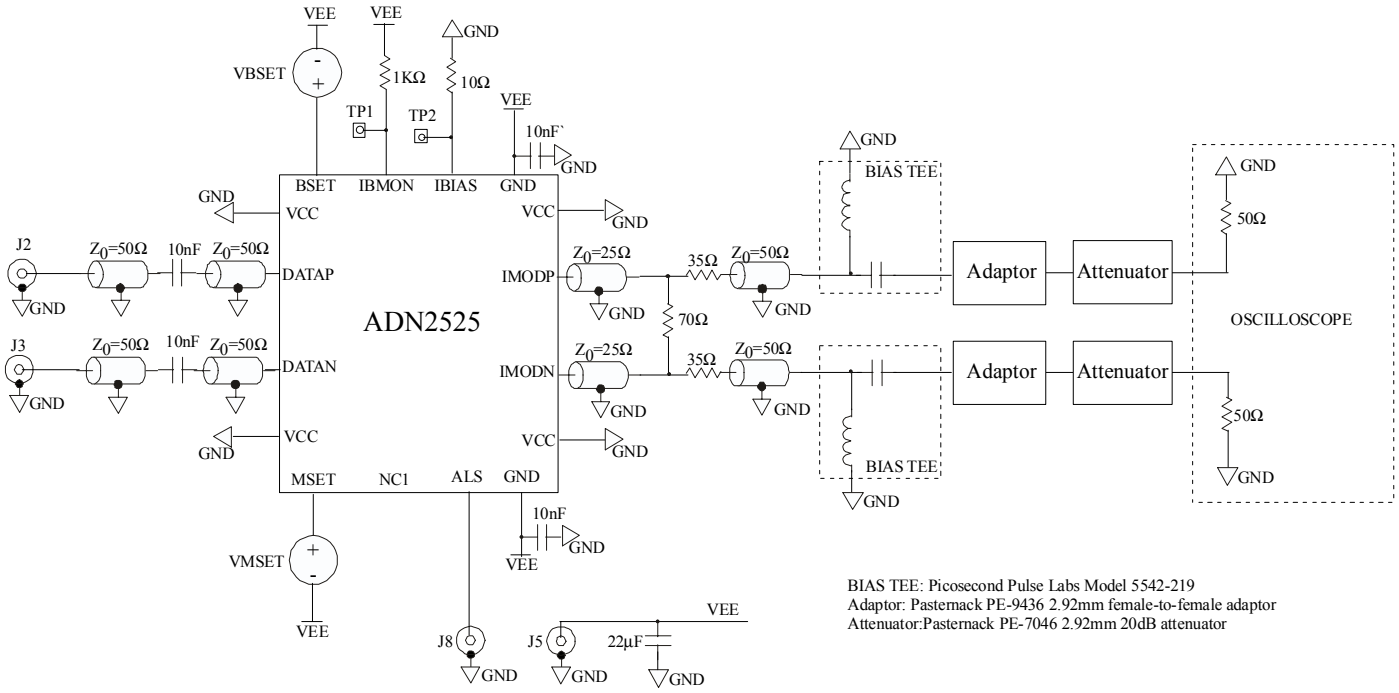


**Figure 3. High-speed characterization circuit**

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| PARAMETER | MIN | MAX | UNITS | CONDITIONS/COMMENTS |
|---|---|---|---|---|
| Supply voltage – VCC to GND | -0.3 | 4.2 | V | |
| IMODP, IMODN to GND | VCC-1.5 | 4.75 | V | |
| DATAP, DATAN to GND | VCC-1.8 | VCC-0.4 | V | |
| All other pins | -0.3 | VCC+0.3 | V | |
| Junction temperature | | 150 | $^0$C | |
| Storage temperature | -65 | 150 | $^0$C | |
| Soldering temperature | | 240 | $^0$C | Less than 10sec |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL SPECIFICATIONS

**Table 3.**

| PARAMETER | MIN | TYP | MAX | UNITS | CONDITIONS/COMMENTS |
|---|---|---|---|---|---|
| $\theta_{J\text{-}TOP}$ | 2.6 | 5.8 | 10.7 | $^0$C/W | Thermal resistance from junction to top of package |
| $\theta_{J\text{-}PAD}$ | 65 | 72.2 | 79.4 | $^0$C/W | Thermal resistance from junction to bottom of exposed pad |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS(Ta=25$^0$C,VCC=3.3V)

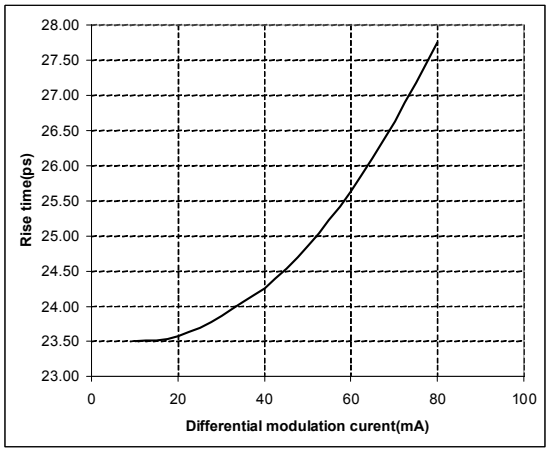


**Figure 4. Rise time vs. IMOD**

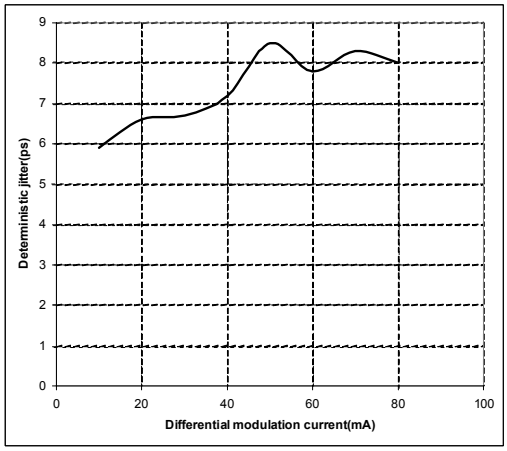


**Figure 7. Deterministic jitter vs. IMOD**

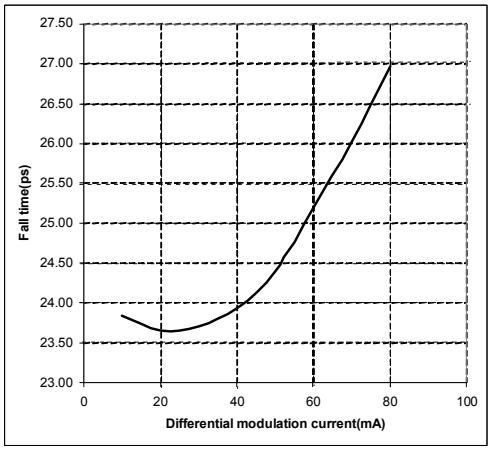


**Figure 5. Fall time vs. IMOD**

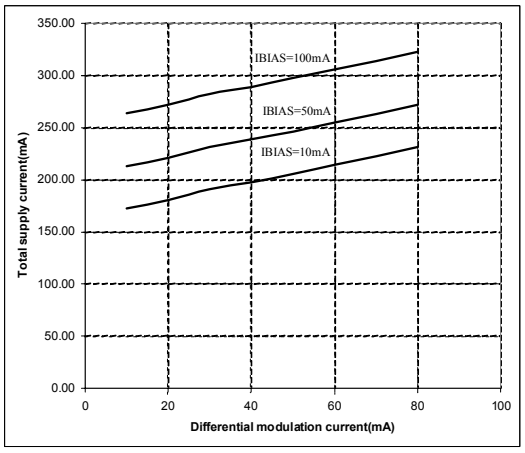


**Figure 8. Total Supply current vs. IMOD**

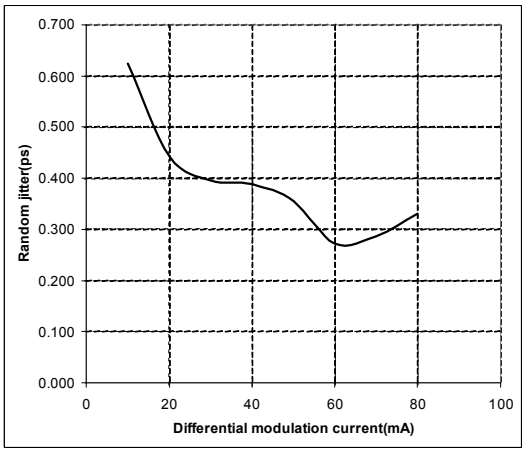


**Figure 6 Random jitter vs. IMOD**

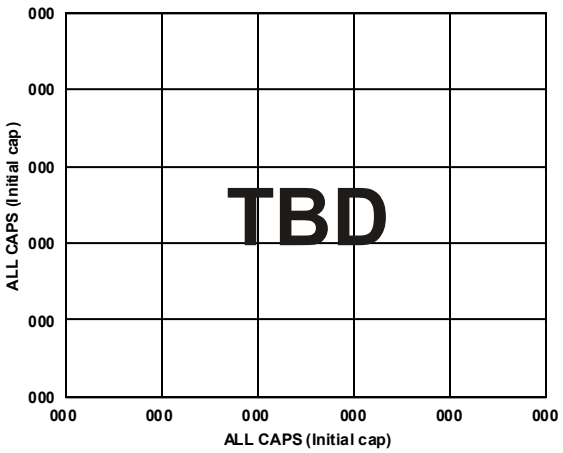


**Figure 9. Differential |S11|**

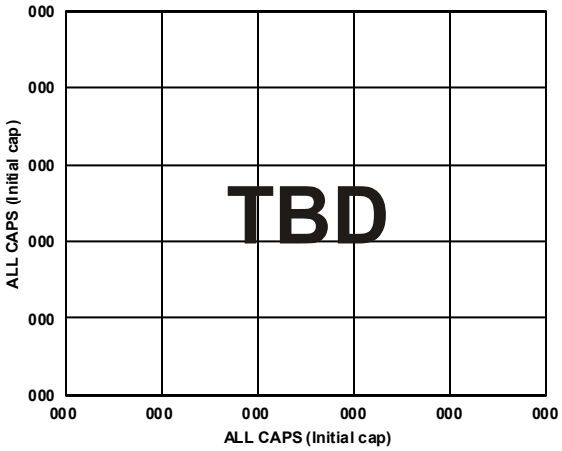


**Figure 10. Differential |S22|**

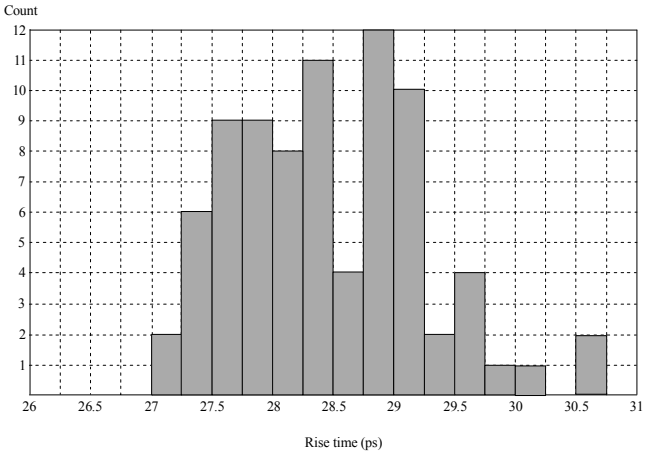


**Figure 11. Worst case rise time distribution**

**(VCC=3.07V, IBIAS=100mA, IMOD=80mA, $T_A$=85°C)**

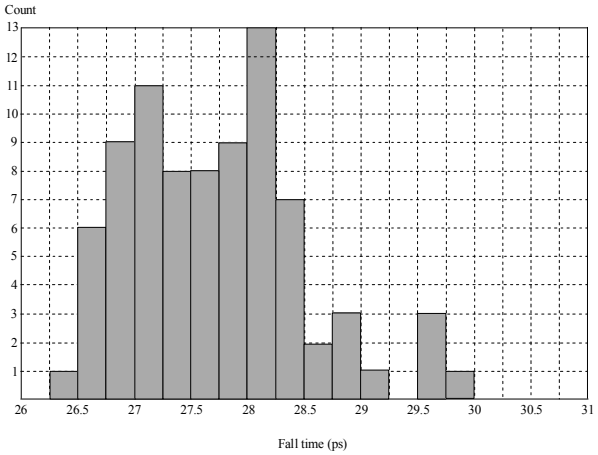


**Figure 12. Worst case fall time distribution**

**(VCC=3.07V, IBIAS=100mA, IMOD=80mA, $T_A$=85°C)**

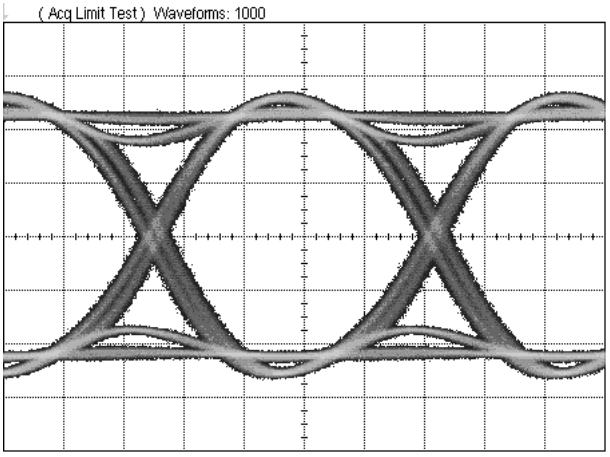


**Figure 13. Electrical eye diagram**

**(SONET OC192, PRBS31, IMOD=80mA)**

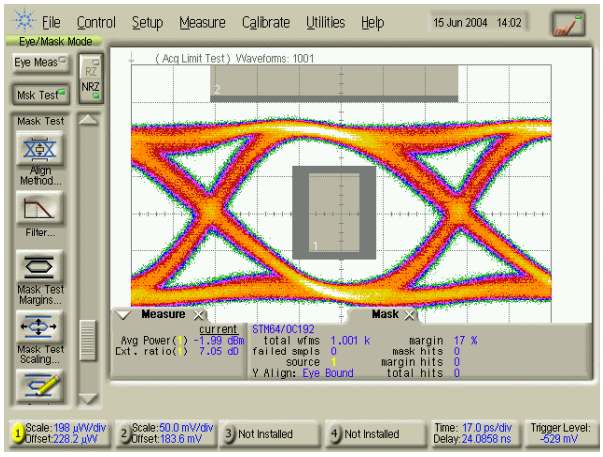


**Figure 14. Filtered SONET OC192 optical eye diagram (PRBS31 pattern, Pav=-2dBm, ER=7dB, 17% mask margin, NEC NX8341UJ TOSA)**

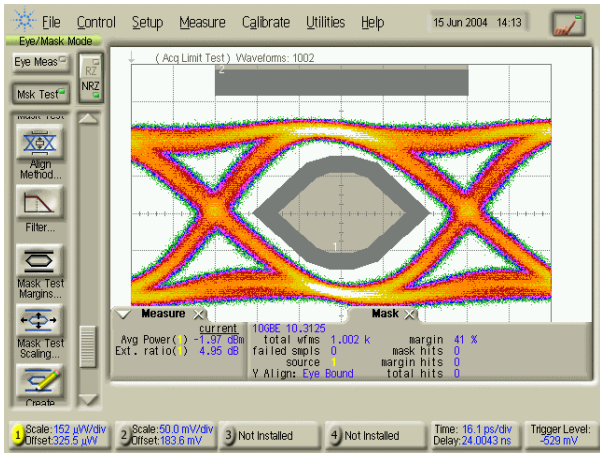


**Figure 15. Filtered 10G Ethernet optical eye (PRBS31 pattern, Pav=-2dBm, ER=5dB, 41% mask margin, diagram NEC NX8341UJ TOSA)**

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

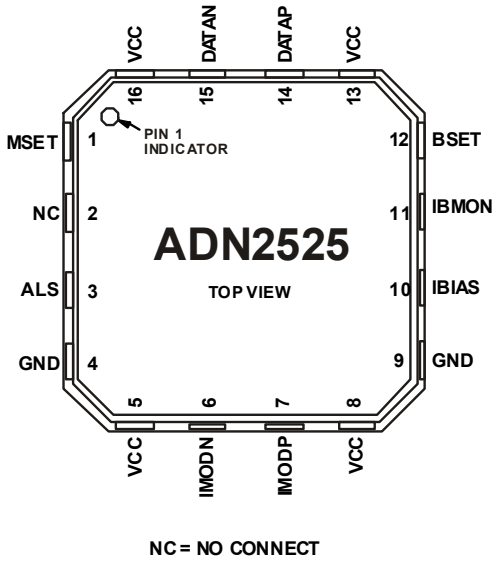


**Figure 16. Pin Configuration**

*Note: There is an exposed pad on the bottom of the package that must be connected to the VCC or GND plane with filled vias.*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | I/O | Description |
|---|---|---|---|
| 1 | MSET | Input | Modulation current control input |
| 2 | NC | N/A | No connect – Leave floating |
| 3 | ALS | Input | Automatic laser shutdown |
| 4 | GND | Power | Negative power supply |
| 5 | VCC | Power | Positive power supply |
| 6 | IMODN | Output | Modulation current negative output |
| 7 | IMODP | Output | Modulation current positive output |
| 8 | VCC | Power | Positive power supply |
| 9 | GND | Power | Negative power supply |
| 10 | IBIAS | Output | Bias current output |
| 11 | IBMON | Output | Bias current monitoring output |
| 12 | BSET | Input | Bias current control input |
| 13 | VCC | Power | Positive power supply |
| 14 | DATAP | Input | Data signal positive input |
| 15 | DATAN | Input | Data signal negative input |
| 16 | VCC | Power | Positive power supply |
| Exposed Pad | Pad | Power | Connect to GND or VCC |

# THEORY OF OPERATION

## GENERAL

As shown in figure 1, the ADN2525 consists of an input stage, and two voltage controlled current sources for bias and modulation. The bias current is available at the IBIAS pin, and also can be monitored at IBMON pin. The MSET voltage is converted to current. This current is applied to a differential pair that switches current into two internal resistors according to the data signal applied to the driver. The voltage generated across these resistors is applied to the output stage circuitry, which produces the differential modulation current that drives the laser. This output stage also implements the active back-match circuitry for proper transmission line matching and power consumption reduction. The ADN2525 can drive a load having differential impedance ranging from 5Ω to 50Ω.

## INPUT STAGE

The input stage of the ADN2525 converts the data signal applied to the DATAP and DATAN pins to a level that ensures proper operation of the high-speed switch. The equivalent circuit of the input stage is shown in figure 17.

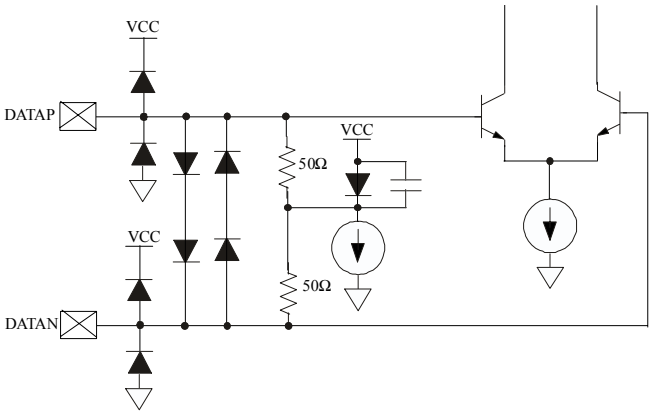


**Figure 17. Equivalent circuit of the input stage**

The DATAP and DATAN pins are terminated internally with a 100Ω differential termination resistor to minimize signal reflections at the input that could otherwise lead to degradation in the output eye diagram. The 100Ω resistor is built as a combination of two 50Ω resistors for each data pin connected to a common mode voltage source that is biasing the input stage transistors. Note that it is not recommended to drive the ADN2525 with single-ended data signal sources.

The ADN2525 input stage must be AC-coupled with the signal source to eliminate the need for matching between the common mode voltages of the data signal source and the input stage of the driver (see figure 18). The AC-coupling capacitors should be chosen so that their impedance is less than 50Ω over the required frequency range. Generally this is achieved using capacitor values from 10nF to 100nF.

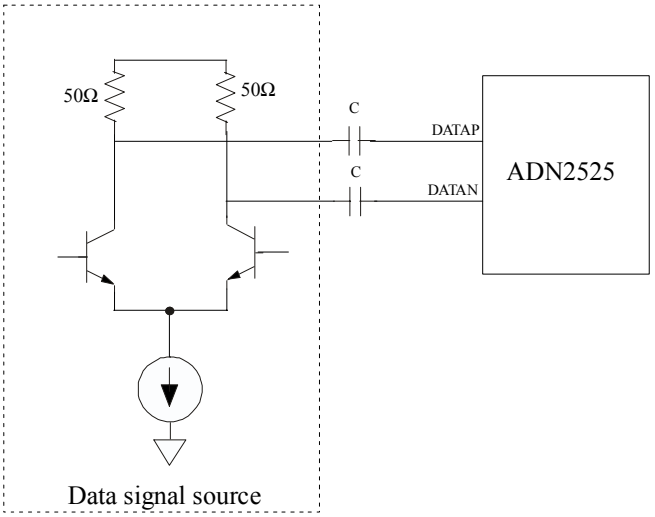


**Figure 18. AC-coupling the data source to the ADN2525 data inputs**

## BIAS CURRENT

The bias current is generated internally using a voltage to current converter, consisting of an internal operational amplifier and a transistor as shown in figure 19.

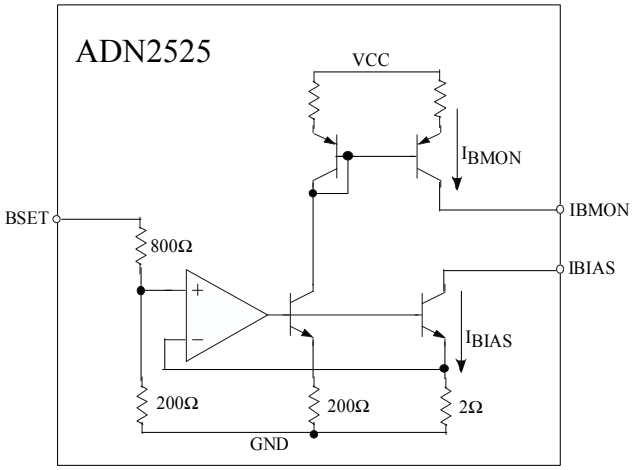


**Figure 19. Voltage to current converter used to generate IBIAS**

The voltage to current conversion factor is set at 100mA/V by the internal resistors. The bias current is monitored using a current mirror with a gain equal to 1/100, given by the ratio of the degeneration resistors (2Ω/200 Ω). The current mirror output is the IBMON pin that sources the IBIAS/100 current from VCC. By connecting a resistor between IBMON and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient, precision resistor must be used for the IBMON resistor ($R_{IBMON}$). Any error in the value of $R_{IBMON}$ due to tolerances or drift in its value over temperature,

contributes to the overall error budget for the IBIAS monitor voltage. If the IBMON voltage is being connected to an ADC for A/D conversion, $R_{IBMON}$ should be placed close to the ADC to minimize errors due to voltage drops on the ground plane.

The equivalent circuits of the BSET, IBIAS and IBMON pins are shown in figures 20, 21 and 22.

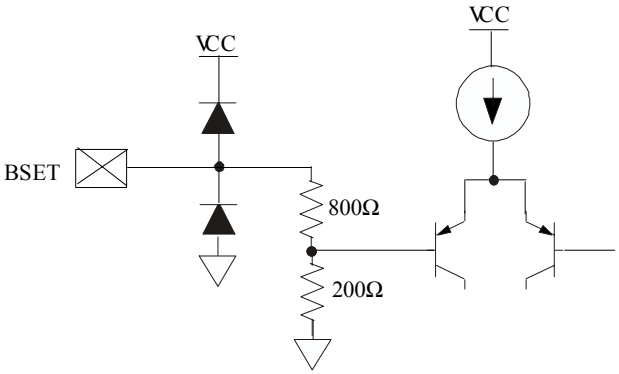


**Figure 20. Equivalent circuit of the BSET pin**

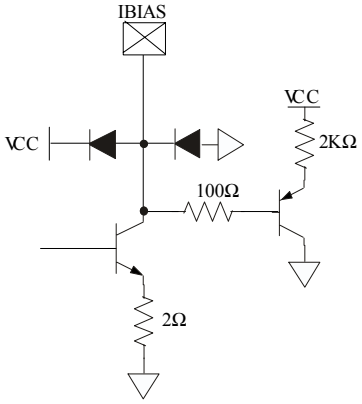


**Figure 21. Equivalent circuit of the IBIAS pin**

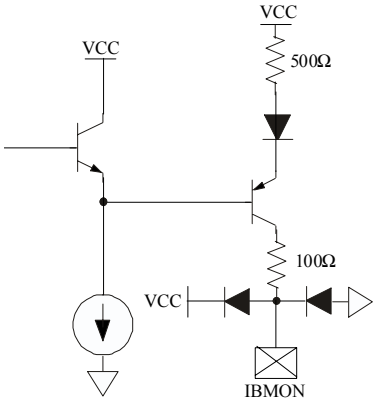


**Figure 22. Equivalent circuit of the IBMON pin**

The recommended configuration for BSET, IBIAS and IBMON is shown in figure 23.

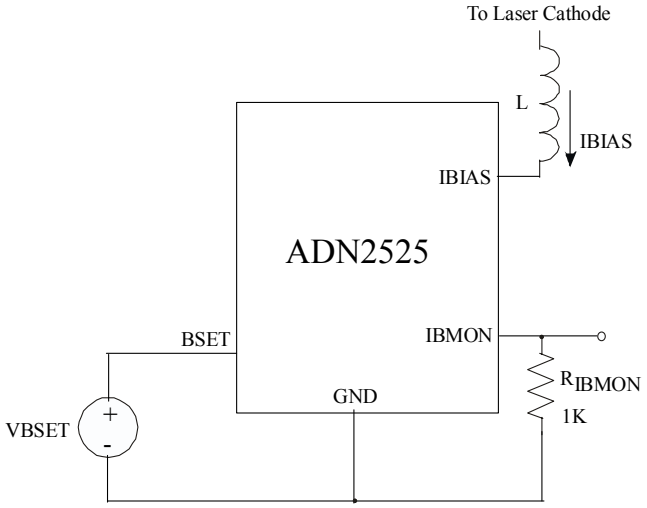


**Figure 23 Recommended configuration for BSET, IBIAS and IBMON pins**

The circuit used to drive the BSET voltage must be capable of driving the 1KΩ input resistance of the BSET pin. For proper operation of the bias current source, the voltage at IBIAS pin must be between the compliance voltage specifications for this pin (see page 2) over supply, temperature and bias current range. The maximum compliance voltage is specified on page 2 for only two bias current levels (10mA and 100mA) but it can be calculated for any bias current using the following formula:

$$V_{COMPLIANCE}(V)=VCC(V)-0.75-4.4\times IBIAS(A)$$

The function of the inductor L is to isolate the capacitance of the IBIAS output from the high frequency signal path.

## AUTOMATC LASER SHUTDOWN (ALS)

The ALS pin is a digital input that enables/disables both the bias and modulation currents depending on the logic state applied (see table 5).

**Table 5**

| ALS logic state | IBIAS and IMOD |
|---|---|
| HIGH | Disabled |
| LOW | Enabled |
| Floating | Enabled |

The ALS pin is compatible with 3.3V CMOS and TTL logic levels. Its equivalent circuit is shown in figure 24.

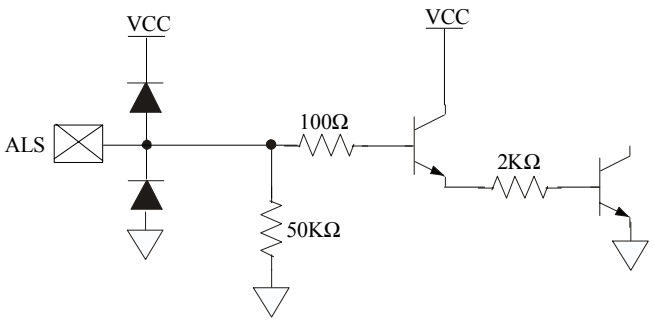


**Figure 24. Equivalent circuit of the ALS pin**

## MODULATON CURRENT

The modulation current can be controlled by applying a DC voltage to the MSET pin. This voltage is converted into a DC current using a voltage to current converter using an operational amplifier and a bipolar transistor as shown in figure 25.

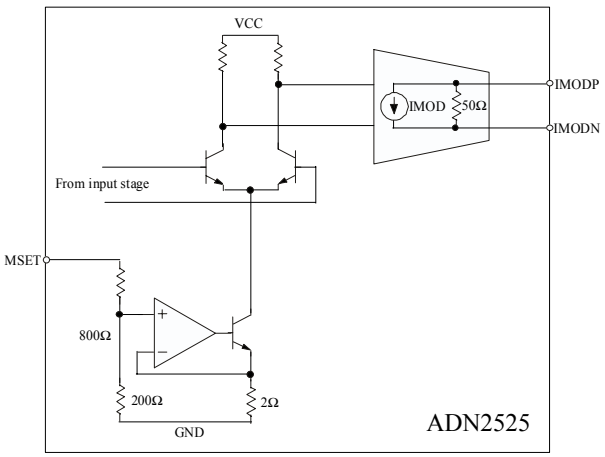


**Figure 25. Generation of modulation current on ADN2525**

This DC current is used as a tail current for the differential pair that generates a high-speed voltage across the resistive loads based on the data signal applied to the input stage (DATAP and DATAN pins). The high-speed differential voltage is applied to the output stage circuitry that generates the differential modulation current available at the IMODP and IMODN pins. The equivalent circuits for MSET, IMODP and IMODN are shown in figures 26 and 27.

The output stage also generates the active back termination, which provides proper transmission line termination. Active back termination uses feedback around an active circuit to synthesize a broadband termination resistance. This provides excellent transmission line termination, while dissipating less power than a traditional resistor passive back termination.

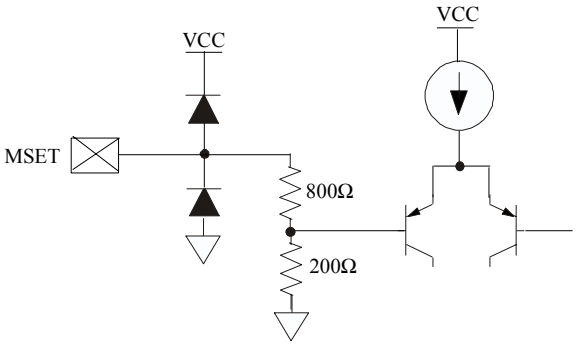


**Figure 26. Equivalent circuit of the MSET pin**

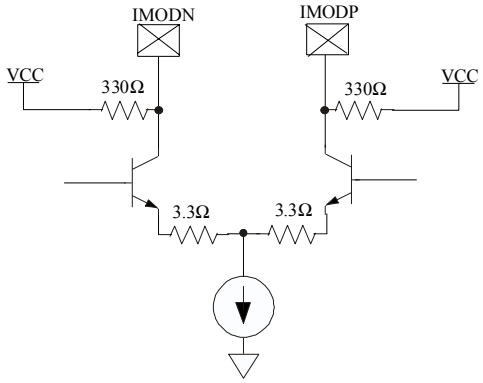


**Figure 27. Equivalent circuit of the IMODP and IMODN pins**

The recommended configuration of the MSET, IMODP and IMODN pins is shown in figure 28.

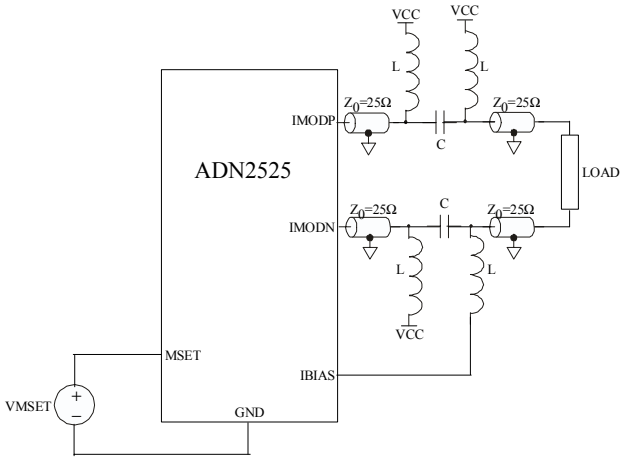


**Figure 28. Recommended configuration for MSET, IMODP and IMODN pins**

The ratio between the voltage applied to the MSET pin and the differential modulation current available at the IMODP and IMODN pins is a function of the load impedance value as shown in figure 29.

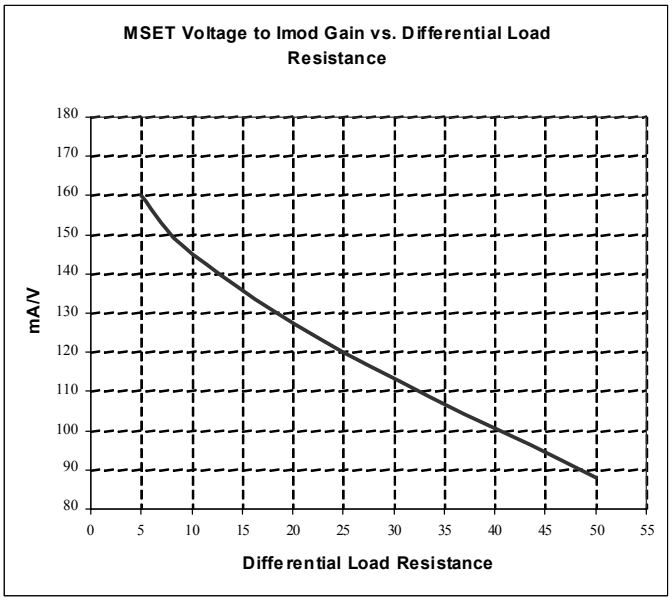


**Figure 29. MSET voltage to modulation current ratio vs. differential load impedance**

Knowing the resistance of the TOSA, the user can calculate the voltage range that should be applied to the MSET pin to generate the required modulation current range.

The circuit used to drive the MSET voltage must be capable of driving the 1KΩ resistance of the MSET pin. In order to be able to drive 80mA modulation currents through the differential load the output stage of the ADN2525 (IMODP, IMODN pins) must be AC-coupled to the load. The voltage at these pins will have a DC component equal to VCC and an AC component with single-ended peak-to-peak amplitude of IMOD×25Ω. This is the case even if the load impedance is less than 50Ω differential, since the transmission line characteristic impedance sets the peak-to-peak amplitude. For normal operation, the voltages at the IMODP and IMODN pins must be within the range shown in figure 30. The user must perform headroom calculations to ensure that the voltages at IMODP and IMODN pins are within the normal operation region for the required modulation currents.

Due to its excellent S22 performance the ADN2525 can drive differential loads that range from 5Ω to 50Ω. In practice many TOSAs have differential resistance less than 50Ω. In this case, with 50Ω differential transmission lines connecting the ADN2525 to the load, the load end of the transmission lines will be mis-terminated. This mis-termination leads to signal reflections back to the driver. The excellent back-termination in the ADN2525 absorbs these reflections, preventing their re-reflection back to the load. This enables excellent optical eye quality to be achieved, even when the load end of the transmission lines is significantly mis-terminated. The connection between the load and the ADN2525 must be made with 50Ω differential (25Ω single-ended) transmission lines so that the driver end of the transmission lines is properly terminated.

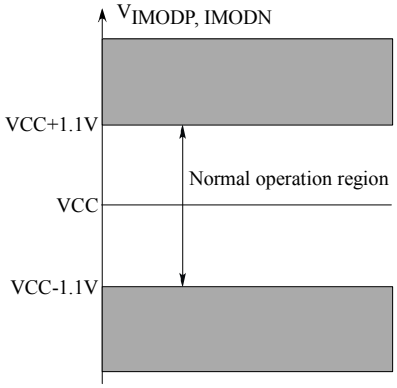


**Figure 30. Allowable range for the voltage at IMODP and IMODN**

## POWER CONSUMPTION

The power dissipated by the ADN2525 is given by

$$P = VCC \times \left( \frac{V_{MSET}}{13.5} + I_{supply} \right) + V_{IBIAS} \times IBIAS$$

Where,

VCC= power supply voltage

IBIAS= the bias current generated by the ADN2525

$V_{MSET}$ = the voltage applied to the MSET pin

$I_{supply}$ = the sum of the current that flows into the VCC, IMODP and IMODN pins of the ADN2525 when IBIIAS=IMOD=0 expressed in Amps (see table 1).

$V_{IBIAS}$=the average voltage on IBIAS pin

Considering $V_{BSET}$/IBIAS=10 as the conversion factor from $V_{BSET}$ to IBIAS, the dissipated power becomes:

$$P = VCC \times \left( \frac{V_{MSET}}{13.5} + I_{supply} \right) + \frac{V_{BSET}}{10} \times V_{IBIAS}$$

To ensure long-term reliable operation, the junction temperature of the ADN2525 must not exceed $125^0$C. For improved heat dissipation the module's case can be used as heat sink as shown in figure 31. A compact optical module is a complex thermal environment, and calculations of device junction temperature using the package $\theta_{J\text{-}A}$ (Junction-to-Ambient thermal resistance) do not yield accurate results.

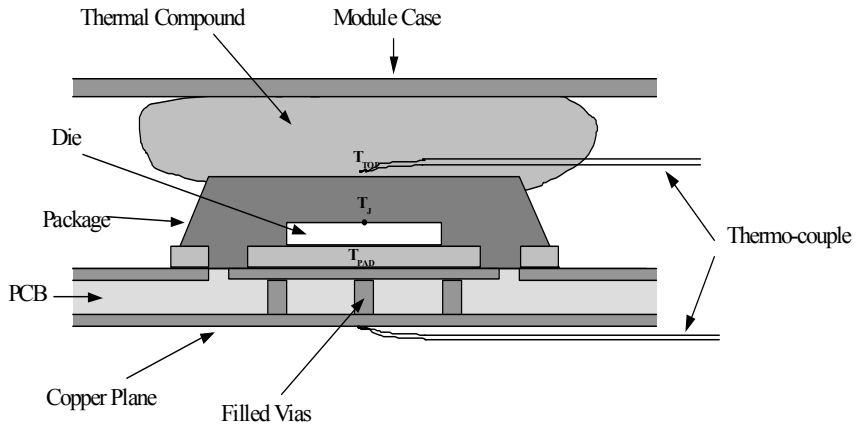


**Figure 31. Typical optical module structure**

The following procedure can be used to estimate the IC junction temperature.

$T_{TOP}$ = Temperature at top of package in $^0$C.

$T_{PAD}$ = Temperature at package exposed paddle in $^0$C.

$T_J$ = IC junction temperature in $^0$C.

P = Power disipation in W.

$\theta_{J\text{-}TOP}$ = Thermal resistance from IC junction to package top.

$\theta_{J\text{-}PAD}$ = Thermal resistance from IC junction to package exposed pad.

$T_{TOP}$ and $T_{PAD}$ can be determined by measuring the temperature at points inside the module, as shown in fig. 30. The thermo-couples should be positioned so as to obtain an accurate measurement of the package top and paddle temperatures. Using this model the junction temperature can be calculated using the formula:

$$T_J = \frac{P \times (\theta_{J-PAD} \times \theta_{J-TOP}) + T_{TOP} \times \theta_{J-PAD} + T_{PAD} \times \theta_{J-TOP}}{\theta_{J-PAD} + \theta_{J-TOP}}$$

Where $\theta_{J\text{-}TOP}$ and $\theta_{J\text{-}PAD}$ are given in table 3 and P is the power dissipated by the ADN2525.

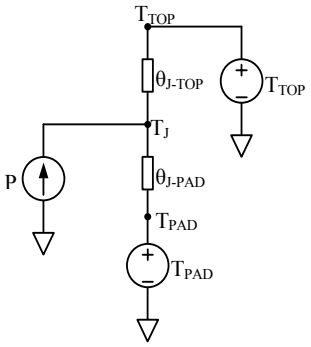


**Fig. 32. Electrical model for thermal calculations**

# APPLICATIONS INFORMATION

## TYPICAL APPLICATION CIRCUIT

Figure 33 shows the typical application circuit for the ADN2525. The DC voltages applied to the BSET and MSET pins control the bias and modulation currents. The bias current can be monitored as a voltage drop across the 1K resistor connected between the IBMON pin and GND. The ALS pin allows the user to turn on/off the bias and modulation currents depending on the logic level applied to the pin. The data signal source must be connected to the DATAP and DATAN pins of the ADN2525 using 50Ω impedance transmission lines. The modulation current outputs IMODP and IMODN must be connected to the load (TOSA) using 50Ω differential (25Ω single-ended) impedance transmission lines. The RF interface between the ADN2525 and the TOSA must be designed to ensure high quality optical eyes.

For more details on how to choose the components from the RF interfacing circuitry please contact the factory

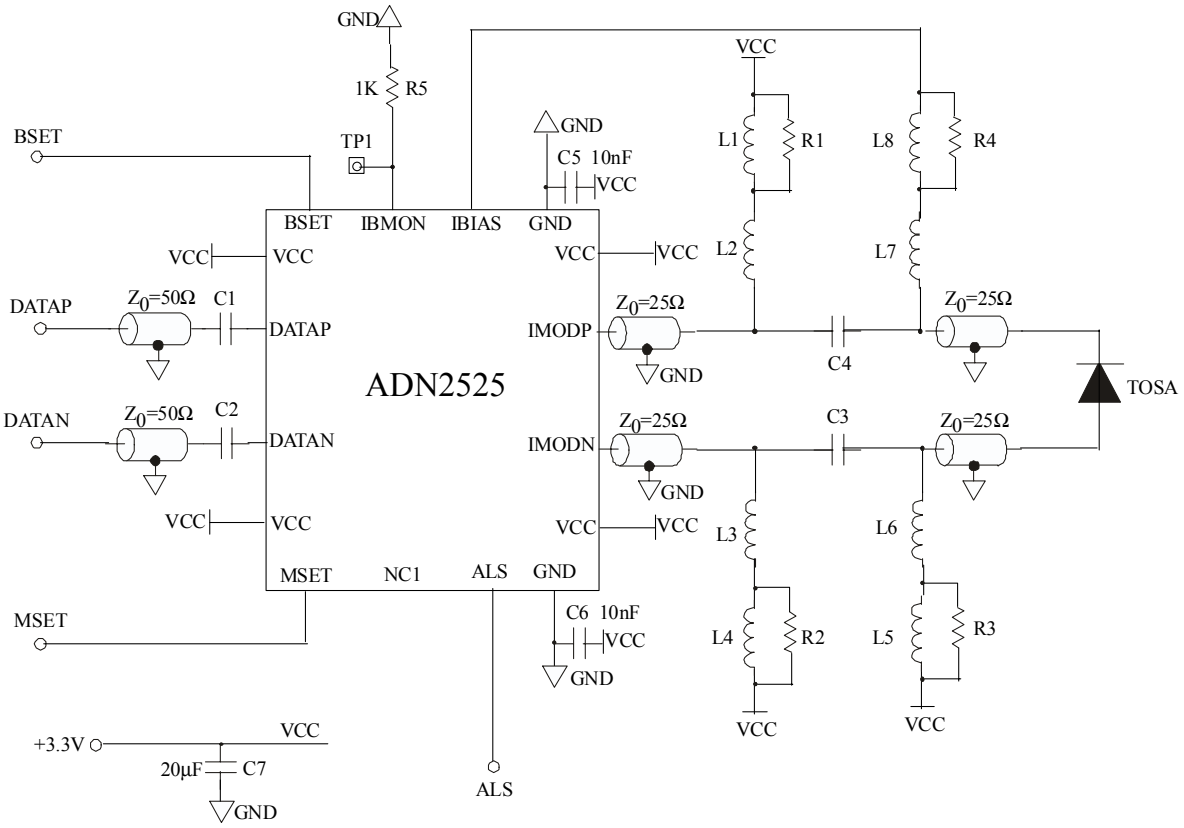


**Figure 33. Typical ADN2525 Application Circuit**

## PCB LAYOUT GUIDELINES

Due to the high frequencies at which the ADN2525 operates, care should be taken when designing the PCB layout in order to obtain optimum performance. It is recommended to use controlled impedance transmission lines for the high-speed signal paths The length of the transmission lines must be kept to a minimum to reduce losses and pattern dependant jitter. The PCB layout must be symmetrical to ensure the balance between the differential inputs/outputs of the ADN2525. All the VCC and GND pins must be connected to solid copper planes using low inductance connections. When the connections are made through vias, multiple vias can be connected in parallel to reduce the parasitic inductance. Each GND pin must be locally decoupled with high quality capacitors. If proper decoupling cannot be achieved using a single capacitor, the user can use multiple capacitors in parallel for each GND pin. A 20µF tantalum capacitor must be used as general decoupling capacitor for the entire module The exposed pad should be connected to the VCC or GND plane using filled vias so that solder does not leak through the vias during reflow. Using filled vias under the package greatly enhances the reliability of the connectivity of the exposed pad to the GND plane during reflow.

## DESIGN EXAMPLE

This section describes a design example that covers the followings:

- Headroom calculations for IBIAS, IMODP and IMODN pins
- Calculation of the typical voltage required at BSET and MSET pins in order to get the desired bias and modulation currents

This design example assumes that the impedance of the TOSA is equal to 25Ω, the forward voltage of the laser at low current is $V_F$=1V, IBIAS=40mA, IMOD=60mA, and VCC=3.3V

### *Headroom calculations*

The headroom calculations must be performed for IBIAS, IMODP and IMODN. The ADN2525 will work within the datasheet specifications if the voltages at the above mentioned pins are within the datasheet specifications (see page 2, Bias current and Modulation current sections).

Considering the typical application circuit shown in figure 33 the voltage at the IBIAS pin can be written as:

$$V_{IBIAS} = VCC - V_F - (IBIAS \times Z_{TOSA}) - V_{L3} - V_{L4}$$

Where,

VCC= supply voltage

$V_F$= the forward voltage across the laser at low current

$Z_{TOSA}$= the impedance of the TOSA

$V_{L3}$, $V_{L4}$= the DC voltage drop across L3 and L4

For proper operation the minimum voltage at the IBIAS pin should be greater than 0.6V.

Assuming that the voltage drop across the 25Ω transmission lines is negligible and $V_{L3}$ =$V_{L3}$=0V, $V_F$=1V, IBIAS=40mA

$$V_{IBIAS}=3.3\text{-}1\text{-}(0.04\times25)=1.3V > 0.6V$$

The maximum voltage at the IBIAS pin must satisfy the condition:

$$V_{IBIASmax} < VCC - 0.75 - 0.44 \times IBIAS(A) = 2.53V$$

$$V_{IBIAS}=1.3V < 2.53V$$

For headroom calculations at the modulation current pins (IMODP, IMODN) the voltage has a DC component equal to VCC due to the AC-coupled configuration and a swing equal to IMOD×25Ω. For normal operation of the ADN2525 the voltage at each modulation output pin should be within the normal operating region shown in figure 27. Assuming the voltage drop across L1 and L2=0V and IMOD=60mA, the minimum voltage at the modulation output pins is equal to:

$$VCC-(IMOD\times25\Omega)/2=VCC-0.75 > VCC-1.1V$$

The maximum voltage at the modulation output pins is equal to:

$$VCC+(IMOD\times25\Omega)/2=VCC+0.75 > VCC+1.1V$$

### *BSET and MSET pin voltage calculation*

In order to get the desired bias and modulation current the BSET and MSET pins of the ADN2525 must be driven with the appropriate DC voltage. The BSET voltage range required at the BSET pin to generate the required IBIAS range can be calculated using the IBIAS/$V_{BSET}$ ratio specified on page 2 of this datasheet. Assuming IBIAS=40mA, the typical IBIAS/$V_{BSET}$ ratio of 100mA/V, the BSET voltage is given by the formula:

$$V_{BSET} = \frac{IBIAS(mA)}{100mA/V} = \frac{40}{100} = 0.4V$$

The BSET voltage range can be calculated using the required IBIAS range, and the minimum and maximum IBIAS/$V_{IBIAS}$ values specified in table 1.

The voltage required at the MSET pin in order to get the desired modulation current can be calculated using the formula:

$$V_{MSET} = \frac{IMOD}{K}$$

Where K is the MSET voltage to IMOD ratio.

The value of K is dependant on the actual impedance of the TOSA and it can be read using the plot shown in figure 28. For an impedance of the TOSA of 25Ω, K=120mA/V. Using the formula shown above, the voltage required at the MSET pin in order to generate 60mA modulation current is 0.5V. The MSET voltage range can be calculated using the required IMOD range, and the minimum and maximum K values. These can be obtained from the following formulae:

$$K_{min} = \frac{70}{88} \times K$$

$$K_{max} = \frac{110}{88} \times K$$

# OUTLINE DIMENSIONS

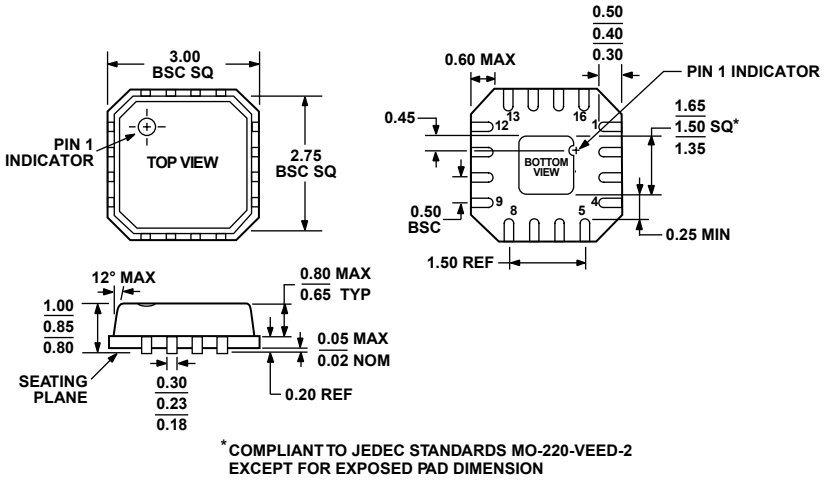


**Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP]**
**3 mm × 3 mm Body**
**(CP-16-3)**
**Dimensions shown in millimeters**

PR05077-0-9/04(PrE)

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Lead Finish |
|---|---|---|---|---|
| ADN2525ACPZ-WP | -40C to +85C | 16-LFCSP, 50pc Waffle Pack | CP-16 | Lead-Free |
| ADN2525ACPZ-500RL7 | -40C to +85C | 16-LFCSP, 500pc Reel | CP-16 | Lead-Free |
| ADN2525ACPZ-REEL7 | -40C to +85C | 16-LFCSP, 7” 1500pc Reel | CP-16 | Lead-Free |