

Laser Driver for Projectors

General Description

The MAX3600 laser driver for projectors supports video imaging with red, blue, and green lasers. Each output includes a 10-bit video digital-to-analog converter (DAC) with programmable gain and offset. For operation with synthetic green lasers, the driver includes a periodic off function and a fourth output with a random-noise generator.

The MAX3600B/R/G are monochrome drivers for blue, red, and green lasers. The MAX3600A guarantees higher full-scale output currents than the MAX3600, and is recommended for new designs.

Applications

RGB Pico Laser Projector
Up to WXGA and 1080p Resolution Projectors
Monochrome Blue, Green, or Red Pico Laser Projector

Typical Operating Circuits and Pin Configuration appear at end of data sheet.

Features

- ◆ Integrates Four Current-Output Laser Drivers
- ◆ Compatible with Red, Blue, and Green Lasers
- ◆ 10-Bit Video DACs, $f_{CLK} = 1\text{MHz to }160\text{MHz}$
- ◆ 8-Bit Gain and Offset DACs
- ◆ 2ns Output Switching Time
- ◆ Serial Port Control
- ◆ Laser Enable
- ◆ Random-Noise Generator and Periodic Off
- ◆ 5mm x 5mm, 40-Pin TQFN Package (0.4mm Pitch)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3600CTL+†	0°C to +70°C	40 TQFN-EP*
MAX3600ACTL+	0°C to +70°C	40 TQFN-EP*
MAX3600RCTL+††	0°C to +70°C	40 TQFN-EP*
MAX3600GCTL+††	0°C to +70°C	40 TQFN-EP*
MAX3600BCTL+††	0°C to +70°C	40 TQFN-EP*

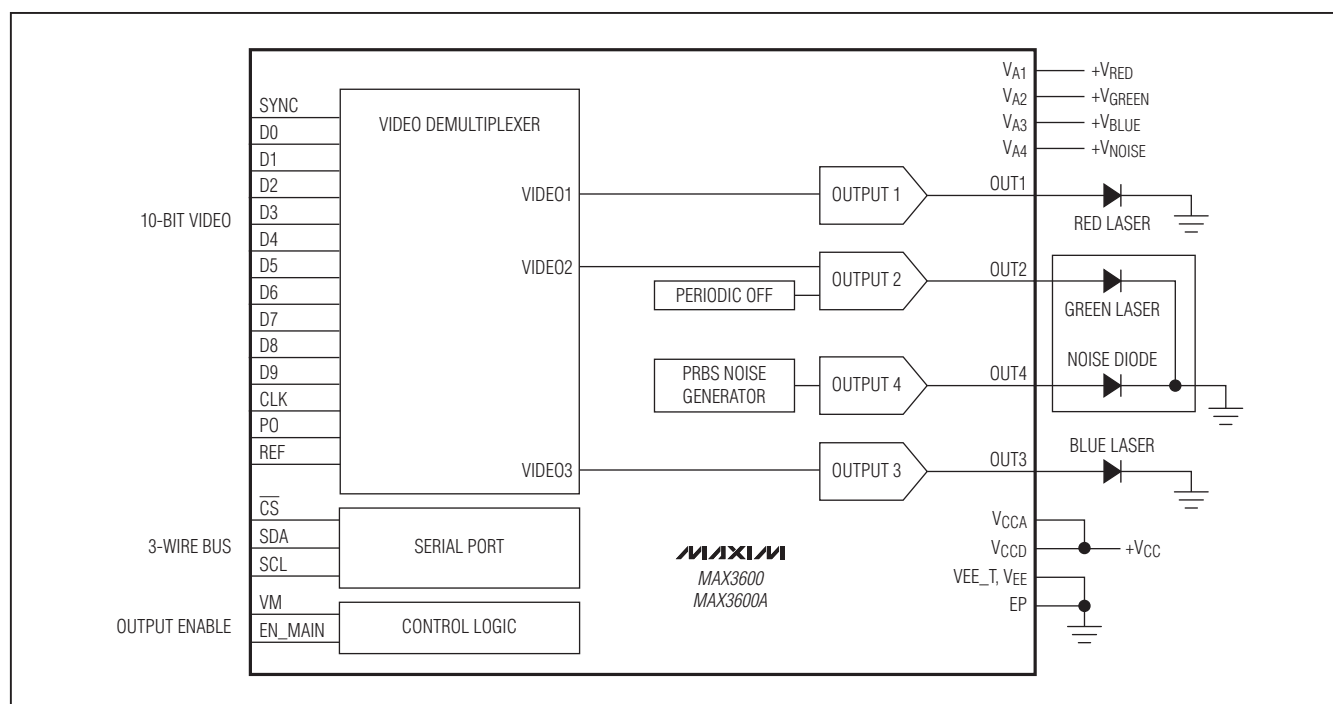
+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

†Not recommended for new designs.

††Future product—contact factory for availability.

Simplified Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, VCCA, VCCD-0.3V to +4.0V
 Voltage Range at VA1, VA2, VA4-0.3V to +6.0V
 Voltage Range at VA3-0.3V to +8.5V
 Voltage Range at OUT1 -0.3V to (VA1 + 0.3V)
 Voltage Range at OUT2 -0.3V to (VA2 + 0.3V)
 Voltage Range at OUT3 -0.3V to (VA3 + 0.3V)
 Voltage Range at OUT4 -0.3V to (VA4 + 0.3V)
 Voltage Range (VA1 - VOUT1), (VA2 - VOUT2),
 (VA4 - VOUT4) 0 to +6.0V
 Voltage Range (VA3 - VOUT3) 0 to +7.5V

Voltage Range at D0 to D9, SYNC, CLK, PO, SCL, SDA,
 \overline{CS} , EN_MAIN, VM, REF, VEE_T, RES .. -0.3V to (VCC + 0.3V)
 Current at OUT1, OUT2, OUT3, OUT4See Table 3
 Current at D0 to D9, SYNC, CLK, PO, SCL, SDA,
 \overline{CS} , EN_MAIN, VM, REF, VEE_T, RES $\pm 50\text{mA}$
 Current at REF $\pm 0.5\text{mA}$
 Continuous Power Dissipation (TA = +70°C)
 40-Pin TQFN (derate 35.7mW/°C above +70°C).....2857mW
 Storage Temperature Range.....-40°C to +150°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = 3.3V $\pm 5\%$, TA = 0°C to +70°C, TJ $\leq +125^\circ\text{C}$, EN_MAIN high, VC_ $\geq 0.9\text{V}$, unless otherwise noted.) (Note 1, Equation 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
VIDEO DAC (10 BITS)							
Maximum Conversion Rate			100	160		Msp/s	
Settling Time		(Note 2)		4		ns	
Rise/Fall Time (20% to 80%)		(Note 2)		1	(4)	ns	
Analog Supply Voltage	VA1, VA2, VA4			> 3.1	6.0	V	
	VA3	OUT3 enabled		> 4.0	8.5		
		OUT3 disabled		> 3.1	8.5		
Compliance Voltage	VC_	VC_ = VA_ - VOUT_		0.5	(6.0)	V	
Analog Supply Current (I _{VA} - I _{OUT}) (Note 3, Figure 8)	IDAC_G0	CLK static	OUT1		18	31	mA
			OUT2		18	34	
			OUT3		19	26	
			OUT4		15	23	
	IDAC_G1			3			
	IDAC_G2		(30)	80			
GAIN DAC (8 BITS): VIDEO_ = 3FFh							
Minimum Full-Scale Current (gs_ = 00h)	GLOW	OUT1	(6)	12	(18)	mA	
		OUT2	(15)	40	(60)		
		OUT3	(3.5)	10	(15)		
		OUT4	(3)	10	(25)		
Maximum Full-Scale Current: MAX3600 (gs_ = FFh)	GHIGH + GLOW	OUT1	175	227	(270)	mA	
		OUT2	550	690	(850)		
		OUT3	140	170	(200)		
		OUT4	140	185	(230)		
Maximum Full-Scale Current: MAX3600A/R/G/B (gs_ = FFh)	GHIGH + GLOW	OUT1	210	280	(330)	mA	
		OUT2	630	760	(955)		
		OUT3	140	170	(210)		
		OUT4	140	185	(300)		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±5%, T_A = 0°C to +70°C, T_J ≤ +125°C, EN_MAIN high, V_C ≥ 0.9V, unless otherwise noted.) (Note 1, Equation 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Settling Time	t _{SG}	To 5% of final value		10	(50)	μs
OFFSET DAC (8 BITS): VIDEO_ = 00h, gs_ = 00h						
Maximum Offset: MAX3600/A/R/G/B	OS _{HIGH}	OUT1	60	83	(110)	mA
		OUT2, OUT3	65	83	(110)	
		OUT4	120	155	(200)	
Offset Error	OS _{LOW}	V _{OUT1} , V _{OUT2} , V _{OUT4} = 1.6V; V _{OUT3} = 2.5V	-25	+0.2	+25	μA
Offset Settling Time	t _{SO}	To 5% of final value		10	(50)	μs
LOGIC I/O: SDA, SCL, CS, VM, EN_MAIN						
Input High Voltage	V _{IH1}	Operating condition	V _{CC} - 0.3		V _{CC} + 0.3	V
Input Low Voltage	V _{IL1}	Operating condition	-0.3		+0.3	V
Input Current		SDA (write), SCL, CS	-10	±0.2	+10	μA
Input Resistance		VM to V _{CCD}	25	60	100	kΩ
		EN_MAIN to V _{EE}	25	60	100	
Input Capacitance		SCL, CS, SDA, VM, EN_MAIN			(1)	pF
Input Hysteresis				100		mV
Enable/Disable Time		From serial port load		< 10		μs
		VM↑ to final value		< 0.25		
		EN_MAIN↑ to final value		< 0.25		
Disable Time	t _{DIS}	EN_MAIN↓ to I _{OUT} ↓		0.01	(1)	μs
Sink Current at SDA		Read mode, V _{SDA} = 0.6V	10	16		mA
VIDEO DATA INPUTS: D0 TO D9, CLK, SYNC, PO						
Minimum Frequency	f _{CLK_MIN}			0.01	(1)	MHz
Maximum Frequency	f _{CLK_MAX}		(140)	> 160		MHz
Clock Duty Cycle		DDR clock, operating condition	(45)		(55)	%
		Standard clock, operating condition	(42)		(58)	
Setup Time	t _{SU}	Operating condition	(0.8)			ns
Hold Time	t _H	Operating condition	(0.8)			ns
Input Switching Time		Operating condition (10% to 90%)		1.5		ns
Input Voltage Range	V _{IN}		-0.3		V _{CC} + 0.3	V
Input High Threshold	V _{IH2}	Relative to V _{REF}			+170	mV
Input Low Threshold	V _{IL2}	Relative to V _{REF}	-170			mV
Reference Voltage	V _{REF}	Operating condition	0.83		V _{CC} /2	V
Data Input Capacitance	C _D			0.4		pF
Termination Resistors	R _{TT}	Figure 6	450	900	1500	Ω
REF Input Current	I _{REF}	V _{REF} = V _{CC} /2	-5	-1.2	+5	μA
Propagation Delay		D0:D9 to OUT_, pixel clocks		3		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±5%, T_A = 0°C to +70°C, T_J ≤ +125°C, EN_MAIN high, V_{C_} ≥ 0.9V, unless otherwise noted.) (Note 1, Equation 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PO GENERATOR						
Pixel Clock Range for PO		Operating condition	24		(102)	MHz
Minimum PO Pulse Width		Four subpixels		3.5		ns
PLL Bandwidth			(560)	800	(1040)	kHz
PRBS OSCILLATOR						
PRBS Oscillator Frequency	f _{PRBS1}	f _{PIXEL} = 24MHz to 102MHz	(100)		(150)	MHz
SERIAL PORT: SDA, SCL, \overline{CS} (Figure 14)						
Maximum Clock Frequency	f _{SCL}	Write mode	(25)			MHz
Input Edge Time		20% to 80%		5		ns
\overline{CS} Leading Time	t _L		(4)			ns
SCL Pulse-Width High	t _{CH}			20		ns
SCL Pulse-Width Low	t _{CL}			20		ns
SCL to SDA Propagation Delay	t _D		(10)			ns
Data In Setup Time	t _{DS}		(10)			ns
Data In Hold Time	t _{DH}		(10)			ns
\overline{CS} Trailing Time	t _T		(10)			ns
POWER SUPPLY: V_{CCA}, V_{CCD}						
Supply Current (I _{VCCA} + I _{VCCD} , g _{S_} = 80h, o _{S_} = 80h, f _{CLK} = 75MHz)	I _{VCC1}	VIDEO_ = 1F0h, CLK_SEL = 0, output disabled		62	80	mA
	I _{VCC2}	CLK_SEL = 1, VIDEO_: 0 ↔ 3FFh repeating		65	90	
	I _{VCC2_ENLO}	Output disabled		60	(70)	
POWER-ON RESET (Figure 15)						
V _{CC} for Chip Enabled	V _{POR1+}			2.9		V
Power-On Reset Parameters	V _{POR2+}	Voltage for output on		V _{CC} - 0.8		V
	V _{POR2-}	Voltage for output off		V _{CC} - 0.9		
	V _{POR3+}	Voltage for output on		3.3		
	V _{POR3-}	Voltage for output off		3.2		
IC Power-Up Time				200		μs

Note 1: Parameters in parentheses () are provided for guidance, but are not tested or guaranteed.

Note 2: Figure 1 shows the AC test circuit. Settling time is defined from the 50% point of a transition to the greater of ±5% of I_{FINAL} or ±1% of I_{SWITCH}. Control register g_{S_} ≥ 34. See Figure 18.

Note 3: I_{DAC} ≈ G₀ + I_{DAC_G1} × V_D + I_{OUT}/I_{DAC_G2}, where V_D is the average video bit density (Δbits/ns) as shown in Table 1.

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Table 1. Example Calculation of Video Bit Density

PIXEL	TIME (ns)	VIDEO CODE	Δ BITS	VD
0	0	1111111111	—	—
1	10	0000000000	10	1.0
2	20	0111111111	9	0.9
3	30	1000000000	10	1.0
4	40	1000000001	1	0.1

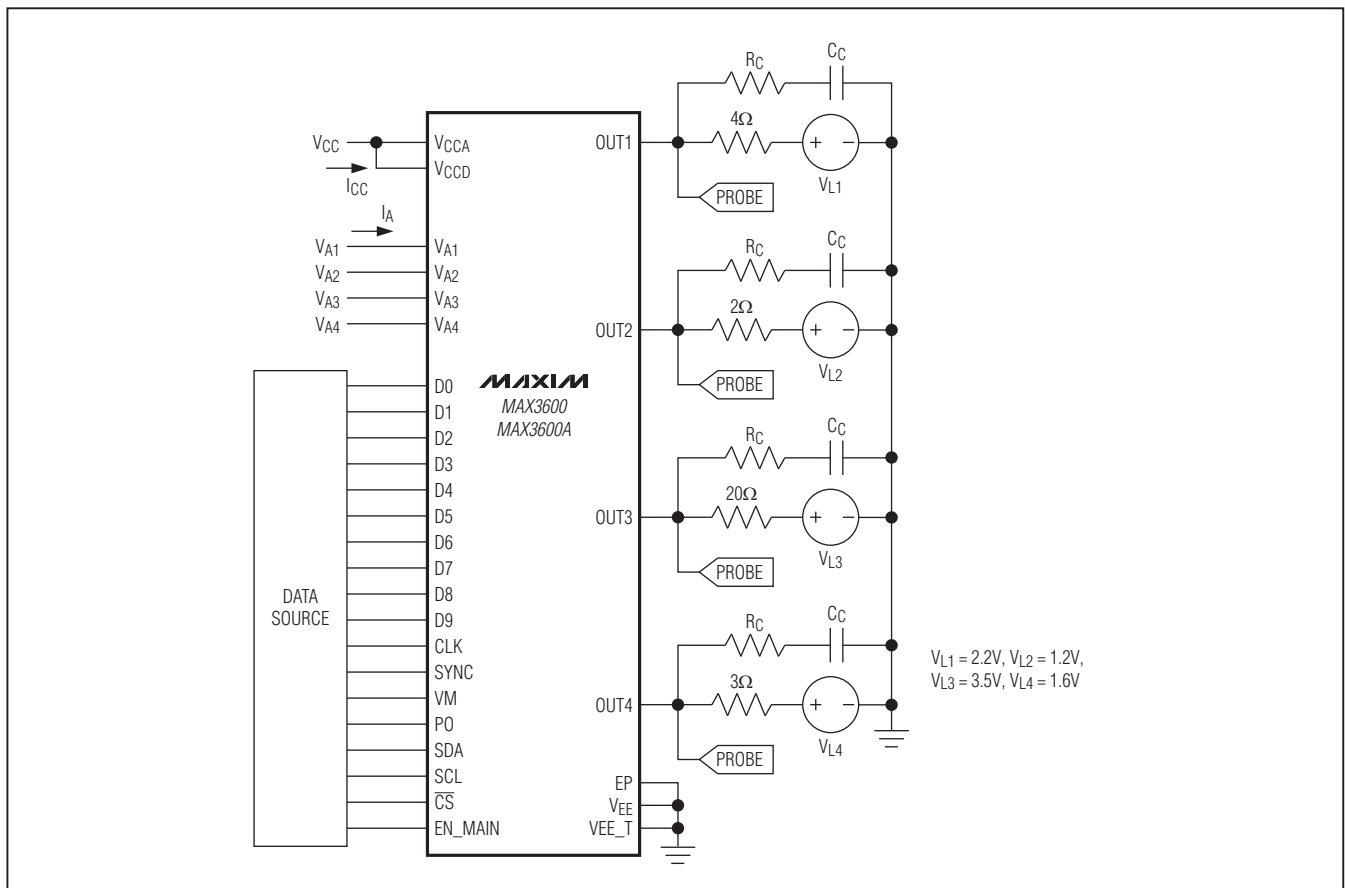
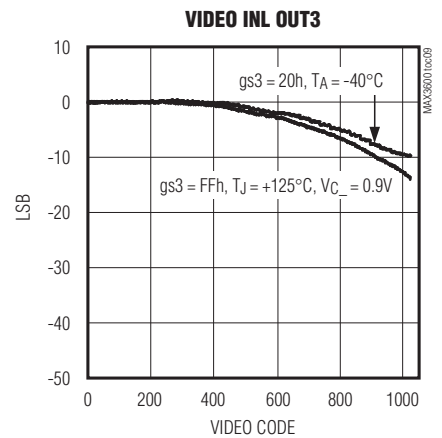
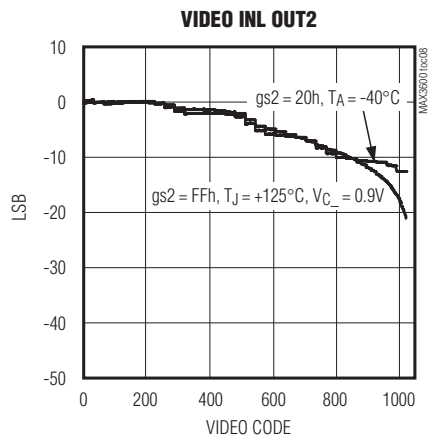
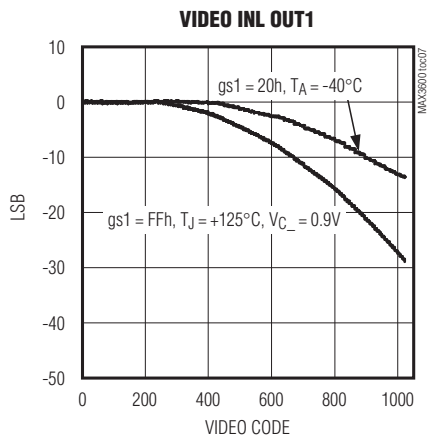
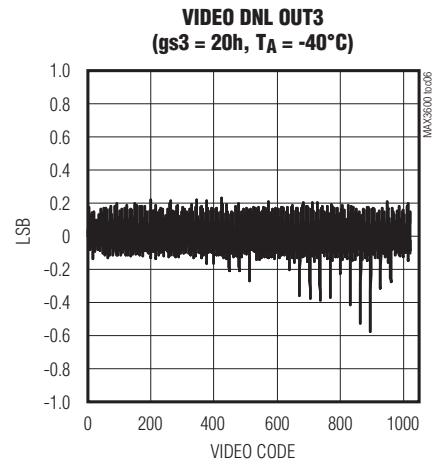
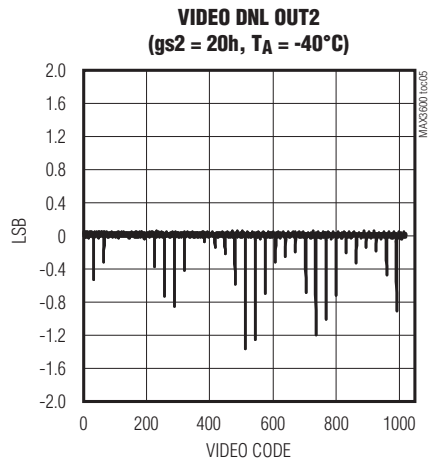
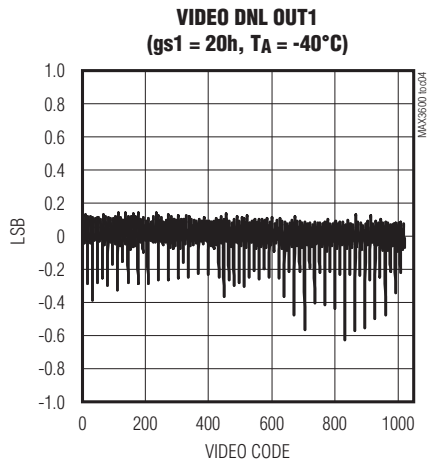
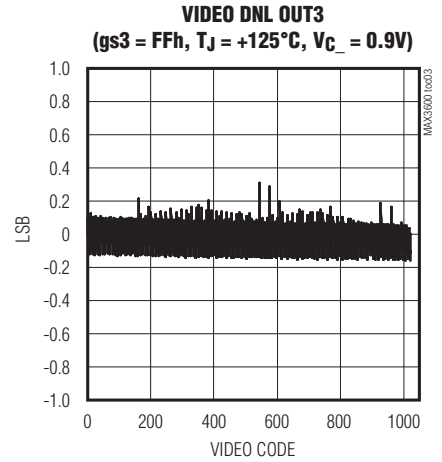
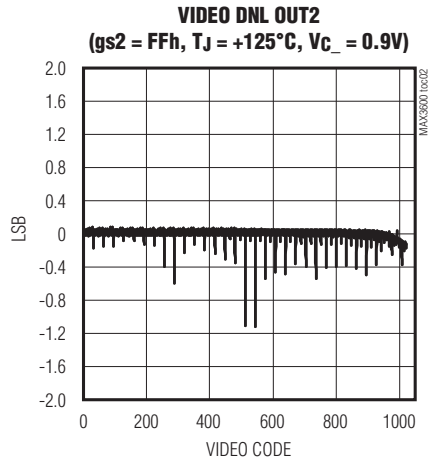
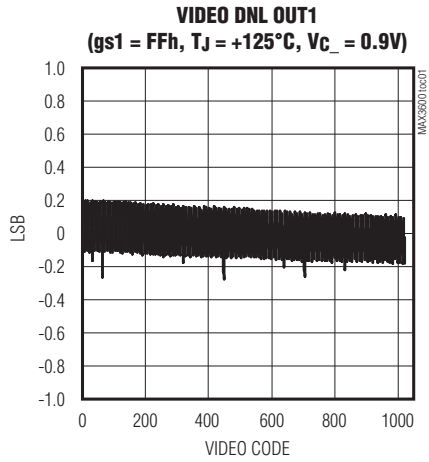


Figure 1. Test Circuit

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Typical Operating Characteristics

($V_{CC} = 3.3V$, $T_A = +25^\circ C$, EN_MAIN high, unless otherwise noted. $V_{C-} = V_{A-} - V_{OUT-}$.)

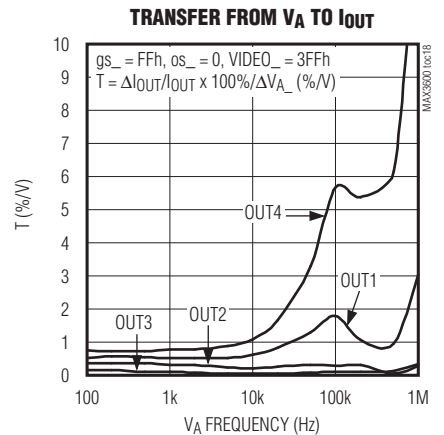
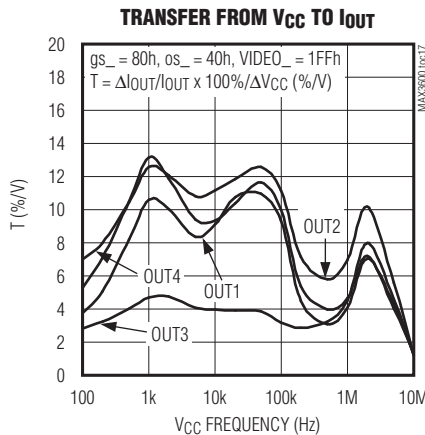
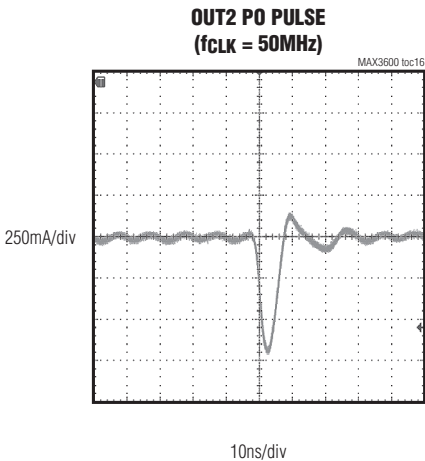
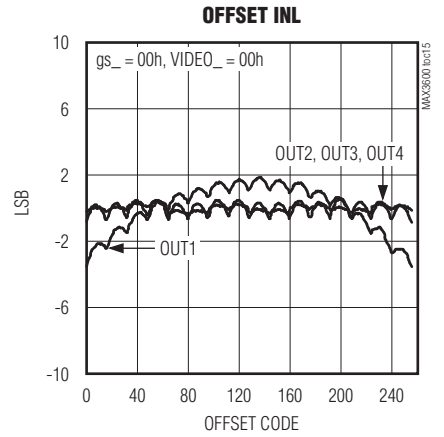
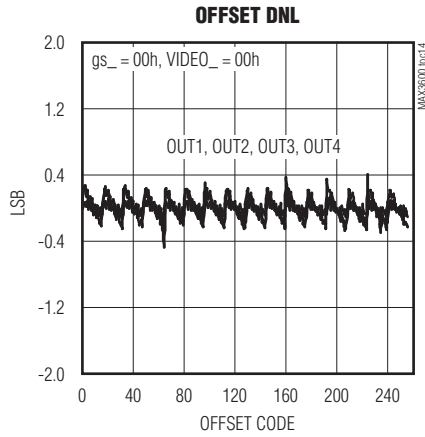
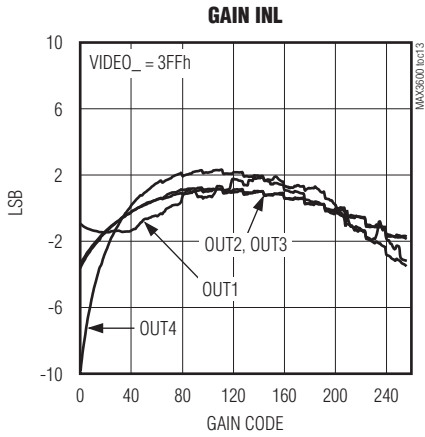
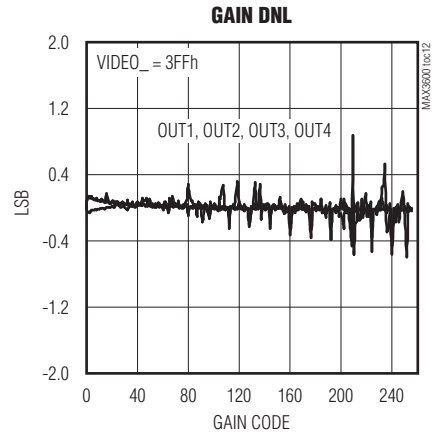
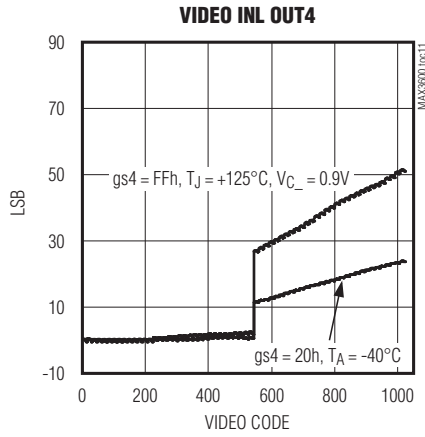
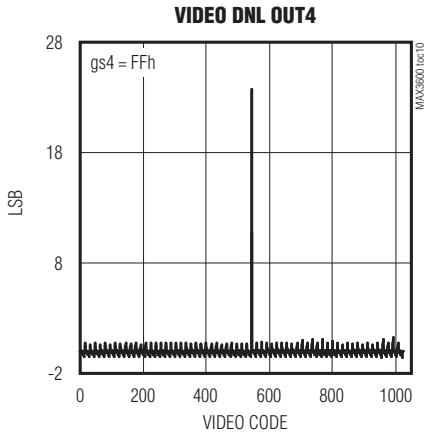


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Typical Operating Characteristics (continued)

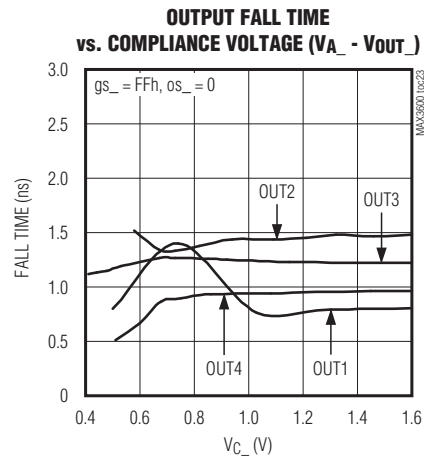
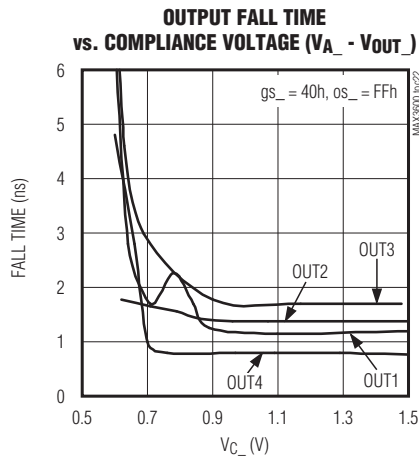
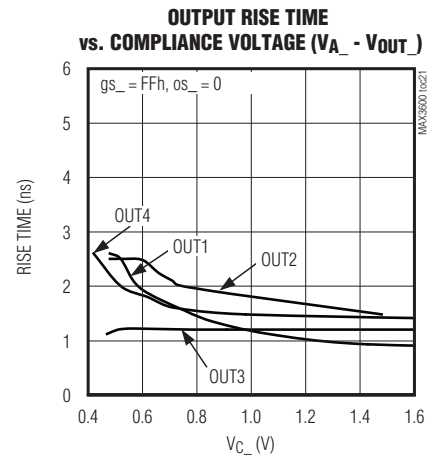
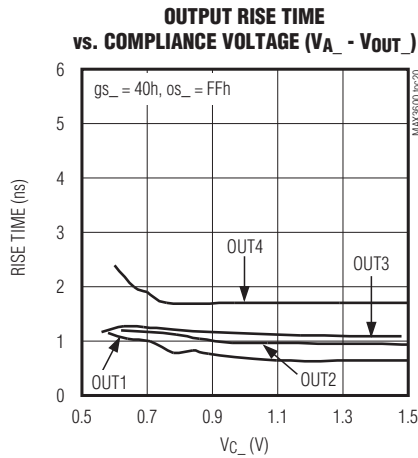
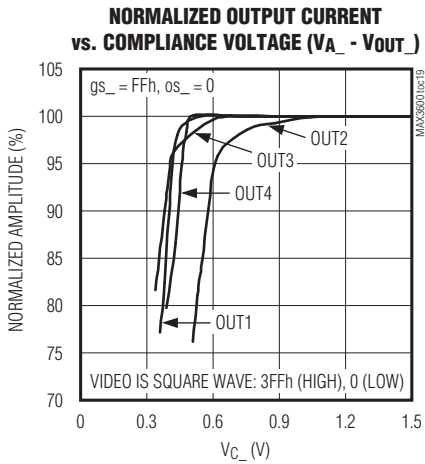
($V_{CC} = 3.3V$, $T_A = +25^\circ C$, EN_MAIN high, unless otherwise noted. $V_{C-} = V_{A-} - V_{OUT-}$)



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Typical Operating Characteristics (continued)

($V_{CC} = 3.3V$, $T_A = +25^\circ C$, EN_MAIN high, unless otherwise noted. $V_{C_} = V_{A_} - V_{OUT_}$)



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Pin Description

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PIN	NAME	FUNCTION
1	D0	Synchronous Video Data Inputs. D0 is the LSB; D9 is the MSB.
2	D1	
3	D2	
4	D3	
5	D4	
6	D5	
7	D6	
8	D7	
9	D8	
10	D9	
11	SYNC	Pixel Clock Input in Configuration 1. See the <i>Typical Operating Circuits</i> .
12	CLK	Video Clock Input
13	RES	Reserved for Future Use. Leave open.
14	OUT3	Connect to Blue Laser Anode. If unused leave open. Available on the MAX3600/A/B only.
15	VA3	Blue Laser Supply Voltage
16, 24, 32	VEE	Ground Connections. Connect to 0V.
17	SDA	Data I/O for Serial Port
18	\overline{CS}	Active-Low Chip Select
19	SCL	Clock Input for Serial Port
20	EN_MAIN	Laser Enable Input. When low, laser current is reduced (3.3V CMOS input with 60k Ω resistor to VEE).
21	VEE_T	Test. Connect to VEE for normal operation.
22	VA4	Noise Diode Supply Voltage
23	OUT4	Connect to Noise Diode Anode. If unused, leave open. Available on the MAX3600/A/G only.
25, 27, 29	VA2	Green Laser Supply Voltage
26, 28, 30	OUT2	Connect to Green Laser Anode. If unused, leave open. Available on the MAX3600/A/G only.
31	N.C.	No Connection. There is no connection from the package to the IC.
33	VM	Video Marker Input. 3.3V CMOS input with 60k Ω pullup to VCCD.
34	VCCA	3.3V Analog Supply. Connect directly to VCCD.
35, 37	VA1	Red Laser Supply Voltage
36	OUT1	Connect to Red Laser Anode. If unused, leave open. Available on the MAX3600/A/R only.
38	VCCD	3.3V Digital Supply. Connect directly to VCCA.
39	REF	Reference Threshold Voltage for Synchronous Inputs
40	PO	Periodic Off Video Data Input. If the periodic off feature is not used, connect the PO pin to ground through a resistor. For periodic off on every pixel, connect PO to VCC through a resistor. ($R_{PO} \approx 2.2k\Omega$ is suitable for all configurations. The resistor is optional, but reduces power.)
—	EP	Exposed Pad. The exposed pad must be connected to VEE.

Laser Driver for Projectors

Detailed Description

The laser driver for projectors supports video imaging with red, blue, and green lasers. Each output includes a 10-bit video DAC with programmable gain and offset.

OUTPUT1, OUTPUT2, and OUTPUT3 support operation with red, green, and blue lasers. OUTPUT4 and the PRBS generator provide noise as required for certain synthetic green lasers. The MAX3600R (Figure 3), MAX3600G (Figure 4), and MAX3600B (Figure 5) are monochrome laser drivers.

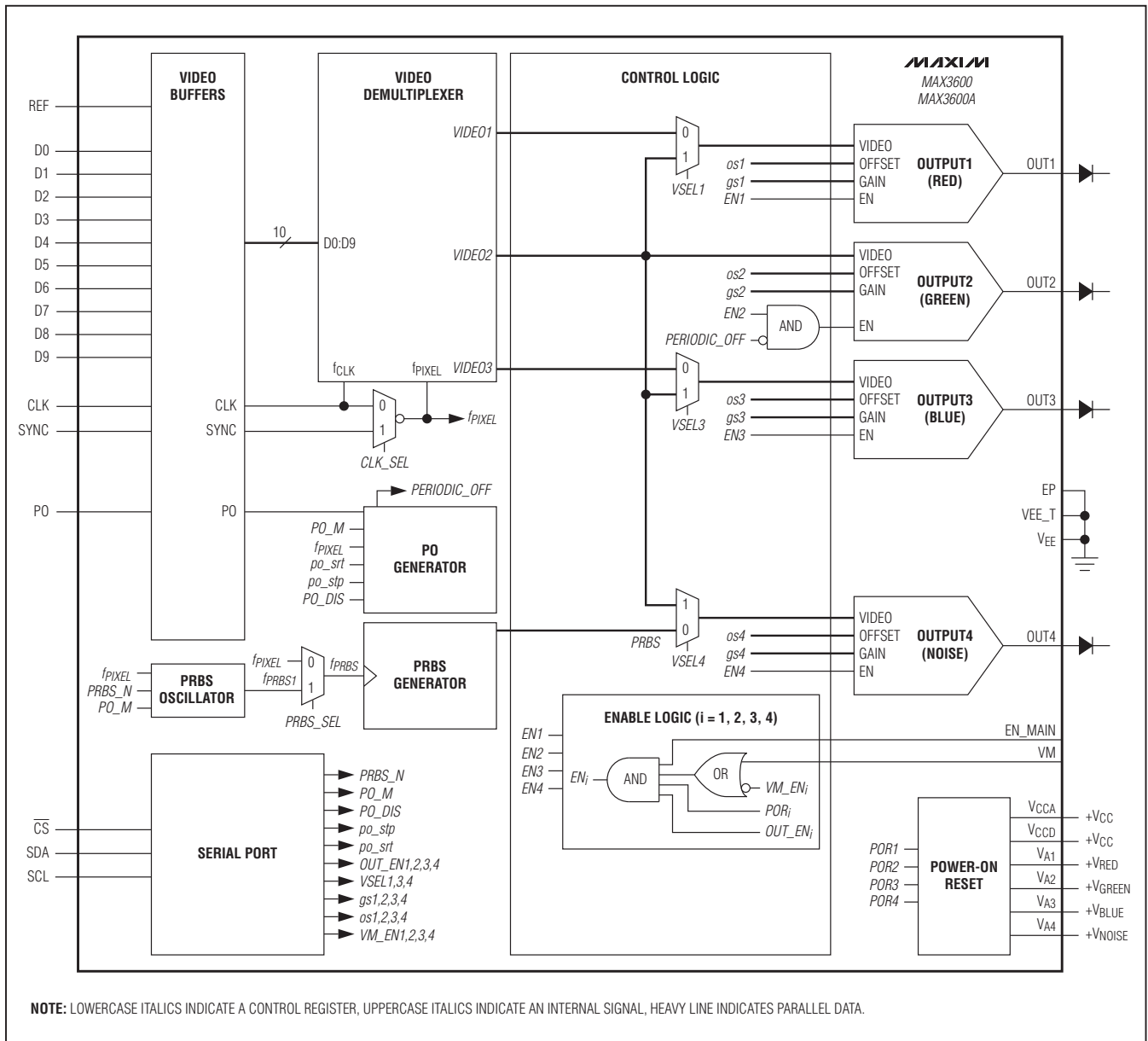


Figure 2. MAX3600/MAX3600A Functional Diagram

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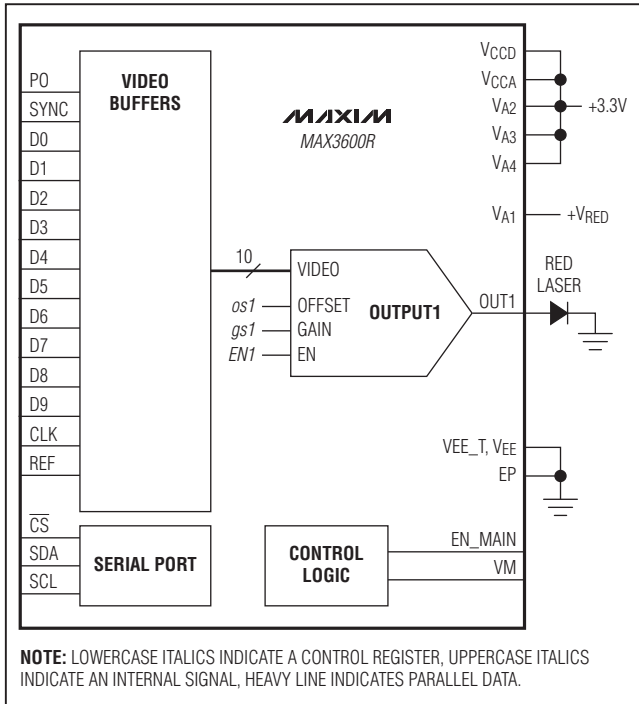


Figure 3. MAX3600R Functional Diagram

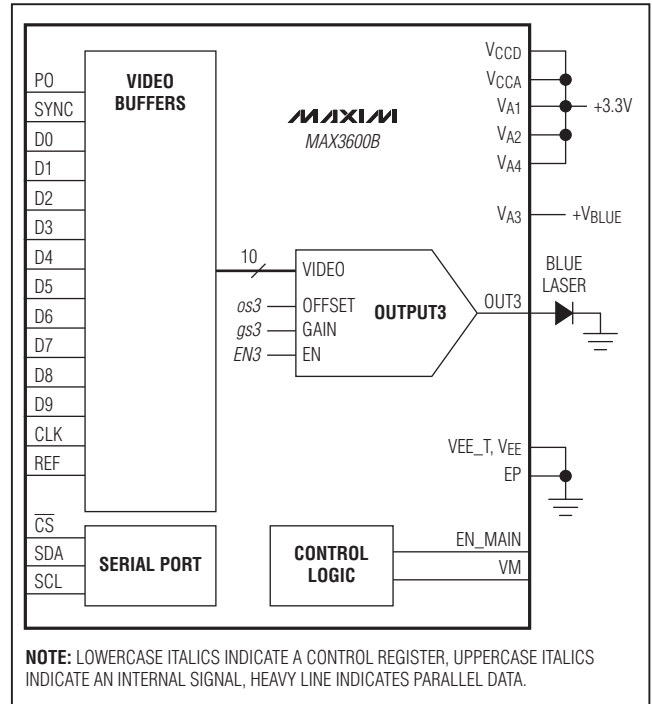


Figure 5. MAX3600B Functional Diagram

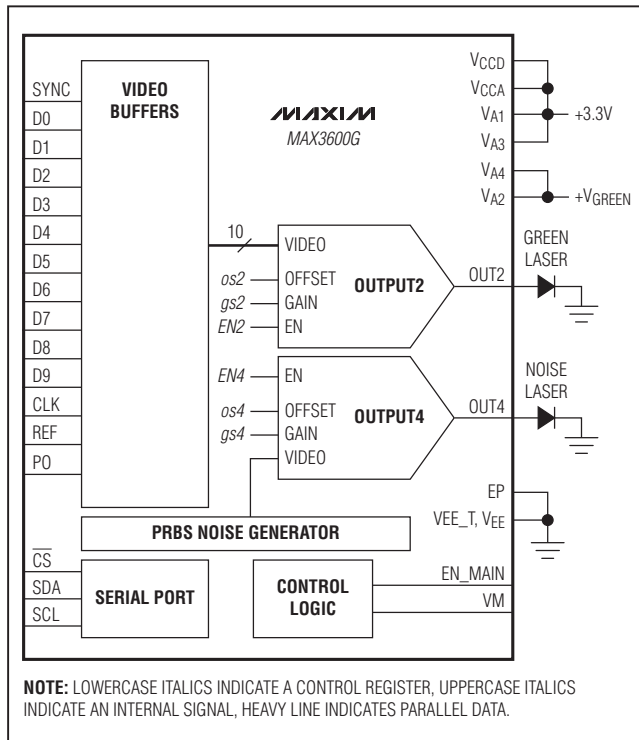


Figure 4. MAX3600G Functional Diagram

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Video Input Buffers

The synchronous video data inputs (D0 to D9, SYNC, CLK, and PO) are pseudo-differential. Each input is compared to VREF, as shown in Figure 6.

D0 to D9, PO, and SYNC can be left open. SYNC can be connected to REF if not used (for reduced power consumption).

Video Demultiplexer

The video demultiplexer (Figure 7) can accommodate configurations as shown in the *Typical Operating Circuits*. In Configuration 1 (Figure 19), 10-bit red, green, and blue video data is time multiplexed. The SYNC signal is used to demultiplex the video data.

In Configuration 2 (Figure 21), each output driver uses VIDEO2 as a data source.

Driver Outputs

The driver outputs provide currents to the lasers as shown in Figure 8.

The transfer characteristic of the driver outputs is shown in Figure 10 and Equation 1.

Equation 1:

$$-I_{OUT} = \frac{VIDEO}{3FFh} \left[\frac{G_{HIGH} \times gs}{FFh} + G_{LOW} \right] + \left[\frac{OS_{HIGH} \times os}{FFh} \right] + OS_{LOW}$$

where:

- Current into the laser driver is positive (out is negative)
- VIDEO is the 10-bit video input
- gs is the 8-bit gain setting register
- os is the 8-bit offset setting register
- GLOW is the minimum gain (mA)
- (GLOW + GHIGH) is the maximum gain (mA)
- OSHIGH is the maximum offset (mA)
- OSLOW is the minimum offset (mA)

The output compliance voltage ($V_{C_} = V_{A_} - V_{OUT_}$, Figure 9) defines the output voltage required to obtain low overshoot and fast settling time.

Table 2 summarizes the typical output current capability for each driver output. Table 3 summarizes the maximum ratings for each driver output.

Table 2. Driver Output Typical Parameter Summary

PARAMETER	OUT1 (mA)	OUT2 (mA)	OUT3 (mA)	OUT4 (mA)
Minimum Gain (G _{LOW})	12	40	10	10
Maximum Gain (G _{LOW} + G _{HIGH})	227	690	170	185
Maximum Offset (O _{HIGH})	83	83	83	155

Table 3. Driver Output Absolute Maximum Ratings (Current Out of Part)

PARAMETER	OUT1 (mA)	OUT2 (mA)	OUT3 (mA)	OUT4 (mA)
DC Current (T _J = +125°C)	320	735	245	310
DC Current (T _J = +110°C)	480	1100	382	465
Peak Current (t < 1μs, T _J = +125°C)	640	1470	490	620

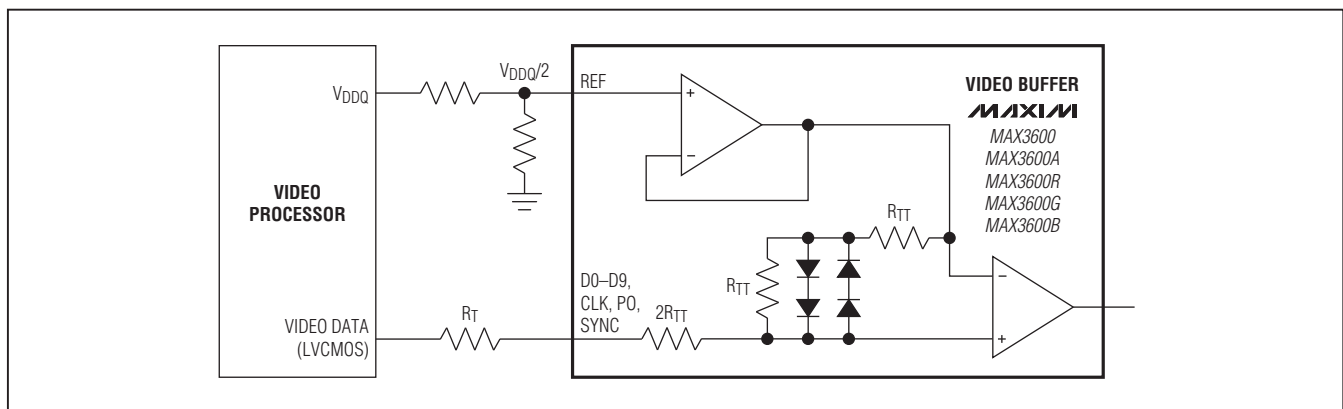


Figure 6. Video Inputs

Laser Driver for Projectors

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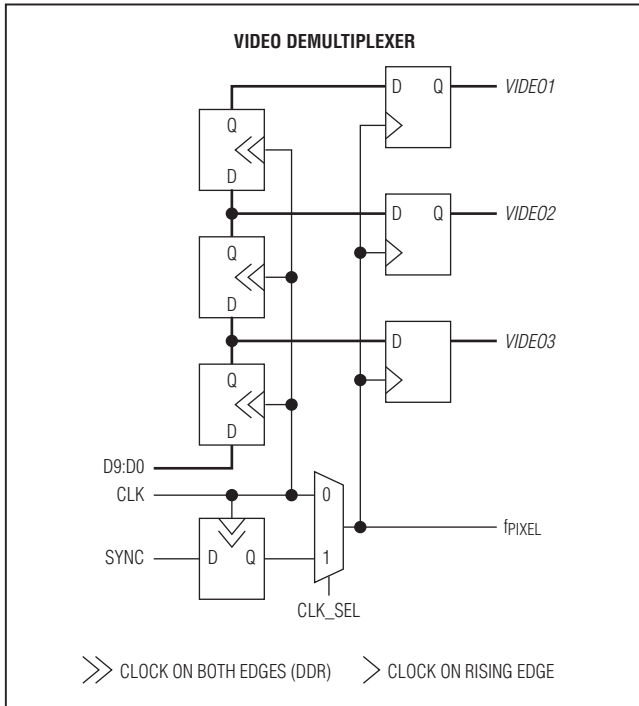


Figure 7. Video Demultiplexer

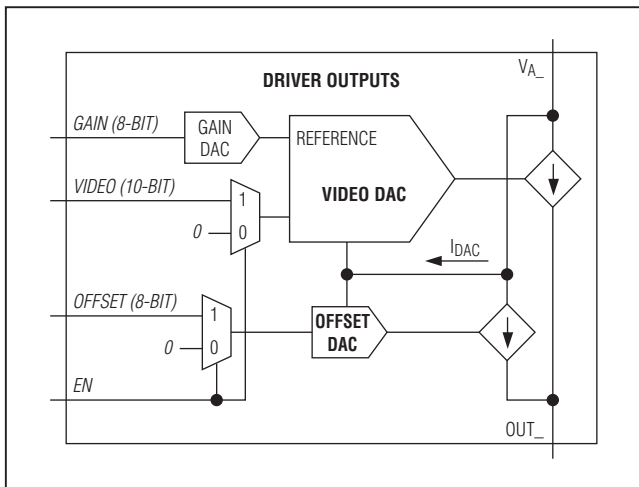


Figure 8. Driver Output

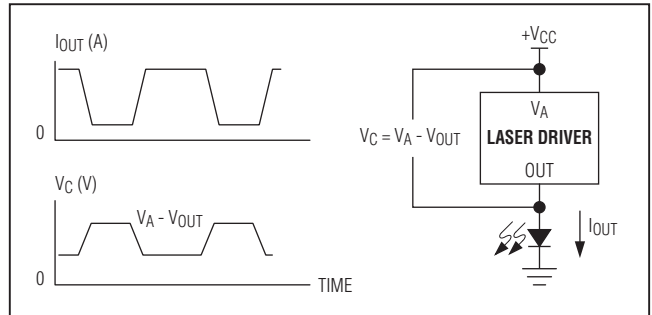


Figure 9. Output Compliance Voltage

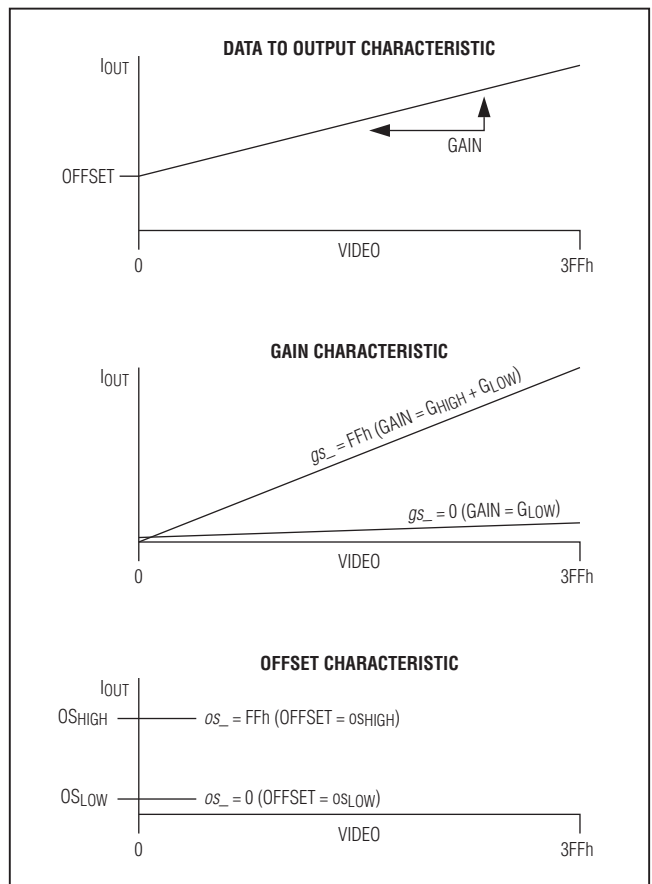


Figure 10. Data to Output Characteristics

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Control Logic

The control logic provides video selection, laser enable, and power savings.

Video Selection

The video demultiplexer creates signals *VIDEO1*, *VIDEO2*, and *VIDEO3*. The *VSEL[1/3/4]* bits can be used to select the input video for *OUTPUT1*, *OUTPUT3*, and *OUTPUT4*.

Laser Control

When *EN_MAIN* is low, all driver outputs are off. This signal works asynchronously (no clock is required to disable outputs).

The video marker (*VM*) input can be used to disable selected outputs when a video signal is not present (Figure 11). The *VM_EN[1:4]* bit settings determine which outputs respond to the *VM* signal.

Propagation delay from *VM*↑ or *EN_MAIN*↑ to output active is typically $35\text{ns} + 2/f_{\text{PIXEL}}$.

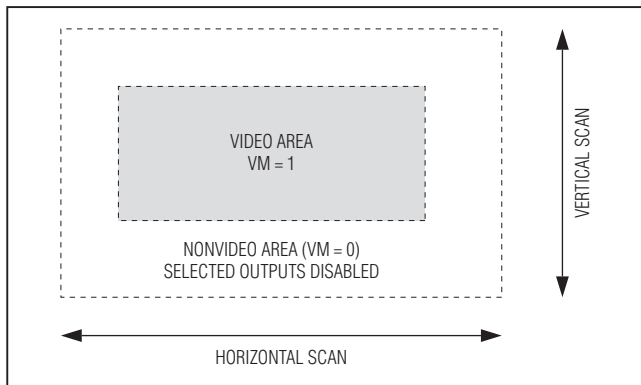


Figure 11. Video Marker

Periodic Off Generator

The periodic off (*PO*) generator quickly switches off *OUTPUT2*. The *PO* event is placed within a pixel if *PO* is set high during a pixel as shown in Figure 12.

The *PO* event location within the pixel is programmed from the serial port. Each pixel is divided into “*m*” equal time subpixels as shown in Figure 13. The *PO_M* setting determines the number of subpixels, where:

$$m = (\text{PO_M} + 1) \times 8$$

The *PO* start and *PO* stop locations (in subpixels) are defined by the *P1*, *P1S*, *P2*, and *P2S* bits.

Start Subpixel =

$$[(P1 + 1) \text{ MOD } (\text{PO_M} + 1)] \times 8 + P1S + 1$$

Stop Subpixel =

$$[(P2 + 1) \text{ MOD } (\text{PO_M} + 1)] \times 8 + P2S + 1$$

The start and stop locations should be selected to ensure that the *PO* event occurs > one rise/fall time from the pixel update. The minimum off-time is four subpixels. Select $P1, P2 \leq \text{PO_M}$.

The *PO* oscillator frequency (f_{PO}) = $f_{\text{PIXEL}} \times (\text{PO_M} + 1)$. The intended operating range for f_{PO} is 133MHz to 200MHz.

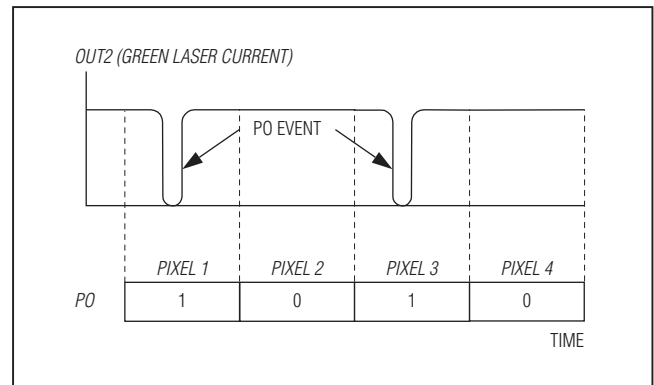


Figure 12. Periodic Off (*PO*) Example

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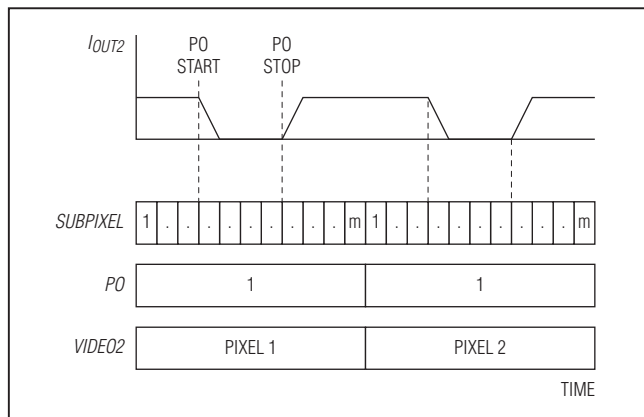


Figure 13. PO Subpixels

Table 4. PO Subpixel Programming

t _{PIXEL} (ns)	PO_M	PRBS_N	SUBPIXELS (m)	f _{PRBS1} (MHz)
10	1	3	16	136
12	1	2	16	125
14	1	0	16	129
16	2	3	24	128
18	2	2	24	125
20	2	1	24	120
22	2	0	24	123
24	3	2	32	125
26	4	3	40	131
28	4	3	40	121
30	4	2	40	125
32	4	1	40	125
34	5	3	48	120
36	5	2	48	125
38	6	3	56	125
40	6	3	56	119

Table 5. PRBS Oscillator

PRBS_N	f _{PRBS1} /f _{PO}
0	0.9
1	0.8
2	0.75
3	0.68

PRBS Oscillator

The PRBS oscillator creates clock f_{PRBS1}, which can be input to the PRBS generator. The oscillator frequency is determined by the PRBS_N bit setting as shown in Table 5. The recommended range for f_{PRBS1} is 100MHz to 150MHz. Note that the PRBS oscillator is not phase-locked to the pixel clock. Therefore, OUT4 updates are not synchronous to the pixel clock when the PRBS oscillator is used.

PRBS Generator

Output 4 can be used to generate random noise. A 32-bit shift register with feedback generates pseudo-random codes. The PRBS_SEL bit selects the PRBS clock source.

Serial Port and Registers

The serial port provides a 3-wire interface with bidirectional data (SDA), clock input (SCL), and a chip-select input (CS) as shown in Figure 14. Table 6 shows the register addresses. The external master initiates a data transfer by asserting the CS pin.

Write Mode (R/W = 0): The master generates 16 clock cycles. It outputs 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master ends the transmission by setting CS high. The laser driver updates control registers on the rising clock edge of the last data bit.

Read Mode (R/W = 1): The master generates 16 clock cycles. It outputs 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the R/W bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master ends the transmission by setting the CS pin high. Read clock speed is determined by the external pullup resistor and parasitic capacitance at the SDA pin.

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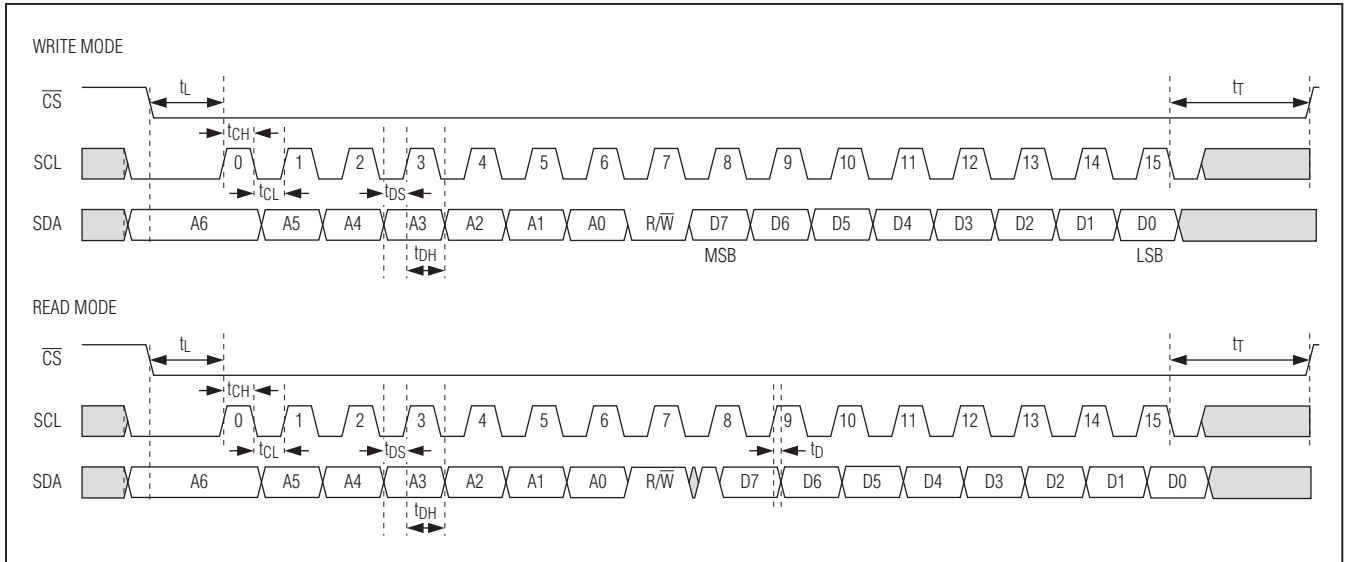


Figure 14. Serial Port Timing Diagram

Table 6. Register Map

ADDRESS	NAME	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
00h	os1	OUTPUT1 Offset	MSB							LSB	
01h	gs1	OUTPUT1 Gain	MSB							LSB	
02h	os2	OUTPUT2 Offset	MSB							LSB	
03h	gs2	OUTPUT2 Gain	MSB							LSB	
04h	os3	OUTPUT3 Offset	MSB							LSB	
05h	gs3	OUTPUT3 Gain	MSB							LSB	
06h	os4	OUTPUT4 Offset	MSB							LSB	
07h	gs4	OUTPUT4 Gain	MSB							LSB	
08h	enable	Enable	OUT_EN1	OUT_EN2	OUT_EN3	OUT_EN4	VM_EN1	VM_EN2	VM_EN3	VM_EN4	
09h	cnfig	Video Data Control	X	X	X	VSEL1	VSEL3	VSEL4	PRBS_SEL	CLK_SEL	
0Ah	osc	Oscillator	X	X	PRBS_N MSB	PRBS_N LSB	PO_DIS	PO_M MSB	PO_M	PO_M LSB	
0Bh	po_srt	PO Start Subpixels	X	X	P1 MSB	P1	P1 LSB	P1S MSB	P1S	P1S LSB	
0Ch	po_stp	PO Stop Subpixels	X	X	P2 MSB	P2	P2 LSB	P2S MSB	P2S	P2S LSB	

Note: Registers default to (0) at power-on (unless a different default value is noted).

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Table 7. cnfig Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:5	X	0	Unused.
4	VSEL1	0	Video select for OUTPUT1. 0 = VIDEO1, 1 = VIDEO2.
3	VSEL3	0	Video select for OUTPUT3. 0 = VIDEO3, 1 = VIDEO2.
2	VSEL4	0	Video select for OUTPUT4. 0 = PRBS, 1 = VIDEO2.
1	PRBS_SEL	0	PRBS clock source select. 1 = fPRBS1, 0 = fPIXEL.
0	CLK_SEL	1	Pixel clock source select. 0 = CLK pin, 1 = SYNC pin.

Table 8. osc Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:6	X	0	Unused.
5:4	PRBS_N	0	PRBS oscillator configuration. See Table 5. Bit 5 is the MSB, and bit 4 is the LSB.
3	PO_DIS	0	Disables the output of the PO pulse generator. When the value is 1, no PO pulses are created.
2:0	PO_M	1	PO oscillator control. See Table 4. Bit 2 is the MSB, and bit 0 is the LSB.

Table 9. po_srt Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:6	X	0	Unused.
5:3	P1	1	These bits contain the P1 parameter used to program the PO start subpixel.
2:0	P1S	4	These bits contain the P1S parameter used to program the PO start subpixel.

Table 10. po_stp Register Bit Description

BIT	NAME	DEFAULT	DESCRIPTION
7:6	X	0	Unused.
5:3	P2	0	These bits contain the P2 parameter used to program the PO stop subpixel.
2:0	P2S	1	These bits contain the P2S parameter used to program the PO stop subpixel.

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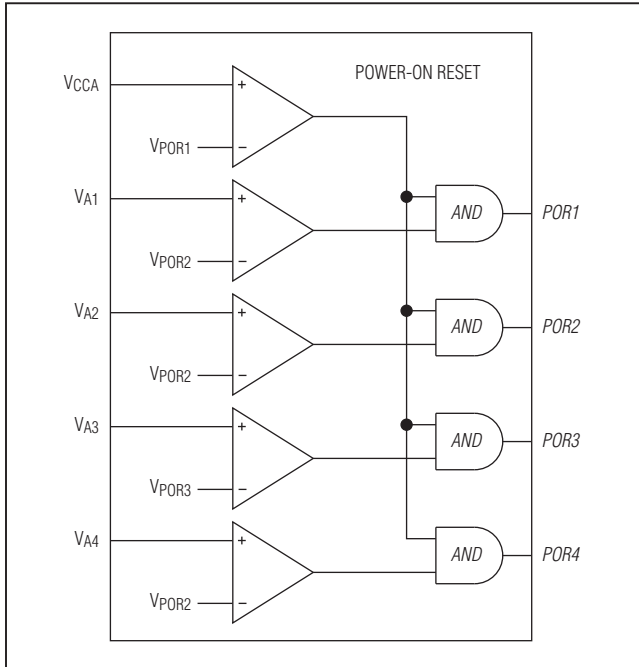


Figure 15. Power-On Reset

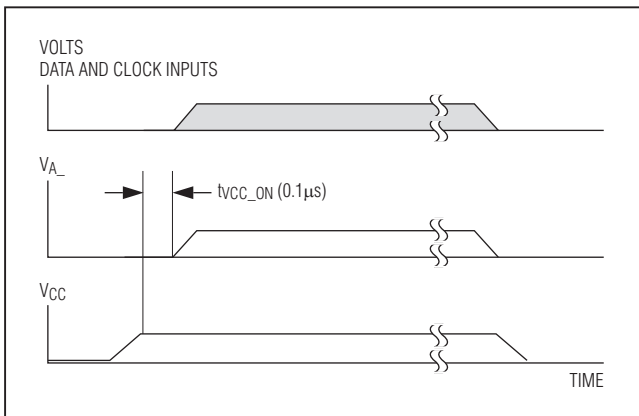


Figure 16. Power-Supply Sequencing

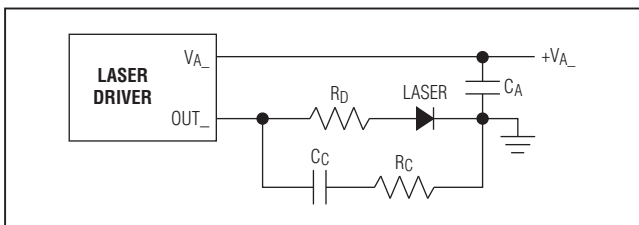


Figure 17. Optional Compensation Components

Power-On-Reset

The power-on reset monitors the supply voltages of the circuit (Figure 15). It is recommended that VCC be applied to the IC before VA1 to VA4 are applied as shown in Figure 16. On power-down, it is recommended that VA1 to VA4 are powered down before VCC. *Failure to follow the sequencing recommendation can result in device stress, but has not been observed to cause immediate damage.*

Design Procedure

Supply Filter

Element CA (see the *Typical Operating Circuits*) is present to reduce supply noise and provide a ground return path for switched current. Select $C_A \geq 10\mu\text{F}$. CA can be composed of two or three capacitors in parallel.

Use care to ensure VA3 does not exceed +9V at any time, including power-on, as this can damage the ESD protection circuitry.

Compensation Network

Optional compensation elements RC and CC can be used to compensate the inductive load of the laser (Figure 17). The resulting filter reduces ringing and increases the switching time of the laser driver. The best values for RC and CC should be found by experimentation. Note that CC must be charged before light output appears from the laser. If a compensation network is used, minimize inductance in the ground return.

Typical starting values:

$$R_C \approx R_L \text{ to } 2 \times R_L \text{ (} R_L = \text{Laser Resistance)}$$

$$C_C \approx 1/(2\pi f_{\text{VIDEO}} \times R_L)$$

Ringing of the green laser can be reduced with resistor RD.

PCB Layout

Place the green laser as close to the laser driver as possible. The green laser typically has a small resistive component and is more sensitive to inductance than other laser connections. The green laser connection should appear as a low-impedance transmission line. Use wide traces located close to the ground plane for maximum capacitance.

The connection from OUT2 to the laser should be as short as possible, ideally < 1cm. The connection distance from the laser cathode, across the ground plane, through the filter capacitor, to VA2, is ideally < 1cm.

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Consider the power supply on the $V_{A_}$ pins. Droop on these pins reduces the compliance voltage. Use two or three capacitors to bypass $V_{A_}$ to ground. Place a small capacitor close to the V_{A2} pin to keep the ground return loop small. A larger capacitor can be located farther from $V_{A_}$.

It is best to solder the laser to the PCB. If a connector is required, minimize inductance. Inductance > 10nH at OUT2 could cause large ringing. When routing OUTPUT1 and OUTPUT2, route connections to the $V_{A_}$ pins on the top layer, and connect the $OUT_$ pins to the laser through vias.

Laser Driver Thermal Considerations

The circuit is designed to meet specifications with an operating junction temperature (T_J) up to +125°C. The junction temperature is estimated by:

$$T_J \approx [(I_{CC})(V_{CC}) + \Sigma (I_{VA_})(V_{C_})] \theta_{JA} + T_A$$

The recommended thermal path is through the package backside exposed pad (EP). A heatsink on the package top does not significantly reduce junction

temperature. Recommendations for PCB design are found in Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Applications Information

Connecting OUT2 and OUT4

It is possible to connect OUT4 and OUT2 to achieve a higher output current. There is a small delay on OUT4 relative to OUT2. Note that OUT4 linearity performance is lower than OUT2 linearity.

Eye Safety

Specification IEC 825 defines the maximum safe output of optical devices. This laser driver provides enable features that aid compliance with IEC 825. Using this laser driver alone does not ensure that a product is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Maxim products are not designed for use as components in systems where the failure of a Maxim product could create a situation where injury could occur.

Table 11. Thermal Design Properties

PARAMETER	SYMBOL	VALUE
Ambient Temperature	T_A	—
Operating Junction Temperature	T_J	$\leq +125^\circ\text{C}$
Thermal Resistance, Junction-to-Case	θ_{JC}	+2°C/W
Thermal Resistance, Junction-to-Ambient, Multilayer Board	θ_{JA-2}	+28°C/W

Note: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

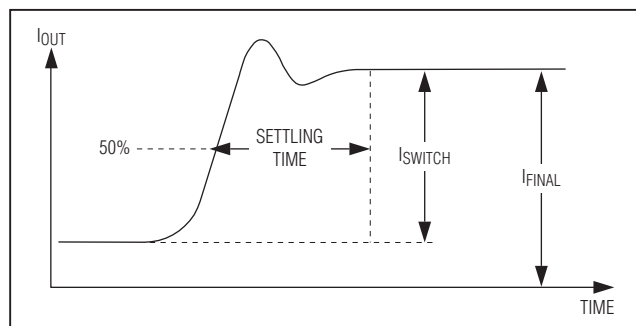


Figure 18. Settling Time and Measurement

Laser Driver for Projectors

Typical Operating Circuits

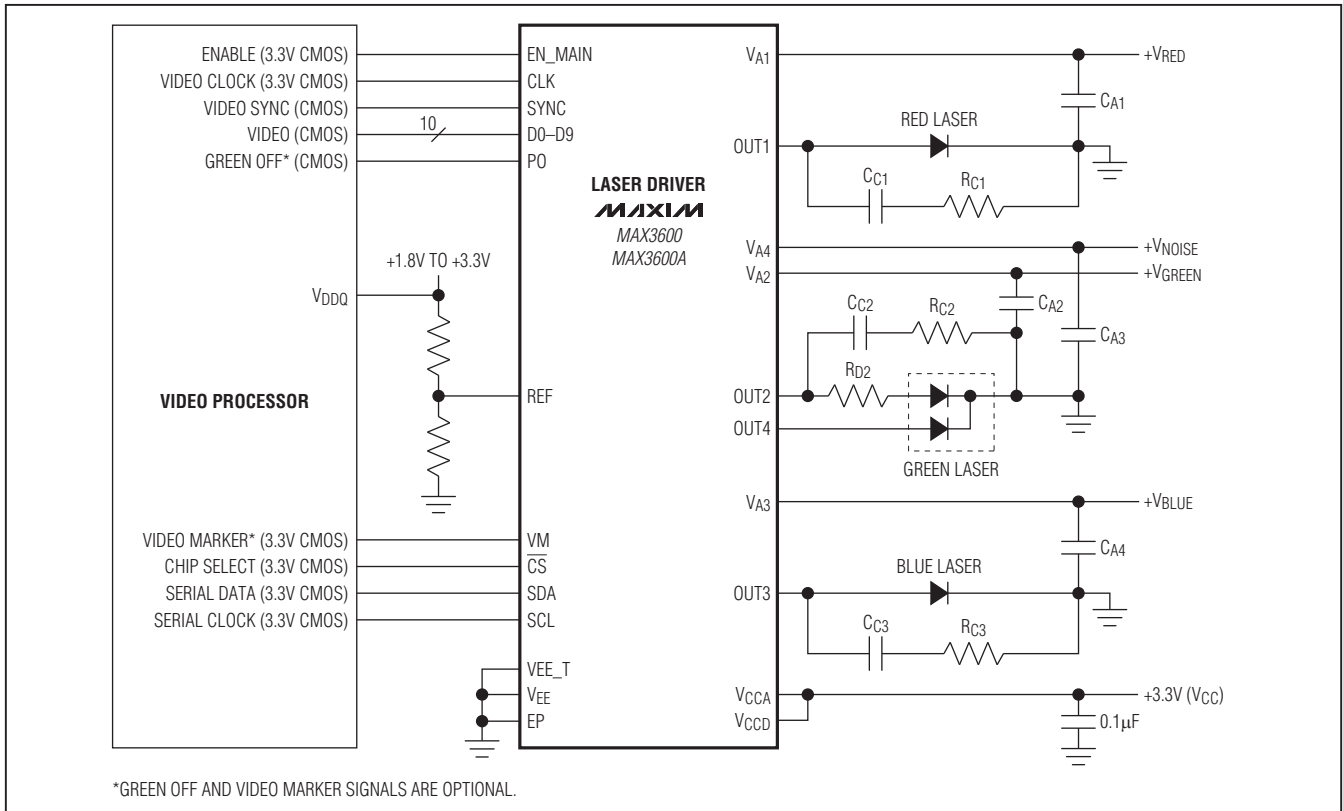


Figure 19. Typical Operating Circuit: Configuration 1

Configuration 1: RGB Laser Driver with DDR Clock

Configuration 1 is described in Figures 19 and 20 and Table 12.

- 10-bit video (D0 = LSB, D9 = MSB), DDR clock
- Data is multiplexed R-G-B (Figure 20)
- SYNC = 1 when blue data is on D0 to D9
- PO event occurs when PO = 1

Table 12. Configuration 1 Register Settings

BIT	SETTING	NOTES
VSEL1	0	VIDEO1 → red laser
VSEL3	0	VIDEO3 → blue laser
VSEL4	0	PRBS → noise diode
CLK_SEL	1	DDR clock with SYNC
OUT_EN[1:4]	1	Enable outputs

Note: See the Detailed Description section for more information about register programming.

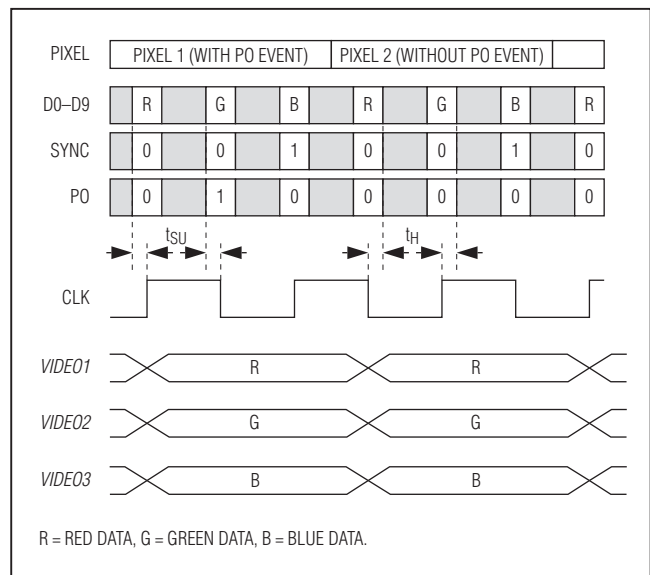


Figure 20. Configuration 1: Video Data Format

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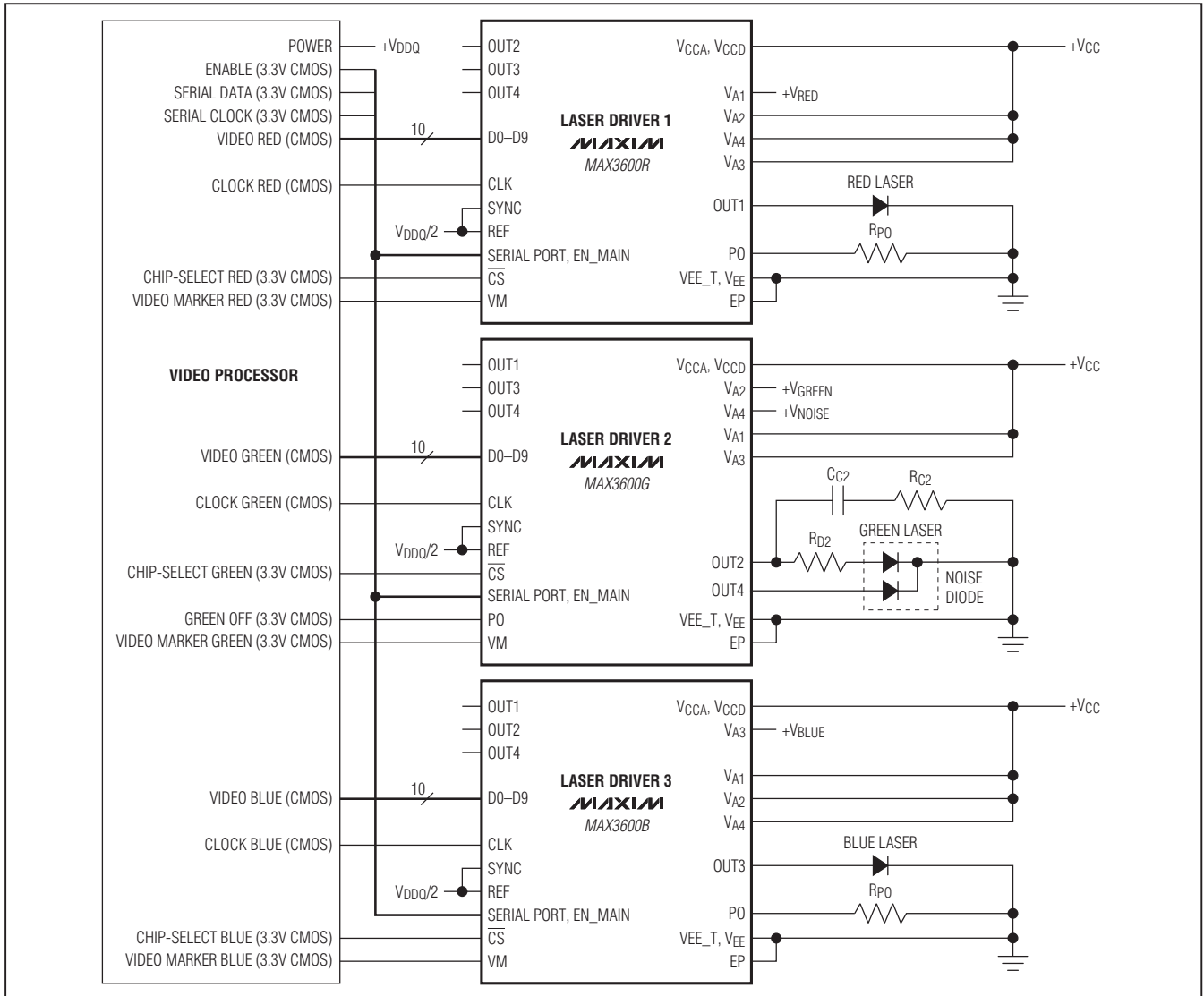


Figure 21. Typical Operating Circuit: Configuration 2

Configuration 2: Video Data with RZ Clock

Configuration 2 is described in Figures 21 and 22 and Table 13.

- 10-bit video (D0 = LSB, D9 = MSB)
- Return-to-zero clock
- Video data is always routed to VIDEO2, for constant delay from clock to output
- Achieves highest possible resolution

Table 13. Configuration 2 Register Settings

LDD	BIT	VALUE	NOTES
1	VSEL1	1	VIDEO2 → red laser
1	OUT_EN1	1	Enable OUT1
1, 2, 3	CLK_SEL	0	Select RZ clock
2	OUT_EN2, OUT_EN4	1	Enable OUT2, OUT4
3	VSEL3	1	VIDEO2 → blue laser
3	OUT_EN3	1	Enable OUT3

Note: See the Detailed Description section for more information about register settings.

Laser Driver for Projectors

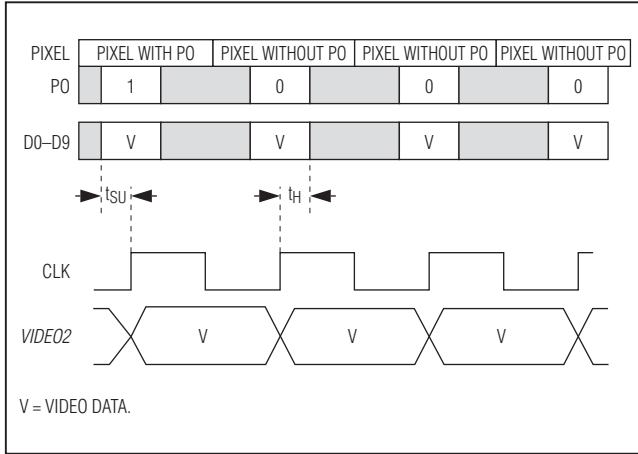
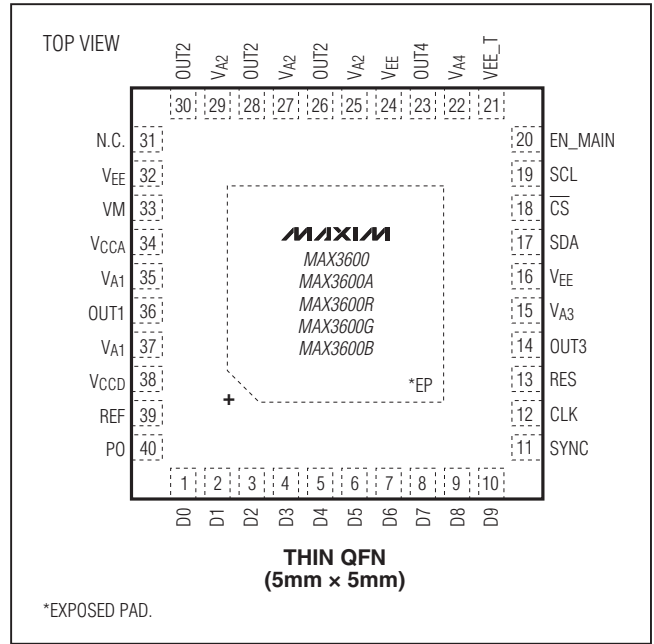


Figure 22. Configuration 2: Video Data Format

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002

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Revision History

MAX3600

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	10/09	Corrected errors for SCL in Figure 14	16
2	8/10	Removed future status from the MAX3600A in the <i>Ordering Information</i> table; added the soldering temperature to the <i>Absolute Maximum Ratings</i> section; in the <i>Electrical Characteristics</i> table updated the analog supply voltage and analog supply current values, added compliance voltage, updated maximum offset values, and added propagation delay; corrected the equation in Note 3; corrected the units for VD in Table 1; replaced Figure 7; added the land pattern no. to the <i>Package Information</i> table	1-5, 13, 22

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