SY84402L

4.25Gbps VCSEL Driver

General Description

The SY84402L is a 3.3V VCSEL driver for applications up to 4.25Gbps. The driver comes in a 2mm x 2mm MLF® package which makes it less than half the size of any other driver operating at that rate. The variable output swing on the SY84402L makes it ideal for use as a VCSEL driver as well as a backplane driver/receiver.

The operational range of the SY84402L control input is from V_{CC}-1.42V (for maximum output swing) to V_{CC} (for minimum output swing). VCTRL can also be driven by a DAC such as those contained in the MIC300X, Micrel's FOM controller family.

The SY84402L provides a VT output for use as a DC bias for AC-coupling to the device. The input termination network can easily be modified to handle a DC-coupled PECL output to save board space by simply tying the VT terminal to ground through a 50 Ohm resistor. The VT pin should be used only as a bias for this device as its current sink/source capability is limited.

All datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

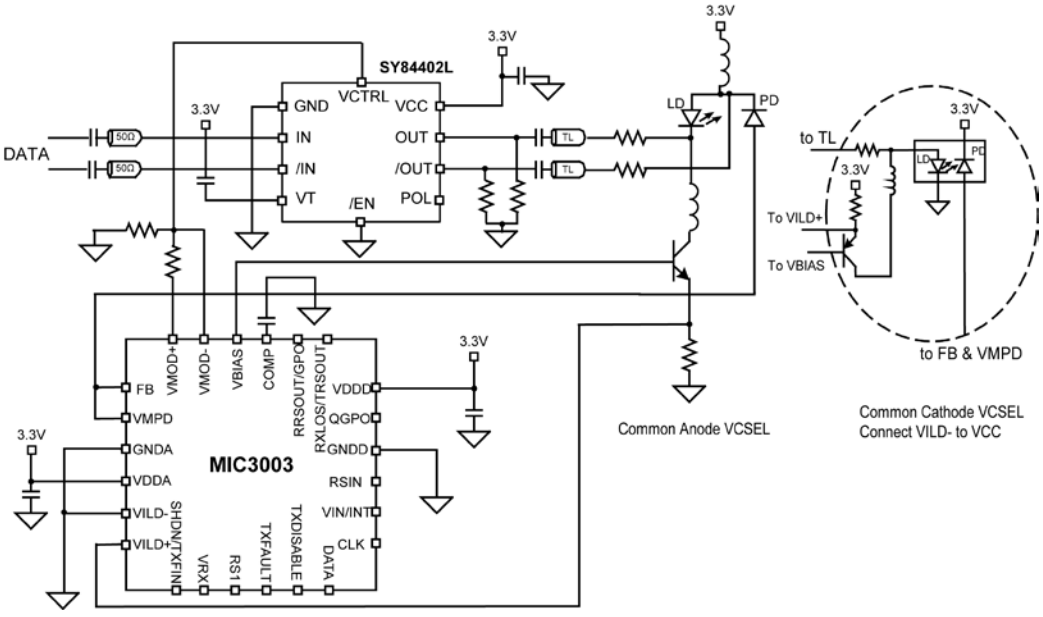
Features

- 3.3V power supply
- Operates from 100Mps up to 4.25Gbps
- 100k-compatible PECL/ECL I/O
- Guaranteed operation over –40°C to +85°C temperature range
- Fully controllable with Micrel MIC300X controller
- Available in ultra-small 10-pin MLF® (2mm x 2mm) package

Applications

- Multirate LAN, SAN applications up to 4.25Gbps: Ethernet, GbE, FC
- SFF, SFP Modules
- Backplane receiver

Typical Application



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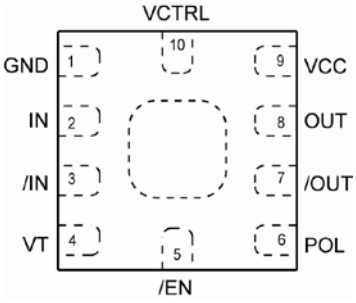
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY84402LMGTR(1)	MLF-10	Industrial	402L with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Pb-Free package is recommended for new designs.

Pin Configuration



10-Pin MLF® (2mm x 2mm) (MLF-10)

Pin Description

Pin Number	Pin Name	Pin Function
1	GND Exposed Pad	GND and Exposed pad must be tied to most negative supply. For LVPECL connect to ground.
2, 3	IN, /IN	Differential input. Both pins are internally terminated with 50Ω to VT. Refer to “Interface driver input to different logic drivers” section for more details.
4	VT	Reference Voltage. Refer to “Interface driver input to different logic drivers” section for proper termination.
5	/EN	Active Low TTL. The driver is enabled when this pin is unconnected or /EN asserted low. The driver is disabled when /EN is asserted high. Pulled down internally with 75kΩ resistor. The polarity of the output in disabled state is inverted when POL is exerted high. Refer to the truth table for details.
6	POL	TTL input, Pulled down internally with 75kΩ resistor. Asserting this pin high will invert output polarity of the input data. If this pin is asserted low or left open, the polarity is kept unchanged. Refer to the truth table for more details.
8, 7	OUT, /OUT	Differential Outputs: Variable swing PECL output pair defaults to undetermined state if inputs left open. See “Typical application” section for recommendations on terminations.
9	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
10	VCTRL	Control Voltage Input: Variable voltage input to control output swings with VCTRL = V_{CC} for minimum swing and VCTRL = V_{CC}-1.42V for maximum swing

Truth Table

IN	/IN	/EN	POL	OUT	/OUT
H	L	L	L	H	L
L	H	L	L	L	H
H	L	L	H	L	H
L	H	L	H	H	L
X	X	H	L	L	H
X	X	H	H	H	L

H: High L: Low X: Don’t care

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Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage ($|V_{CC}–GND|$) ..... 3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
MLF® (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF® (Ψ_{JB})
  Junction-to-Board ..... 32°C/W

DC Electrical Characteristics[4]

V_{CC} = +3.3V ±10%, T_A = –40°C to +85°C, and R_L = 50Ω to V_{CC} –2V unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Max V_{CC}, no load			50	mA
V_{OH}	Output HIGH Voltage		V_{CC} –1.145	V_{CC} –1.020	V_{CC} –0.895	V
V_{OL}	Output LOW Voltage	V_{CTRL} = V_{CC} – 1.42V	V_{CC} –1.945	V_{CC} -1.820	V_{CC} –1.695	V
V_{OPP}	Output swing	V_{CTRL} = V_{CC} – 1.42V		800		mV
		V_{CTRL} = V_{CC}		100		mV
V_{IH}	Input HIGH Voltage		V_{CC}–1.165		V_{CC}–0.880	V
V_{IL}	Input LOW Voltage		V_{CC}–1.945		V_{CC}–1.625	V
V_{IN}	Input Voltage Swing	Single ended	100		1700	mV_{PP}
$R_{IN(DATA)}$	Input Resistance at IN, /IN, Single Ended		45	50	55	Ω
VT	Reference Voltage			V_{CC} -1.32		V
VCMR	Common Mode Range	Note 5	V_{CC} –1.3		V_{CC}	V
V_{CTRL}	Output swing control voltage		V_{CC} –1.42		V_{CC}	V

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.
4. Specification for packaged product only.
5. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min.) and 1V.

AC Electrical Characteristics

V_{CC} = +3.3V ±10% and GND = 0V; T_A = –40°C to +85°C, R_L = 50Ω to V_{CC} –2V unless otherwise noted.

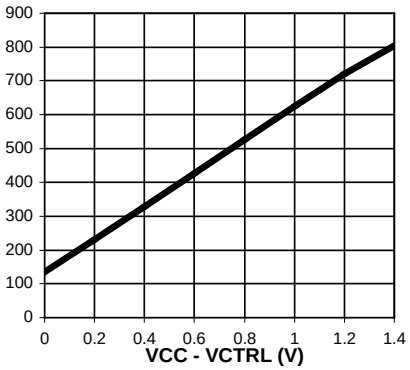
Symbol	Parameter	Condition	Min	Typ	Max	Units
	Maximum Data Rate	NRZ Data	4.25			Gbps
t_r, t_f	Output Rise/Fall Times (20% to 80%)	OUT, /OUT, Note 6	30	60	80	ps

Notes:

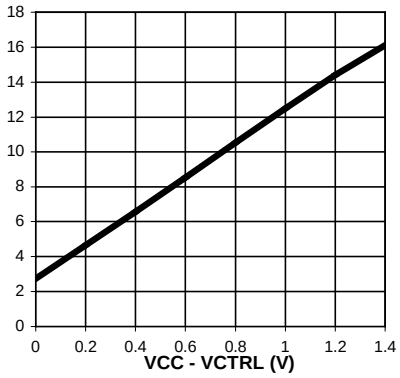
6. Output with VCTRL = V_{CC} – 1.42V.

Typical Characteristics

Typical Output Swing vs. VCTRL

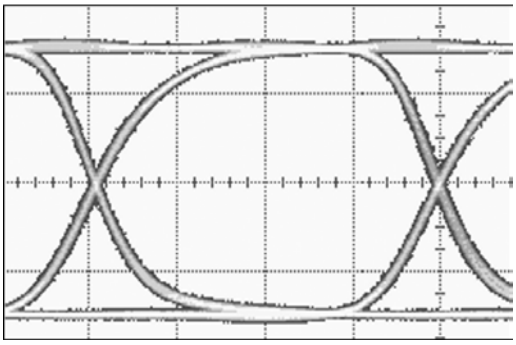


Typical Modulation Current in 50Ω Load

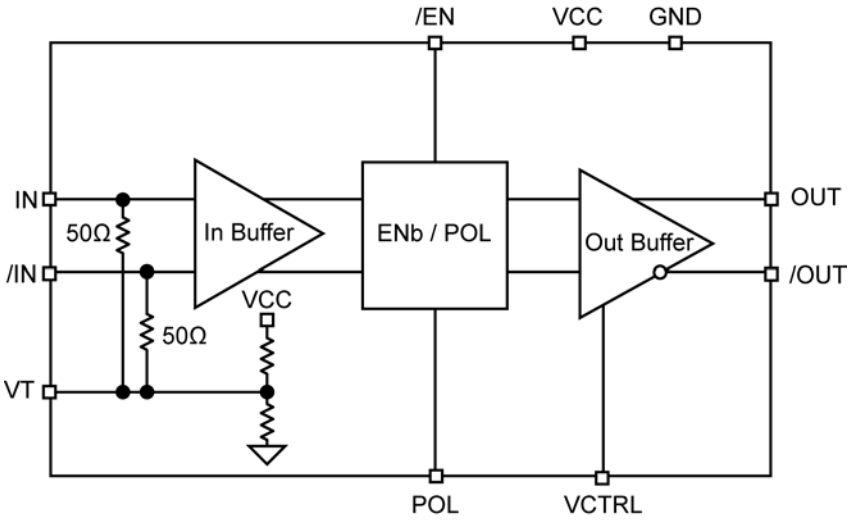


Functional Characteristics

Electrical Eye Diagram at 4.25Gbps, PRBS 2^7–1, R_L = 50Ω



Functional Block Diagram



Functional Description

As shown on the block diagram above, the driver is composed from an input buffer, Enable and polarity block, and output buffer. In order to accommodate VCSELs with different polarity and keep the data non inverted, the input data polarity can be inverted by setting pin 6 (POL) high. The modulation current into the VCSEL is determined by the ratio between the output voltage swing and the total load including VCSEL's equivalent resistance and any damping series resistor. The output signal amplitude is determined by the voltage applied at pin 10 (VCTRL) which should be within the range of VCC-1.42 to VCC.

Input and Output Stages

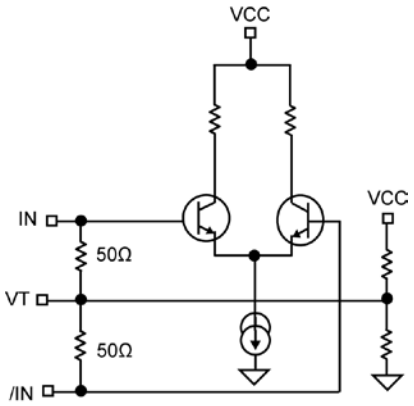


Figure 1a. Simplified Driver Input Stage

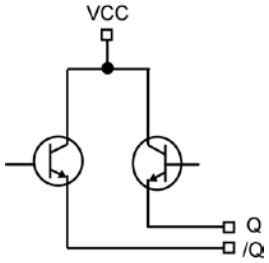


Figure 1b. Simplified Driver Output Stage

Interfacing Driver Input to Different Logic Drivers

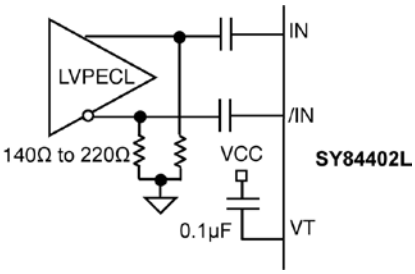


Figure 2a. AC-Coupled Input to LVPECL

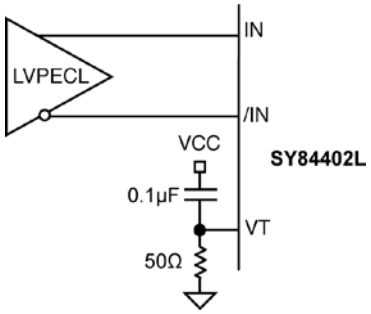


Figure 2b. DC-Coupled Input to LVPECL

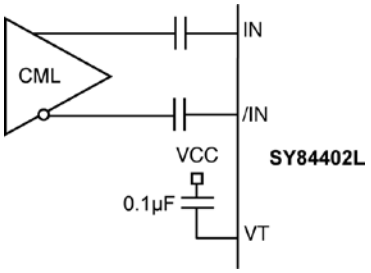


Figure 2c. AC-Coupled Input to CML

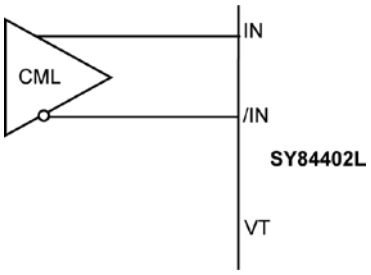


Figure 2d. DC-Coupled Input to CML

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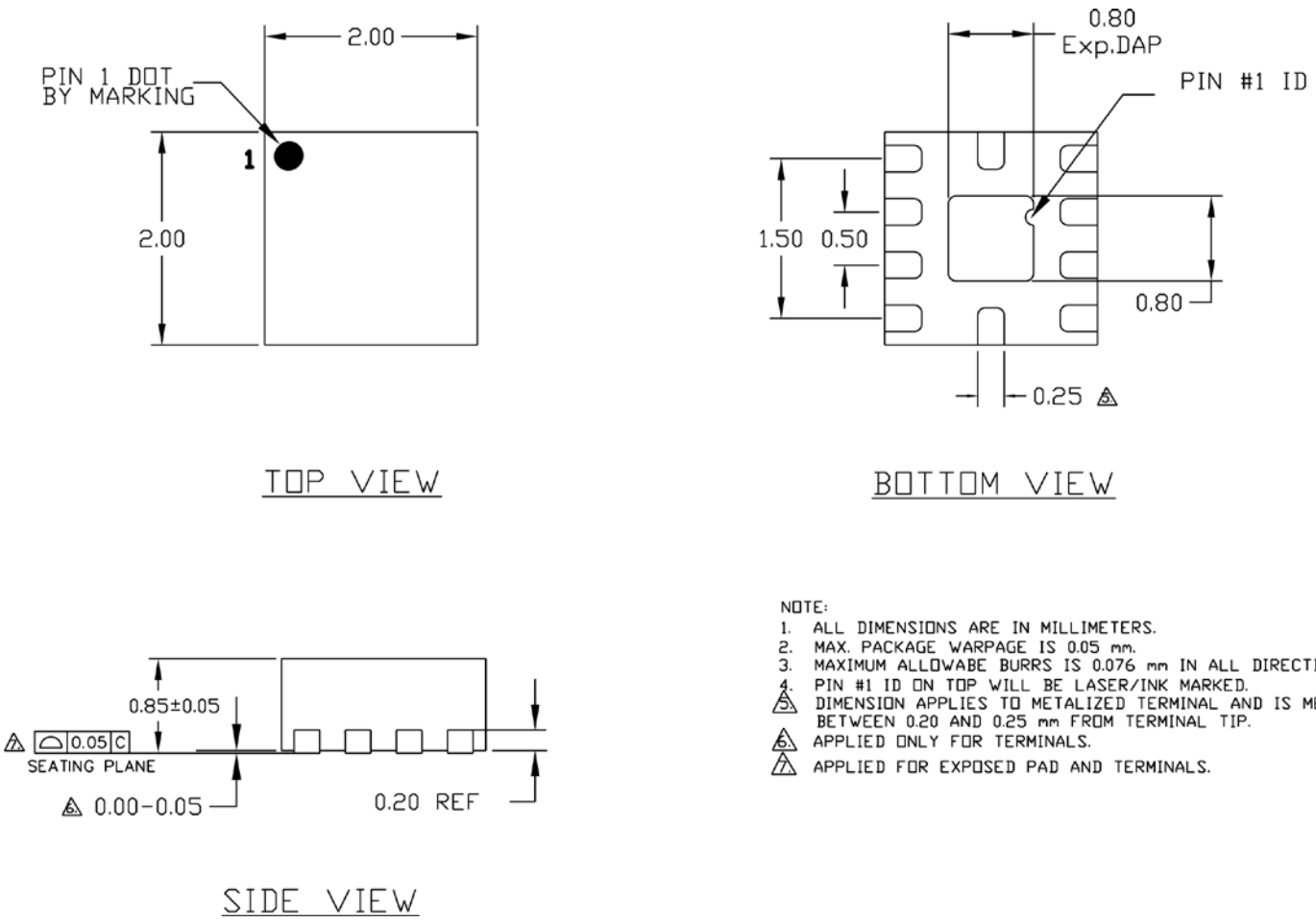
Package Information



10-Pin EPAD *Micro*LeadFrame® (MLF-10)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a plane equivalent to device GND for proper thermal management.

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