

CAT9554, CAT9554A

8-bit I²C and SMBus I/O Port with Interrupt

Description

The CAT9554 and CAT9554A are CMOS devices that provide 8-bit parallel input/output port expansion for I²C and SMBus compatible applications. These I/O expanders provide a simple solution in applications where additional I/Os are needed: sensors, power switches, LEDs, pushbuttons, and fans.

The CAT9554/9554A consist of an input port register, an output port register, a configuration register, a polarity inversion register and an I²C/SMBus-compatible serial interface.

Any of the eight I/Os can be configured as an input or output by writing to the configuration register. The system master can invert the CAT9554/9554A input data by writing to the active-high polarity inversion register.

The CAT9554/9554A features an active low interrupt output which indicates to the system master that an input state has changed.

The device's extended addressing capability allows up to 8 devices to share the same bus. The CAT9554A is identical to the CAT9554 except the fixed part of the I²C slave address is different. This allows up to 16 of devices (eight CAT9554 and eight CAT9554A) to be connected on the same bus.

Features

- 400 kHz I²C Bus Compatible (Note 1)
- 2.3 V to 5.5 V Operation
- Low Stand-by Current
- 5 V Tolerant I/Os
- 8 I/O Pins that Default to Inputs at Power-up
- High Drive Capability
- Individual I/O Configuration
- Polarity Inversion Register
- Active Low Interrupt Output
- Internal Power-on Reset
- No Glitch on Power-up
- Noise Filter on SDA/SCL Inputs
- Cascadable up to 8 Devices
- Industrial Temperature Range
- 16-lead SOIC and TSSOP, and 16-pad TQFN (4 x 4 mm) Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

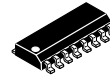
- White Goods (dishwashers, washing machines)
- Handheld Devices (cell phones, PDAs, digital cameras)
- Data Communications (routers, hubs and servers)

1. All I/Os are set to inputs at RESET.



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SOIC-16
W SUFFIX
CASE 751BG

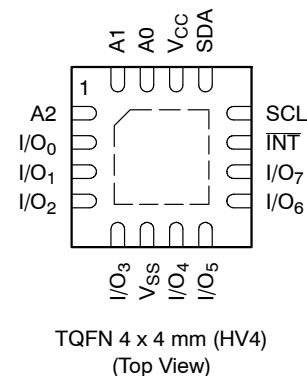
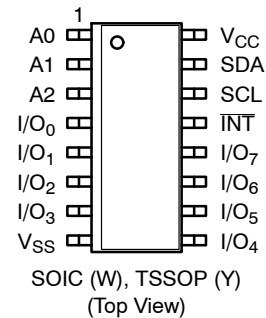


TQFN-16
HV4 SUFFIX
CASE 510AE



TSSOP-16
Y SUFFIX
CASE 948AN

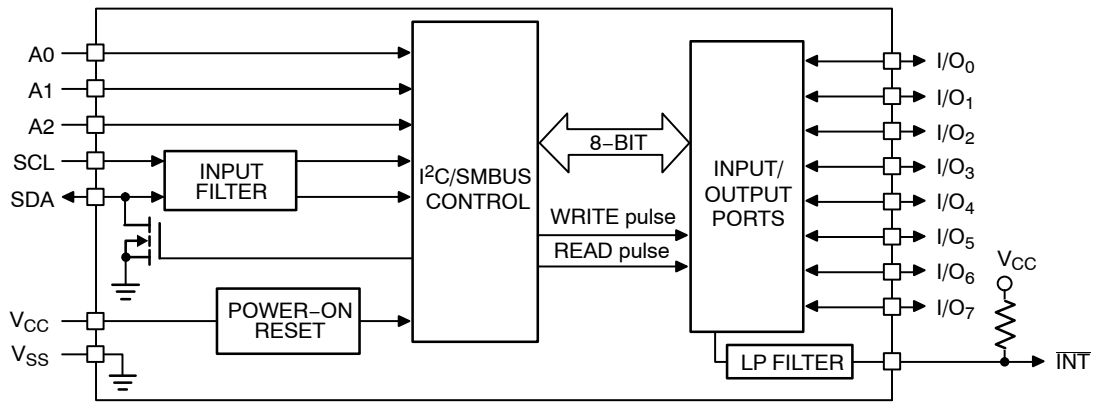
PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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Note: All I/Os are set to inputs at RESET.

Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

| SOIC / TSSOP | TQFN | Pin Name | Function |
|--------------|------|--------------------|--|
| 1 | 15 | A0 | Address Input 0 |
| 2 | 16 | A1 | Address Input 1 |
| 3 | 1 | A2 | Address Input 2 |
| 4–7 | 2–5 | I/O _{0–3} | Input/Output Port 0 to Input/Output Port 3 |
| 8 | 6 | V _{SS} | Ground |
| 9–12 | 7–10 | I/O _{4–7} | Input/Output Port 4 to Input/Output Port 7 |
| 13 | 11 | INT | Interrupt Output (open drain) |
| 14 | 12 | SCL | Serial Clock |
| 15 | 13 | SDA | Serial Data |
| 16 | 14 | V _{CC} | Power Supply |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameters | Ratings | Units |
|--|--------------|-------|
| V _{CC} with Respect to Ground | -0.5 to +6.5 | V |
| Voltage on Any Pin with Respect to Ground | -0.5 to +5.5 | V |
| DC Current on I/O ₀ to I/O ₇ | ±50 | mA |
| DC Input Current | ±20 | mA |
| V _{CC} Supply Current | 85 | mA |
| V _{SS} Supply Current | 100 | mA |
| Package Power Dissipation Capability (T _A = 25°C) | 1.0 | W |
| Junction Temperature | +150 | °C |
| Storage Temperature | -65 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Reference Test Method | Min | Units |
|-------------------------------|--------------------|------------------------|------|-------|
| V _{ZAP} (Note 2) | ESD Susceptibility | JEDEC Standard JESD 22 | 2000 | Volts |
| I _{LTH} (Notes 2, 3) | Latch-up | JEDEC Standard 17 | 100 | mA |

2. This parameter is tested initially and after a design or process change that affects the parameter.

3. Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to V_{CC} +1 V.

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Table 4. D.C. OPERATING CHARACTERISTICS ($V_{CC} = 2.3$ to 5.5 V; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------|---|-----|------|------|---------------|
| SUPPLIES | | | | | | |
| V_{CC} | Supply voltage | | 2.3 | – | 5.5 | V |
| I_{CC} | Supply current | Operating mode; $V_{CC} = 5.5$ V; no load; $f_{SCL} = 100$ kHz | – | 104 | 175 | μA |
| I_{stbl} | Standby current | Standby mode; $V_{CC} = 5.5$ V; no load; $V_I = V_{SS}$; $f_{SCL} = 0$ kHz; I/O = inputs | – | 550 | 700 | μA |
| I_{stbh} | Standby current | Standby mode; $V_{CC} = 5.5$ V; no load; $V_I = V_{CC}$; $f_{SCL} = 0$ kHz; I/O = inputs | – | 0.25 | 1 | μA |
| V_{POR} | Power-on reset voltage | No load; $V_I = V_{CC}$ or V_{SS} | – | 1.5 | 1.65 | V |

SCL, SDA, INT

| | | | | | | |
|-------------------|--------------------------|----------------------------|---------------------|---|---------------------|---------------|
| V_{IL} (Note 4) | Low level input voltage | | –0.5 | – | $0.3 \times V_{CC}$ | V |
| V_{IH} (Note 4) | High level input voltage | | $0.7 \times V_{CC}$ | – | 5.5 | V |
| I_{OL} | Low level output current | $V_{OL} = 0.4$ V | 3 | – | – | mA |
| I_L | Leakage current | $V_I = V_{CC}$ or V_{SS} | –1 | – | +1 | μA |
| C_I (Note 5) | Input capacitance | $V_I = V_{SS}$ | – | – | 6 | pF |
| C_O (Note 5) | Output capacitance | $V_O = V_{SS}$ | – | – | 8 | pF |

A0, A1, A2

| | | | | | | |
|-------------------|--------------------------|--|------|---|-----|---------------|
| V_{IL} (Note 4) | Low level input voltage | | –0.5 | – | 0.8 | V |
| V_{IH} (Note 4) | High level input voltage | | 2.0 | – | 5.5 | V |
| I_{LI} | Input leakage current | | –1 | – | 1 | μA |

I/Os

| | | | | | | |
|----------------|---------------------------|---|------|----|------|---------------|
| V_{IL} | Low level input voltage | | –0.5 | – | 0.8 | V |
| V_{IH} | High level input voltage | | 2.0 | – | 5.5 | V |
| I_{OL} | Low level output current | $V_{OL} = 0.5$ V; $V_{CC} = 2.3$ V (Note 6) | 8 | 10 | – | mA |
| | | $V_{OL} = 0.7$ V; $V_{CC} = 2.3$ V (Note 6) | 10 | 13 | – | mA |
| | | $V_{OL} = 0.5$ V; $V_{CC} = 4.5$ V (Note 6) | 8 | 17 | – | mA |
| | | $V_{OL} = 0.7$ V; $V_{CC} = 4.5$ V (Note 6) | 10 | 24 | – | mA |
| | | $V_{OL} = 0.5$ V; $V_{CC} = 3.0$ V (Note 6) | 8 | 14 | – | mA |
| | | $V_{OL} = 0.7$ V; $V_{CC} = 3.0$ V (Note 6) | 10 | 19 | – | mA |
| V_{OH} | High level output voltage | $I_{OH} = -8$ mA; $V_{CC} = 2.3$ V (Note 7) | 1.8 | – | – | V |
| | | $I_{OH} = -10$ mA; $V_{CC} = 2.3$ V (Note 7) | 1.7 | – | – | V |
| | | $I_{OH} = -8$ mA; $V_{CC} = 3.0$ V (Note 7) | 2.6 | – | – | V |
| | | $I_{OH} = -10$ mA; $V_{CC} = 3.0$ V (Note 7) | 2.5 | – | – | V |
| | | $I_{OH} = -8$ mA; $V_{CC} = 4.75$ V (Note 7) | 4.1 | – | – | V |
| | | $I_{OH} = -10$ mA; $V_{CC} = 4.75$ V (Note 7) | 4.0 | – | – | V |
| I_{IH} | Input leakage current | $V_{CC} = 3.6$ V; $V_I = V_{CC}$ | – | – | 1 | μA |
| I_{IL} | Input leakage current | $V_{CC} = 5.5$ V; $V_I = V_{SS}$ | – | – | –100 | μA |
| C_I (Note 5) | Input capacitance | | – | – | 5 | pF |
| C_O (Note 5) | Output capacitance | | – | – | 8 | pF |

4. $V_{IL \text{ min}}$ and $V_{IH \text{ max}}$ are reference values only and are not tested.

5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

6. The total current sunk by all I/Os must be limited to 100 mA and each I/O limited to 25 mA maximum.

7. The total current sourced by all I/Os must be limited to 85 mA.

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Table 5. A.C. CHARACTERISTICS ($V_{CC} = 2.3\text{ V to }5.5\text{ V}$; $T_A = -40^\circ\text{C to }+85^\circ\text{C}$, unless otherwise specified.) (Note 8)

| Symbol | Parameter | Standard I ² C | | Fast I ² C | | Units |
|---------------------------|--|---------------------------|------|-----------------------|-----|-------|
| | | Min | Max | Min | Max | |
| F _{SCL} | Clock Frequency | | 100 | | 400 | kHz |
| t _{HD:STA} | START Condition Hold Time | 4 | | 0.6 | | μs |
| t _{LOW} | Low Period of SCL Clock | 4.7 | | 1.3 | | μs |
| t _{HIGH} | High Period of SCL Clock | 4 | | 0.6 | | μs |
| t _{SU:STA} | START Condition Setup Time | 4.7 | | 0.6 | | μs |
| t _{HD:DAT} | Data In Hold Time | 0 | | 0 | | μs |
| t _{SU:DAT} | Data In Setup Time | 250 | | 100 | | ns |
| t _R (Note 9) | SDA and SCL Rise Time | | 1000 | | 300 | ns |
| t _F (Note 9) | SDA and SCL Fall Time | | 300 | | 300 | ns |
| t _{SU:STO} | STOP Condition Setup Time | 4 | | 0.6 | | μs |
| t _{BUF} (Note 9) | Bus Free Time Between STOP and START | 4.7 | | 1.3 | | μs |
| t _{AA} | SCL Low to Data Out Valid | | 3.5 | | 0.9 | μs |
| t _{DH} | Data Out Hold Time | 100 | | 50 | | ns |
| T _i (Note 9) | Noise Pulse Filtered at SCL and SDA Inputs | | 100 | | 100 | ns |

| Symbol | Parameter | Min | Max | Units |
|--------|-----------|-----|-----|-------|
|--------|-----------|-----|-----|-------|

PORT TIMING

| | | | | |
|-----------------|-----------------------|-----|-----|----|
| t _{PV} | Output Data Valid | | 200 | ns |
| t _{PS} | Input Data Setup Time | 100 | | ns |
| t _{PH} | Input Data Hold Time | 1 | | μs |

INTERRUPT TIMING

| | | | | |
|-----------------|-----------------|--|---|----|
| t _{IV} | Interrupt Valid | | 4 | μs |
| t _{IR} | Interrupt Reset | | 4 | μs |

8. Test conditions according to "AC Test Conditions" table.

9. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

Table 6. A.C. TEST CONDITIONS

| | |
|-----------------------------------|--|
| Input Rise and Fall time | ≤ 10 ns |
| CMOS Input Voltages | 0.2 V _{CC} to 0.8 V _{CC} |
| CMOS Input Reference Voltages | 0.3 V _{CC} to 0.7 V _{CC} |
| TTL Input Voltages | 0.4 V to 2.4 V |
| TTL Input Reference Voltages | 0.8 V, 2.0 V |
| Output Reference Voltages | 0.5 V _{CC} |
| Output Load: SDA, I ^{NT} | Current Source I _{OL} = 3 mA; C _L = 100 pF |
| Output Load: I/Os | Current Source: I _{OL} /I _{OH} = 10 mA; C _L = 50 pF |

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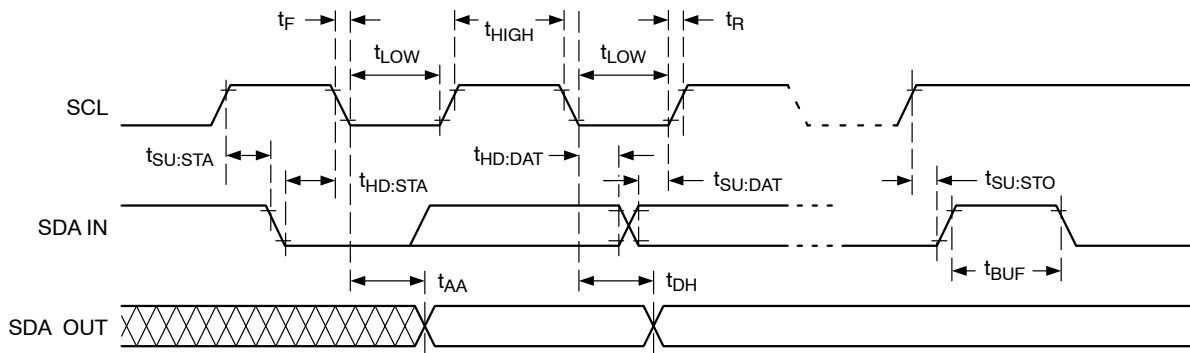


Figure 2. I²C Serial Interface Timing

Pin Description

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull-up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs. A pull-up resistor must be connected from SDA line to V_{CC}. The value of the pull-up resistor, R_P, can be calculated based on minimum and maximum values from Figure 3 and Figure 4 (see Note).

A0, A1, A2: Device Address Inputs

These inputs are used for extended addressing capability. The A0, A1, A2 pins should be hardwired to V_{CC} or V_{SS}. When hardwired, up to eight CAT9554/9554As may be addressed on a single bus system. The levels on these inputs are compared with corresponding bits, A2, A1, A0, from the slave address byte.

I/O₀ to I/O₇: Input / Output Ports

Any of these pins may be configured as input or output. The simplified schematic of I/O₀ to I/O₇ is shown in Figure 5. When an I/O is configured as an input, the Q1 and Q2 output transistors are off creating a high impedance input with a weak pull-up resistor (typical 100 kΩ). If the I/O pin is configured as an output, the push-pull output stage is enabled. Care should be taken if an external voltage is applied to an I/O pin configured as an output due to the low impedance paths that exist between the pin and either V_{CC} or V_{SS}.

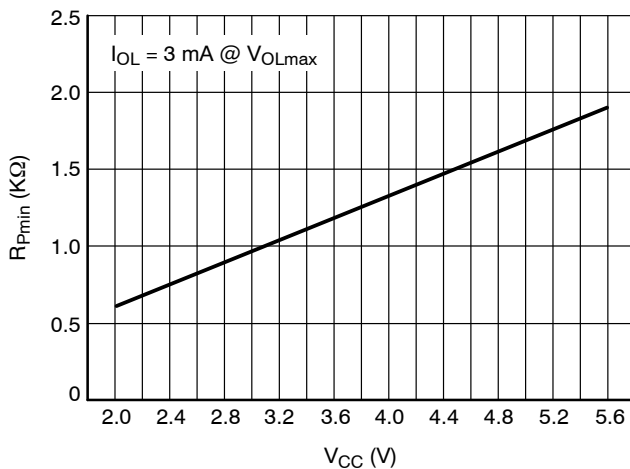


Figure 3. Minimum R_P Value vs. Supply Voltage

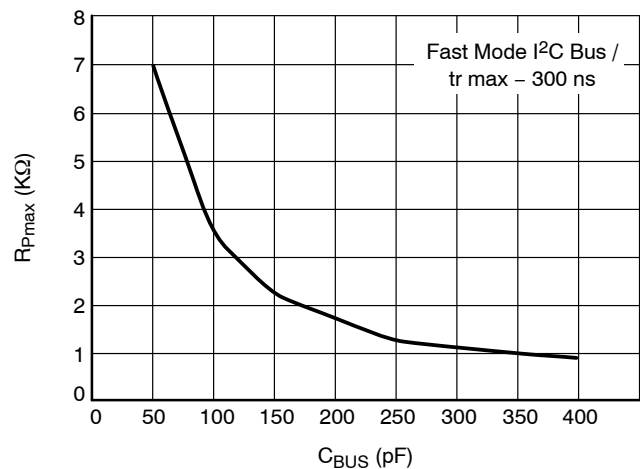


Figure 4. Maximum R_P Value vs. Bus Capacitance

NOTE: According to the Fast Mode I²C bus specification, for bus capacitance up to 200 pF, the pull up device can be a resistor. For bus loads between 200 pF and 400 pF, the pull-up device can be a current source (I_{max} = 3 mA) or a switched resistor circuit.

INT: Interrupt Output

The open-drain interrupt output is activated when one of the port pins configured as an input changes state (differs from the corresponding input port register bit state). The interrupt is deactivated when the input returns to its previous

state or the input port register is read. Changing an I/O from an output to an input may cause a false interrupt if the state of the pin does not match the contents of the input port register.

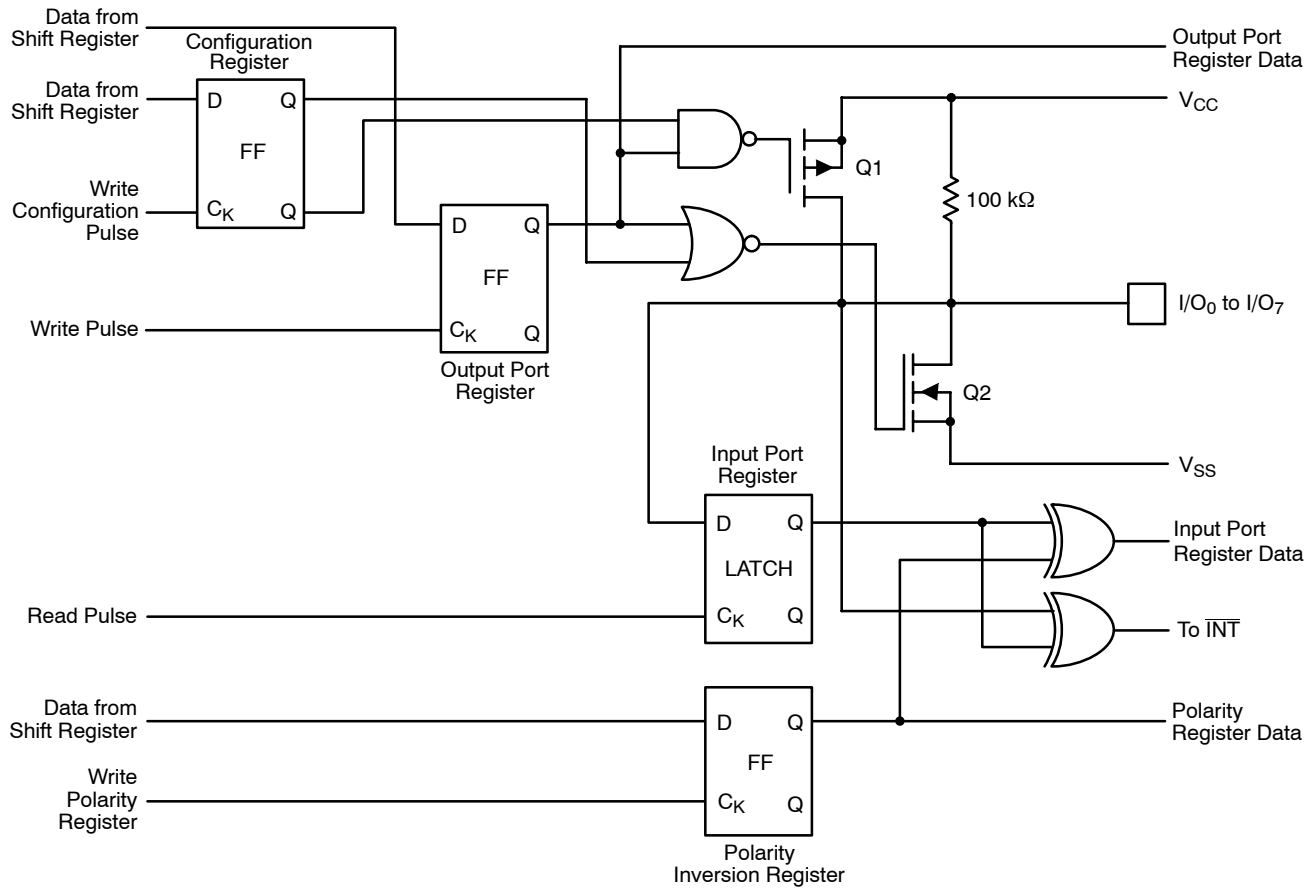


Figure 5. Simplified Schematic of I/O₀ to I/O₇

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Functional Description

The CAT9554 and CAT9554A general purpose input/output (GPIO) peripherals provide up to eight I/O ports, controlled through an I²C compatible serial interface.

The CAT9554/9554A support the I²C Bus data transmission protocol. This I²C Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9554/9554A operate as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I²C Bus Protocol

The features of the I²C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 6).

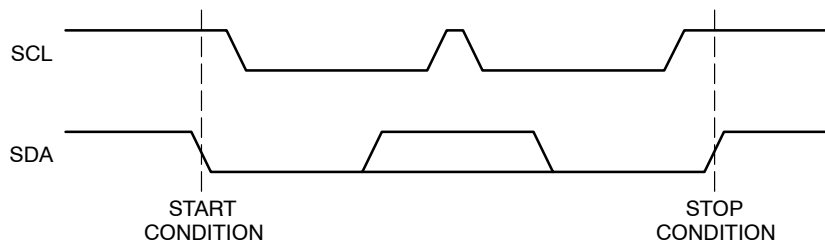


Figure 6. START/STOP Condition

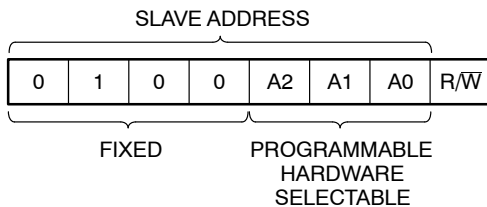


Figure 7. CAT9554 Slave Address

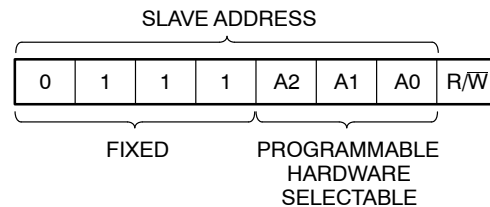


Figure 8. CAT9554A Slave Address

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9554/9554A monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9554/9554A for a read or write operation. The four most significant bits of the slave address are fixed as binary 0100 for the CAT9554 (Figure 7) and as 0111 for the CAT9554A (Figure 8). The CAT9554/9554A uses the next three bits as address bits.

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7-bit slave address is the R/W bit that specifies whether a read or write operation is to be performed. When this bit is set to "1", a read operation is initiated, and when set to "0", a write operation is selected.

Following the START condition and the slave address byte, the CAT9554/9554A monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9554/9554A then performs a read or a write operation depending on the state of the R/W bit.

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Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 6).

The CAT9554/9554A responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT9554/9554A begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9554/9554A will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a STOP condition to return the CAT9554/9554A to the standby power mode and place the device in a known state.

Registers and Bus Transactions

The CAT9554/9554A consist of an input port register, an output port register, a polarity inversion register and a configuration register. Table 7 shows the register address table. Tables 8 to 11 list Register 0 through Register 3 information.

Table 7. REGISTER COMMAND BYTE

| Command (hex) | Protocol | Function |
|---------------|-----------------|-----------------------------|
| 0x00 | Read byte | Input port register |
| 0x01 | Read/write byte | Output port register |
| 0x02 | Read/write byte | Polarity inversion register |
| 0x03 | Read/write byte | Configuration register |

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

Table 8. REGISTER 0 – INPUT PORT REGISTER

| bit | I ₇ | I ₆ | I ₅ | I ₄ | I ₃ | I ₂ | I ₁ | I ₀ |
|---------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 9. REGISTER 1 – OUTPUT PORT REGISTER

| bit | O ₇ | O ₆ | O ₅ | O ₄ | O ₃ | O ₂ | O ₁ | O ₀ |
|---------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 10. REGISTER 2 – POLARITY INVERSION REGISTER

| bit | N ₇ | N ₆ | N ₅ | N ₄ | N ₃ | N ₂ | N ₁ | N ₀ |
|---------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 11. REGISTER 3 – CONFIGURATION REGISTER

| bit | C ₇ | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ |
|---------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

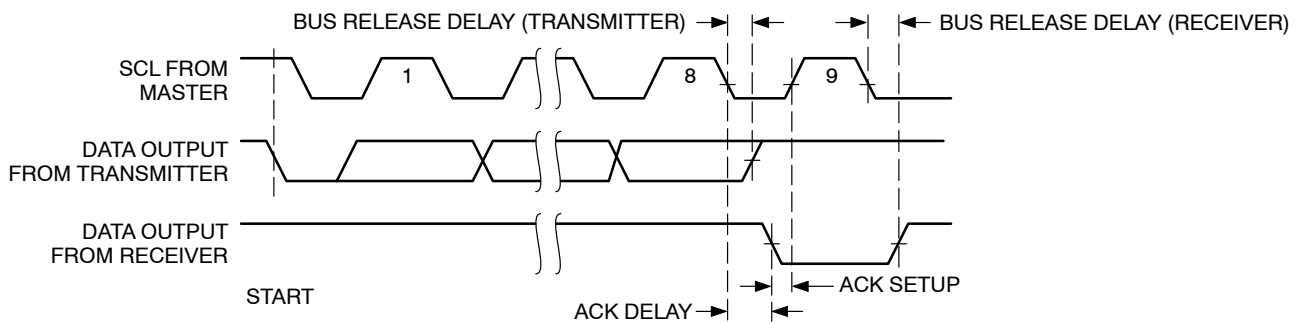


Figure 9. Acknowledge Timing

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The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip-flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register is set ("1") the corresponding input port data is inverted. If a bit in the polarity inversion register is cleared ("0"), the original input port polarity is retained.

The configuration register sets the directions of the ports. Set the bit in the configuration register to enable the

corresponding port pin as an input with a high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At power-up, the I/Os are configured as inputs with a weak pull-up resistor to V_{CC} .

Data is transmitted to the CAT9554/9554A registers using the write mode shown in Figure 10 and Figure 11.

The CAT9554/9554A registers are read according to the timing diagrams shown in Figure 12 and Figure 13. Once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte will be sent.

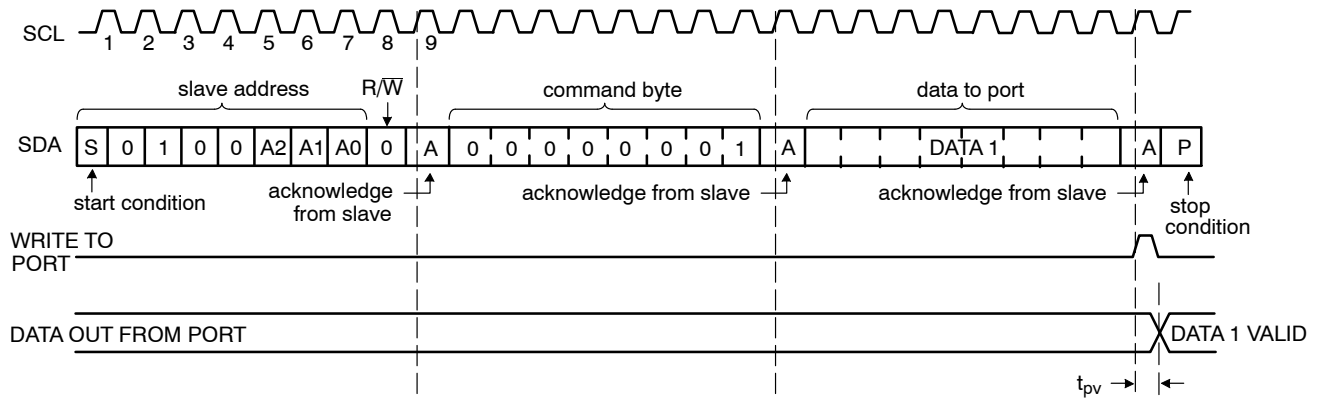


Figure 10. Write to Output Port Register

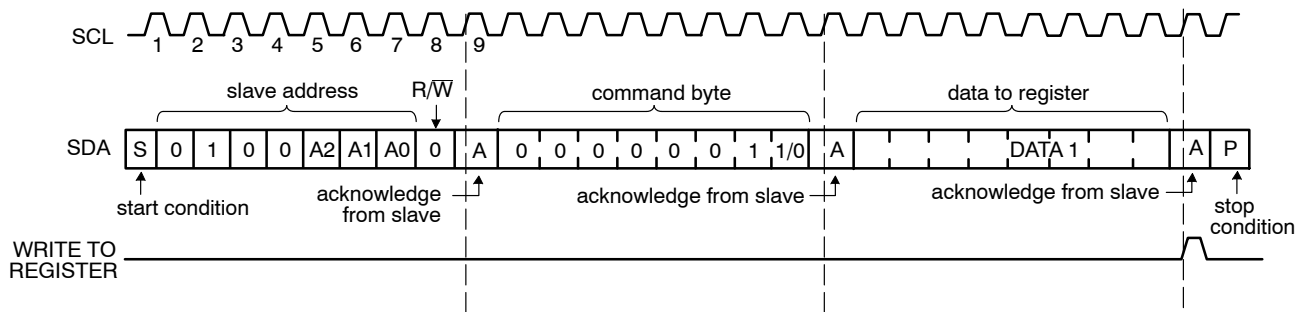


Figure 11. Write to Configuration or Polarity Inversion Register

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Power-On Reset Operation

When the power supply is applied to V_{CC} pin, an internal power-on reset pulse holds the CAT9554/9554A in a reset state until V_{CC} reaches V_{POR} level. At this point, the reset

condition is released and the internal state machine and the CAT9554/9554A registers are initialized to their default state.

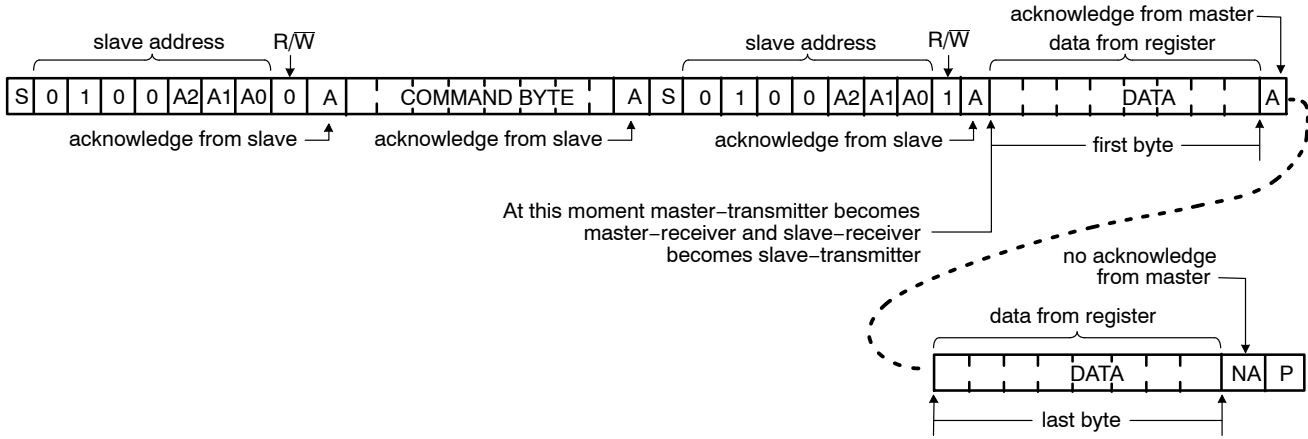


Figure 12. Read from Register

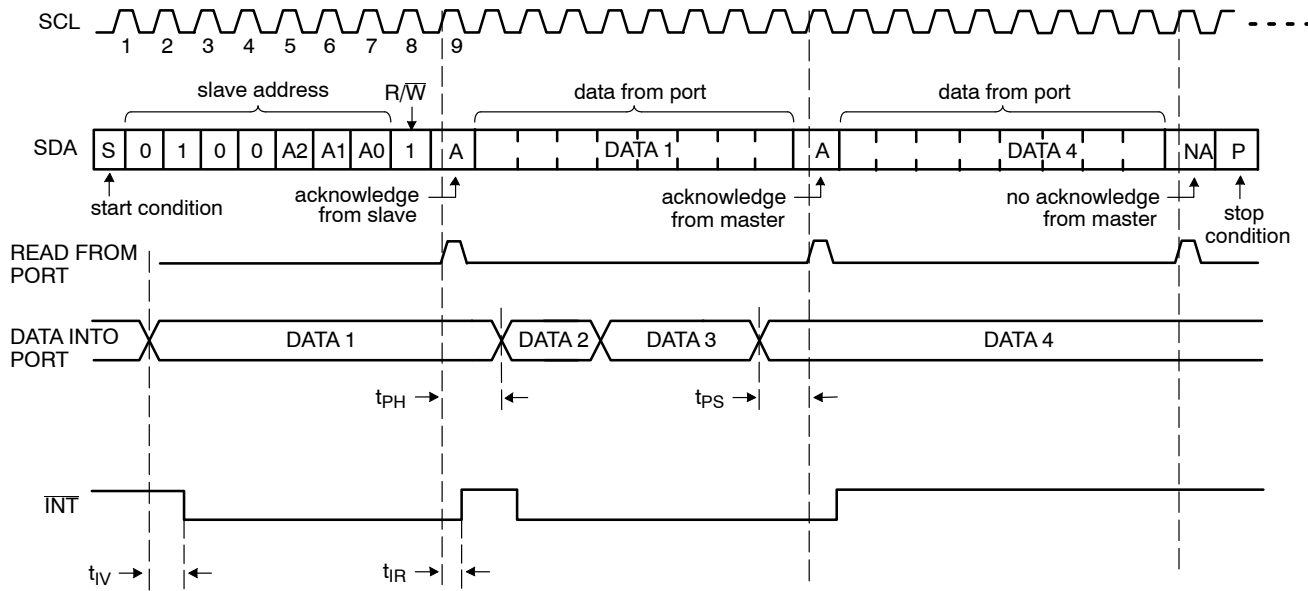
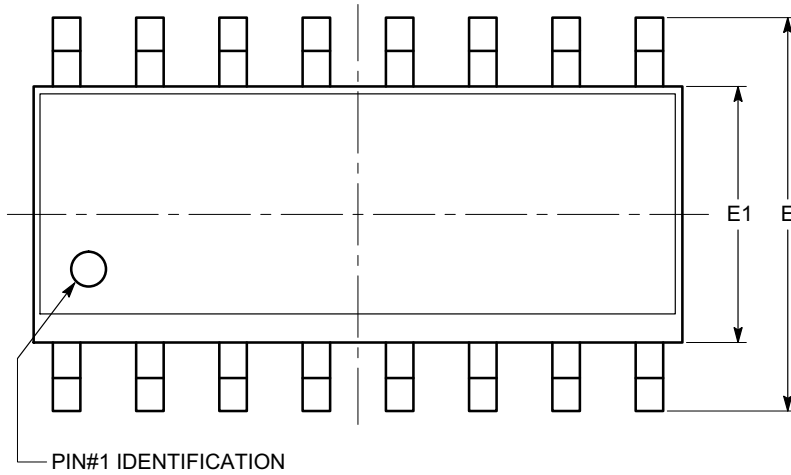


Figure 13. Read Input Port Register

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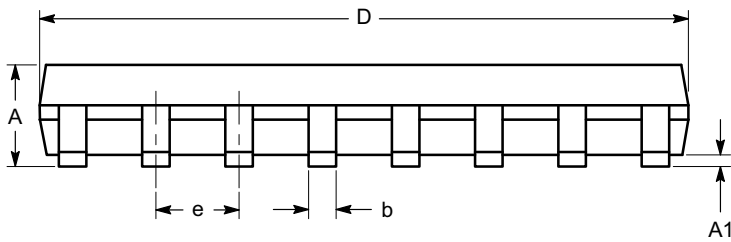
PACKAGE DIMENSIONS

SOIC-16, 150 mils
CASE 751BG-01
ISSUE O

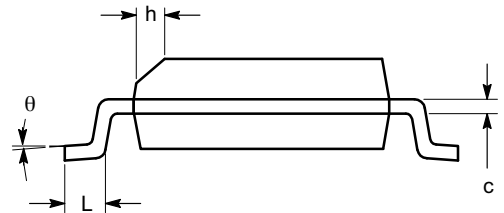


| SYMBOL | MIN | NOM | MAX |
|----------|----------|------|-------|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 9.80 | 9.90 | 10.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0° | | 8° |

TOP VIEW



SIDE VIEW



END VIEW

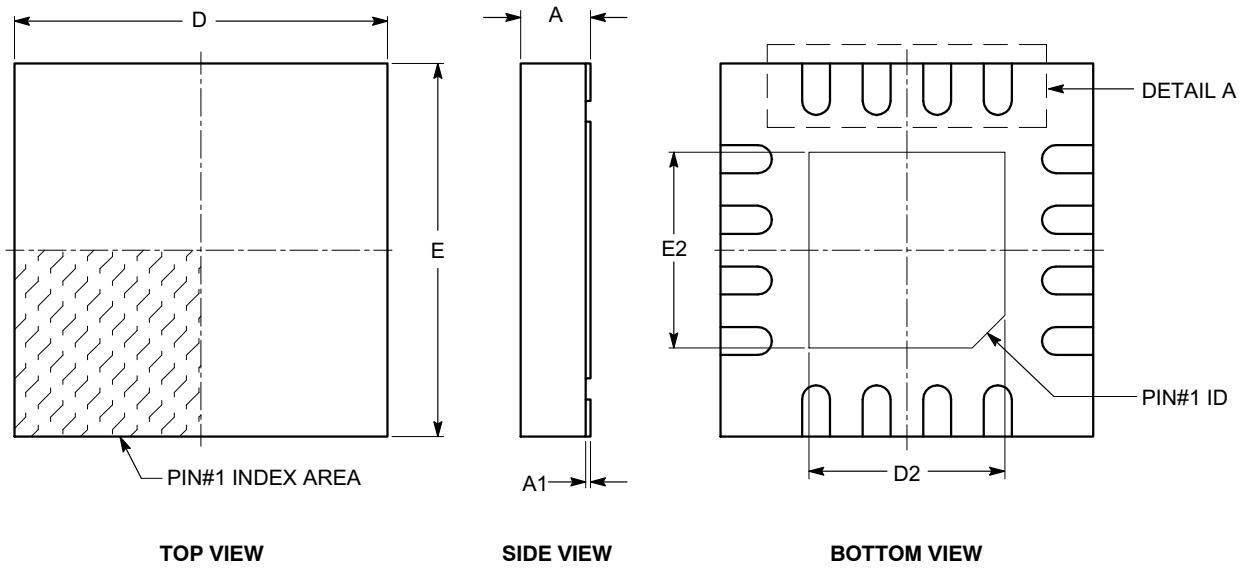
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

CAT9554, CAT9554A

PACKAGE DIMENSIONS

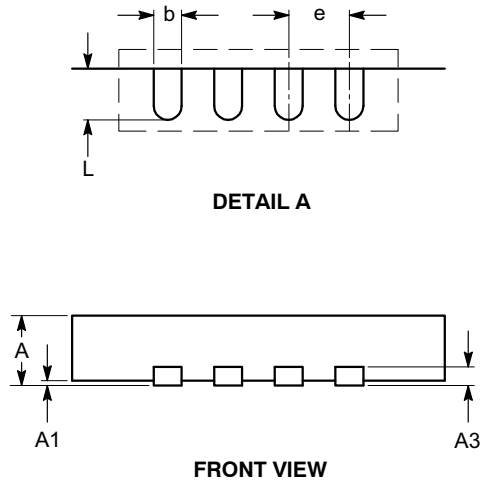
TQFN16, 4x4
CASE 510AE-01
ISSUE A



| SYMBOL | MIN | NOM | MAX |
|--------|----------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.00 | --- | 2.25 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.00 | --- | 2.25 |
| e | 0.65 BSC | | |
| L | 0.45 | --- | 0.65 |

Notes:

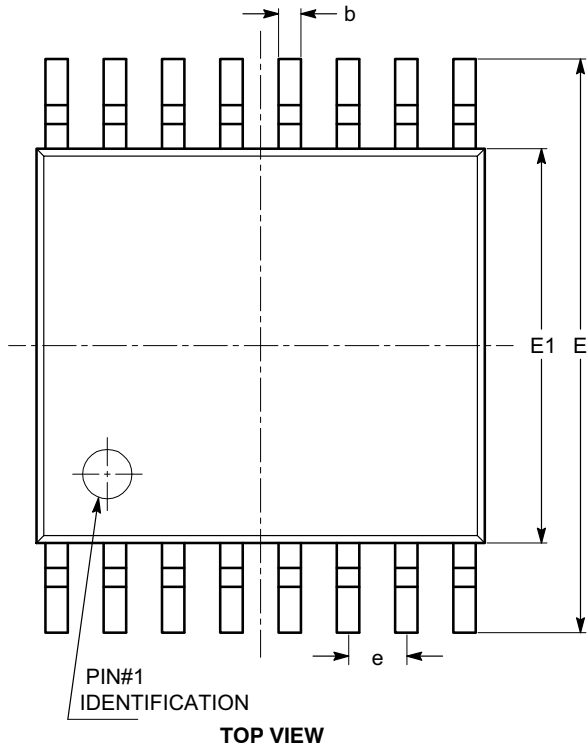
- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-220.



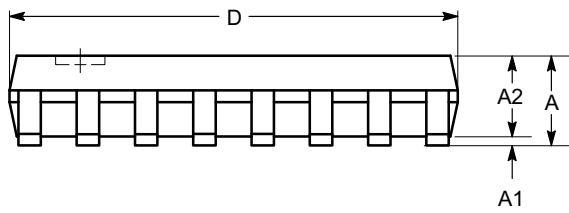
CAT9554, CAT9554A

PACKAGE DIMENSIONS

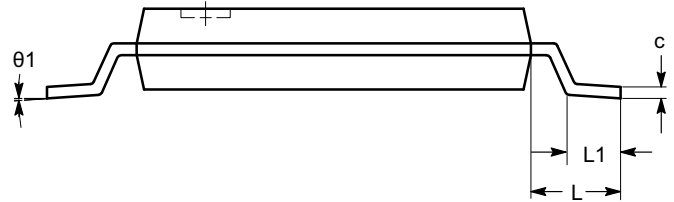
TSSOP16, 4.4x5
CASE 948AN-01
ISSUE O



| SYMBOL | MIN | NOM | MAX |
|----------|----------|-----|------|
| A | | | 1.10 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.85 | | 0.95 |
| b | 0.19 | | 0.30 |
| c | 0.13 | | 0.20 |
| D | 4.90 | | 5.10 |
| E | 6.30 | | 6.50 |
| E1 | 4.30 | | 4.50 |
| e | 0.65 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.45 | | 0.75 |
| θ | 0° | | 8° |



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

CAT9554, CAT9554A

Example of Ordering Information (Note 12)

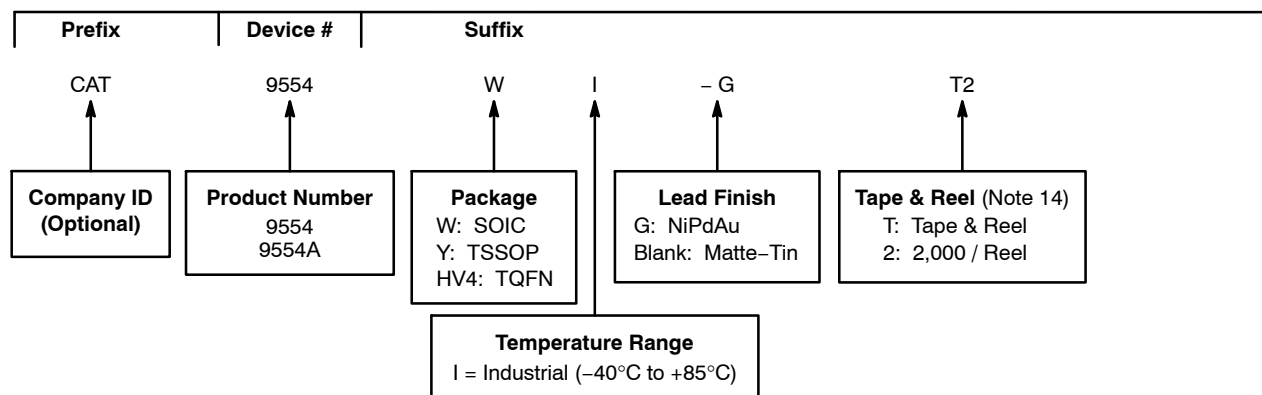


Table 12. ORDERING INFORMATION

| Part Number | Package | Lead Finish |
|------------------|---------|-------------|
| CAT9554WI-G | SOIC | NiPdAu |
| CAT9554WI-GT2 | SOIC | NiPdAu |
| CAT9554YI-G | TSSOP | NiPdAu |
| CAT9554YI-GT2 | TSSOP | NiPdAu |
| CAT9554HV4I-G | TQFN | NiPdAu |
| CAT9554HV4I-GT2 | TQFN | NiPdAu |
| CAT9554AWI-G | SOIC | NiPdAu |
| CAT9554AWI-GT2 | SOIC | NiPdAu |
| CAT9554AYI-G | TSSOP | NiPdAu |
| CAT9554AYI-GT2 | TSSOP | NiPdAu |
| CAT9554AHV4I-G | TQFN | NiPdAu |
| CAT9554AHV4I-GT2 | TQFN | NiPdAu |

10. All packages are RoHS-compliant (Lead-free, Halogen-free).


11. The standard lead finish is NiPdAu.

12. The device used in the above example is a CAT9554WI-GT2 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel, 2,000/Reel).

13. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

14. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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