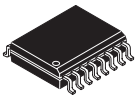
Document Number: MC33094
Rev. 1.0, 10/2006

Ignition Control

33094

IGNITION CONTROL



DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42567B
16-PIN SOICW

Designed for automotive ignition applications in 12 V systems, the 33094 provides outstanding control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing these devices for ignition coil control exhibit exceptional fuel efficiency and low exhaust emissions. The device is designed to be controlled from a single–ended Hall Sensor input. The circuit is built using high–density Integrated–Injection Logic (IIL) processing incorporating high current–gain PNP and NPN transistors.

The 33094 is packaged in an economical surface mount package and specified over an ambient temperature of –40°C to 125°C with a maximum junction temperature of 150°C.

Features

- External Capacitors Program the Device's Timing Characteristics
- Overvoltage Shutdown Protection
- Auto Start–Up Capability After Overvoltage Condition Ceases
- Allows for Push Start–Up in Automotive Applications
- Ignition Coil Current Limiting
- Ignition Coil Voltage Limiting
- Band Gap Reference for Enhanced Stability Over Temperature
- Negative Edge Filter for Hall Sensor Input Transient Protection
- Hall Sensor Inputs for RPM and Position Sensing
- Pb-Free Packaging Designated by Suffix Code EG

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33094DW/R2	-40°C to 125°C	16 SOICW
MCZ33094EG/R2		

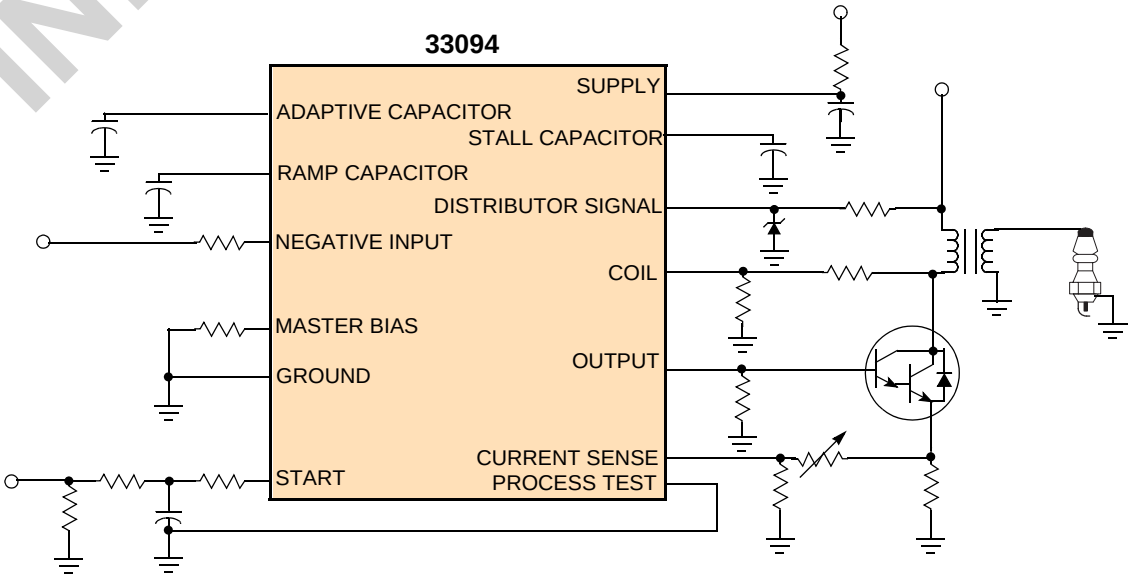


Figure 1. 33094 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

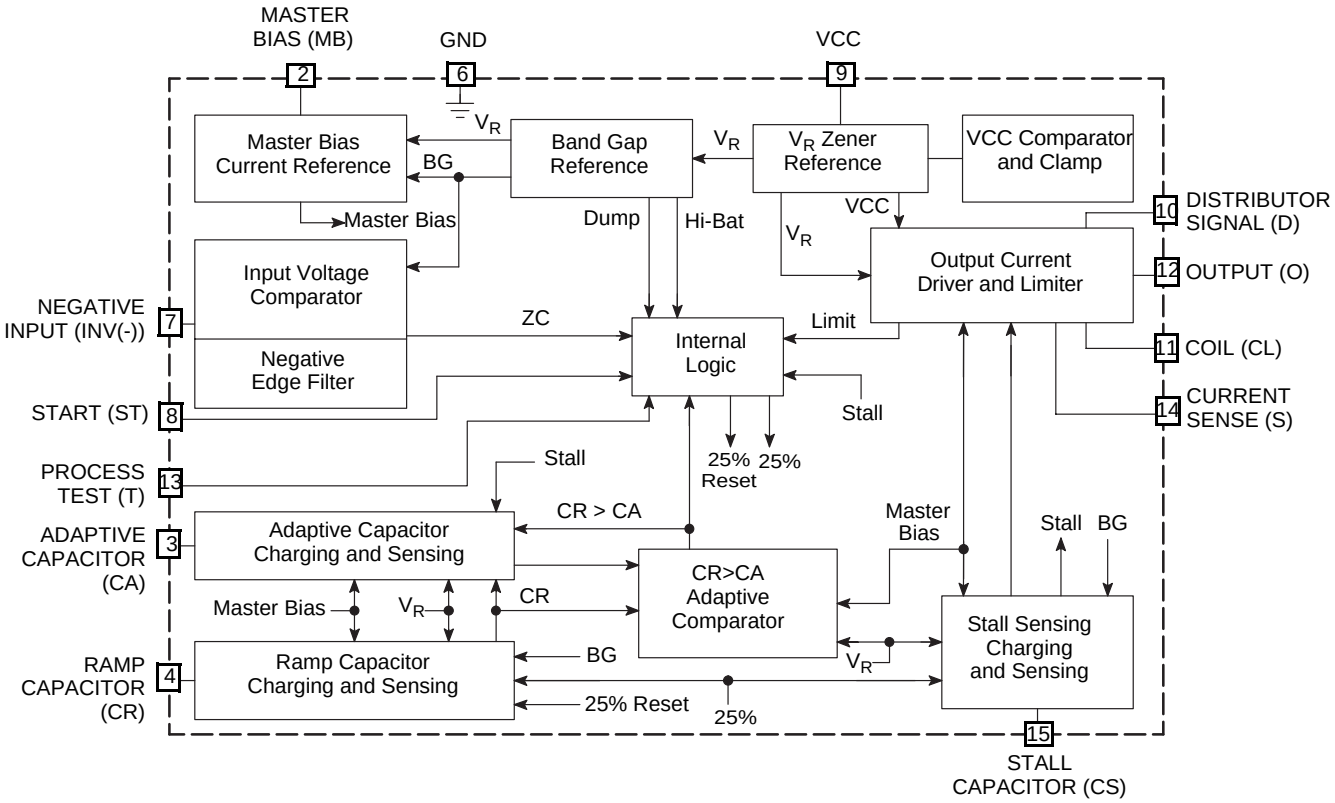


Figure 2. 33094 Simplified Internal Block Diagram

PIN CONNECTIONS

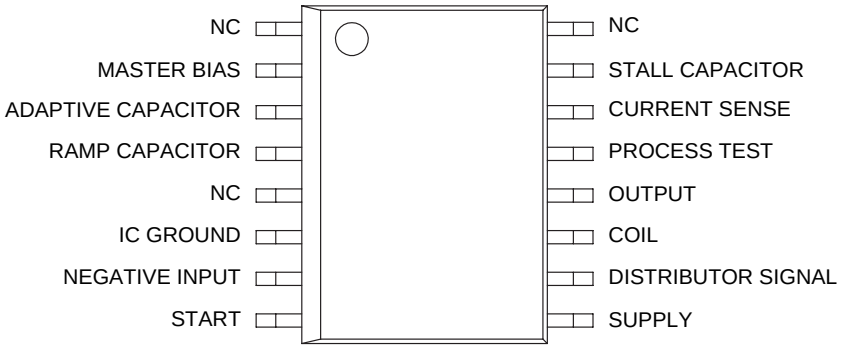


Figure 3. 33094 Pin Connections

Table 1. 33094 Pin Definitions

Pin Number	Pin Name	Formal Name	Definition
1, 5, 16	NC	No Connect	No Connection to the circuit
2	MB	Master Bias	Internal bias circuit set pin - ext. resistor
3	CA	Adaptive Capacitor	Manages dwell timing - ext. capacitor
4	CR	Ramp Capacitor	Manages dwell timing - ext. capacitor
6	GND	IC Ground	Supply ground
7	VIN(-)	Negative Input	Distributor signal from a sensor
8	ST	Start	Start/Run mode input
9	VCC	Supply	Supply voltage (battery, ingition ON)
10	D	Distributor Signal	Monitor for the battery side of the spart coil
11	CL	Coil	Sparl coil voltage monitor
12	O	Output	Supplies base current to the ext. Darlington transnsior
13	T	Process Test	Used to measure internal functions
14	S	Current Sense	Spark coil current sensing input
15	CS	Stall Capacitor	Controls spark coil current - ext. capacitor

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage	V_{CC}	28.6	V
Operating Frequency Range	f_{OP}	1.0 to 400	Hz
THERMAL RATINGS			
Junction Temperature	T_J	150	°C
Operating Temperature Continuous Limited	T_A	 -30 to 105 -40 to 125	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Peak Package Reflow Temperature During Reflow (2), (3)	T_{PPRT}	Note 3	°C
THERMAL RESISTANCE			
Thermal Resistance	$R_{\theta JA}$	97	°C/W

Notes

1. ESD data is available upon request.
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{D} = V_{CC} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY AND MASTER BIAS					
Supply Current (V_{CC} = 16V, $V_{IN(-)}$ = 0V, V_D = 3.0V, V_{CA} = V_{CR} = V_{CS} = V_{ST} = Open) (4)	I_{CC}	5.0	8.4	18	mA
Overvoltage Shutdown ($V_{IN(-)}$ = 0V, V_{CA} = Open, V_{CS} = 3.0V, V_{ST} = 28V) (5)	V_{CC3}	23.7	27.5	31	V
Start-V_{CC} Latch ($V_{IN(-)}$ = 0V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 25V, V_D = 14V I_{ST} = 40mA)	V_{CC5}	8.0	16.1	–	V
Adaptive Dwell High Supply Voltage ($V_{IN(-)}$ = 11V, V_{CA} = Open, V_{CR} = 3.0V, V_{CS} = 3.0V, V_{ST} = 6.0V, V_D = 13V)					V
Threshold (6)	V_{CC1}	16.5	18.9	19.5	
Hysteresis (7)	$V_{CC2\ (HYS)}$	0.2	0.5	0.8	
Master Bias Voltage (V_{CC} = 16V, $V_{IN(-)}$ = 0V, V_D = 3.0V, V_{CA} = V_{CR} = V_{CS} = V_{ST} = Open) (8)	V_{MB}	1.12	1.2	1.32	V
INPUTS					
Input Positive Threshold Voltage (V_{CC} = 6.0V, V_{CA} = V_{CR} = Open, V_{CS} = 1.0V, V_{ST} = 6.0V) (9)	$V_{IN(-)(TH)A}$	50	54	65	%V_{CC}
Input Positive Threshold Voltage (V_{CC} = 16V, V_{CA} = V_{CR} = Open, V_{CS} = 1.0V, V_{ST} = 10V) (10)	$V_{IN(-)(TH)B}$	50	54	65	%V_{CC}
Input Hysteresis (V_{CC} = 6.0V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 6.0V) (11)	$V_{IN(-)(HYS)A}$	0.6	0.72	1.2	V
Input Hysteresis (V_{CC} = 16V, V_D = 3.0V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 10V) (12)	$V_{IN(-)(HYS)B}$	1.6	2.23	3.2	V
Input Impedance (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_D = 3.0V, V_{CA} = V_{CR} = V_{CS} = V_{ST} = Open) (13)	Z_I	70	94	250	kΩ

Notes

4. Current sourced into Supply pin.
5. Ramp up V_{CC} from 24 to 31V in 0.1 increments and note the supply voltage, V_{CC}, which causes V_O to fall below 1.0V.
6. Ramp up V_{CC} from 14 to 20V in 0.1 increments and measure V_{CC}, when ICA ≤ 2.0 μA.
7. Ramp down V_{CC} from 20 to 14V and measure V_{CC}, when ICA ≥ 2.0 μA and compute hysteresis difference from V_{CC1}.
8. Voltage measured at Master Bias pin.
9. Ramp up $V_{IN(-)}$ from 1.0 to 5.0V in 0.1 increments. Record $V_{IN(-)}$ when I_{CR} goes positive and convert to % of V_{CC} by dividing by V_{CC}.
10. Ramp up $V_{IN(-)}$ from 3.0 to 10V in 0.1 increments. Record $V_{IN(-)}$ when I_{CR} goes positive and convert to % of V_{CC} by dividing by V_{CC}.
11. Ramp up $V_{IN(-)}$ from $V_{IN(-)(TH)A}$ in 0.1 increments. Record $V_{IN(-)}$ when I_{CR} goes positive. $V_{IN(-)(HYS)A}$ = $V_{IN(-)(TH)A}$ - ($V_{IN(-)}$).
12. Ramp up $V_{IN(-)}$ from $V_{IN(-)(TH)B}$ in 0.1 increments. Record $V_{IN(-)}$ when I_{CR} goes positive. $V_{IN(-)(HYS)B}$ = $V_{IN(-)(TH)B}$ - ($V_{IN(-)}$).
13. Measure $I_{IN(-)}$ into Pin 7; Z_I = 10 V/$I_{IN(-)}$.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{D} = V_{CC} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT AND DWELL					
Output Current ($V_{IN(-)}$ = 0V, V_{CA} = V_{CR} = Open, V_{CS} = 3.0V, V_{ST} = 10V, V_O = 2.1V) (14)					mA
Normal Condition (V_{CC} = 14V, V_D = 6.0V)	I_{O1}	40	52	65	
High Voltage Condition (V_{CC} = 14V, V_D = 22V)	I_{O2}	40	52	65	
Output Leakage Current (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 10V, V_S = 0V, V_D = 18V, V_O = 0V) (15)	I_{O3}	1.0	-1.33	100	µA
Output Clamp Voltage (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 10V, V_D = 14V, V_O = 0V, V_{CL} = 20V, I_{CL} = 10mA) (16)	V_{CL}	13.7	14.52	15.58	V
Output Clamp Dynamic Impedance (VCC = 14V, $V_{IN(-)}$ = 10V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 10V, V_D = 14V, V_O = 0V, I_{CL} = 12mA, ΔI_{CL} = 2.0mA) (17)	Z_{CL}	10	37	75	Ω
Dwell (18)					%
Normal Condition: D1 = (I_{CA2}/I_{CA1}) x CR Data from I_{CA2}, I_{CA1}, and CR characteristics	D1	14.5	17.6	20.5	
High Voltage Condition: D2 = (I_{CA3}/I_{CA1}) x CR Data from I_{CA3}, I_{CA1}, and CR characteristics	D2	4.1	5.3	5.9	
Adaptive Dwell Logic, Ramp Threshold (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_{CA} = V_{CS} = Open, V_{ST} = 0V, V_S = 0V, V_D = 10V) (14)	V_{CRO}	-60	0	60	mV
Soft Shutdown Voltage (V_{CC} = 6.0V, $V_{IN(-)}$ = 10V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 0V) Measure V_S	V_{SS}	0	1.48	16.7	mV

Notes

14. Capability measured by forcing the Output to 2.0V with the Current Sense pin (S) open while measuring the Output current to ground.
15. Measured by clamping the output voltage with the S pin to ground, then increasing the V_D from 6.0 to 18V and measuring output leakage current to ground.
16. Output Clamp voltage with reference to ground while forcing 10mA into the Coil pin (CL).
17. Output Clamp impedance measured with I_{CL} = 11 ±1.0mA into the Coil pin (CL) and noting the corresponding Output Clamp Voltage change (Z_{CL} = $\Delta V_{CL}/\Delta I_{CL}$).
18. Dwell is defined as Run Mode Down Current divided by the Run Mode Up Current times the Ramp Control Current Ratio and is calculated from other measured characteristics as defined above.
19. Set the V_{CR} (ramp Capacitor) voltage to 1.5V; Ramp V_{CR} voltage from 1.8 to 2.2V in 0.02V increments and note the Ramp voltage (V_{CR}) which causes the Output voltage to go > 1.0V; V_{CRO} = 2.0V - V_{CR}.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_D = V_{CC} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ADAPTIVE CAPACITOR					
Run Mode, Adaptive, Charge Current (VCC = 6.0V, $V_{IN(-)}$ = 5.0V, V_{CA} = Open, V_{CR} = 3.0V, V_{CS} = 3.0V, V_{ST} = 6.0V) (20)	I_{CA1}	-7.91	-6.53	-5.62	µA
Run Mode, Adaptive Capacitor, Discharge Current (V_{CA} = Open, V_{CR} = 3.0V, V_{CS} = 3.0V, V_{ST} = 6.0V)					µA
Normal Condition (V_{CC} = 6.0V, $V_{IN(-)}$ = 10V)	I_{CA2}	3.7	4.77	5.63	
High Voltage Condition (V_{CC} = 22V, $V_{IN(-)}$ = 17V, V_D = 13V)	I_{CA3}	1.05	1.43	1.82	
Start Mode, Adaptive Capacitor Currents (V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 10V)					µA
Charge Current (V_{CC} = 5.0V, $V_{IN(-)}$ = 10V) (21)	I_{CA4}	-112	-87	-80	
Discharge Current (V_{CC} = 6.0V, $V_{IN(-)}$ = 0V) (22)	I_{CA5}	67.6	89.4	109	
Start Mode, Adaptive Capacitor, Clamp Voltage (V_{CC} = 6.0V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 10V)					V
High Clamp Voltage ($V_{IN(-)}$ = 10V)	V_{CA1}	2.23	2.30	2,65	
Low clamp Voltage ($V_{IN(-)}$ = 0V)	V_{CA2}	0.95	1.1	1.26	
Adaptive Gain (V_{CC} = 14V, $V_{IN(-)}$ = 11V, V_{ST} = 6.0V, V_{CA} = Open, V_{CR} = 3.0V, V_{CS} = 3.0V, V_D = 13V) (23)	AG	0.85	0.99	1.15	Times
STALL CAPACITOR					
Start Mode, Stall Control, Charge Current (V_{CC} = 5.0V, $V_{IN(-)}$ = 0V, V_{CA} = V_{CR} = Open, V_{CS} = 1.0V, V_{ST} = 10V)	I_{CS1}	-2.7	-2.33	-2.13	µA
Run Mode, Stalled, Stall Control, Discharge Current (V_{CC} = 14V, $V_{IN(-)}$ = 0V, V_{CA} = V_{CR} = Open, V_{CS} = 1.0V, V_{ST} = 0V)	I_{CS2}	7.5	9.69	13.2	µA
Run Mode, Stall Control, Charge Current (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_{CA} = 2.0V, V_{CR} = 3.0V, V_{CS} = 1.0V, V_{ST} = 0V)	ICS3	-33.1	-27	-23.5	µA
Run Mode, Stall Control, Discharge Current (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_{CA} = 2.0V, V_{CR} = Open, V_{CS} = 1.0V, V_{ST} = 0V, V_{MB} = 0V)	ICS4	0.76	1.02	1.26	µA
Stall Control Threshold Voltage (V_{CC} = 14V, $V_{IN(-)}$ = 0V, V_{CA} = V_{CR} = Open, V_{ST} = 0V) (24)	V_{CS1}	1.95	2.06	2.45	V
Stall Control Saturation Voltage (V_{CC} = 14V, $V_{IN(-)}$ = 0V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 0V)	V_{CS2}	20	35.3	165	mV

Notes

20. Open V_{CR} (Ramp Capacitor) initially then force V_{CR} = 3.9V and measure ICA1.
21. Start Mode Adaptive Control sourcing current.
22. Start Mode Adaptive Control sink current.
23. Measure I_{CA}. Calculate: AG = I_{CR1}/I_{CA}.
24. Ramp V_{CS} (Stall Capacitor) from 1.5 to 2.5V in 20 mV steps. Record V_{CS} when I_{CS} goes negative.
25. Set V_{ST} = 10V, V_{CS} = 1.0V, Fail if output is on. Set V_{CS} = 3.0V, Fail if output in off.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_D = V_{CC} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
RAMP CAPACITOR					
Ramp Control Current Ratio (V_{CC} = 14V, $V_{IN(-)}$ = 0V, V_{CR} = 3.0V, V_{ST} = 0V, V_{CA} = V_{CS} = Open) (26)	CR	22	24.4	28	%
Ramp Capacitor Reset Hysteresis (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_{CA} = 2.0V, V_{CS} = 3.0V, V_{ST} = 6.0V) (27)	$V_{CR(hyh)}$	6.0	19.19	180	mV

Notes

26. Set V_{CA} (Adaptive Capacitor) to 0.5V, then open V_{CA}. Set V_{CR} (Ramp Capacitor) to 0.9V Percent ratio of CR UpCurrent as compared to the CR Down Current; (I_{CR1}/(I_{CR1}-I_{CR2}) x 100).
27. Open V_{CR}, Force V_{CR} = 1.3V. Ramp V_{CR} down in 30mV steps until I_{CR} goes negative, V_{CR1}. Ramp V_{CR} up in 3.0mV steps, toggle input between steps, until I_{CR} goes positive, V_{CR2}. $V_{CR(hys)}$-V_{CR2} - V_{cr1}.

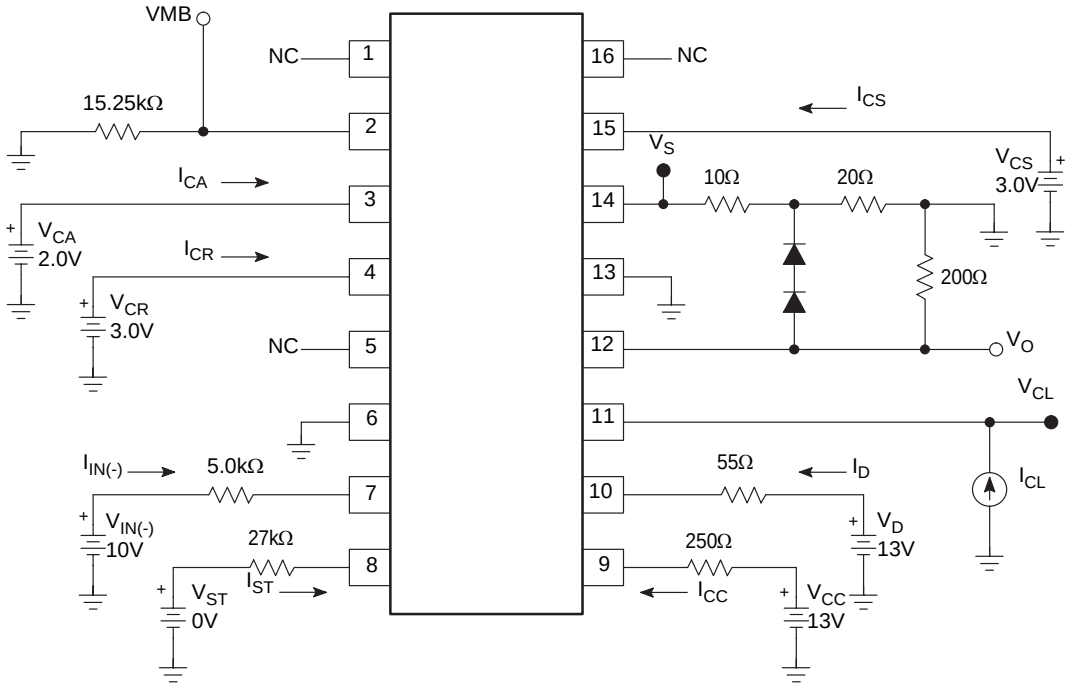


Figure 4. Test Circuit

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{CC} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING					
Negative Edge Filter, Falling Edge Time Constant (V_{CC} = 16V, $V_{IN(-)}$ = 0V, V_{CA} = V_{CR} = V_{CS} = Open, V_{ST} = 10V (28)	t_1	400	613.65	1000	µs
Propagation Delay Time (V_{CC} = 14V, $V_{IN(-)}$ = 10V, V_{CA} = V_{CS} = Open, V_{CR} =3.0V, V_{ST} = 0V) (29)	t_2	0	3.45	15	µs
Start Delay, Positive Edge (Data from I_{CA4}, V_{CA1}, V_{CA2}) (30)	t_{SDP}	1.15	1.46	1.71	ms
Start Delay, Negative Edge (Data from V_{CA4}, I_{CA5}, V_{CA2}, t_1) (31)	t_{SDN}	1.19	2.06	2.8	ms
Start to Output Disable Time (32)	t_{SOD}	71	87	107	ms
Stall to Spark Output Propagation Delay (Data from I_{CS3}, V_{CS1}, V_{CS2}) (33)	t_{SSD}	4.6	7.48	8.8	ms
Stall Shutdown Time (Data from I_{CS2}, V_{CS1}, V_{CS2}) (34)	t_{SST}	13.6	20.9	26.5	ms
Stall Frequency (35)	f_{SS}	1.69	2.26	2.8	Hz
Battery Interrupt Time (V_{CC} = $V_{IN(-)}$ = V_{ST} = 0V, V_{CA} = V_{CR} = Open, V_{CS} = 6.0V) (36)	t_{BIT}	25	66.65	200	ms

Notes

28. Measure time until V_O > 0.2V. The Negative Edge Filter prevents multiple output sparks caused by switching transients present at the input by disabling the once used input for the filter time t.
29. Propagation delay time measurement of input to output response; Step change $V_{IN(-)}$ from 0 to 10V. Measure the time required for V_O < 1.5V
30. $t_{SDP} = (V_{CA1} - V_{CA2}) \times CA/I_{CA4}$; CA = 0.1 µF
31. $t_{SDN} = [(V_{CA1} - V_{CA2}) \times CA/I_{CA5}]+t_1$; CA = 0.1 µF
32. $t_{SOD} = (V_{CA1} - V_{CA2}) \times CS/I_{CA1}$; CS = 0.1 µF
33. $t_{SSD} = (V_{CA1} - V_{CA2}) \times CS/I_{CA3}$; CS = 0.1 µF
34. $t_{SST} = (V_{CA1} - V_{CA2}) \times CS/I_{CA2}$; CS = 0.1 µF
35. $f_{SS} = 1/[(5.4/V_{IN(-)(TH)}) + (4.3/I_{CS4}) + (2/I_{CS2})] \times CS$; CS = 0.1 µF
36. $t_{BIT} = [(V_{CS} - 0.7V)/I_{CS1}] \times CS$; CS = 0.1 µF

TIMING DIAGRAMS

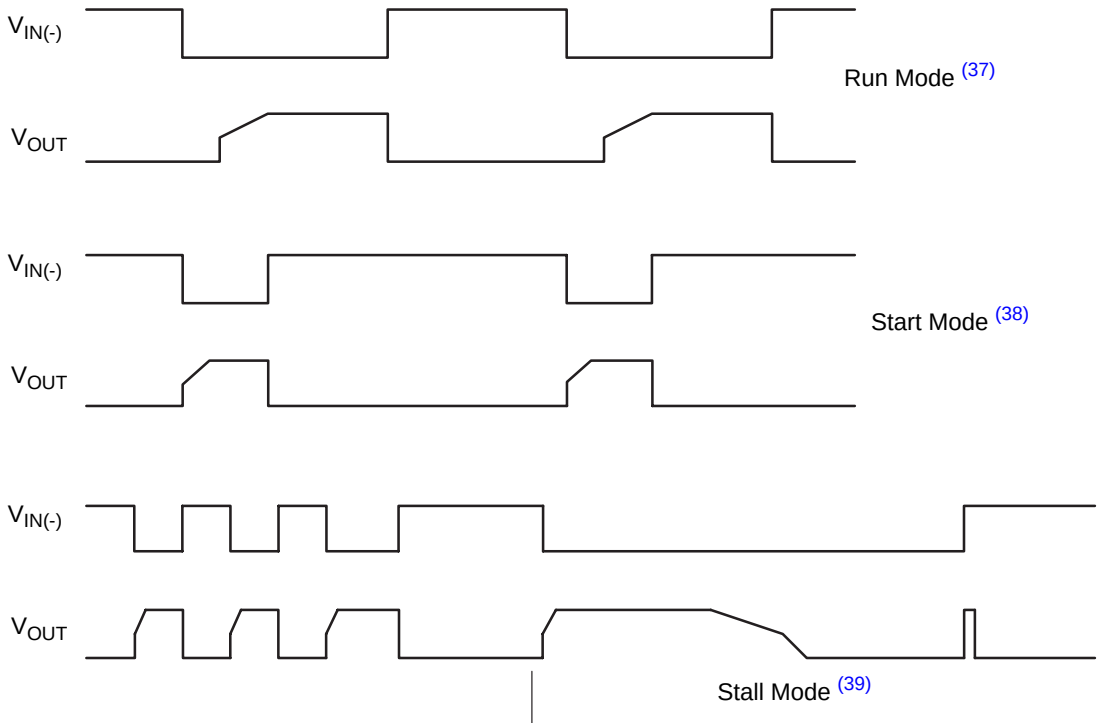


Figure 5. Basic Timing Diagrams

Notes

37. The falling edge of the $V_{IN(-)}$ signals is a charge command, while the rising edge signals a spark command.
38. During start mode. stall conditions are prevented.
39. During a stall, the coil is discharged slowly and a quick charge and spark occur on the next spark command.

ELECTRICAL PERFORMANCE CURVES

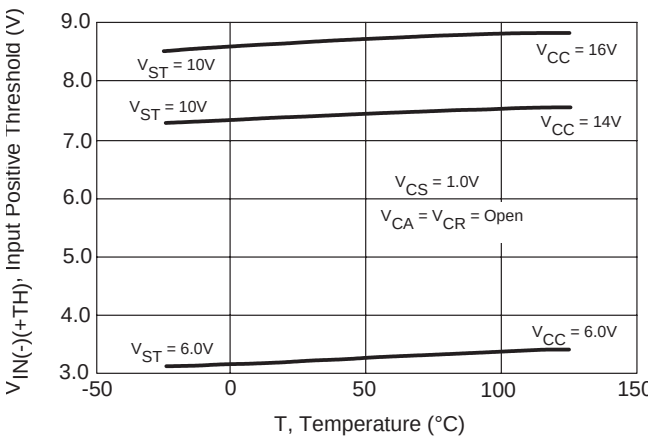


Figure 6. Input positive Threshold Voltage versus Temperature

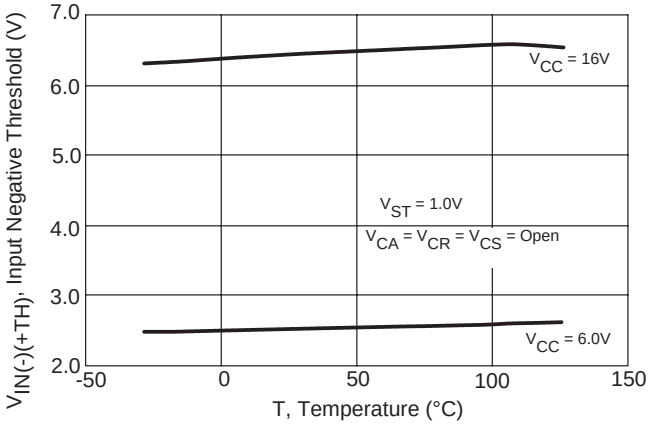


Figure 7. Input Negative Threshold Voltage versus Temperature

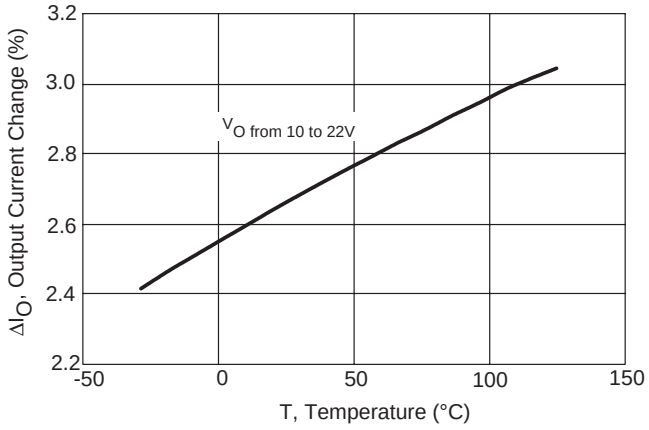


Figure 8. Output Current Change versus Temperature

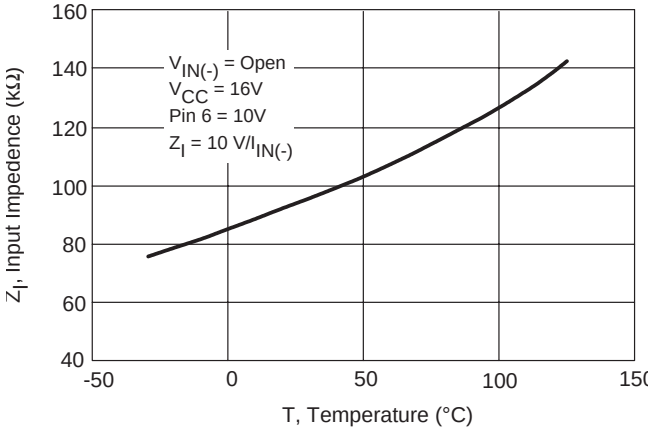


Figure 9. Input Impedance versus Temperature

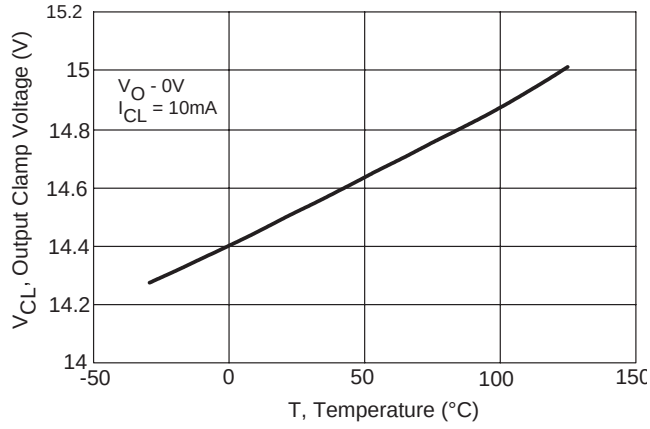


Figure 10. Output Clamp Voltage versus Temperature

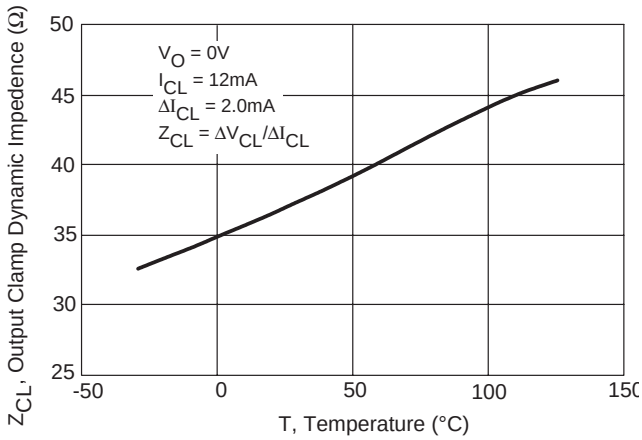


Figure 11. Output Clamp Dynamic Impedance versus Temperature

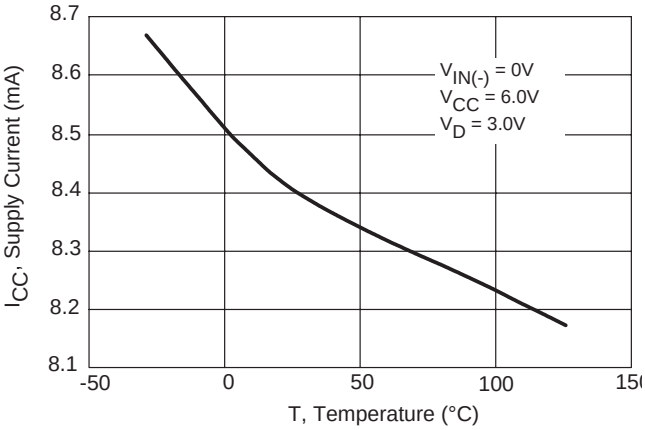


Figure 12. Supply Drain Current versus Temperature

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MC33094DW is designed for engine compartment use in 12 V automotive ignition applications to provide high performance control of the ignition coil when used with an appropriate Freescale Power Darlington Transistor. Engine control systems utilizing these devices for ignition coil control exhibit superior fuel efficiency and lower exhaust emissions over predecessor systems. The device is designed for single input control from a Hall sensor to determine crankshaft position.

The device, a bipolar linear integrated circuit, is built using high–density Integrated–Injection Logic (IIL) processing incorporating high current–gain PNP and NPN transistors. All module inputs are transient voltage protected through the use of resistors, capacitors, and/or zener diodes working in conjunction with internal protection elements. These elements provide protection of critical circuitry from externally induced high–voltage transients which may degrade the devices operational performance. At the module level, it is recommended that the VCC pin of the device be transient decoupled using an external resistor and capacitor to work in conjunction with the on–chip internal zener string to provide robust module protection of the device power pin. The D (Distributor Signal) input of module should be protected from transients through the use of an external resistor and zener diode. The Start input (ST) of the module should be decoupled through the use of two resistors and a capacitor to work in conjunction with the on–chip internal clamp (Figure 13).

The output of the device incorporates a high current–gain PNP designed to drive an external power Darlington transistor to provide control of the ignition coil. The output drive is carefully synchronized with the output from the distributor. The charging and discharging of three capacitors, external to the device, provide timing signals which program the dwell and charge time control of the ignition coil over a wide rpm range.

The timing and charge/discharge rates of the three external capacitors are accurately controlled by internal circuitry acted upon by sensor and distributor signal detection of the device.

A feedback path from the emitter of the external power Darlington transistor to the device provide monitoring of the ignition coil current. An internal comparator of the device senses and limits the maximum ignition coil current to approximately 6.5 amps. Other circuitry within the device provides an interruption of the coil current so as to generate the spark, or slowly discharges the coil in a controlled manner so as to prevent a spark and limit the total module energy dissipation.

When the external Darlington is switched off, the Darlington collector will instantly experience a dramatic increase in voltage as a result of the collapsing field of the ignition coil (inductive kick). The external voltage divider working in conjunction with the internal device zener string and power PNP form a dynamic clamp which limits the inductive kick voltage to less than 350 V. This feature protects the Darlington transistor from damaging stress or breakdown.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

BLOCK DIAGRAM DESCRIPTION (Figure 2)

The Band–Gap Reference generates a nominal 1.2V having very good stability with temperature variations. The Band–Gap Reference conceptually provides a low temperature drift voltage by summing a strongly negative Temperature Coefficient (TC) voltage with an equally strong positive TC voltage. The negative TC voltage element is a result of a transistor emitter–to–base voltage while the positive TC voltage is developed as a result of a positive TC current imposed across a resistor. The positive TC current relies on the matching of currents in different sizes of transistors. The result is a very stable reference voltage independent of temperature variations. The Band–Gap Reference voltage provides a thermally stable voltage reference for critically sensitive circuits within the IC. It also sets the master bias current for all precision currents on the IC.

The V_R Zener Reference block contains a 6.75 V zener regulator, which also exhibits a very low temperature coefficient.

The V_{CC} Comparator and Clamp block limits the V_{CC} voltage to one V_{BE} plus three zener drops in addition to comparing the V_{CC} voltage to 15 and 22V. When the V_{CC} voltage is greater than either of these two values, the IC changes the adaptive capacitor discharge rate and when above 22V the IC forces the coil current to shutdown. The minimum V_{CC} value the IC will operate at is 4.0V and V_{BAT} of 5.0V. Below 7.5V, the V_R reference is no longer maintained, and the IC consumes excess power and excess voltage is dropped in the external V_{CC} resistor.

The Master Bias Current Reference block generates precise currents used throughout the IC. The MB pin is held at 1.2V by a differential amplifier with feedback. Capacitive loading on the MB pin reduces the effectiveness of the internal dominant pole, and loading as modest as 200pF may cause the differential amplifier to oscillate.

The Input Voltage Comparator block requires an input signal between ground and V_{BAT} and detects the swing in the input signal (V_{IN}(-)). The thresholds for the input comparator are approximately 56.2% of V_{BAT} for rising signals and 36% of V_{BAT} for falling signals. The input signal may come from a Hall effect sensor or reluctance sensor on the distributor.

The Negative Edge Filter block is an inverting buffer for the signal from the Input Voltage Comparator and has a time constant of approximately 0.1μs for rising edges and 500μs for falling edges.

The Adaptive Capacitor Charging and Sensing block charges, discharges, and senses the adaptive capacitor voltage. The adaptive capacitor has a single charge rate of 8.4μA and two discharge rates. The 1.688μA slow discharge rate is used only during very high V_{CC} operation and represents an effort to reduce excess dwell and therefore power dissipation during high voltage operation. The 5.88μA discharge rate is used under normal V_{CC} operating conditions. Under a start mode, this block will discharge the adaptive capacitor forcing an enhanced start mode dwell. The start/run modes are set internally by detecting the engine frequency, which corresponds to the ramp capacitor voltage.

The Stall Capacitor Charging and Sensing block controls the charging and discharging rates of the stall capacitor. The charging rate is 31.5μA, and the two discharging rates are 1.0μA and 7.0μA. The stall capacitor potential commands the IC to maintain or reduce the coil current. When the engine is turning very slowly (or stalled), the stall capacitor will have enough time to discharge below threshold and thereby reduce coil current. The output current limiter forces the coil current to be proportional to the stall capacitor voltage when the stall capacitor voltage is less than 2.0V.

The Ramp Capacitor Charging and Sensing block charges the ramp capacitor at approximately 8.4μA and discharges it at about 33.6μA. The charging circuit is always on and sources current during the “not 25%” part of the engine cycle. The discharging circuit is only on and sinking current during the “25%” part of the engine cycle. The positive edge of the distributor input signal sets the 25% mode, and the ramp comparator output clears this mode.

The CR > CA Adaptive Comparator block signals the point where the ramp capacitor voltage is greater than the adaptive capacitor voltage. The point at which the two capacitor voltages are equal is the point where charging of the coil is begun. The adaptive algorithm used in the IC maintains the required excess dwell throughout all reasonable accelerations and decelerations without causing excess coil power dissipation, in addition, it insures that more than adequate spark energy is available for very high engine speeds, when excess dwell is impossible.

The Output Current Driver and Limiter block sources a limited supply current of about 50mA to the base of the Darlington power transistor. The Darlington will cause the coil to conduct to about 6.5 amps and the voltage drop on the S pin of the IC will rise to the threshold of the current limiter. The current limiter will then hold the coil current at that level until either a spark is commanded by the logic block, or the engine begins to stall (causing the coil to slowly discharge).

The Internal Logic block performs the required memory and gating functions on the IC to implement the adaptive ignition control algorithm.

FUNCTIONAL DEVICE OPERATION

IGNITION CIRCUIT OPERATION DESCRIPTION

When initially powered up, all module capacitors start discharged (0V). The V_{CC} capacitor will power up first, and the IC's internal logic latches are indeterminate. The following conditions will hold: STALL = 1, because the stall capacitor voltage is less than 2.0 V; 25% = 0, because the ramp capacitor is less than the Band Gap Reference voltage (V_{BG}); and I_{COIL} = 0 amps, because the stall capacitor is at 0V.

Because 25% = 0, the ramp capacitor charges towards Vr. At cranking frequencies, the ramp capacitor always exceeds the start mode threshold at the input (ZC or V_{IN}-1), and therefore the stall signal resets the start mode latch upon the first ac signal (this causes the adaptive capacitor to be discharged). With the adaptive capacitor held low, very high rates of acceleration are possible. If the adaptive capacitor were allowed to adapt the dwell at low frequencies, severe limitations to engine acceleration would occur.

See Figure 15. At point A, a spark from the previous cycle occurs as the field around the coil collapses rapidly. At the same time ZC (V_{IN}- > 10V) will set the 25% clock signal which commands the adaptive and ramp capacitors to discharge and the stall capacitor to charge. At point B, as the ramp capacitor voltage crosses the 1.2V (V_{BG}) level, the 25% clock is cleared and the polarities and amplitude of the ramp and stall capacitor currents change to their appropriate levels. At this point the adaptive capacitor is discharged and begins to float. At point C, the coil turns on and ramps until the coil current is limited to 6.5 amps. The adaptive capacitor, at point D, remains discharged and the dwell is maximized to 6.5 amps because the start/run latch has yet to be set. At point E, ZC (V_{IN}- > 10V, ZC = high) turns the coil off causing a spark to occur and at which point a new cycle begins. As the engine frequency increases, the peak voltage on the ramp capacitor at the ac signal will fall below the start mode enable threshold level. The start mode enable detector then sets the start/run latch to the run mode (CA_{DUMP} = 0) by clocking a zero into the start/run latch at the zero cross. At this time the adaptive algorithm is evoked and the adaptive capacitor is allowed to charge and discharge according to it's other logical inputs. After normal run mode operation is entered, the start mode may not be reentered even though the ramp capacitor voltage again exceeds the start mode enable threshold. A start mode may only be evoked by a STALL signal transition from logic 1 to 0. The STALL signal transition occurs at a V_{IN}- frequency of approximately 2.0 Hz.

The IC and circuit provides for other than normal starting procedures such as push starting the engine. Since the stall capacitor will be discharged in this low frequency mode, the IC will provide a spark timing with a maximum retardation of about 6.5ms.

After the start mode operation is exited, the normal operation algorithm is entered and a different sequence of events dominate the IC's performance. See Figures 16, 17, and 18. At point A, the spark from the previous cycle occurs and the 25% part of the cycle begins. During this part of the cycle, the stall capacitor will charge and the ramp and adaptive capacitors will discharge. At point B, the "not 25%" part of the cycle, also called the 75% part of the cycle, begins. The stall capacitor discharges, while the ramp capacitor charges. During this part of the cycle the adaptive capacitor floats. At point C, the ramp capacitor voltage equals the voltage on the adaptive capacitor. At this time, the coil turns on and the coil current ramps to the point where it is limited. When the coil current reaches the limit, point D, the adaptive capacitor begins to charge, until zero cross (ZC = 1logic(high)), point E. This turns the coil off and induces a spark. The 75% part of the cycle lasts until point E, at which time the cycle begins again.

The adaptive dwell algorithm causes the engine to maintain a fixed percent of excess dwell time (if possible). The mechanism that permits this involves the floating nature of the adaptive capacitor. During engine deceleration, the initial coil turn–on might occur early, but the next coil turn–on will be retarded to it's correct location due to the % adjusted adaptive capacitor charge time. During acceleration, the coil may not charge up as early as desired the first time, however, the spark will still be correctly slaved to the distributor. The side effect of this is that the adaptive capacitor will not receive as much charge time for that cycle and will have a lower average value the next cycle, thus starting the coil charging sooner, as can be seen in Figure 17. In this figure, the output voltage rises before the adaptive capacitor charge signal occurs.

See Figure 13. In the Stall mode the output is slaved by the stall capacitor. The stall capacitor can discharge completely, but starting at point X it charges during the 25% of the engine cycle (duration of when ZC is logic high = 1). At the same time a spark from the previous cycle occurs. The DWELL signal will be high as long as the engine is in stall, but falls gradually preventing a spark at point Y when the STALL goes low starting at 2.4V. The coil will be slaved to the stall capacitor, and at point Z the coil will charge to 6.5 amps as the stall capacitor charges to 2.0V. At that time the STALL comparator will trip (STALL = 0) and the DWELL signal will fall, triggering a reduced spark with some retardation (6.5ms). At this point a new cycle begins.

Each of the three different modes (Stall, Start, and Run) have their own differences. The Stall capacitor controls the output in the stall mode, however is disabled in both the start and run modes. The output is clamped longer in the start mode as compared to the run mode due to the more energy/ current in the coil causing a longer/bigger spark.

Other less likely operating sequences are possible. For example, there is a possibility of V_{CC} exceeding 15V during engine operation (High battery = logic 1). Above about 17V on V_{BAT}, the excess current limit percentage falls to 5% to conserve IC and circuit power dissipation. Above 25V, current to the coil is disabled. Care was placed in this design to account for all possible operating modes.

TYPICAL APPLICATIONS

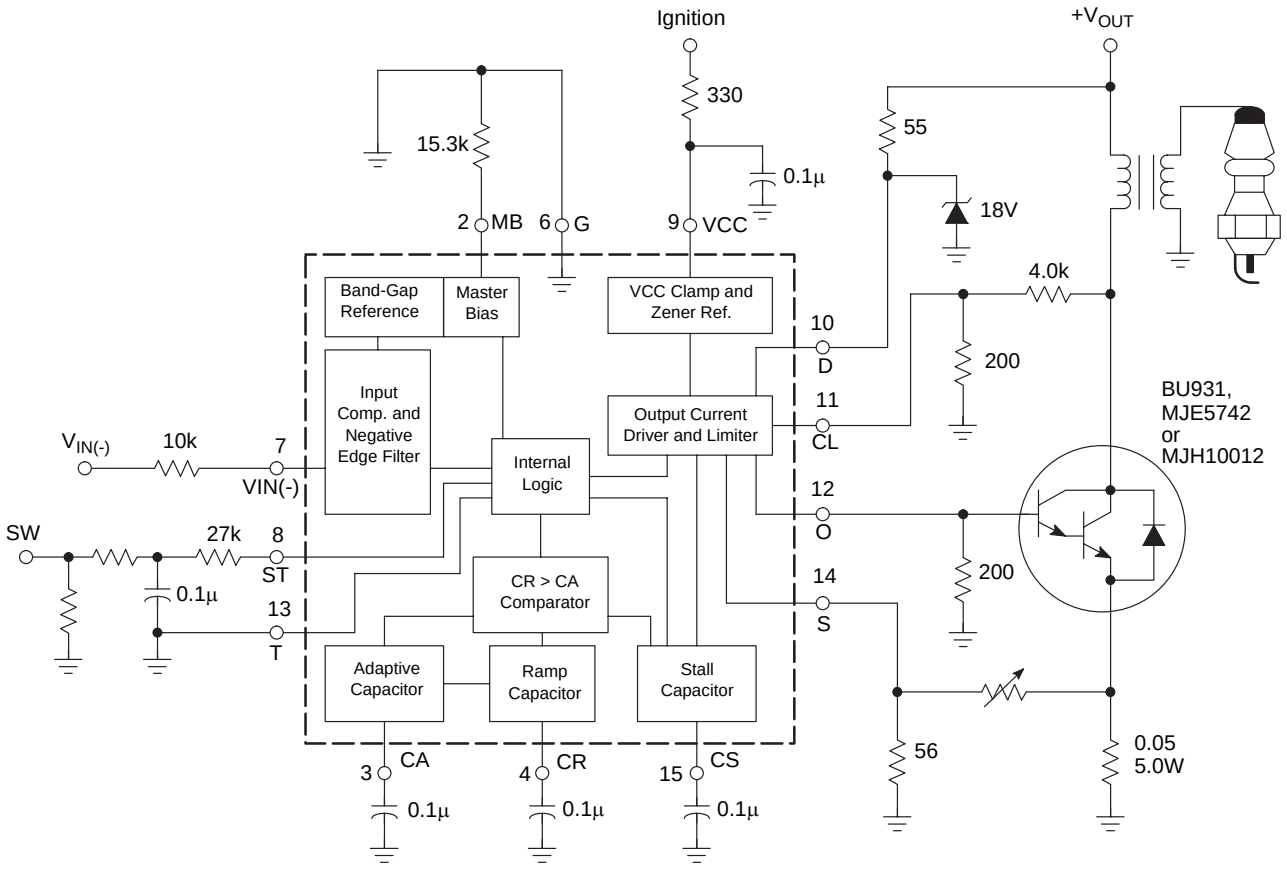


Figure 13. Typical Ignition Circuit Application

INTRODUCTION

The MC33094 is designed for engine compartment use in 12V automotive ignition applications to provide high performance control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing these devices for ignition coil control exhibit superior fuel efficiency and lower exhaust emissions over predecessor systems. The device is designed for single input control from a Hall sensor to determine crankshaft position.

The device, a bipolar linear integrated circuit, is built using high–density Integrated–Injection Logic (IIL) processing incorporating high current–gain PNP and NPN transistors. All module inputs are transient voltage protected through the use of resistors, capacitors, and/or zener diodes working in conjunction with internal protection elements. These elements provide protection of critical circuitry from externally induced high–voltage transients which may degrade the devices operational performance. At the module level, it is recommended the VCC pin of the device be transient decoupled using an external resistor and capacitor to work in conjunction with the on–chip internal zener string to provide robust module protection of the device power pin. The D (Distributor input) input of module should be protected from transients through the use of an external resistor and zener diode. The Start input of the module should be decoupled through the use of two resistors and a capacitor to work in conjunction with the on–chip internal clamp (Figure 13).

The output of the device incorporates a high current–gain PNP designed to drive an external power Darlington transistor to provide control of the ignition coil. The output drive is carefully synchronized with the output from the distributor. The charging and discharging of three capacitors, external to the device, provide timing signals which program the dwell and charge time control of the ignition coil over a wide RPM range.

The timing and charge/discharge rates of the three external capacitors are accurately controlled by internal circuitry acted upon by sensor and distributor signal detection of the device.

A feedback path from the emitter of the external power Darlington transistor to the device provide monitoring of the

ignition coil current. An internal comparator of the device senses and limits the maximum ignition coil current to approximately 6.5 amps. Other circuitry within the device provides an interruption of the coil current so as to generate the spark, or slowly discharges the coil in a controlled manner so as to prevent a spark and limit the total module energy dissipation.

When the external Darlington is switched off, the Darlington collector will instantly experience a dramatic increase in voltage as a result of the collapsing field of the ignition coil (inductive kick). The external voltage divider working in conjunction with the internal device zener string and power PNP form a dynamic clamp which limits the inductive kick voltage to less than 350V. This feature protects the Darlington transistor from damaging stress or breakdown.

IGNITION CIRCUIT OPERATION DESCRIPTION

When initially powered up, all module capacitors start discharged (0V). The VCC capacitor will power up first, and the IC's internal logic latches are indeterminate. The following conditions will hold: STALL = 1, because the stall capacitor voltage is less than 2.0 V; 25% = 0, because the ramp capacitor is less than the Band Gap Reference voltage (V_{BG}); and I_{COIL} = 0 amps, because the stall capacitor is at 0V.

Because 25% = 0, the ramp capacitor charges towards V_R. At cranking frequencies, the ramp capacitor always exceeds the start mode threshold at the input (ZC), and therefore the stall signal resets the start mode latch upon the first ac signal (this causes the adaptive capacitor to be discharged). With the adaptive capacitor held low, very high rates of acceleration are possible. If the adaptive capacitor were allowed to adapt the dwell at low frequencies, severe limitations to engine acceleration would occur.

See Figure 14. At point A, a spark from the previous cycle occurs as the field around the coil collapses rapidly. At the same time ZC (ZC (input) = high(1)) will set the 25% clock signal which commands the adaptive and ramp capacitors to discharge and the stall capacitor to charge. At point B, as the ramp capacitor voltage crosses the 1.2V (V_{BG}) level, the 25% clock is cleared and the polarities and amplitude of the ramp and stall capacitor currents change to their appropriate levels. At this point the adaptive capacitor is discharged and begins to float. At point C, the coil turns on and ramps until the coil current is limited to 6.5 amps. The adaptive capacitor, at point D, remains discharged and the dwell is maximized to 6.5 amps because the start/run latch has yet to be set. At point E, ZC (ZC = high) turns the coil off causing a spark to occur and at which point a new cycle begins. As the engine frequency increases, the peak voltage on the ramp capacitor at the ac signal will fall below the start mode enable threshold level. The start mode enable detector then sets the start/run latch to the run mode (CADUMP = 0) by clocking a zero into the start/run latch at the zero cross. At this time the adaptive algorithm is evoked and the adaptive capacitor is allowed to charge and discharge according to it's other logical inputs. After normal run mode operation is entered, the start mode may not be reentered even though the ramp capacitor voltage again exceeds the start mode enable threshold. A start mode may only be evoked by a STALL signal transition from logic 1 to 0. The STALL signal transition occurs at a ZC frequency of approximately 2.0 Hz.

The IC and circuit provides for other than normal starting procedures such as push starting the engine. Since the stall capacitor will be discharged in this low frequency mode, the IC will provide a spark timing with a maximum retardation of about 6.5 ms.

After the start mode operation is exited, the normal operation algorithm is entered and a different sequence of events dominate the IC's performance. See Figures 16, Figures 17 and Figures 18. At point A, the spark from the previous cycle occurs and the 25% part of the cycle begins. During this part of the cycle, the stall capacitor will charge and the ramp and adaptive capacitors will discharge. At point B, the "not 25%" part of the cycle, also called the 75% part of the cycle, begins. The stall capacitor discharges, while the ramp capacitor charges. During this part of the cycle the adaptive capacitor floats. At point C, the ramp capacitor voltage equals the voltage on the adaptive capacitor. At this time, the coil turns on and the coil current ramps to the point where it is limited. When the coil current reaches the limit, point D, the adaptive capacitor begins to charge, until zero cross (ZC = 1logic(high)), point E. This turns the coil off and induces a spark. The 75% part of the cycle lasts until point E, at which time the cycle begins again.

The adaptive dwell algorithm causes the engine to maintain a fixed percent of excess dwell time (if possible). The mechanism that permits this involves the floating nature of the adaptive capacitor. During engine deceleration, the initial coil turn–on might occur early, but the next coil turn–on will be retarded to it's correct location due to the % adjusted adaptive capacitor charge time. During acceleration, the coil may not charge up as early as desired the first time, however, the spark will still be correctly slaved to the distributor. The side effect of this is that the adaptive capacitor will not receive as much charge time for that cycle and will have a lower average value the next cycle, thus starting the coil charging sooner, as can be seen in Figure 18. In this figure, the output voltage rises before the adaptive capacitor charge signal occurs.

See Figure 14. In the Stall mode the output is slaved by the stall capacitor. The stall capacitor can discharge completely, but starting at point X it charges during the 25% of the engine cycle (duration of when ZC is logic high = 1). At the same time a spark from the previous cycle occurs. The DWELL signal will be high as long as the engine is in stall, but falls gradually preventing a spark at point Y when the STALL goes low starting at 2.4V. The coil will be slaved to the stall capacitor, and at point Z the coil will charge to 6.5 amps as the stall capacitor charges to 2.0V. At that time the STALL comparator will trip (STALL = 0) and the DWELL signal will fall, triggering

a reduced spark with some retardation (6.5 ms). At this point a new cycle begins.

Each of the three different modes (Stall, Start, and Run) have their own differences. The Stall capacitor controls the output in the stall mode, however is disabled in both the start and run modes. The output is clamped longer in the start mode as compared to the run mode due to the more energy/ current in the coil causing a longer/bigger spark.

Other less likely operating sequences are possible. For example, there is a possibility of VCC exceeding 15V during engine operation (High battery = logic 1). Above about 17V on Vbat, the excess current limit percentage falls to 5% to conserve IC and circuit power dissipation. Above 25V, current to the coil is disabled. Care was placed in this design to account for all possible operating modes.

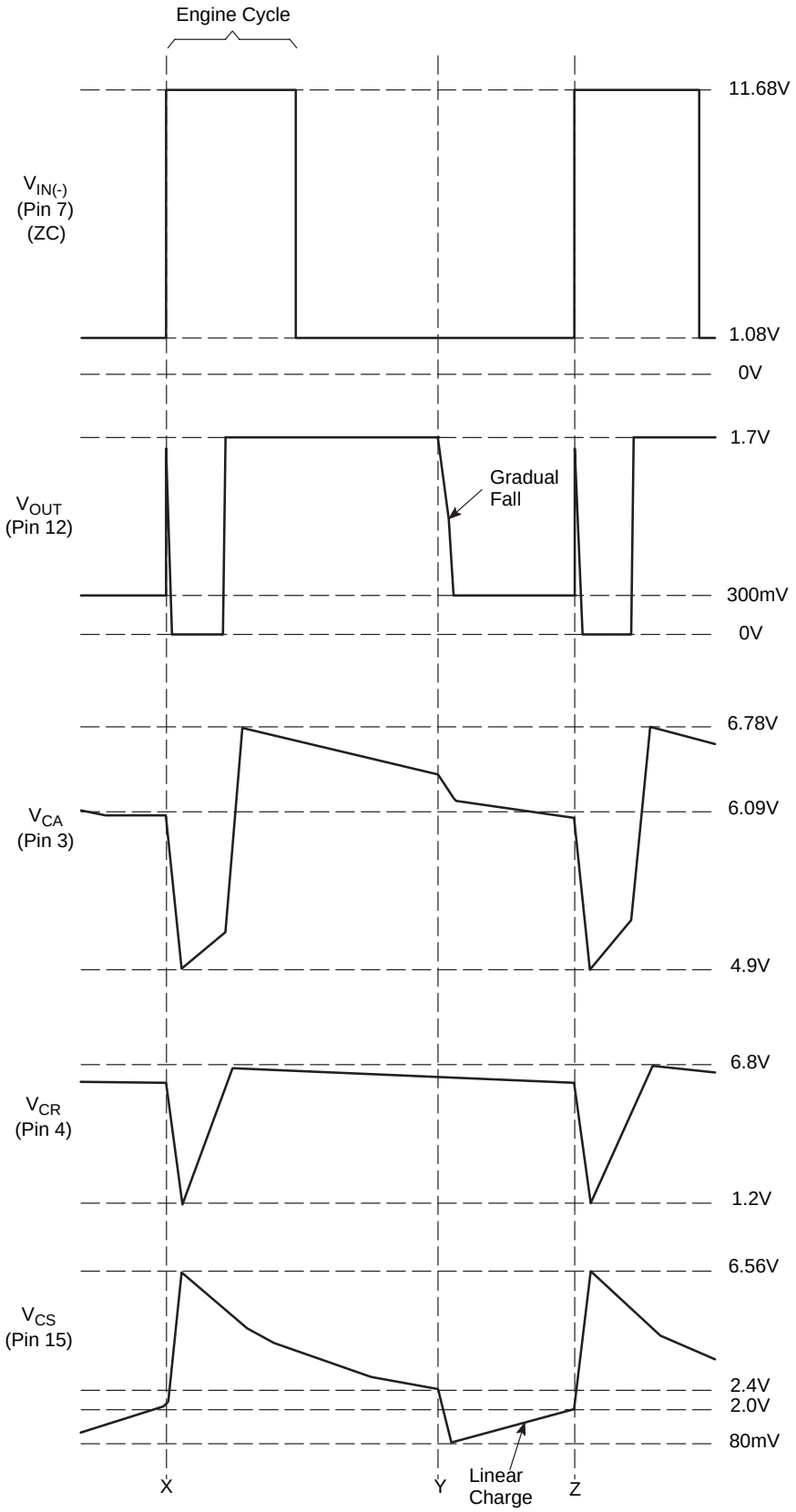


Figure 14. Stall Mode 60 RPM (Frequency: 2.0 Hz @ 100 ms)

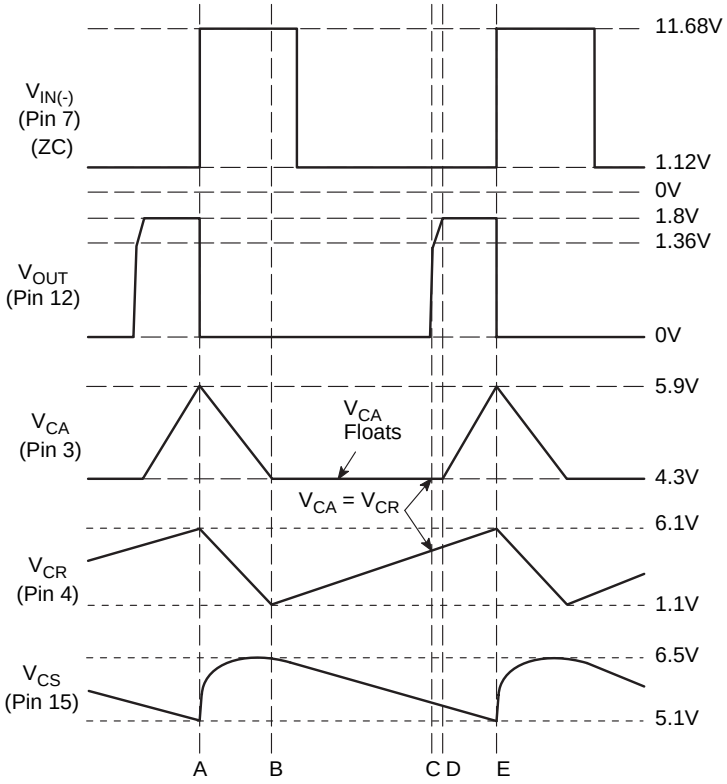


Figure 15. Start Mode 300 RPM (Frequency: 10 Hz @ 20 ms)

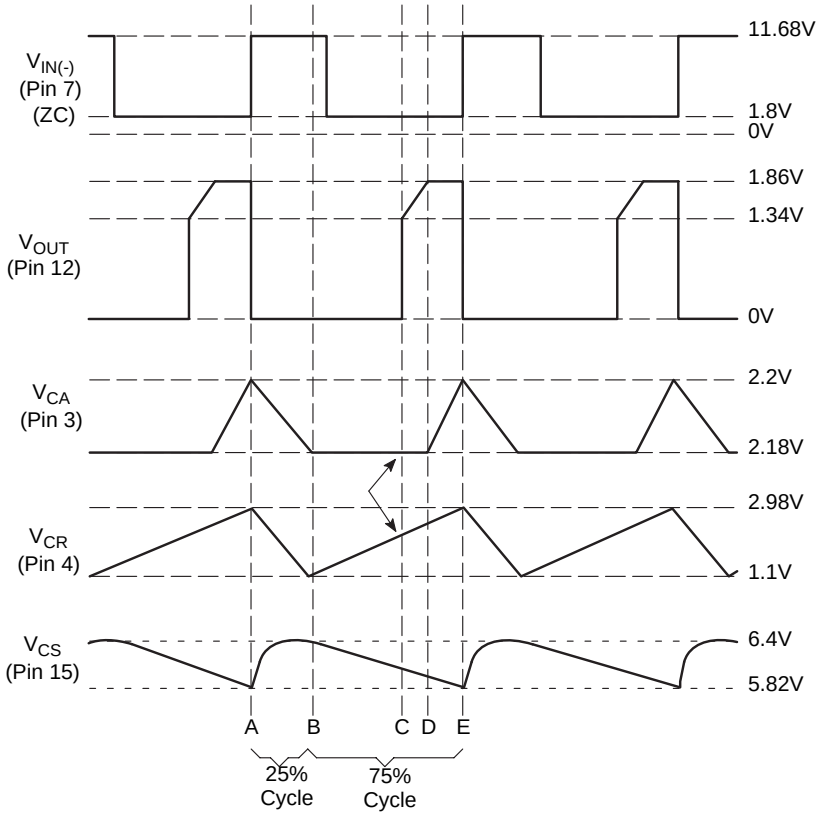


Figure 16. Run Mode 900 RPM (Frequency: 30 Hz @10 ms)

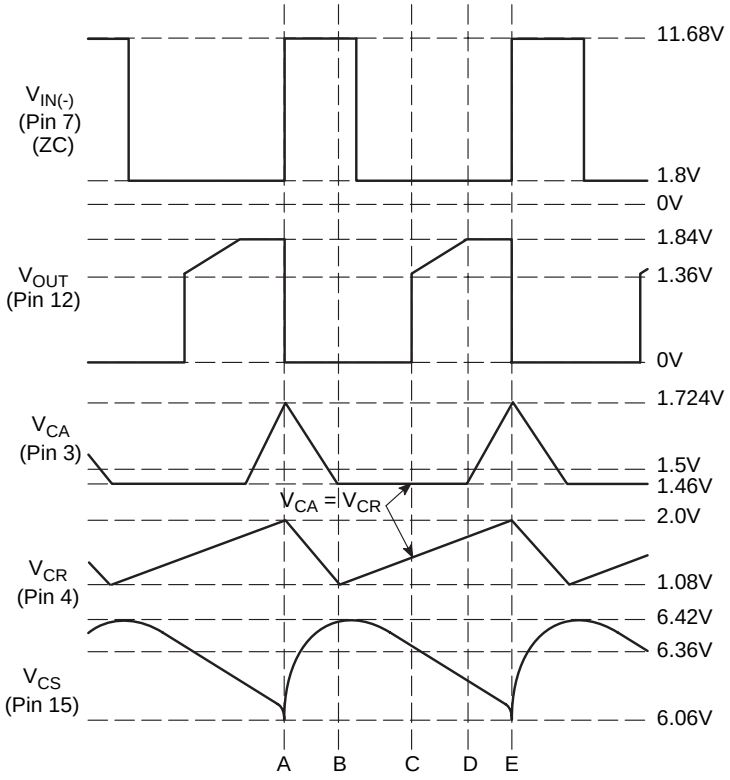


Figure 17. Run Mode 2000 RPM (Frequency: 66.67 Hz @ 5.0 ms)

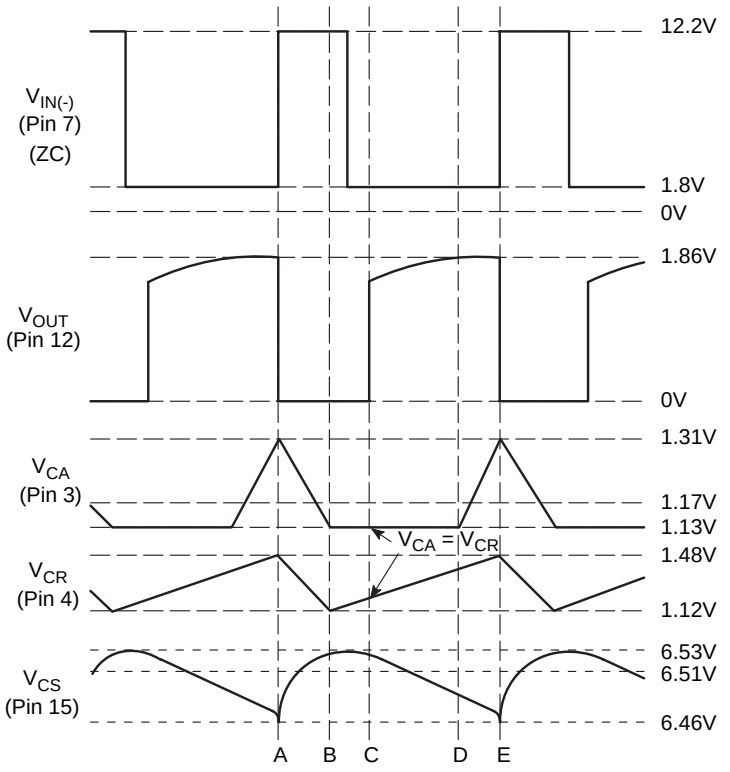
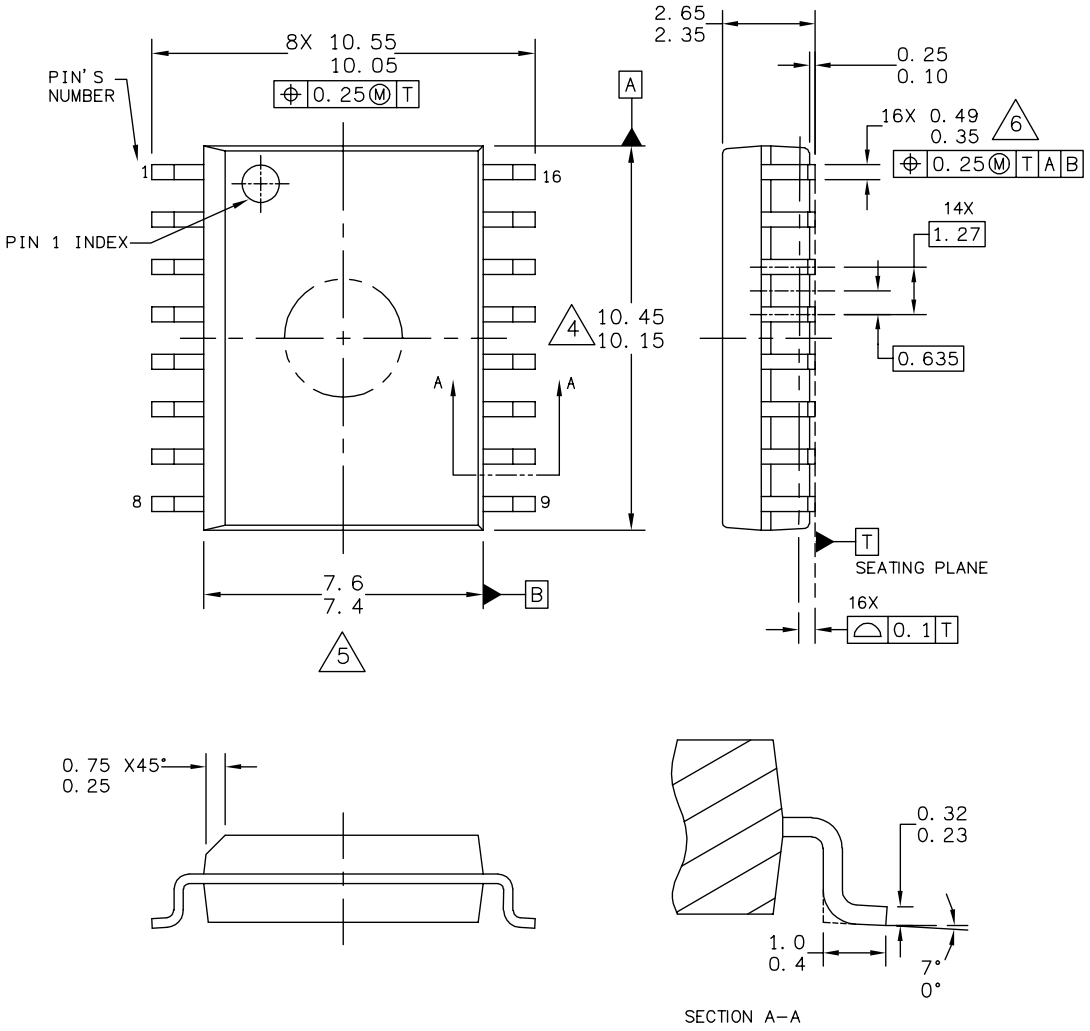


Figure 18. Run Mode 5000 RPM (Frequency: 166.67 Hz @ 2.0 ms)

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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	STANDARD: JEDEC MS-013AA	

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EG SUFFIX (PB-FREE)
16-PIN
PLASTIC PACKAGE
98ASB42567B
ISSUE F

33094

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	10/2006	• Initial Release • Converted to Freescale format • Added MCZ33094EG/R2 to the Ordering Information • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. • Added note Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics. on page 4

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