21555 Non-Transparent PCI-to-PCI Bridge

Datasheet

Product Features

- Full compliance with the *PCI local Bus Specification*, Revision 2.2, plus:
  - —PCI Power Management support
  - —Vital Product Data (VPD) support
  - —CompactPCI Distributed Hot-Swap support
- 3.3-V operation with 5.0-V tolerant I/O
- Selectable asynchronous or synchronous primary and secondary interface clocks
- Concurrent primary and secondary bus operation
- Fully compliant with the *Advanced Configuration Power Interface* (ACPI) specification
- Fully compliant with the *PCI Bus Power Management* specification
- Queuing of multiple transactions in either direction
- 256 bytes of posted write (data and address) buffering in each direction
- 256 bytes of read data buffering in each direction
- Four delayed transaction entries in each direction
- Two dedicated I2O delayed transaction entries
- Two sets of standard PCI Configuration registers corresponding to the primary and secondary interface; each set is accessible from either the primary or secondary interface
- Direct offset address translation for downstream memory and I/O transactions
- Hardware enable for secondary bus central functions
- IEEE Standard 1149.1 boundary-scan JTAG interface
- Four primary interface base address configuration registers for downstream forwarding, with size and prefetchability programmable for all four address ranges
- Three secondary interface address configuration registers specifying local address ranges for upstream forwarding, with size and prefetchability programmable for all three address ranges
- Inverse decoding above the 4 GB address boundary for upstream DACs
- Ability to generate Type 0 and Type 1 configuration commands on the primary or secondary interface via configuration or I/O CSR accesses
- Ability to generate I/O commands on the primary or secondary interface via I/O CSR accesses
- I2O message unit
- Doorbell registers for software generation of primary and secondary bus interrupts, 16 bits per interface
- Eight Dwords of scratchpad registers
- Generic own bit (can memory-map) semaphore
- Parallel flash ROM interface with primary bus expansion ROM base address register
- Serial ROM interface
- Secondary bus arbiter support for up to nine external devices at 33 MHz and up to four external devices at 66 MHz (in addition to the 21555)
- Secondary bus clock output for synchronous operation
- Four 32-bit base address configuration registers mapping the 21555 control and status registers (CSRs)
- Available in 33 MHz and 66 MHz versions

Order Number: 278320-002

Contents

1.0 Introduction 5
1.1 Comparing 21555 and Standard PCI-to-PCI Bridge 5
1.2 Architectural Overview 8
2.0 Pin Assignment 10
2.1 Pin Location List (Alphanumeric) 12
2.2 Pin Signal List (Alphanumeric) 17
3.0 Electrical Specifications 22
3.1 PCI Electrical Specification Conformance 22
3.2 Absolute Maximum Ratings 22
3.3 DC Specifications 23
3.4 AC Timing Specifications 23
3.4.1 Clock Timing Specifications 23
3.4.2 PCI Signal Timing Specifications 25
3.4.3 Reset Timing Specifications 26
3.4.4 Serial ROM Timing Specifications 27
3.4.5 Parallel ROM Timing Specifications 27
3.4.6 JTAG Timing Specifications 28
4.0 Mechanical Specifications 29

Figures

1 21555 Intelligent Controller Application 6
2 21555 Microarchitecture 9
3 21555 PBGA Cavity Down View 11
4 PCI Clock Signal AC Parameter Measurements 25
5 PCI Signal Timing Measurement Conditions 25
6 304 PBGA (Four-Layer) Package 29

Tables

1 21555 and PPB Feature Comparison 7
2 Signal Type Abbreviations 10
3 21555 Pin Location List (Alphanumeric) 12
4 21555 Pin Signal List (Alphanumeric) 17
5 Absolute Maximum Ratings 22
6 Functional Operating Range 22
7 DC Parameters 23
8 33 MHz PCI Clock Signal AC Parameters 24
9 66 MHz PCI Clock Signal AC Parameters 24
10 33 MHz PCI Signal Timing Specifications 26
11 66 MHz PCI Signal Timing Specifications 26
12 Reset Timing Specifications 26
13 Serial ROM Timing Specifications 27
14 Parallel ROM Timing Specifications 27
15 JTAG Timing Specifications 28

16 304-Point 4-Layer PBGA Package Dimensions 30

1.0 Introduction

Intel's 21555 is a PCI peripheral device that performs PCI bridging functions for embedded and intelligent I/O applications. The 21555 has a 64-bit primary interface, a 64-bit secondary interface, and 66-MHz capability. The 21554 a related PCI peripheral device, has a 64-bit primary interface, a 64-bit secondary interface, and 33-MHz capability."

The 21555 is a "non-transparent" PCI-to-PCI bridge that acts as a gateway to an intelligent subsystem. It allows a local processor to independently configure and control the local subsystem. The 21555 implements an I2O message unit that enables any local processor to function as an intelligent I/O processor (IOP) in an I2O-capable system. Because the 21555 is architecture independent, it works with any host and local processors that support a PCI bus. This architecture independence enables vendors to leverage existing investments while moving products to PCI technology.

Unlike a transparent PCI-to-PCI bridge, the 21555 is specifically designed to bridge between two processor domains. The processor domain on the primary interface of the 21555 is also referred to as the host domain, and its processor is the host processor. The secondary bus interfaces to the local domain and the local processor. Special features include support of independent primary and secondary PCI clocks, independent primary and secondary address spaces, and address translation between the primary (host) and secondary (local) domains.

The 21555 enables add-in card vendors to present to the host system a higher level of abstraction than is possible with a transparent PCI-to-PCI bridge. The 21555 uses a Type 0 configuration header, which presents the entire subsystem as a single "device" to the host processor. This allows loading of a single device driver for the entire subsystem, and independent local processor initialization and control of the subsystem devices. Because the 21555 uses a Type 0 configuration header, it does not require hierarchical PCI-to-PCI bridge configuration code.

The 21555 forwards transactions between the primary and secondary PCI buses as does a transparent PCI-to-PCI bridge. In contrast to a transparent PCI-to-PCI bridge, however, the 21555 can translate the address of a forwarded transaction from a system address to a local address, or vice versa. This mechanism allows the 21555 to hide subsystem resources from the host processor and to resolve any resource conflicts that may exist between the host and local subsystems.

The 21555 operates at 3.3 V and is also 5.0-V I/O tolerant. Adapter cards designed using the 21555 can be keyed as universal, thus permitting use in either a 5-V or 3-V slot.

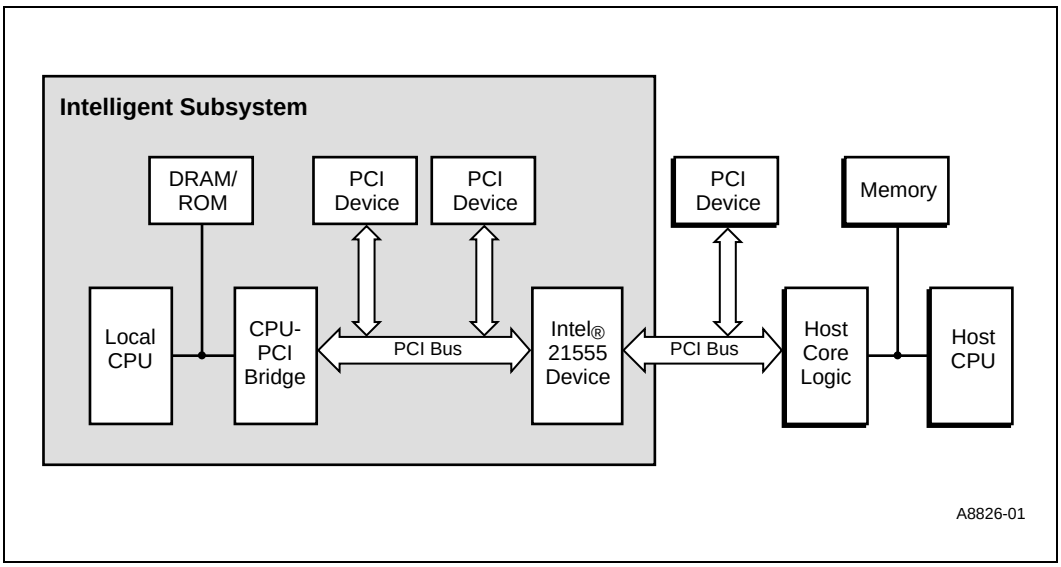
1.1 Comparing 21555 and Standard PCI-to-PCI Bridge

The 21555 is functionally similar to a standard PCI-to-PCI bridge (PPB) in that both provide a connection path between devices attached to two independent PCI buses. A 21555 and a PPB allow the electrical loading of devices on one PCI bus to be isolated from the other bus while permitting concurrent operation on both buses. Because the *PCI Local Bus Specification* restricts PCI option cards to a single electrical load, the ability of PPBs and the 21555 to spawn PCI buses enables the design of multi device PCI option cards. The key difference between a PPB and the 21555 is that the presence of a PPB in a connection path between the host processor and a device is transparent to devices and device drivers, while the presence of the 21555 is not. This difference enables the 21555 to provide features that better support the use of intelligent controllers in the subsystem.

It was a primary goal of the PCI-to-PCI bridge architecture that a PPB be transparent to devices and device drivers. For example, no changes are needed to a device driver when a PCI peripheral is located behind a PPB. Once configured during system initialization, a PPB operates without the aid of a device driver. A PPB does not require a device driver of its own since it does not have any resources that must be managed by software during run-time. This requirement for transparency forced the usage of a flat addressing model across PCI-to-PCI bridges. This means that a given physical address exists at only one location in the PCI bus hierarchy and that this location may be accessed by any device attached at any point in the PCI bus hierarchy. As a consequence, it is not possible for a PPB to isolate devices or address ranges from access by devices on the opposite interface of a PPB. The PPB architecture assumes that the resources of any device in a PCI system are configured and managed by the host processor.

However, there are applications where the transparency of a PCI-to-PCI bridge is not desired. For example, Figure 1 shows a hypothetical PCI add-in card used for an intelligent subsystem application.

Figure 1. 21555 Intelligent Controller Application



Assume that the local processor on the add-in card is used to manage the resources of the devices attached to the add-in card's local PCI bus. Assume also that it is desirable to restrict access to these same resources from other PCI bus masters in the system and from the host processor. In addition, there is a need to resolve address conflicts that may exist between the host system and the local processor. The non transparency of the 21555 is perfectly suited to this kind of configuration, where a transparent PCI-to-PCI bridge is problematic.

Because the 21555 is not transparent, the device driver for the add-in card must be aware of the presence of the 21555 and manage its resources appropriately. The 21555 allows the entire subsystem to appear as a single virtual device to the host. This enables configuration software to identify the appropriate driver for the subsystem.

With a transparent PCI-to-PCI bridge, a driver does not need to know about the presence of the bridge and manage its resources. The subsystem appears to the host system as individual PCI devices on a secondary PCI bus, not as a single virtual device.

Table 1 shows a comparison between a 21555 and a standard transparent PCI-to-PCI bridge.

Table 1. 21555 and PPB Feature Comparison

Feature	21555	PCI-to-PCI Bridge
Transaction forwarding	Adheres to PPB ordering rules.	Adheres to PPB ordering rules.
	Uses posted writes and delayed transactions.	Uses posted writes and delayed transactions.
	Adheres to PPB transaction error and parity error guidelines, although some errors may be reported differently.	Adheres to PPB transaction error and parity error guidelines.
Address decoding	Base address registers are used to define independent downstream and upstream forwarding windows.	PPB base and limit address registers are used to define downstream forwarding windows.
	Inverse decoding is only used for upstream transactions above the 4 GB boundary.	Inverse decoding for upstream forwarding.
Address translation	Supported for both memory and I/O transactions.	No translation, a flat address model is assumed.
Configuration	Downstream devices are not visible to host.	Downstream devices are visible to host.
	Does not require hierarchical configuration code (Type 0 configuration header).	Requires hierarchical configuration code (Type 1 configuration header).
	Does not respond to Type 1 configuration transactions.	Forwards and converts Type 1 configuration transactions.
	Supports configuration access from the secondary bus. Implements separate set of configuration registers for the secondary interface.	Does not support configuration access from the secondary bus. Same set of configuration registers is used to control both primary and secondary interfaces.
Run-time resources	Includes features such as doorbell interrupts, I2O message unit, and so on, that must be managed by the device driver.	Typically has only configuration registers; no device driver is required.
Clocks	Generates secondary bus clock output.	Generates one or more secondary bus clock outputs.
	Asynchronous secondary clock input is also supported.	
Secondary bus central functions	Implements secondary bus arbiter. This function can be disabled.	Implements secondary bus arbiter.
	Drives secondary bus AD, C/BE#, and PAR during reset. This function can be disabled.	Drives secondary bus AD, C/BE#, and PAR during reset.

1.2 Architectural Overview

The 21555 consists of the following function blocks:

Data Buffers

Data buffers include the buffers along with the associated data path control logic. Delayed transaction buffers contain the compare functionality for completing delayed transactions. The blocks also contain the watchdog timers associated with the buffers. The data buffers are as follows:

- Four-entry downstream delayed transaction buffer
- Four-entry upstream delayed transaction buffer
- 256-byte downstream posted write buffer
- 256-byte upstream posted write buffer
- 256-byte downstream read data buffer
- 256-byte upstream read data buffer
- Two downstream I2O delayed transaction entries

Registers

The following register blocks also contain address decode and translation logic, I2O message unit, and interrupt control logic:

- Primary interface header Type 0 configuration registers
- Secondary interface header Type 0 configuration registers
- Device-specific configuration registers
- Memory and I/O mapped control and status registers

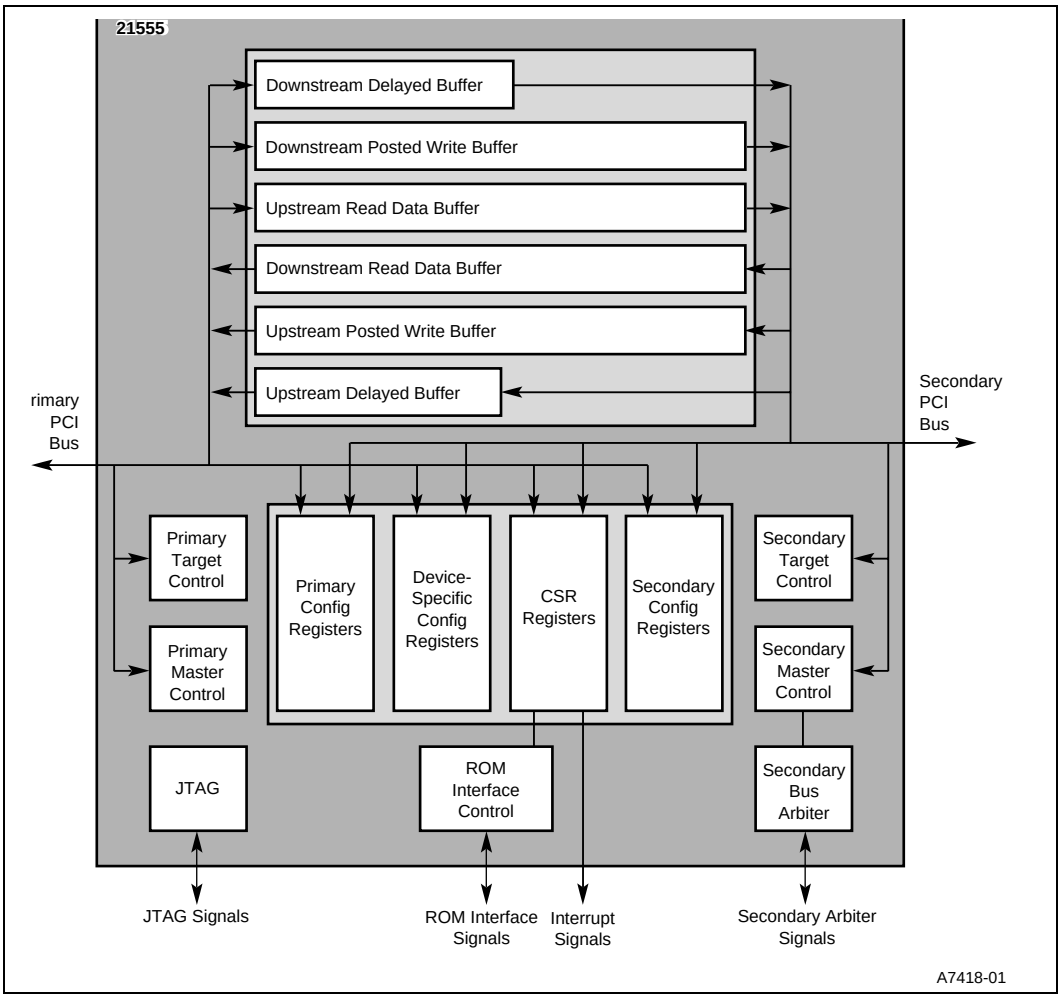
Control Logic

The 21555 has the following control logic:

- Primary PCI target control logic
- Primary PCI master control logic
- Secondary PCI target control logic
- Secondary PCI master control logic
- ROM interface control logic for both serial and parallel ROM connections (interfaces between the ROM registers and ROM signals)
- Secondary PCI bus arbiter interface to secondary bus device request and grant lines, as well as the 21555 secondary master control logic
- JTAG control logic

Figure 2 shows the 21555 microarchitecture.

Figure 2. 21555 Microarchitecture



2.0 Pin Assignment

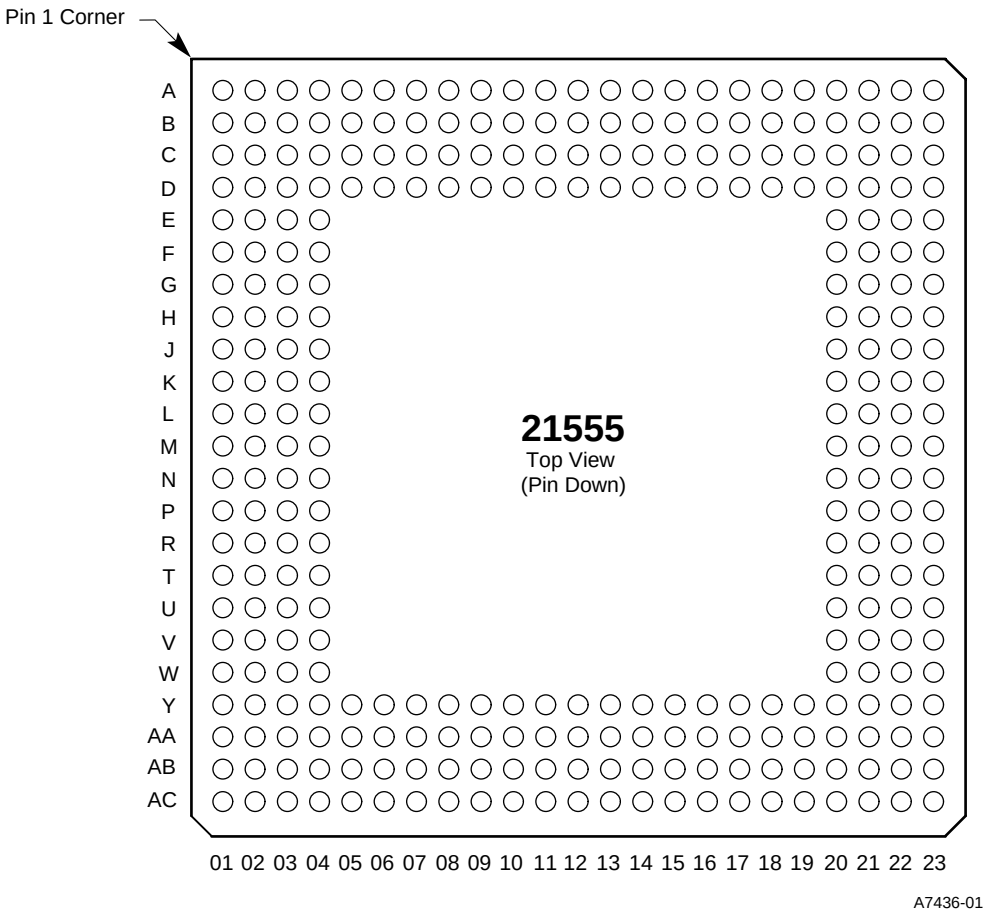
This chapter describes the 21555 pin assignment and lists the pins according to location and in alphabetic order.

Figure 3 shows the 21555 304-point ball grid array (PBGA), representing the pins in vertical rows labeled numerically, and horizontal rows labeled alphabetically. Table 2 defines the signal type abbreviations used in the signal and pin tables for this specification. Table 3 and Table 4 use these alphanumerics to identify pin assignments.

Table 2. Signal Type Abbreviations

Signal Type	Description
I	Standard input only.
O	Standard output only.
TS	Tristate bidirectional.
STS	Sustained tristate. Active low signal must be pulled high for one clock cycle when deasserting.
OD	Standard open drain.

Figure 3. 21555 PBGA Cavity Down View



2.1 Pin Location List (Alphanumeric)

Table 3 lists the 21555 pins in order of location, showing the location code, signal name, and signal type of each pin.

Figure 3 provides the map for identifying the pin location codes, listed in alphanumeric order in the PBGA Location column.

Table 2 defines the signal type abbreviations used in the Type column.

Table 3. 21555 Pin Location List (Alphanumeric) (Sheet 1 of 5)

PBGA Location	Signal Name	Type	PBGA Location	Signal Name	Type
A1	s_req_l[4]	I	AA7	p_ad[12]	TS
A2	s_req_l[3]	I	AA8	p_ad[10]	TS
A3	s_req_l[1]	I	AA9	p_cbe_l[0]	TS
A4	s_ad[29]	TS	AA10	p_ad[5]	TS
A5	s_ad[27]	TS	AA11	vss	P
A6	s_ad[25]	TS	AA12	vdd	P
A7	s_cbe_l[3]	TS	AA13	vss	P
A8	s_ad[22]	TS	AA14	p_cbe_l[7]	TS
A9	s_ad[20]	TS	AA15	p_cbe_l[4]	TS
A10	s_ad[16]	TS	AA16	vdd	P
A11	s_frame_l	STS	AA17	p_ad[58]	TS
A12	s_devsel_l	STS	AA18	p_ad[54]	TS
A13	s_par	TS	AA19	vss	P
A14	s_ad[13]	TS	AA20	vdd	P
A15	s_ad[10]	TS	AA21	p_ad[46]	TS
A16	s_m66ena	I	AA22	p_ad[42]	TS
A17	s_cbe_l[0]	TS	AA23	vdd	P
A18	s_ad[6]	TS	AB1	p_ad[16]	TS
A19	s_ad[3]	TS	AB2	vss	P
A20	s_ad[1]	TS	AB3	p_trdy_l	STS
A21	s_req64_l	STS	AB4	p_stop_l	STS
A22	vdd	P	AB5	p_serr_l	OD
A23	s_cbe_l[6]	TS	AB6	p_ad[15]	TS
AA1	p_ad[18]	TS	AB7	vss	P
AA2	vss	P	AB8	vss	P
AA3	p_ad[17]	TS	AB9	p_ad[8]	TS
AA4	vss	P	AB10	p_ad[6]	TS
AA5	vdd	P	AB11	vdd	P
AA6	p_par	TS	AB12	p_ad[1]	TS

Table 3. 21555 Pin Location List (Alphanumeric) (Sheet 2 of 5)

PBGA Location	Signal Name	Type
AB13	p_ad[0]	TS
AB14	p_cbe_l[6]	TS
AB15	p_ad[63]	TS
AB16	p_ad[60]	TS
AB17	vss	P
AB18	p_ad[55]	TS
AB19	p_ad[53]	TS
AB20	p_ad[51]	TS
AB21	p_ad[48]	TS
AB22	vss	P
AB23	vdd	P
AC1	vdd	P
AC2	vdd	P
AC3	p_frame_l	STS
AC4	p_devsel_l	STS
AC5	p_perr_l	STS
AC6	p_cbe_l[1]	TS
AC7	p_ad[14]	TS
AC8	p_ad[11]	TS
AC9	p_m66ena	I
AC10	p_ad[7]	TS
AC11	p_ad[3]	TS
AC12	p_ad[2]	TS
AC13	p_ack64_l	STS
AC14	p_cbe_l[5]	TS
AC15	p_ad[61]	TS
AC16	p_ad[59]	TS
AC17	p_ad[56]	TS
AC18	vdd	P
AC19	p_ad[52]	TS
AC20	p_ad[50]	TS
AC21	p_ad[47]	TS
AC22	p_ad[45]	TS
AC23	p_ad[44]	TS
B1	vdd	P
B2	vss	P
B3	s_req_l[0]	I

PBGA Location	Signal Name	Type
B4	vdd	P
B5	s_ad[26]	TS
B6	s_ad[24]	TS
B7	s_idsel	I
B8	vss	P
B9	s_ad[18]	TS
B10	vss	P
B11	vss	P
B12	s_trdy_l	STS
B13	s_serr_l	OD
B14	s_ad[14]	TS
B15	s_ad[12]	TS
B16	vdd	P
B17	s_ad[9]	TS
B18	s_ad[7]	TS
B19	s_ad[4]	TS
B20	vdd	P
B21	vss	P
B22	vss	P
B23	vdd	P
C1	s_req_l[6]	I
C2	s_req_l[7]	I
C3	s_req_l[2]	I
C4	s_ad[31]	TS
C5	s_ad[28]	TS
C6	vss	P
C7	s_ad[23]	TS
C8	s_ad[21]	TS
C9	s_ad[17]	TS
C10	vdd	P
C11	s_irdy_l	STS
C12	s_stop_l	STS
C13	s_perr_l	STS
C14	s_ad[15]	TS
C15	vdd	P
C16	vss	P
C17	vss	P

Table 3. 21555 Pin Location List (Alphanumeric) (Sheet 3 of 5)

PBGA Location	Signal Name	Type	PBGA Location	Signal Name	Type
C18	s_ad[5]	TS	F1	s_gnt_l[6]	TS
C19	s_ad[2]	TS	F2	s_gnt_l[7]	TS
C20	s_ack64_l	STS	F3	s_gnt_l[5]	TS
C21	s_cbe_l[5]	TS	F4	vss	P
C22	s_par64	TS	F20	vss	P
C23	s_cbe_l[4]	TS	F21	vss	P
D1	s_gnt_l[1]	TS	F22	s_ad[56]	TS
D2	s_gnt_l[2]	TS	F23	s_ad[57]	TS
D3	s_req_l[8]	I	G1	s_gnt_l[8]	TS
D4	s_req_l[5]	I	G2	vss	P
D5	s_ad[30]	TS	G3	s_clk	I
D6	vdd	P	G4	s_clk_o	O
D7	vdd	P	G20	vdd	P
D8	vss	P	G21	s_ad[53]	TS
D9	s_ad[19]	TS	G22	s_ad[54]	TS
D10	vdd	P	G23	s_ad[55]	TS
D11	s_cbe_l[2]	TS	H1	s_rst_l	O
D12	vss	P	H2	s_inta_l	OD
D13	s_cbe_l[1]	TS	H3	tdi	I
D14	vdd	P	H4	vdd	P
D15	s_ad[11]	TS	H20	vdd	P
D16	vss	P	H21	s_ad[50]	TS
D17	s_ad[8]	TS	H22	s_ad[51]	TS
D18	vdd	P	H23	s_ad[52]	TS
D19	s_ad[0]	TS	J1	tdo	O
D20	s_cbe_l[7]	TS	J2	tck	I
D21	vss	P	J3	trst_l	I
D22	s_ad[61]	TS	J4	tms	I
D23	s_ad[62]	TS	J20	vdd	P
E1	s_rst_in_l	I	J21	s_ad[47]	TS
E2	s_gnt_l[4]	TS	J22	s_ad[48]	TS
E3	s_gnt_l[3]	TS	J23	s_ad[49]	TS
E4	s_gnt_l[0]	TS	K1	sr_cs	O
E20	s_ad[63]	TS	K2	pr_ad[7]	TS
E21	s_ad[60]	TS	K3	pr_ad[6]	TS
E22	s_ad[58]	TS	K4	vss	P
E23	s_ad[59]	TS	K20	vss	P

Table 3. 21555 Pin Location List (Alphanumeric) (Sheet 4 of 5)

PBGA Location	Signal Name	Type	PBGA Location	Signal Name	Type
k21	s_ad[45]	TS	R3	vdd	P
k22	vss	P	R4	p_clk	I
k23	s_ad[46]	TS	R20	l_stat	TS
L1	pr_ad[4]	TS	R21	s_ad[33]	TS
L2	pr_ad[3]	TS	R22	s_ad[32]	TS
L3	pr_ad[2]	TS	R23	s_pme_l	I
L4	pr_ad[5]	TS	T1	p_ad[30]	TS
L20	s_ad[44]	TS	T2	p_ad[31]	TS
L21	s_ad[42]	TS	T3	p_req_l	TS
L22	s_ad[41]	TS	T4	vdd	P
L23	s_ad[43]	TS	T20	vdd	P
M1	pr_ad[0]	TS	T21	s_vio	I
M2	pr_rd_l	O	T22	p_enum_l	OD
M3	pr_ad[1]	TS	T23	p_pme_l	OD
M4	vdd	P	U1	p_ad[27]	TS
M20	vdd	P	U2	p_ad[29]	TS
M21	vdd	P	U3	vss	P
M22	s_ad[40]	TS	U4	p_ad[28]	TS
M23	vss	P	U20	p_par64	TS
N1	pr_wr_l	O	U21	p_vio	I
N2	pr_ale_l	O	U22	vdd	P
N3	pr_cs_l / pr_rdy	O/I	u23	p_ad[32]	TS
N4	pr_clk	O	V1	p_ad[25]	TS
N20	s_ad[36]	TS	V2	p_ad[26]	TS
N21	s_ad[39]	TS	V3	p_ad[24]	TS
N22	s_ad[38]	TS	V4	vss	P
N23	s_ad[37]	TS	V20	vss	P
P1	p_rst_l	I	V21	p_ad[35]	TS
P2	p_inta_l	OD	V22	p_ad[33]	TS
P3	scan_ena	I	V23	p_ad[34]	TS
P4	vss	P	W1	p_idsel	I
P20	vss	P	W2	p_cbe_l[3]	TS
P21	s_ad[35]	TS	W3	p_ad[23]	TS
P22	s_ad[34]	TS	W4	p_ad[20]	TS
P23	vss	P	W20	p_ad[40]	TS
R1	p_gnt_l	I	W21	p_ad[38]	TS
R2	vss	P	W22	p_ad[36]	TS

Table 3. 21555 Pin Location List (Alphanumeric) (Sheet 5 of 5)

PBGA Location	Signal Name	Type	PBGA Location	Signal Name	Type
W23	p_ad[37]	TS	y12	vss	P
y1	p_ad[21]	TS	y13	p_req64_l	STS
y2	p_ad[22]	TS	y14	vdd	P
y3	p_ad[19]	TS	y15	p_ad[62]	TS
y4	p_cbe_l[2]	TS	y16	vss	P
y5	p_irdy_l	STS	y17	p_ad[57]	TS
y6	vdd	P	y18	vdd	P
y7	p_ad[13]	TS	y19	p_ad[49]	TS
y8	vss	P	y20	p_ad[43]	TS
y9	p_ad[9]	TS	y21	p_ad[41]	TS
y10	vdd	P	y22	p_ad[39]	TS
y11	p_ad[4]	TS	y23	vss	P

2.2 Pin Signal List (Alphanumeric)

Table 4 lists the 21555 signals in alphanumeric order, showing the name, location code, and type of each signal.

Figure 3 provides the map for identifying the pin location codes that are listed under PBGA Location column.

Table 2 defines the signal type abbreviations used in the Type column.

Table 4. 21555 Pin Signal List (Alphanumeric) (Sheet 1 of 5)

Signal Name	PBGA Location	Type	Signal Name	PBGA Location	Type
l_stat	R20	TS	p_ad[27]	U1	TS
p_ack64_l	AC13	STS	p_ad[28]	U4	TS
p_ad[0]	AB13	TS	p_ad[29]	U2	TS
p_ad[1]	AB12	TS	p_ad[30]	T1	TS
p_ad[2]	AC12	TS	p_ad[31]	T2	TS
p_ad[3]	AC11	TS	p_ad[32]	U23	TS
p_ad[4]	Y11	TS	p_ad[33]	V22	TS
p_ad[5]	AA10	TS	p_ad[34]	V23	TS
p_ad[6]	AB10	TS	p_ad[35]	V21	TS
p_ad[7]	AC10	TS	p_ad[36]	W22	TS
p_ad[8]	AB9	TS	p_ad[37]	W23	TS
p_ad[9]	Y9	TS	p_ad[38]	W21	TS
p_ad[10]	AA8	TS	p_ad[39]	Y22	TS
p_ad[11]	AC8	TS	p_ad[40]	W20	TS
p_ad[12]	AA7	TS	p_ad[41]	Y21	TS
p_ad[13]	Y7	TS	p_ad[42]	AA22	TS
p_ad[14]	AC7	TS	p_ad[43]	Y20	TS
p_ad[15]	AB6	TS	p_ad[44]	AC23	TS
p_ad[16]	AB1	TS	p_ad[45]	AC22	TS
p_ad[17]	AA3	TS	p_ad[46]	AA21	TS
p_ad[18]	AA1	TS	p_ad[47]	AC21	TS
p_ad[19]	Y3	TS	p_ad[48]	AB21	TS
p_ad[20]	W4	TS	p_ad[49]	Y19	TS
p_ad[21]	Y1	TS	p_ad[50]	AC20	TS
p_ad[22]	Y2	TS	p_ad[51]	AB20	TS
p_ad[23]	W3	TS	p_ad[52]	AC19	TS
p_ad[24]	V3	TS	p_ad[53]	AB19	TS
p_ad[25]	V1	TS	p_ad[54]	AA18	TS
p_ad[26]	V2	TS	p_ad[55]	AB18	TS

Table 4. 21555 Pin Signal List (Alphanumeric) (Sheet 2 of 5)

Signal Name	PBGA Location	Type	Signal Name	PBGA Location	Type
p_ad[56]	AC17	TS	pr_ad[2]	L3	TS
p_ad[57]	Y17	TS	pr_ad[3]	L2	TS
p_ad[58]	AA17	TS	pr_ad[4]	L1	TS
p_ad[59]	AC16	TS	pr_ad[5]	L4	TS
p_ad[60]	AB16	TS	pr_ad[6]	K3	TS
p_ad[61]	AC15	TS	pr_ad[7]	K2	TS
p_ad[62]	Y15	TS	pr_ale_l	N2	O
p_ad[63]	AB15	TS	pr_clk	N4	O
p_cbe_l[0]	AA9	TS	pr_cs_l / pr_rdy	N3	O/I
p_cbe_l[1]	AC6	TS	pr_rd_l	M2	O
p_cbe_l[2]	Y4	TS	pr_wr_l	N1	O
p_cbe_l[3]	W2	TS	p_vio	U21	I
p_cbe_l[4]	AA15	TS	s_ack64_l	C20	STS
p_cbe_l[5]	AC14	TS	s_ad[0]	D19	TS
p_cbe_l[6]	AB14	TS	s_ad[1]	A20	TS
p_cbe_l[7]	AA14	TS	s_ad[2]	C19	TS
p_clk	R4	I	s_ad[3]	A19	TS
p_devsel_l	AC4	STS	s_ad[4]	B19	TS
p_enum_l	T22	OD	s_ad[5]	C18	TS
p_frame_l	AC3	STS	s_ad[6]	A18	TS
p_gnt_l	R1	I	s_ad[7]	B18	TS
p_idsel	W1	I	s_ad[8]	D17	TS
p_inta_l	P2	OD	s_ad[9]	B17	TS
p_irdy_l	Y5	STS	s_ad[10]	A15	TS
p_m66ena	AC9	I	s_ad[11]	D15	TS
p_par	AA6	TS	s_ad[12]	B15	TS
p_par64	U20	TS	s_ad[13]	A14	TS
p_perr_l	AC5	STS	s_ad[14]	B14	TS
p_pme_l	T23	OD	s_ad[15]	C14	TS
p_req_l	T3	TS	s_ad[16]	A10	TS
p_req64_l	Y13	STS	s_ad[17]	C9	TS
p_rst_l	P1	I	s_ad[18]	B9	TS
p_serr_l	AB5	OD	s_ad[19]	D9	TS
p_stop_l	AB4	STS	s_ad[20]	A9	TS
p_trdy_l	AB3	STS	s_ad[21]	C8	TS
pr_ad[0]	M1	TS	s_ad[22]	A8	TS
pr_ad[1]	M3	TS	s_ad[23]	C7	TS

Table 4. 21555 Pin Signal List (Alphanumeric) (Sheet 3 of 5)

Signal Name	PBGA Location	Type	Signal Name	PBGA Location	Type
s_ad[24]	B6	TS	s_ad[61]	D22	TS
s_ad[25]	A6	TS	s_ad[62]	D23	TS
s_ad[26]	B5	TS	s_ad[63]	E20	TS
s_ad[27]	A5	TS	s_cbe_l[0]	A17	TS
s_ad[28]	C5	TS	s_cbe_l[1]	D13	TS
s_ad[29]	A4	TS	s_cbe_l[2]	D11	TS
s_ad[30]	D5	TS	s_cbe_l[3]	A7	TS
s_ad[31]	C4	TS	s_cbe_l[4]	C23	TS
s_ad[32]	R22	TS	s_cbe_l[5]	C21	TS
s_ad[33]	R21	TS	s_cbe_l[6]	A23	TS
s_ad[34]	P22	TS	s_cbe_l[7]	D20	TS
s_ad[35]	P21	TS	s_clk	G3	I
s_ad[36]	N20	TS	s_clk_o	G4	O
s_ad[37]	N23	TS	s_devsel_l	A12	STS
s_ad[38]	N22	TS	s_frame_l	A11	STS
s_ad[39]	N21	TS	s_gnt_l[0]	E4	TS
s_ad[40]	M22	TS	s_gnt_l[1]	D1	TS
s_ad[41]	L22	TS	s_gnt_l[2]	D2	TS
s_ad[42]	L21	TS	s_gnt_l[3]	E3	TS
s_ad[43]	L23	TS	s_gnt_l[4]	E2	TS
s_ad[44]	L20	TS	s_gnt_l[5]	F3	TS
s_ad[45]	K21	TS	s_gnt_l[6]	F1	TS
s_ad[46]	K23	TS	s_gnt_l[7]	F2	TS
s_ad[47]	J21	TS	s_gnt_l[8]	G1	TS
s_ad[48]	J22	TS	s_idsel	B7	I
s_ad[49]	J23	TS	s_inta_l	H2	OD
s_ad[50]	H21	TS	s_irdy_l	C11	STS
s_ad[51]	H22	TS	s_m66ena	A16	I
s_ad[52]	H23	TS	s_par	A13	TS
s_ad[53]	G21	TS	s_par64	C22	TS
s_ad[54]	G22	TS	s_perr_l	C13	STS
s_ad[55]	G23	TS	s_pme_l	R23	I
s_ad[56]	F22	TS	s_req_l[0]	B3	I
s_ad[57]	F23	TS	s_req_l[1]	A3	I
s_ad[58]	E22	TS	s_req_l[2]	C3	I
s_ad[59]	E23	TS	s_req_l[3]	A2	I
s_ad[60]	E21	TS	s_req_l[4]	A1	I

Table 4. 21555 Pin Signal List (Alphanumeric) (Sheet 4 of 5)

Signal Name	PBGA Location	Type	Signal Name	PBGA Location	Type
s_req_l[5]	D4	I	vdd	D7	P
s_req_l[6]	C1	I	vdd	D10	P
s_req_l[7]	C2	I	vdd	D14	P
s_req_l[8]	D3	I	vdd	D18	P
s_req64_l	A21	STS	vdd	G20	P
s_rst_in_l	E1	I	vdd	H4	P
s_rst_l	H1	O	vdd	H20	P
s_serr_l	B13	OD	vdd	J20	P
s_stop_l	C12	STS	vdd	M4	P
s_trdy_l	B12	STS	vdd	M20	P
scan_ena	P3	I	vdd	M21	P
sr_cs	K1	O	vdd	R3	P
s_vio	T21	I	vdd	T4	P
tck	J2	I	vdd	T20	P
tdi	H3	I	vdd	U22	P
tdo	J1	O	vdd	Y6	P
tms	J4	I	vdd	Y10	P
trst_l	J3	I	vdd	Y14	P
vdd	A22	P	vdd	Y18	P
vdd	AA5	P	vss	AA2	P
vdd	AA12	P	vss	AA4	P
vdd	AA16	P	vss	AA11	P
vdd	AA20	P	vss	AA13	P
vdd	AA23	P	vss	AA19	P
vdd	AB11	P	vss	AB2	P
vdd	AB23	P	vss	AB7	P
vdd	AC1	P	vss	AB8	P
vdd	AC2	P	vss	AB17	P
vdd	AC18	P	vss	AB22	P
vdd	B1	P	vss	B2	P
vdd	B4	P	vss	B8	P
vdd	B16	P	vss	B10	P
vdd	B20	P	vss	B11	P
vdd	B23	P	vss	B21	P
vdd	C10	P	vss	B22	P
vdd	C15	P	vss	C6	P
vdd	D6	P	vss	C16	P

Table 4. 21555 Pin Signal List (Alphanumeric) (Sheet 5 of 5)

Signal Name	PBGA Location	Type	Signal Name	PBGA Location	Type
vss	C17	P	vss	M23	P
vss	D8	P	vss	P4	P
vss	D12	P	vss	P20	P
vss	D16	P	vss	P23	P
vss	D21	P	vss	R2	P
vss	F4	P	vss	U3	P
vss	F20	P	vss	V4	P
vss	F21	P	vss	V20	P
vss	G2	P	vss	Y8	P
vss	K4	P	vss	Y12	P
vss	K20	P	vss	Y16	P
vss	K22	P	vss	Y23	P

3.0 Electrical Specifications

This section specifies the following electrical behavior of the 21555:

- PCI electrical conformance.
- Absolute maximum ratings.
- DC specifications.
- AC timing specifications.

3.1 PCI Electrical Specification Conformance

The 21555 PCI pins conform to the basic set of PCI electrical specifications in the *PCI Local Bus Specification*, Revision 2.2. See that document for a complete description of the PCI I/O protocol and pin AC specifications.

3.2 Absolute Maximum Ratings

The 21555 is specified to operate at a maximum frequency of 33 MHz or 66 MHz if 66 MHz capable, at a junction temperature (T_j) not to exceed 125°C. Table 5 lists the absolute maximum ratings for the 21555. Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only. Operating beyond the functional operating range is not recommended and extended exposure beyond the functional operating range may affect reliability. Table 6 lists the functional operating range.

Table 5. Absolute Maximum Ratings

Parameter	Minimum	Maximum
Junction temperature, T_j	—	125°C
Supply voltage V_{cc}	—	4.3 V
Maximum voltage applied to signal pins	—	5.5 V
Maximum power, P_{WC}	—	3.0 W
Storage temperature range, T_{stg}	–55°C	125°C

Table 6. Functional Operating Range

Parameter	Minimum	Maximum
Supply voltage, V_{cc}	3.0 V	3.6 V
Operating ambient temperature, T_a	0°C	70°C

3.3 DC Specifications

Table 7 defines the DC parameters met by all 21555 signals under the conditions of the functional operating range.

Note: In Table 7, currents into the chip (chip sinking) are denoted as positive (+) current. Currents from the chip (chip sourcing) are denoted as negative (–) current.

Table 7. DC Parameters

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{cc}	Supply voltage	—	3.0	3.6	V
V_{il}	Low-level input voltage[a]	—	–0.5	0.3 V_{cc}	V
V_{ih}	High-level input voltage[a]	—	0.5 V_{cc}	V_{IO} + 0.5 V	V
V_{ol}	Low-level output voltage[b]	I_{out} = 1500 µA	—	0.1 V_{cc}	V
V_{ol5V}	Low-level output voltage[c]	I_{out} = 6 mA	—	0.55	V
V_{oh}	High-level output voltage[b]	I_{out} = –500 µA	0.9 V_{cc}	—	V
V_{oh5V}	High-level output voltage[c]	I_{out} = –2 mA	2.4	—	V
I_{il}	Low-level input leakage current[a,d]	0 <V_{in} <V_{cc}	—	±10	µA
C_{in}	Input pin capacitance	—	—	10.0	pF
C_{IDSEL}	p_idsel pin capacitance	—	—	8.0	pF
C_{clk}	p_clk, s_clk pin capacitance	—	5.0	12.0	pF

a. Guarantees meeting the specification for the 5-V signaling environment.
b. For 3.3-V signaling environment.
c. For 5-V signaling environment.
d. Input leakage currents include high-Z output leakage for all bidirectional buffers with tristate outputs.

3.4 AC Timing Specifications

The next sections specify the AC characteristics met by all 21555 signals under the conditions of the functional operating range:

- Clock timing.
- PCI signal timing.
- Reset timing.
- Serial ROM timing.
- Parallel ROM timing.
- JTAG timing.

3.4.1 Clock Timing Specifications

The AC specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. The output responses are delays from clock to signal. The AC specifications are defined separately for each clock domain within the 21555.

Table 8 and Table 9 specify p_clk and s_clk parameter values for clock signal AC timing, and Figure 4 shows the AC parameter measurements for the p_clk and s_clk signals. See also Figure 5 for a further illustration of signal timing. Unless otherwise indicated, all AC parameters are guaranteed when tested within the functional operating range of Table 6.

Table 8. 33 MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	p_clk,s_clk cycle time	30	∞	ns
T_{high}	p_clk, s_clk high time	11	—	ns
T_{low}	p_clk, s_clk low time	11	—	ns
–	p_clk, s_clk slew rate[a]	1	4	V/ns
T_{sclk}	Delay from p_clk to s_clk[b]	3	15	ns
T_{sclkr}	p_clk rising to s_clk_o rising	0	8	ns
T_{sclkf}	p_clk falling to s_clk_o falling[c]	0	8	ns
T_{dskew}	s_clk_o duty cycle skew from p_clk duty cycle[C]	—	0.75	ns

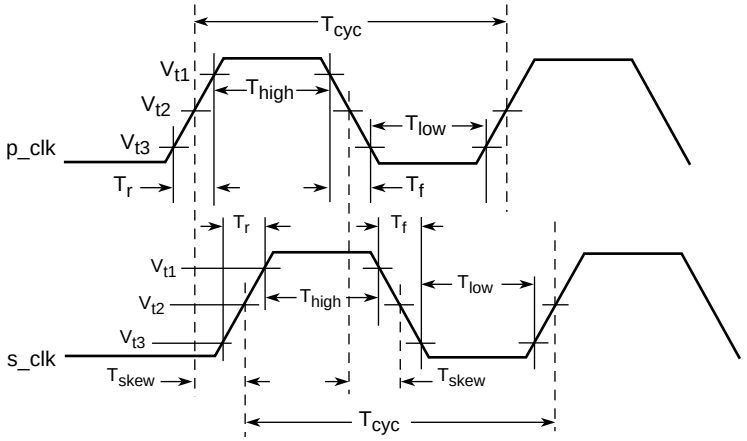
a. 0.2 V_{CC} to 0.6 V_{CC}.
b. Required when the 21555 is operating in synchronous mode.
c. Measured with 30 pF lumped load.

Table 9. 66 MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	p_clk,s_clk cycle time	15	30	ns
T_{high}	p_clk, s_clk high time	6	—	ns
T_{low}	p_clk, s_clk low time	6	—	ns
–	p_clk, s_clk slew rate[a]	1.5	4	V/ns
T_{sclk}	Delay from p_clk to s_clk[b]	3	15	ns
T_{sclkr}	p_clk rising to s_clk_o rising	0	13	ns
T_{sclkf}	p_clk falling to s_clk_o falling[c]	0	13	ns
T_{dskew}	s_clk_o duty cycle skew from p_clk duty cycle[C]	—	0.75	ns

a. 0.2 V_{CC} to 0.6 V_{CC}.
b. Required when the 21555 is operating in synchronous mode.
c. Measured with 30 pF lumped load.

Figure 4. PCI Clock Signal AC Parameter Measurements



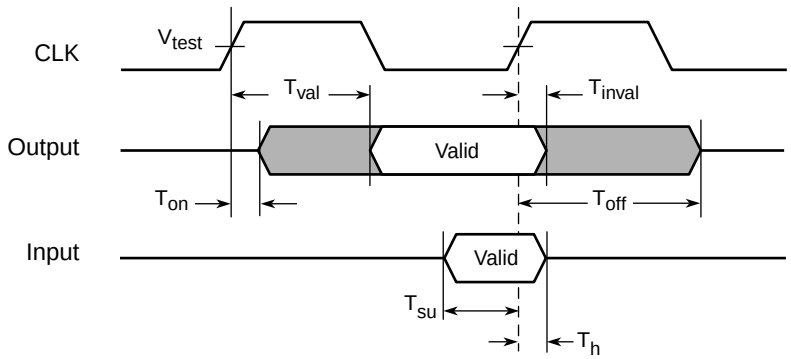
Notes:
T_{t1} - 2.0 V for 5-V signals; 0.5 V_{cc} for 3.3-V clocks
T_{t2} - 1.5 V for 5-V signals; 0.4 V_{cc} for 3.3-V clocks
T_{t3} - 0.8 V for 5-V signals; 0.3 V_{cc} for 3.3-V clocks

A7834-01

3.4.2 PCI Signal Timing Specifications

Figure 5 and Tables 10 and 11 show the PCI signal timing specifications.

Figure 5. PCI Signal Timing Measurement Conditions



Note: T_{test} - 1.5 V for 5-V signals; 0.4 V_{cc} for 3.3-V signals

A7835-01

Table 10. 33 MHz PCI Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay — bused signals[a,b,c]	2	11	ns
$T_{val(ptp)}$	CLK to signal valid delay — point-to-point[a,b,c]	2	12	ns
T_{on}	Float to active delay[a,b]	2	—	ns
T_{off}	Active to float delay[a,b]	—	28	ns
T_{su}	Input setup time to CLK — bused signals[a,b,c]	7	—	ns
$T_{su(ptp)}$	Input setup time to CLK—point-to-point[a,b,c]	10, 12	—	ns
T_{h}	Input signal hold time from CLK[a,b]	0	—	ns

a. See Figure 5.
b. All primary interface signals are synchronized to p_clk. All secondary interface signals are synchronized to s_clk.
c. Point-to-point signals are p_req_l, s_req_l[8:0], p_gnt_l, and s_gnt_l[8:0]. Bused signals are p_ad, p_cbe_l, p_par, p_par64, p_perr_l, p_serr_l, p_frame_l, p_irdy_l, p_trdy_l, p_devsel_l, p_stop_l, p_idsel, p_req64_l, p_ack64_l, s_ad, s_cbe_l, s_par, s_par64, s_perr_l, s_serr_l, s_frame_l, s_irdy_l, s_trdy_l, s_devsel_l, s_stop_l, s_req64_l, s_ack64_l, and s_idsel.

Table 11. 66 MHz PCI Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	CLK to signal valid delay — bused signals[a,b,c]	2	6	ns
$T_{val(ptp)}$	CLK to signal valid delay — point-to-point[a,b,c]	2	6	ns
T_{on}	Float to active delay[a,b]	2	—	ns
T_{off}	Active to float delay[a,b]	—	14	ns
T_{su}	Input setup time to CLK — bused signals[a,b]	3	—	ns
$T_{su(ptp)}$	Input setup time to CLK—point-to-point[a,b]	5	—	ns
T_{h}	Input signal hold time from CLK[a,b]	0	—	ns

a. See Figure 5.
b. All primary interface signals are synchronized to p_clk. All secondary interface signals are synchronized to s_clk.
c. Point-to-point signals are p_req_l, s_req_l[8:0], p_gnt_l, and s_gnt_l[8:0]. Bused signals are p_ad, p_cbe_l, p_par, p_par64, p_perr_l, p_serr_l, p_frame_l, p_irdy_l, p_trdy_l, p_devsel_l, p_stop_l, p_idsel, p_req64_l, p_ack64_l, s_ad, s_cbe_l, s_par, s_par64, s_perr_l, s_serr_l, s_frame_l, s_irdy_l, s_trdy_l, s_devsel_l, s_stop_l, s_req64_l, s_ack64_l, and s_idsel.

3.4.3 Reset Timing Specifications

Table 12 shows the reset timing specifications for p_rst_l and s_rst_l.

Table 12. Reset Timing Specifications (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
T_{rst}	p_rst_l active time after power stable	1	—	µs
$T_{rst-clk}$	p_rst_l active time after p_clk stable	100	—	µs
$T_{rst-off}$	p_rst_l active-to-output float delay	—	40	ns
T_{srst}	s_rst_l active after p_rst_l assertion	—	40	ns
$T_{srst-on}$	s_rst_l active time after s_clk stable	100	—	µs
T_{dsrst}	s_rst_l deassertion after p_rst_l deassertion	0	25	Cycles
–	p_rst_l slew rate[a]	50	—	mV/ns

Table 12. Reset Timing Specifications (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
T_{rrsus}	s_req64_l asserted to s_rst_l deasserted	10*T_{cyc}	—	ns[a]
T_{rrval}	s_rst_l to s_req64_l deasserted delay time	0 T_{cyc}	—	ns[a]
T_{rrsu}	REQ64# to RST# deasserting setup time	T_{cyc}	—	ns
T_{rrh}	REQ64# from RST# deasserting hold time	0	50	ns

a. Applies to rising (deasserting) edge only.

3.4.4 Serial ROM Timing Specifications

Table 13 shows the serial ROM timing specifications.

Table 13. Serial ROM Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{scval}	pclk to pr_ad[0] serial ROM clock valid	—	14	ns
T_{son}	pr_ad float to active delay	2	—	ns
T_{soff}	pr_ad active to float delay	—	28	ns
T_{ssu}	pr_ad[1] di to pr_ad[0] serial ROM clock setup time	400	—	ns
T_{sh}	pr_ad[1] to pr_ad[0] serial ROM clock hold time	20	—	ns
T_{smcs}	sr_cs minimum low time	400	—	ns
T_{scyc}	pr_ad[0] serial ROM clock cycle time	1000	—	ns

3.4.5 Parallel ROM Timing Specifications

Table 14 shows the parallel ROM timing specifications.

Table 14. Parallel ROM Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{pas}	pr_ale_l setup to pr_clk rising	30	—	ns
T_{pcc}	pr_clk cycle time	60	—	ns
T_{pacs}	pr_ale_l rising to pr_cs_l falling	25	—	ns
T_{pcsl}	pr_cs_l low	200	—	ns
T_{pcrw}	pr_cs_l falling to pr_rd_l or pr_wr_l falling	25	—	ns
T_{prs}	pr_ad setup time to pr_rd_l rising	180	—	ns
T_{prh}	pr_ad hold time from pr_rd_l rising	0	—	ns
T_{prv}	pr_clk rising to pr_ad valid	0	15	ns

3.4.6 JTAG Timing Specifications

Table 15 shows the JTAG timing specifications.

Table 15. JTAG Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{jr}	tck frequency	0	5	MHz
T_{jp}	tck period	200	∞	ns
T_{ght}	tck high time	100	—	ns
T_{glt}	tck low time	100	—	ns
T_{jrt}	tck rise time[a]	—	10	ns
T_{gft}	tck fall time[b]	—	10	ns
T_{js}	tdi, tms setup time to tck rising edge	10	—	ns
T_{jh}	tdi, tms hold time from tck rising edge	25	—	ns
T_{jd}	tdo valid delay from tck falling edge[c]	—	30	ns
T_{jfd}	tdo float delay from tck falling edge	—	30	ns

a. Measured between 0.8 V and 2.0 V.
b. Measured between 2.0 V and 0.8 V.
c. C_1=50 pF.

4.0 Mechanical Specifications

The 21555 is contained in an industry-standard 304 PBGA, a four-layer plastic ball grid array package, as shown in Figure 6.

Figure 6. 304 PBGA (Four-Layer) Package

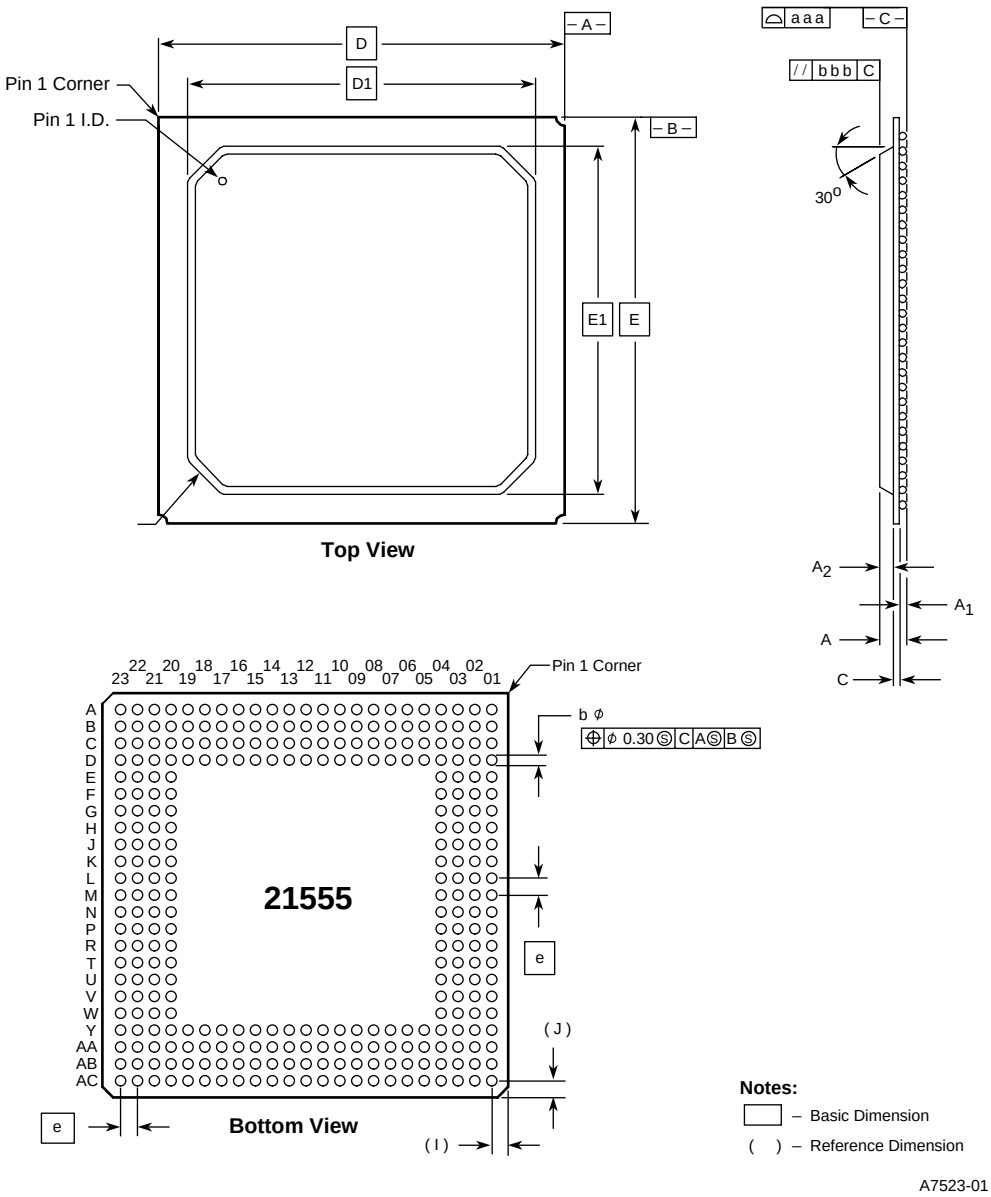


Table 16 lists the package dimensions in millimeters.

Table 16. 304-Point 4-Layer PBGA Package Dimensions

Symbol	Dimension	Minimum Value	Nominal Value	Maximum Value
e	Ball pitch	—	1.27 BSC[a]	—
A	Overall package height	2.12	2.33	2.54
A_1	Package standoff height	0.50	0.60	0.70
A_2	Encapsulation thickness	1.12	1.17	1.22
b	Ball diameter	0.60	0.76	0.90
C	Substrate thickness		0.56 reference[b]	
aaa	Coplanarity	—	—	0.2
bbb	Overall package planarity	—	—	0.15
D	Overall package width	30.80	31.00	31.20
D_1	Overall encapsulation width	—	26.00	26.70
E	Overall package width	30.80	31.00	31.20
E_1	Overall encapsulation width	—	26.00	26.70
I	Location of first row (*x*-direction)	—	1.53 reference[b]	—
J	Location of first row (*y*-direction)	—	1.53 reference[b]	—

a. ANSI Y14.5M-1982 American National Standard Dimensioning and Tolerancing, Section 1.3.2, defines Basic Dimension (BSC) as: A numerical value used to describe the theoretically exact size, profile, orientation, or location of a feature or datum target. It is the basis from which permissible variations are established by tolerances on other dimensions, in notes, or in feature control frames.
b. The value for this measurement is for reference only.

21555 Non-Transparent PCI-to-PCI Bridge

Specification Update

December 2002

Notice: The 21555 may contain design defects or errors known as errata. Characterized errata that may cause the 21555's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278337-008

Contents

Revision History 5
Preface 7
Summary Table of Changes 8
Identification Information 11
Errata 12
Specification Changes 14
Specification Clarifications 15
Documentation Changes 16

Revision History

Date	Version	Description
12/19/02	008	The following changes have been made to this document: • 21555 bridge steppings have changed to A3. Markings have been updated as well. See "Markings" on page 11. • Added related document to "Affected Documents/Related Documents" on page 7. • Status for Errata 1 and 2 are changed to Fixed. See "Errata" on page 9. • Specification change - 21555 bridge PCI compliancy now at Version 2.3. See "Specification Changes" on page 9. • Documentation changes - Data sheet and User Manual include 2.3 compliance information. See "Added Section 3.1.1 PCI Local Bus Compliance" on page 22. and "Change to Tables 61 and 62 in Section 16.5.2" on page 22.
6/12/02	007	Added Errata 2.
4/12/02	006	Added Errata 1.
6/11/01	005	Corrected PBGA package description from 2-layer to 4-layer within this document.
6/7/01	004	Documentation changes: (See page 9) • Replaced last row of Table 2-3. See Section 14 on Page 21. • Changed l_stat description in Section 11-5. See Section 15 on Page 22.
5/24/01	003	Documentation changes: (See page 8) • Added Markings Table on page 11. • Insert reference to 21554 for improved accuracy. See Section 3 on Page 16. • Remove misplaced sections from Chapter 4. See Section 4 on Page 17. • Remove unnecessary parenthetical phrase. See Section 5 on Page 19. • Change **p_clk** and **s_clk** signal description. See Section 6 on Page 19. • Remove incorrect sentence from Hot Swap input pin description. See Section 7 on Page 19. • Change or remove three (3) references to the 21554. See Section 8 on Page 19. • Update D7:D6 byte offset descriptions. See Section 9 on Page 20. • Remove three references to CLS=4. See Section 10 on Page 20. • Additional information about JTAG pin termination requirements. See Section 11 on Page 20. • Emphasize special handling of the JTAG **tms** signal for Hot insertion applications.See Section 12 on Page 20. • Changed Section 12.2.1 and JTAG description. See Section 13 on Page 21.
9/15/00	002	Added specification change to PBGA package dimensions for coplanarity maximum value.
2/21/00	001	This new Specification Update document contains: • One Specification Change that announces coplanarity value changes. Two Documentation changes that: • Correct the JTAG timing specifications. • Correct the coplanarity values in the datasheet document.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
21555 Non-Transparent PCI-to-PCI Bridge Advance Information Datasheet (specification)	278320
21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual	278321
21555AA/BA and 21555AB/BB Differences Application Note	278669

Nomenclature

Errata are design defects or errors. These may cause the 21555's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the **21555 Non-Transparent PCI-to-PCI Bridge** product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark)	
or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings		Page	Status	ERRATA
	A2	A3			
1.	X		12	Fixed	"21555AA/BA boundary Scan Implementation is not compliant with IEEE 1149.1"
2.	X		13	Fixed	"21555AA/BA I2O Circuitry Will Not Work Asynchronously"

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	A2	A3			
1	X	X	14	Doc change	PBGA Package Dimensions for coplanarity changed from maximum value 0.15 mm to maximum value 0.2 mm.
2		X	14	Doc change	PCI 2.3 Compliance

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	DOCUMENTATION CHANGES
1	278320-001	16	Datasheet "Section 3.4.6: JTAG Timing Specifications"
2	278320-001	16	Datasheet "Section 4.0, Table 16, 304-Point 4-Layer PBGA Package Dimensions"
3	278321-001	16	User's Manual: "Add a Specific Reference to 21554 to first Introduction Paragraph"
4	278321-001	17	User's Manual: "Remove Sections 4.2 through 4.2.4 to Section 2.3.4"
5	278321-001	19	User's Manual: "Remove unnecessary parenthetical phrase from ROM Interface Signal description"
6	278321-001	19	User's Manual: "Table 10-1 p_clk and s_clk descriptions need correction and updating"
7	278321-001	19	User's Manual:"Section 11.2.1, Hot Insertion Input Pin Description Change"
8	278321-001	19	User's Manual: "Remove or change 3 incorrect references to the 21554"
9	278321-001	20	User's Manual: "Section 16.1Byte Offset of D7:D6 needs updating"

Documentation Changes

10	278321-001	20	User's Manual: "Remove reference to CLS=4"
11	278321-001	20	User's Manual: "JTAG Action during Hot insertion"
12	278321-001	20	User's Manual: "Internal and External Signal Terminations"
13	278321-001	21	User's Manual: "Change to Initialization Section 12.2.1 and JTAG Description"
14	278321-001	21	User's Manual: "Change to Chapter 2, Table 2-3 p_req64_l description"
15	278321-001	22	User's Manual: "Change to Section 11.5 l_stat pin description"
16	278320-001	22	Data sheet: "Added Section 3.1.1 PCI Local Bus Compliance"
16	278321-001	22	User's Manual: "Change to Tables 61 and 62 in Section 16.5.2"

Identification Information

Markings

Package Markings	REV_ID Register Value[1]	Speed (MHz)	Stepping
Intel FW21555AA	02h	33	A2
Intel FW21555BA	02h	66	A2
Intel FW21555AB	03h	33	A3
Intel FW21555BB	03h	66	A3

1. Identified in a PCI system by reading the value in the REV_ID register.

Errata

1. 21555AA/BA boundary Scan Implementation is not compliant with IEEE 1149.1

Problem: There is a one cycle delay before valid BSDL data is pushed out to the pins. The problem is due to an incorrect inversion in the equation that generates the JTAG update.

Implication: The parallel output data from any bi-directional pins, purely output pins or control cells, will be driven out exactly one clock after the UPDATE state. This is in violation of the IEEE1149.1 Specification.

Workaround: Although the 21555 JTAG implementation is non-compliant, it may still be usable for test purposes if the following considerations are understood:

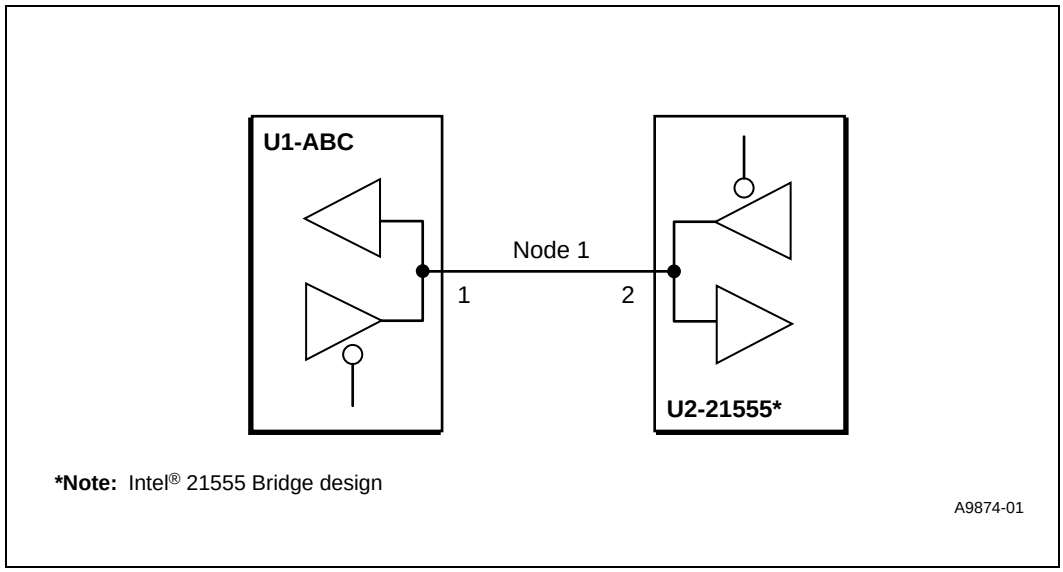
Workaround 1: In-Circuit testers should test for the parallel output data to be on the pins of the chip, at least one clock after the UPDATE state. Typically Automated Test Pattern Generator (ATPG) test vectors will test for this state upon exiting the UPDATE state. This test should be delayed one clock from the ATPG vectors. Also, In-Circuit testers should ensure that data is driven onto pins of the 21555, one clock after UPDATE, to avoid any potential of back driving a pin.

Workaround 2: Standalone boundary scan testers and In-Circuit testers performing chained boundary scan tests, should understand that the Parallel Output UPDATE data, being delayed by one clock, may cause bus contention and back driving during that one clock period, assuming the vectors change bus driving sources in one vector. This is because in chained boundary scan tests, all components execute TAP instructions in Parallel (or lock step), and vector generation algorithms optimize the number of vectors.

To understand the potential issue in detail, refer to the diagram below. Node 1 is a bi-directional node, with U1.1 and U2.2 connected as shown. Assuming that U1 is an IEEE1149.1 compliant device, that U2 is the 21555, and that the control cells of the 21555 were set during the vectors to enable the driver of U2.2 to drive to U1.1 (receiver). When switching drivers from U2 to U1, U2 should tri-state its driver prior to, or at the same time as, U1 enables its driver. Since the 21555 UPDATES its Parallel Outputs one clock late and the control cells which enable U2's drivers are Parallel Outputs which again updates one clock cycle late then U2.2, which will be driving at the same time U1.1 is driving. This contention will happen for one TCK cycle, until U2 UPDATES its parallel outputs. The period of this contention is dependent on the TCK frequency rate.

A remedy to the 21555's late UPDATE is to ensure the chained Boundary Scan tester's vectors do not switch bus driver directions in one vector. This means that one vector should disable U2's driver, and the next vector should enable U1's driver. ATPG vectors typically are not manually manageable in this way and this requirement may force an engineer's manual intervention. No single stepping of test clock through the TAP State Machine should be allowed with the 21555 in the boundary scan chain. The resulting contention would increase the potential back drive time, increasing the possibility of device damage.

Figure 1. Node Boundary



Status: Fixed.This behavior has been corrected in the 21555AB/BB Step A3 device.

2. 21555AA/BA I²O Circuitry Will Not Work Asynchronously

Problem: The I^2O circuitry does not function properly in asynchronous mode.

The root cause of this problem is the synchronization logic between the primary and secondary clock domains - they are incorrectly wired.

Implication: The I^2O circuitry will not function in asynchronous mode and can hang the system.

Workaround: There is no workaround for applications that require asynchronous operation of the I^2O circuitry. Although the 21555 I^2O circuitry is improperly implemented for asynchronous operation, the device will work properly in synchronous mode.

Status: Fixed. This behavior has been corrected in the 21555AB/BB Step A3 device.

Note: No changes were made to the BSDL file when correcting this problem.

Specification Changes

1. PBGA Package Dimensions for coplanarity changed from maximum value 0.15 mm to maximum value 0.2 mm.

Per PCN notification 961, the 304-point 4-layer PBGA package dimensions for symbol aaa, coplanarity, are changed from maximum value 0.15 mm to maximum value 0.2 mm.

2. PCI 2.3 Compliance

The PCI Special Interest Group ratified the PCI version 2.3 specification. To meet new requirements, an additional bit was added in the Command Register and an additional bit added in the Status Register of the 21555 bridge. The new register bits information is presented in the "Documentation Changes" section of this Specification Update.

Specification Clarifications

1. None for this revision of this specification update.

Documentation Changes

1. Section 3.4.6: JTAG Timing Specifications

Table 1 has been updated and now appears as follows:

Table 1. JTAG Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{jr}	tck frequency	0	5	MHz
T_{jp}	tck period	200	∞	ns
T_{ght}	tck high time	100	—	ns
T_{glt}	tck low time	100	—	ns
T_{jrt}	tck rise time[1]	—	10	ns
T_{gft}	tck fall time[2]	—	10	ns
T_{js}	tdi, tms setup time to tck rising edge	10	—	ns
T_{jh}	tdi, tms hold time from tck rising edge	25	—	ns
T_{jd}	tdo valid delay from tck falling edge[3]	—	30	ns
T_{jfd}	tdo float delay from tck falling edge	—	30	ns

1. Measured between 0.8 V and 2.0 V.
2. Measured between 2.0 V and 0.8 V.
3. C_1=50 pF.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information Datasheet (278320).*

2. Section 4.0, Table 16, 304-Point 4-Layer PBGA Package Dimensions

Issue: The maximum value for symbol aaa, dimension coplanarity, has been changed from 0.15 mm to a value of 0.2 mm.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information Datasheet (278320).*

3. Add a Specific Reference to 21554 to first Introduction Paragraph

Issue: Refer to Chapter 1, Page 1-1, first paragraph, third sentence, first clause: change:
"A related peripheral device, " to say "The 21554, a related peripheral device, has a 64-bit primary interface,".
The entire paragraph should appear as follows: "Intel's 21555 is a PCI peripheral device that performs PCI bridging functions for embedded and intelligent I/O applications. The 21555 has a 64-bit primary interface, a 64-bit secondary interface, and 66-MHz capability. The 21554 a related PCI peripheral device, has a 64-bit primary interface, a 64-bit secondary interface, and 33-MHz capability."

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

4. Remove Sections 4.2 through 4.2.4 to Section 2.3.4

Issue: Remove these sections:

4.2 64-Bit Operation

The 21555 provides 64-bit extension support on the primary and secondary interfaces. Both 64-bit and 32-bit operation are supported on both interfaces.

This section describes how to use the 64-bit extensions. It describes the conditions under which a transaction can be treated as a 64-bit transaction and includes information about how the transaction is forwarded.

4.2.1 Address Phase of 64-Bit Transactions

When a transaction using the primary bus 64-bit extension is a single address cycle (SAC)—that is, the address falls below the 4GB boundary, and the upper 32 bits of the address are assumed to be zero—**AD<63:32>** and **C/BE#<7:4>** are not defined but are driven to valid logic level during the address phase.

When the transaction is a dual address cycle (DAC), that is, the address falls above the 4GB boundary and the upper 32 bits of the address are non-zero, signals **AD<63:32>** contain the upper 32 bits of the address for both address phases. Signals **C/BE#<7:4>** contain the memory bus command during both address phases. A 64-bit target then has the opportunity to decode the entire 64-bit address and bus command after the first address phase. A 32-bit target needs both address phases to decode the full address and bus command.

4.2.2 Data Phase of 64-Bit Transactions

During memory write transactions, when the 21555 has driven **REQ64#** to indicate it is initiating a 64-bit transfer, the 21555 drives the following during the data phase:

- The low 32 bits of data on **AD<31:0>**
- The low four byte enable bits on **C/BE#<3:0>**
- The high 32 bits of data on **AD<63:32>**
- The high four byte enable bits on **C/BE#<7:4>**

When the 21555 detects **ACK64#** asserted by the target at the same time that it detects **DEVSEL#** asserted, every data phase then consists of 64 bits and eight byte enable bits.

For write transactions, when the 21555 does not detect **ACK64#** asserted at the same time that it detects **DEVSEL#** asserted, the 21555 redirects the write data that it has on the **AD<63:32>** bus to **AD<31:0>** during the second data phase. Similarly, the upper four byte enable bits are redirected to **C/BE#<3:0>** during the second data phase. All data phases then consist of 32 bits.

For 64-bit memory write transactions that end at an odd Dword boundary, the 21555 drives the byte enable bits to 1 during the last data phase. Signals **AD<63:32>** are then unpredictable but are driven to a valid logic level.

For read transactions, when the 21555 has asserted **REQ64#,** it drives 8 bits of byte enables on **C/BE#<7:0>**. Since the only read transactions that use the 64-bit extension are prefetchable memory read transactions, the byte enable bits are always zero. Therefore, no special redirection is needed based on the target's assertion or lack of assertion of **ACK64#**. When the target asserts **ACK64#** at the same time that it asserts **DEVSEL#**, all read data transfers then consist of 64 bits and the target drives **PAR64**, which covers **AD<63:32>** and **C/BE#<7:4>**. When the target does not assert **ACK64#** when it asserts **DEVSEL#**, all data phases then consist of 32 bits.

4.2.3 64-Bit Transactions Received by the 21555

When the 21555 is the target of a transaction and the 21555 detects **REQ64#** asserted during a memory transaction to be forwarded across the bridge, the 21555 either asserts **ACK64#** at the same time that it asserts **DEVSEL#** to indicate its ability to perform 64-bit data transfers. Under certain circumstances, the 21555 does not use the 64-bit extension as a target and therefore does not assert **ACK64#**.

The 21555 does not assert **ACK64#** when any of the following is true:

- Signal **REQ64#** was not asserted by the initiator.
- The 21555 is responding to a non-prefetchable memory read transaction.
- The 21555 is responding to an I/O transaction.
- The 21555 is responding to a configuration transaction.
- Only 1 Dword of data was read from the target.

When the 21555 is the target of a 64-bit memory write transaction, it is able to accept 64 bits of data during each data phase.

When the 21555 is the target of a 64-bit prefetchable memory read transaction, it supplies 64 bits of read data during each data phase and drives **PAR64** corresponding to **AD<63:32>** and **C/BE#<7:4>**, for each data phase. When an odd number of Dwords was read from the target and the 21555 has asserted **ACK64#** when returning read data to the initiator, the 21555 disconnects before the last odd Dword is returned. The 21555 may have read an odd number of Dwords because of either a target disconnect or a master latency timer expiration during 32-bit data transfers on the opposite interface.

4.2.4 64-Bit Extension Support During Reset

When the 21555 supports a 64-bit interface on its primary bus, it samples **p_req64_l** while **p_rst_l** is asserted to determine whether the PCI 64-bit extension signals are connected on the board. When **p_req64_l** is high, the 64-bit extension signals are not connected and the 21555 drives the 64-bit extension outputs to have valid logic levels on the inputs. The 21555 treats all transactions on the primary interface as 32-bit transactions. When **p_req64_l** is low, the 64-bit signals are connected to pull-up resistors on the board and the 21555 does not perform any input biasing. In this case, the 21555 can treat memory write and prefetchable memory read transactions as 64-bit transactions on the primary interface, as previously described in this section.

The 21555 always asserts **s_req64_l** low during **s_rst_l** assertion to indicate that the 64-bit extension is supported on the secondary bus. Individual pull-up resistors must always be supplied for **s_ad<63:32>**, **s_cbe_l<7:4>**, and **s_par6**4.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

5. Remove unnecessary parenthetical phrase from ROM Interface Signal description

Issue: Refer to Section 6.1, Table 6-1, Page 6-2. Under pr_ad[6], remove from the last sentence: "(if implemented)."

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

6. Table 10-1 p_clk and s_clk descriptions need correction and updating

Issue: Refer to Table 10-1, pages 10-1 and 10-2, the last sentences in the **p_clk** and **s_clk** Signal Name descriptions. The sentences are inaccurate. The paragraphs below contain the corrected sentences.

p_clk	I	Primary interface PCI CLK. This signal provides timing for all transactions on the primary PCI bus. All primary PCI inputs are sampled on the rising edge of **p_clk**, and all primary PCI outputs are driven from the rising edge of **p_clk**. The 21555 operates in a frequency range from 0 MHz to 66 MHz in synchronous mode. In asynchronous mode the 21555 supports a clocking ratio (defined p_clk : s_clk or s_clk : p_clk) of a maximum ratio 2.5 : 1 with the upper frequency limit for either clock input being 66MHz.

s_clk	I	Secondary interface PCI CLK. This signal provides timing for all transactions on the secondary PCI bus. All secondary PCI inputs are sampled on the rising edge of **s_clk**, and all secondary PCI outputs are driven from the rising edge of **s_clk**. The 21555 operates in a frequency range from 0 MHz to 66 MHz in synchronous mode. In asynchronous mode the 21555 supports a clocking ratio (defined p_clk : s_clk or s_clk : p_clk) of a maximum ratio 2.5 : 1 with the upper frequency limit for either clock input being 66MHz

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

7. Section 11.2.1, Hot Insertion Input Pin Description Change

Issue: Refer to section 11.2.1, on page 11-3, Last paragraph. Remove the last sentence That paragraph should appear as follows:
"The 21555 is selected to be the secondary bus central function when it detects **pr_ad[6]** low when **s_rst_l** is asserted. When the 21555 detects this condition, it immediately drives **s_ad**, **s_cbe_l**, and **s_par** low and tristates secondary bus control signals for the duration of secondary bus reset. When the 21555 implements a 64-bit secondary interface, it also asserts **s_req64_l**, but tristates all other secondary bus 64-bit extension signals."

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

8. Remove or change 3 incorrect references to the 21554

Issue: The following three entries that refer to the 21554 were modified:

- Page 9-3, Table 9-3, Row Labeled "Downstream Delayed Read", Change "21554" to "21555".
- Page 9-4, Table 9-3, Row Labeled "Upstream Delayed Read", Change "21554" to "21555".
- Section 11.3, Page 11-4, End of Step 3, Remove "(21554 only.)".

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

9. Section 16.1Byte Offset of D7:D6 needs updating

Issue: Refer to Section 16.1, Table 16-1, on page 16-4, the D7:D6 Byte Offset Register Name and Reset Value row. Add the following information to the Register Name and Reset Value (Hex) columns.

D5	Secondary SERR# Disable	00	Y	Y	Y
D7:D6	Mode Settings Configuration Register	Determined by Parallel ROM Strapping Options	—	N	Y
DB:D8	Reset Control	0000	—	Primary	Y

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

10. Remove reference to CLS=4

Issue: Remove the following lines:
Section 2.3.1.4, Page 2-14 delete "A full cache line threshold is used for CLS=4".
Section 2.4.2.2, Table 2-25, Page 2-36. Delete two sentences: "When CLS=4 a full cache line threshold is used.".

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321)*

11. JTAG Action during Hot insertion

Issue: Change Table 12-1 row 3 to be as follows:

tms	I	The JTAG test mode select pin, **tms** causes state transitions in the Test Access Port (TAP) controller. The **tms** signal is pulled high by a weak pull-up resistor internal to the device. If this pin is low while **t_rst_l** is low the device can enter an unsupported mode. Other devices that are not on early power and are connected to the JTAG Scan Chain, pull **tms** low during Hot Insertion causing the 21555 to enter the unsupported mode. During the Hot Insertion isolate this signal from other JTAG devices on the circuit board or JTAG scan chain.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

12. Internal and External Signal Terminations

Issue: Change Table 12-1 rows 1 and 4 to be as follows:

tck	I	JTAG boundary-scan clock. Signal **tck** is the JTAG logic control clock. This pin has an internal weak pull-down resistor.
trst_l	I	JTAG TAP reset and disable. When low, JTAG is disabled and the TAP controller is asynchronously forced into the reset state, which in turn asynchronously initializes other test logic. An unterminated **trst_l** is pulled high by a weak pull-up resistor internal to the device. The TAP controller must be reset before the JTAG circuits can function. For normal JTAG TAP port operation, this signal must be high. Prior to normal 21555 operation, this signal must be strobed low or pulled low with a 1kΩ resistor.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

13. Change to Initialization Section 12.2.1 and JTAG Description

Issue: Change to second paragraph. Also made a change to normal operation description note for JTAG below Figure 12-1. The section now appears as follows:

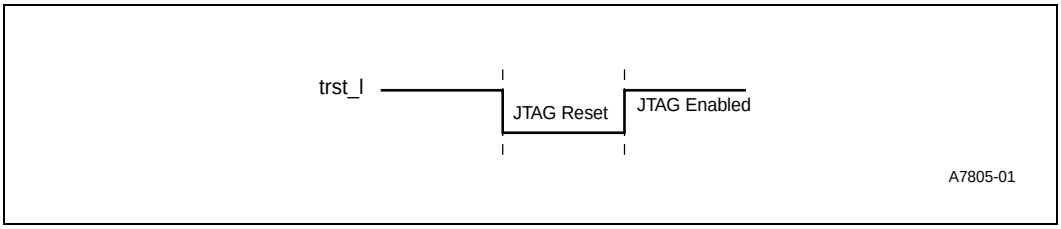
12.2.1 Initialization

The test access port controller and the instruction register output latches are initialized and JTAG is disabled while the **trst_l** input is asserted low (see Figure 12-1). While signal **trst_l** is low, the test access port controller enters the test-logic reset state. This results in the instruction register being reset which holds the bypass register instruction. During test-logic reset state, all JTAG test logic is disabled, and the device performs normal functions. The test access port controller leaves this state only after **trst_l** (low) goes high and an appropriate JTAG test operation sequence is sent on the tms and tck pins.

For the 21555 to operate properly, the JTAG logic must be reset. The controller resets:

- Asynchronously with the assertion of **trst_l** .
- Synchronously after five **tck** clock cycles, with **tms** held high.

Figure 12-1. Signal trst_l States



Note: Prior to normal 21555 operation, this signal must be strobed low or pulled low with a 1kΩ resistor.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

14. Change to Chapter 2, Table 2-3 p_req64_l description

Issue: The last row of Table 2-3 now appears as follows:

p_req64_l	STS	Primary PCI interface request 64-bit transfer. Signal p_req64_l is asserted by the initiator to indicate that the initiator is requesting 64-bit data transfer. Signal p_req64_l has the same timing as p_frame_l. When deasserting, p_req64_l is driven to a deasserted state for one clock cycle and is then sustained by an external pull-up resistor. The 21555 samples p_req64_l during primary reset to enable the 64-bit extension signals. If p_req64_l is sampled high during primary reset, the primary 64-bit extension is disabled and assumed not connected. The 21555 then drives p_ad[63:32], p_cbe_l[7:4], and p_par64 to valid logic levels. ***Note:*** Refer to the ROM Interface signal pr_ad[1] description in Chapter 6, Table 6-1 for information on primary bus 64-bit extension operation upon deassertion of r_rst_in_l.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

15. Change to Section 11.5 l_stat pin description

Issue: Last bullet changed and last note removed. The last bullet now appears as follows:

•Support bi-directional pin, l_stat. This signal functions as both a micro-switch sensor input and a LED control output. 2 ms of debounce is built into the 21555 l_stat pin.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

16. Added Section 3.1.1 PCI Local Bus Compliance

Issue: Added Section 3.1.1 that includes new bit information to meet *PCI Local Bus Specification 2.3* requirements. The new section appears as follows:

3.1.1 Added Bits for PCI Local Bus Specification 2.3 Compliance

Two bits were added to the 21555 bridge to meet *PCI Local Bus Specification 2.3* requirements: Bit 10 in the Command Registers and Bit 3 in the Status Registers. The A3 Stepping of the bridge now includes these new features.

Note: For a description of the added bits, please refer to the *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual.*

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Datasheet (278320).*

17. Change to Tables 61 and 62 in Section 16.5.2

Issue: Two bits were added to the 21555 bridge to meet *PCI Local Bus Specification 2.3* requirements. As a result, Bit 10 information was added to Table 61 in Section 16.5.2 in the Command Registers and Bit 3 information was added to Table 62 in Section 16.5.2 in the Status Registers. The A3 Stepping of the bridge now includes these new features. The new information appears in the tables as follows:

Table 61. Primary and Secondary Command Registers

Offsets	Primary Command	Secondary Command
Primary byte	05:04h	45:44h
Secondary byte	45:44h	05:04h

Bit	Name	R/W	Description
10[1]	Interrupt Disable Bit	R/W	This bit disables the 21555 from asserting p_inta_l / s_inta_l. • When 0, enables the 21555 to assert its p_inta_l / s_inta_l signal. • When 1, disables the 21555 ability to assert the p_inta_l / s_inta_l signal. This bit's state after RST# is 0.

1. Bit not used and does not apply to Step A2 of product

Table 62. Primary and Secondary Status Registers

Offsets	Primary Status	Secondary Status
Primary byte	07:06h	47:46h
Secondary byte	47:46h	07:06h

Bit	Name	R/W	Description
3[1]	Interrupt Status Bit	R	This bit reflects the state of the interrupt in the 21555 bridge. • Only when the Interrupt Disable Bit in the command register is set to 0 and the appropriate interrupt status bit set to 1 will the p_inta_l/s_inta_l signals be asserted. • Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.

1. Bit not used and does not apply to Step A2 of product

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

21555AA/BA and 21555AB/BB Differences

Application Note

October 2002

Order Number: 278669-001

Contents

1.0 Introduction 5
1.1 Changes to the 21555 Bridge 5
2.0 Stepping Differences 5
3.0 I2O Asynchronous Operation 5
4.0 BSDL Data Being Driven Late 6
5.0 New Feature - PCI 2.3 Compliance 6

1.0 Introduction

This document defines the differences between the 21555AA/BA bridge when compared with the 21555AB/BB bridge. The 21555 bridge is a second generation Non-Transparent PCI-to-PCI bridge.

1.1 Changes to the 21555 Bridge

After the introduction of the 21555AA/BA bridge, two errata were discovered

- The I_2O circuitry would not work in asynchronous mode.
- The BSDL circuitry was driving data one cycle late.

Additionally, the PCI standards committee ratified the new PCI 2.3 Specification, which required an additional bit to be added to the control register and status register.

The new 21555AB/BB bridge version addresses all three of these issues.

Note: This Differences document is not a stand-alone document and does not provide complete 21555 bridge details. The intent here is only to highlight the feature differences between the 21555AA/BA and the 21555BA/BB steppings. Please be sure to review the data sheet and spec updates for more complete information on the device.

2.0 Stepping Differences

Table 1. Stepping Differences

Package Markings	REV_ID Register Value[a]	Speed (MHz)	Stepping
Intel FW21555AA	02h	33	A2
Intel FW21555BA	02h	66	A2
Intel FW21555AB	03h	33	A3
Intel FW21555BB	03h	66	A3

a. Identified in a PCI system by reading the value in the REV_ID register.

3.0 I2O Asynchronous Operation

The 21555AA/BA devices would not operate asynchronously. This behavior has been corrected in the 21555AB/BB device. Please refer to the device data sheet for information on I_2O operation.

4.0 BSDL Data Being Driven Late

The 21555AA/BA BSDL (Boundary-Scan Description Language) data was being driven one clock cycle late causing a potential device contention issue if BSDL was single stepped during testing. This behavior has been corrected in the 21555AB/BB device. The BSDL file does not change.

5.0 New Feature - PCI 2.3 Compliance

The PCI Special Interest Group ratified the PCI 2.3 specification requiring an additional bit in the control register and an additional bit in the status register. The new register bits are as follows:

Table 1. Primary and Secondary Command Registers

Offsets	Primary Command	Secondary Command
Primary byte	05:04h	45:44h
Secondary byte	45:44h	05:04h

Bit	Name	R/W	Description
10	Interrupt Disable Bit	R/W	This bit disables the 21555 from asserting p_inta_l / s_inta_l. • When 0, enables the 21555 to assert its p_inta_l / s_inta_l signal. • When 1, disables the 21555 ability to assert the p_inta_l / s_inta_l signal. This bit's state after RST# is 0.

Note: Please refer to the following documentation for more information:

- *21555 Non-transparent PCI-to-PCI Bridge Datasheet*
- *21555 Non-transparent PCI-to-PCI Bridge User's Manual*
- *21555 Non-transparent PCI-to-PCI Bridge Hardware Implementation manual*
- *21555 Specification Update*

Table 2. Primary and Secondary Status Registers

Offsets	Primary Status	Secondary Status
Primary byte	07:06h	47:46h
Secondary byte	47:46h	07:06h

Bit	Name	R/W	Description
3	Interrupt Status Bit	R	This bit reflects the state of the interrupt in the 21555 bridge. • Only when the Interrupt Disable Bit in the command register is set to 0 and the appropriate interrupt status bit set to 1 will the p_inta_l/s_inta_l signals be asserted. • Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.