

PI3HDX511F

HDMI 1.4b 3.4Gbps ReDriver Jitter Cleaner with DP++ Level Shifter, Cable ID, DDC Buffer/Switch

Features

- Ultra-low power HDMI 1.4b compliant ReDriver™
- Dual-mode DisplayPort Level Shifter/ReDriver with pin option
- Operation up to 3.4 Gbps per lane (340MHz pixel clock)
- Sink-side application support with TMDS Data & Clock pin swaps and high 15dB EQ options
- 4K2K Ultra-HD, 3D Video formats (1080p, 1080i, 720p), 48-bit per pixel Deep Color support
- Ultra-low standby current 2uA with DDC passive switch mode
- Flexible 6 steps input equalization control steps: 2.5/5/7.5 dB for short cable range and 5/10/15 dB for long cable modes.
- Pre-emphasis 3 steps setting: 0/1.5/2.5 dB
- Automatic TMDS output disable with squelch or HPD detection in the no-signal input condition
- Selectable Active DDC buffer mode for 1.8-3.3V DDC
- Max 120mW with LDO Bypass 1.5V power supply mode
- Integrated ESD Protection: 8kV HBM for all IO pins per JEDEC standard
- Power Supply: 3.3V single or 3.3/1.5V dual power supply
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>

Application(s)

- Notebook, Desktop Computers
- Displays, Monitors
- A/V receivers, Set Top Box, Video Players
- Repeaters and Switch Boxes



Figure 1-1 DP++ Level Shifter in Notebook PC

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

ReDriver is a trademark of Diodes Incorporated.

Description

The DIODES™ PI3HDX511F is a ultra-low power HDMI 1.4b Re-Driver and dual-mode DisplayPort level shifter up to 3.4Gbps data rate with 48-bpp Deep Color support.

In the mobile platforms, extending battery hours have been one of the most challenges for system designers. The PI3HDX511F has rich power saving features to extend the battery life with 2uA stand-by current and other features like LDO disable pins, Active/Passive DDC switch, Output squelch and HPD (Hot plug Detect) detection. The PI3HDX511F can support both source and sink side system application. For Sink side (Recepticle) application, it supports 6-step input EQ adjustment and data/clock pin order swap.

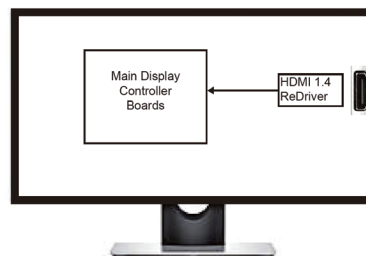


Figure 1-2 HDMI Port in All-In-One PC

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX511FZLCEX	ZLC	40-pin, 3x6mm (TQFN)
PI3HDX511FZLCIEX	ZLC	40-pin, 3x6mm (TQFN)

Notes:

- I = Industrial
- E = Pb-free and Green
- X suffix = Tape/Reel

2. General Information

2.1 Revision History

Date	Description
June 2016	P10 - Add Eye opening measurement with different test set-up in the functional description. Expand I-temp grade support in the ordering information.
July 2016	Add more contents to assist the system design-in in Application page 20 eg. PCB layout, HDMI compliance report.
Sep 2016	Add clarity for the total power dissipation in the Open-drain and the Double termination modes in p1, p12 and p13.
Feb 2017	Add Via in the package mechanical drawing
Jun 2017	I-temp ordering part number added . Diodes Datasheet style updated.
Nov 2017	Package outline drawing updated.
Aug 2018	Remove HDMI active cable/dongle application.
Nov 2020	Updated Package from ZL Package to ZLC Package
Nov 2022	Updated Package Drawing Updated to Official Format

2.2 Products Comparison

	PI3HDX511F	PI3HDX511D	PI3VDP1431	PI3HDX511E
Package	40-pin contact	30-pin contact	32-pin contact	32-pin contact
Body Size(mm)	3x9	2,5x4.5	3x9	3x9
Power Supply	1.5V Core, 3.3V IO power	3.3V	3.3V	3.3V
Data/Clock Pin Swap	Yes	No	No	No
Low Power LDO Bypass	Yes	No	No	No
Power Dissipation	70mA@1.5V, 3mA@3.3V	120mA @ 3.3V	120mA @ 3.3V	120mA @ 3.3V
DDC channels	Passive Switch or Buffers	Passive Switch only	Passive Switch or Buffers	Passive Switch or Buffers
Applications	TMDS ReDriver DP++ Level Shifter	TMDS ReDriver DP++ level shifter	DP++ level shifter	TMDS ReDriver DP++ level shifter
	Sink and Source devices.	Space-limited ultra mobile system	Source Devices like NoteBook PC system	Source Devices requires P2P with PI3HDMI511 earlier part.

2.3 Related Products

Part Numbers	Products Description
PI3DPX1203B	8.1Gbps Displayport 1.4 Linear Redriver. Low-jitter, Latency Free.
PI3HDX1204B1	6Gbps HDMI 2.0 Redriver and Displayport Level Shifter, Low-jitter, High EQ.
PI3HDX414	1:4 Active 3.4Gbps HDMI 1.4b Splitter/DeMux with Signal Conditioning
PI3HDX412BD	1:2 Active 3.4Gbps HDMI 1.4b Splitter/DeMux with Signal Conditioning
PI3HDX621	2:1 Active 3.4Gbps HDMI 1.4b Switch
PI3HDMI336	3:1 Active 2.5Gbps HDMI Switch with I2C control and ARC Transmitter
PI3DPX1202	5.4Gbps Displayport 1.2 Redriver with built-in auto test mode
PI3WVR12612	Wide Voltage Range DisplayPort™ & HDMI Video 1:2 Mux/DeMux

2.4 Reference Document

Document	Description
HDMI 1.4	High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC

2.5 Product Status Definition

	Product Status	Definition
Advanced	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Diodes Incorporated reserves the right to make product specification changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Diodes Incorporated reserves the right to make changes at any time without notice to improve datasheet informative or reference contents.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Diodes Incorporated. The datasheet is for reference information only.

Contents

1. Product Summary	1
2. General Information	2
2.1 Revision History	2
2.2 Products Comparison	2
2.3 Related Products	3
2.4 Reference Document	3
2.5 Product Status Definition	3
3. Pin Configuration	5
3.1 Package Pinout	5
3.2 Pin Description	6
4. Functional Description	8
4.1 Block Diagram	8
4.2 Function Description	9
5. Electrical Specification	12
5.1 Absolute Maximum Ratings	12
5.2 Recommended Operation Conditions	12
5.3 Electrical Characteristics	12
5.4 Output Eye: EQ Settings and Input Trace Length (Informative)	18
6. Applications	20
6.1 HDMI 1.8V DDC Buffer Usage Case	20
6.2 Application Block Diagram	21
6.3 Output Eye Measurement Data	22
6.4 Layout Guidelines	23
6.5 HDMI 2.0 Compliance Test	28
7. Packaging Mechanical, Ordering Information	31
7.1 Packaging Mechanical Outline	31
7.2 Part Marking Information	32
7.3 Tape & Reel Materials and Design	33
8. Important Notice	36

3. Pin Configuration

3.1 Package Pinout

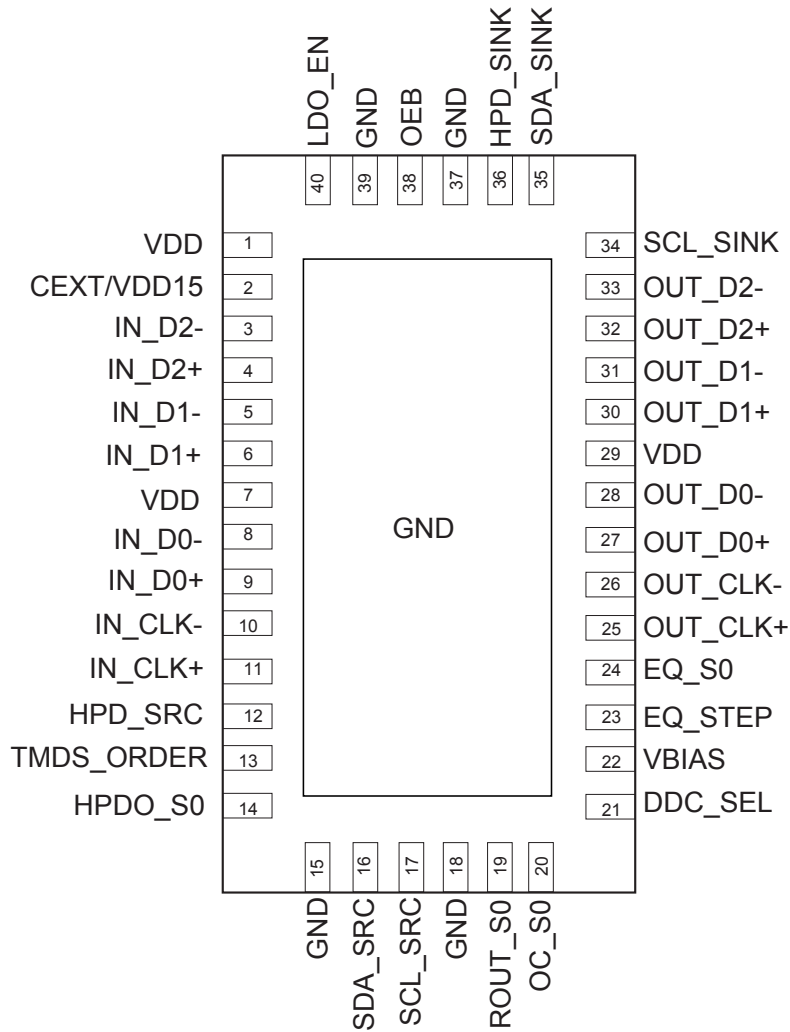


Figure 3-1 Pinout Configuration

3.2 Pin Description

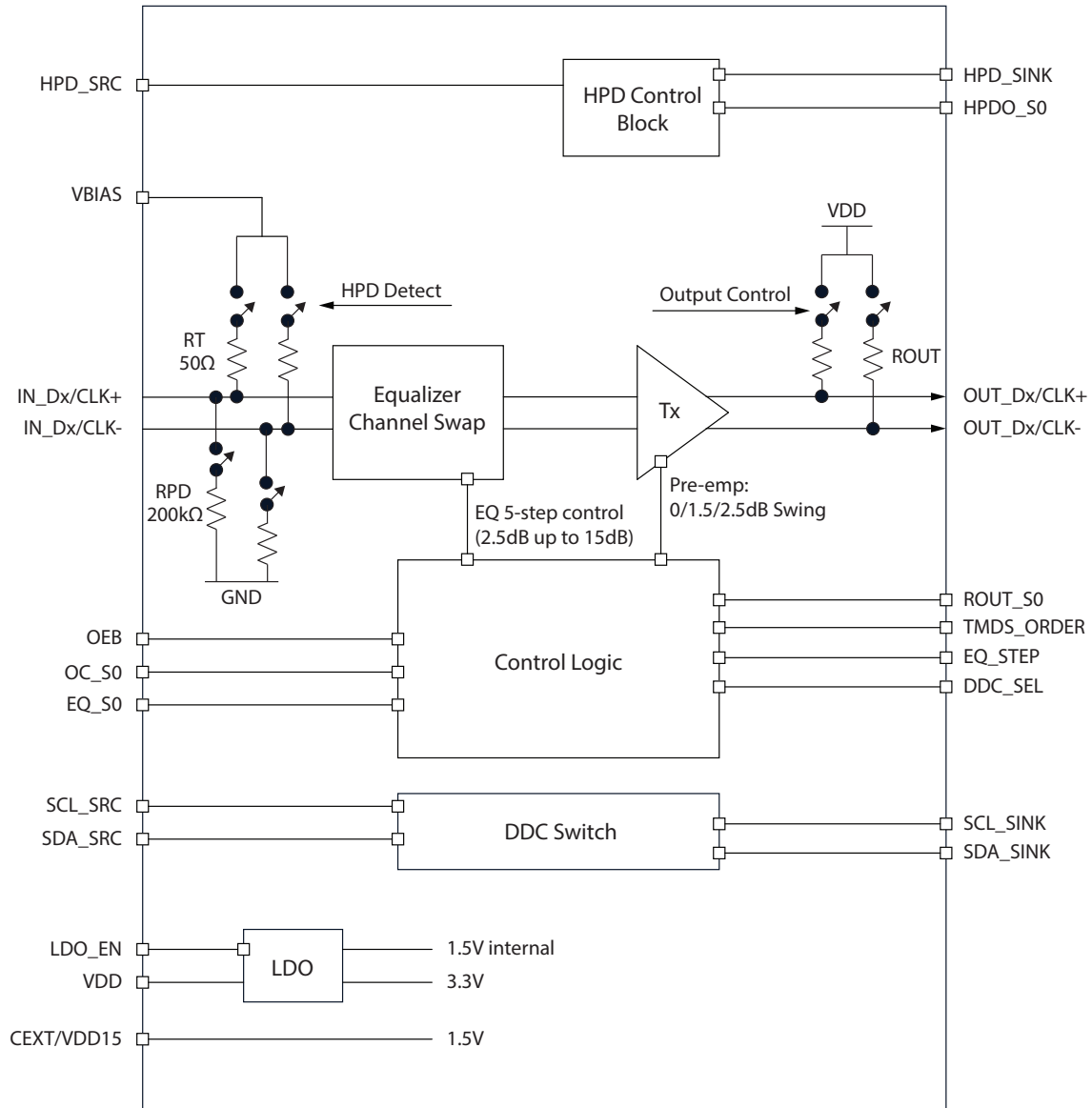
Pin #	Pin Name	Type	Description
1, 7, 29	VDD	PWR	3.3V power supply. Add external 0.1uF decoupling capacitor to GND.
2	CEXT/VDD15	PWR	LDO output for internal core power supplier. VDD15: When LDO_EN is low "0", this shared pin be a VDD15 in dual power supply operation. Apply 1.5V power CEXT: When LDO_EN is high "1", this pin be a CEXT in 3.3V single power supply operation. Add external capacitor (2.2uF-4.7uF) to GND.
3	IN_D2-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
4	IN_D2+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
5	IN_D1-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
6	IN_D1+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
8	IN_D0-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
9	IN_D0+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
10	IN_CLK-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
11	IN_CLK+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
12	HPD_SRC	O	HPD output to source side
13	TMDS_ORDER	I	TMDS pin order swap control with internal pull high. Default is D2/D1/D0/CLK input sequence.
14	HPDO_S0	I	HPD_SRC output control with internal pull high. Default is Open drain output
15, 18, 37, 39, Center Pad	GND	GND	Ground
16	SDA_SRC	IO	Source side DDC Data
17	SCL_SRC	IO	Source side DDC Clock
19	ROUT_S0	I	TMDS output enable with double termination or open-drain selection. Default is Active high, double termination output. Active low is open-drain output. Internal pull high to VDD.
20	OC_S0	I	TMDS output pre-emphasis value selection. Default is 1.5dB pre-emphasis setting. Internally tied with 50% of VDD (or VDD/2).
21	DDC_SEL	I	DDC buffer or Passive switch control. Default is Passive switch mode. Internal pull high.
22	VBIAS	I	TMDS input termination voltage control. Default is HDMI input mode. Internally pull high. Pull-down is for Displayport input mode.
23	EQ_STEP	I	EQ_step selection control. Default is low-side setting of 2.5/5/7.5dB. Internally pull high. High-side EQ values are 5/10/15dB with external pull-down.
24	EQ_S0	I	TMDS input three-level equalization selection. Default is middle EQ value setting. Internally 50% of VDD (VDD/2).
25	OUT_CLK+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
26	OUT_CLK-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
27	OUT_D0+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
28	OUT_D0-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"

Pin Description Cont.

Pin #	Pin Name	Type	Description
30	OUT_D1+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
31	OUT_D1-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
32	OUT_D2+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
33	OUT_D2-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
34	SCL_SINK	IO	Sink side DDC Clock for connector
35	SDA_SINK	IO	Sink side DDC Data for connector
36	HPD_SINK	I	Sink side HPD (Hot Plug Detect) input. Active high pin. Default is inactive for power saving. Internally pull-down at 120 kΩ.
38	OEB	I	Output Enable control. Active low for normal operation. Active high for disable output HDMI signals. Internally pull-down with 100 kΩ.
40	LDO_EN	I	Power supply mode control pin for 1.5/3.3V or 3.3V Default is 3.3V operation with active high. Internally pull high. 1.5/3.3V dual power is active low.

4. Functional Description

4.1 Block Diagram



4.2 Function Description

Squelch Mode

Automatic output squelch function disables TMDS output when no Input signal presents. Output Disable (Squelch) Mode uses TMDS Clock signal detection. When low voltage levels on the TMDS input clock are detected, Squelch state enables and TMDS outputs shall be disabled. When the TMDS clock inputs are above the pre-determined threshold voltage, TMDS outputs shall return to the normal swing voltage levels.

TMDS Output Shut Down

When HPD_SINK pin floats or ties to GND, TMDS outputs shall shut down to sleep mode; HPD_SINK does not control DDC channel. TMDS Pin Order Configuration Table

TMDS_ORDER	Functional Description	Note
"0"	CLK/D0/D1/D2 pin order	
"1" or "NC"	D2/D1/D0/CLK pin order	Default

DDC Mode Selection DDC_SEL Configuration Table

DDC_SEL	Functional Description	Note
"0"	Active DDC Buffer	
"1" or "NC"	Passive Switch	Default

LDO Enable Configuration Table

DDC_SEL	Pin 1	Pin 2	Functional Description
"0"	3.3V	1.5V	Dual power supply mode 3.3/1.5V
"1"	3.3V	External capacitor	Default. Recommend 2.2~4.7uF pull down capacitor.

Pre-emphasis Truth Table

ROUT_S0	OC_S0	Single-end Vswing	Pre-emphasis	Functional Description
"0"	"0"	500 mV	0 dB	Open drain output.
	"NC" or VDD/2	500 mV	1.5 dB	Open drain output(Default)
	"1"	500 mV	2.5 dB	Open drain output
"1"	"0"	500 mV	0 dB	Double termination
	"NC" or VDD/2	500 mV	1.5 dB	Double termination(Default)
	"1"	500 mV	2.5 dB	Double termination

TMDS Input Termination Voltage Control VBIAS

VBIAS	Functional Description
"1", "NC"	HDMI input. VBIAS ties to VDD.
"0"	DisplayPort input. VBIAS ties to GND.

EQ Step Selection Control EQ_STEP

EQ_STEP	Functional Description
"1", "NC"	2.5, 5, 7.5dB EQ setting with EQ_S0 control pin
"0"	5, 10, 15dB EQ setting with EQ_S0 control pin

Output Data Signals EQ_S0 Configuration

EQ_S0	Functional Description		Note
	EQ_STEP = "1"	EQ_STEP = "0"	
"0"	2.5 dB	5 dB	TMDS Clock(CLK) channel EQ is always fixed as 3dB without pre-emphasis.
"NC" , "VDD/2"	5 dB	10 dB	
"1"	7.5 dB	15 dB	

Sink Side Hot Plug Detect HPD_SINK

EQ_STEP	Functional Description
"1"	Normal mode
"0"	Disable output signal for power saving mode

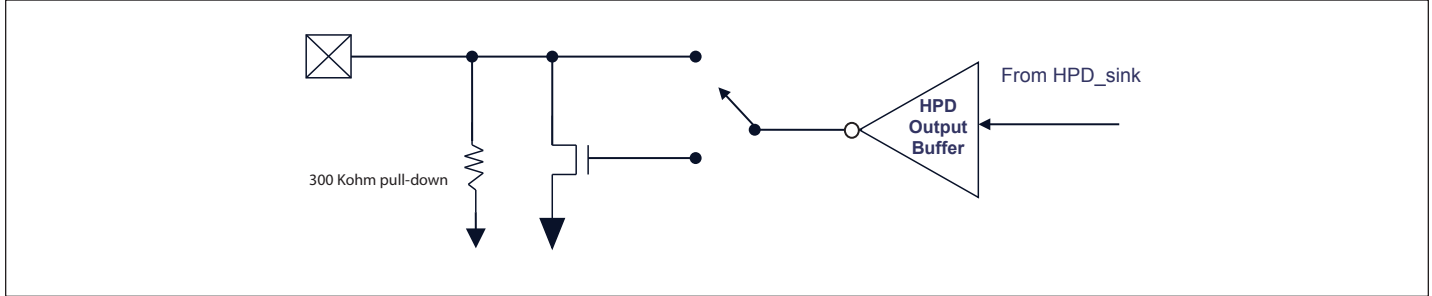
Source Side Hot Plug Detect Output Control HPDO_S0

EQ_STEP	Functional Description
"1" or "NC"	Open drain output (Default)
"0"	Inverted Buffer output of HPD_SINK signal

Output Enable Control Truth Table

EQ_STEP	Functional Description
"0"	Active Low. Normal mode
"1"	Disable output signal for power saving mode PI3HDX511FA

Source-side Output Block Diagram



Note:
1) Open drain buffer is recommended with external pull-up resistor to < 4.5V power supply.

5. Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential	-0.5V to +4.5V
All Input and Output pins	-0.5V to 4.5V
5V Tolerance I/O Pins (SDA_SINK, SCL_SINK, HPD_SINK)	-0.5V to 5.5V
Power Dissipation Continuous	1.0W
ESD, HBM	-2kV to 2kV
Storage Temperature	-65°C to +150°C
Junction Temperature (T _J)	125°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect inoperability and degradation of device reliability and performance.

5.2 Recommended Operation Conditions

Symbol	Parameter ⁽¹⁾	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply Voltage	2.89	3.3	3.6	V
		1.42	1.5	1.57	V
T _A	Ambient Operating Temperature	0		70	°C
	Industrial Operating Temperature	-40		85	°C

Note
(1) Industrial temperature -40 to +85 °C can be guaranteed by design. Commercial temperature 0 to +70 °C is supported by the production-tested.

5.3 Electrical Characteristics

5.3.1 DC Electrical Characteristics

Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Single Power Supply						
I _{DD33}	3.3V Power @ 0dB Pre-Emp	Outputs Enable (open drain 500mV, 0 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		110		mA
I _{DD33}	3.3V Power@ 0dB Pre-Emp	Outputs Enable (Double termination 500mV, 0 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		180		mA
I _{DD33}	3.3V Power @ 2.5dB Pre-Emp	Outputs Enable (Open Drain 500mV, 2.5 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		133		mA
I _{DD33}	3.3V Power @ 2.5dB Pre-Emp	Outputs Enable (Double termination 500mV, 2.5 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		211		mA

Power Consumption Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dual Power Supply						
I _{DD15}	1.5V @ open drain 500mV, 0dB	Outputs Enable (open drain 500mV, 0dB pre-emphasis), terminated OUT_D [0:2] and CLK with 50 ohms to Vdd		58	70	mA
	1.5V @ double termination 500mV, 0dB	Outputs Enable (open drain 500mV, 0dB pre-emphasis), terminated OUT_D [0:2] and CLK with 50 ohms to Vdd		78.2		mA
	1.5V @ double termination 500mV, 2.5dB	Outputs Enable (open drain 500mV, 0dB pre-emphasis), terminated OUT_D [0:2] and CLK with 50 ohms to Vdd		93.2		mA
I _{DD33}	3.3V IO current			2	3	mA
Stand-by Current						
I _{STB}	Standby mode Current; VDD = 3.6V	DDC passive switch (open drain & double termination); OEB = 1, HPD_SINK = 0		40		μA
		DDC active buffer (open drain & double termination); OEB = 1, HPD_SINK = 0		1.5		mA
		DDC Passive Switch (open drain & double termination); OEB= 1 and HPD_SINK = 0		0		mA
		DDC active buffer (open drain & double termination); OEB= 0 and HPD_SINK = 0		1.44		mA
Squelch Current						
I _{SQLH}	Squelch mode current; VDD = 3.6V	DDC passive switch; No input clock VDD=3.6V, HPD_SINK=3.6V		2.68	3.0	mA
		DDC active buffer; No input clock VDD=3.6V, HPD_SINK=3.6V		3.52	4.1	mA

Note:

1. Current is due to internal 100kΩ pull-down of OE pin drawing extra current (~36uA). If forced by a separate power supply with all other control pins open, lower current is seen (~4uA).

HPD Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HPD_SRC						
V _{OL}	Buffer output low voltage	IOL = 4 mA			0.4	V
	Open drain output low voltage	IOL = 4 mA	0		0.4	V
V _{OH}	Buffer output high voltage	IOH = 0.1 mA	VDD-1.55			V
I _{OFF}	Off leakage current	VDD=0, VIN=3.6V			25	uA

PI3HDX511F

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{OZ}	Open drain output leakage current	VDD=3.6V, VIN=3.6V			25	µA
HPD_SINK						
I _{IH}	High level digital input current	V _{IH} = 5.5V	-10		80	µA
I _{IL}	Low level digital input current	V _{IL} = GND	-10		10	µA
V _{IH}	High level digital input voltage	VDD=3.3V	2.0			V
V _{IL}	Low level digital input voltage		0		0.8	V

Control Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OEB with 100k Pull to GND						
I _{IH}	High level digital input current	V _{IH} = 3.3V, VDD=3.3V	-10		80	µA
I _{IL}	Low level digital input current	V _{IL} = GND	-10		10	µA
V _{IH}	High level digital input voltage		2.0			V
V _{IL}	Low level digital input voltage		0		0.8	V
EQ_S0, OC_S0 with 100k Pull High and 100k Pull Low when TMDS is Active						
I _{IH}	High level digital input current	V _{IH} = 3.3V, VDD=3.3V	-10		40	µA
I _{IL}	Low level digital input current	V _{IL} = GND, VDD=3.3V	-40		10	µA
ROUT_S0, TMDS_ORDER, EQ_STEP, VBIAS, LDO_EN, DDC_SEL, HPDO_S0						
I _{IH}	High level digital input current	V _{IH} = VDD	-10		10	µA
I _{IL}	Low level digital input current	V _{IL} = GND	-20		10	µA
V _{IH}	High level digital input voltage		2.0			V
V _{IL}	Low level digital input voltage		0		0.8	V

DDC Channel Switch

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{LK}	Input leakage current	DDC switch is off, V _{in} = 5.5V	-10		30	µA
C _{IO}	Input/Output capacitance when passive switch on	V _{Ipp} (peak-peak) = 1V, 100 kHz		10		pF
R _{ON}	Passive Switch resistance	I _O = 3mA, V _O = 0.4V		30	50	Ω
V _{PASS}	Switch Output voltage	V _I =3.3V, I _I =100µA VDD=3.3V	1.5	2.0	2.5	V

DDC Channel Buffers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{IH_SRC}	Source Side DDC Buffer Input High Voltage		0.6			V
V _{IL_SRC}	Source Side DDC Buffer Input Low Voltage				0.4	V

PI3HDX511F
DDC Channel Switch Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{OL_SRC}	Source Side DDC Buffer Output Low Voltage	External pull-up to VDD from 1.5kΩ to 10kΩ	0.47	0.52	0.6	V
V _{OL_SINK}	Sink Side DDC Buffer Output Low Voltage				0.2	V
V _{IH_SINK}	Sink Side DDC Buffer Input High Voltage		2.0			V
V _{IL_SINK}	Sink Side DDC Buffer Input Low Voltage				0.8	V
C _{I_SRC}	Source side DDC capacitance when active switch is on, or passive switch off	V _{Ipp} (peak-peak)=1V, 100 KHz		5		pF
C _{I_SINK}	Sink side DDC capacitance when active switch is on, or passive switch off			5		pF

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{OH}	Single-ended high level output voltage	VDD = 3.3V, R _{OUT} =50Ω	VDD-10		VDD+10	mV
V _{OL}	Single-ended low level output voltage		VDD-600		VDD-400	mV
V _{SWING}	Single-ended output swing voltage		400		600	mV
V _{OD(O)} ⁽¹⁾	Overshoot of output differential voltage				180 ⁽¹⁾	mV
V _{OD(U)} ⁽²⁾	Undershoot of output differential voltage				200 ⁽²⁾	mV
V _{OC(SS)}	Change in steady-state common-mode output voltage between logic states				5	mV
I _{OS}	Short Circuit output current at open drain mode	Short to VDD	-12		12	mA
	Short Circuit output current at double termination mode	Short to VDD	-24		24	mA
V _{I(open)}	Single-ended input voltage under high impedance or open case	I _I = 10uA	VDD-10		VDD+10	mA
R _T	Input termination resistance	V _{IN} = 2.9V	45	50	55	Ω
I _{OZ}	Leakage current with Hi-Z I/O	VDD = 3.6V			30	μA

Note

(1) Overshoot of output differential voltage VOD(O) = (VSWING(MAX) * 2) * 15%

(2) Undershoot of output differential voltage VOD(U) = (VSWING(MIN) * 2) * 25%

5.3.2 AC Electrical Characteristics

TMD5 Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
t_{pd}	Propagation delay	VDD = 3.3V, ROUT = 50Ω			2000	ps	
t_r/t_f	Differential output signal rise/fall time (20% - 80%), open drain, 0dB pre-emphasis				120		
	Differential output signal rise/fall time (20% - 80%), open drain, 2.5dB pre-emphasis				100		
$t_{sk(p)}$	Pulse skew				10		50
$t_{sk(D)}$	Intra-pair differential skew				23		50
$t_{sk(o)}$	Inter-pair differential skew						100
$t_{jit(pp)}$	Peak-to-peak output jitter CLK residual jitter	Data Input = 3.4 Gbps		30	60		
$t_{jit(pp)}$	Peak-to-peak output jitter DATA residual Jitter			40	70		
t_{en}	Enable time				50	μs	
t_{dis}	Disable time				0.01		

DDC I/O Pins (Passive Switch Mode)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{pd(DDC)}$	Propagation delay from SCL_SINK/SDA_SINK to SCL/SDA, or SCL/SDA to SCL_SINK/SDA_SINK in passive switch.	CL = 10pF in passive switch			5	ns

DDC I/O Pins (Active Buffer Mode)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	LOW-to-HIGH propagation delay	SCL/SDA to SCL/SDA_SINK		169	255	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL/SDA to SCL/SDA_SINK	10	103	300	ns
t_{PLH}	LOW-to-HIGH propagation delay	SCL/SDA_SINK to SCL/SDA	25	67	110	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL/SDA_SINK to SCL/SDA		118	230	ns

Control and Status Pins (HPD_SINK, HPD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{pd(HPD)}$	Propagation delay from HPD_SINK to the active port of HPD, high to low	CL = 10pF, pull high resistor=1kΩ		10		ns

PI3HDX511F

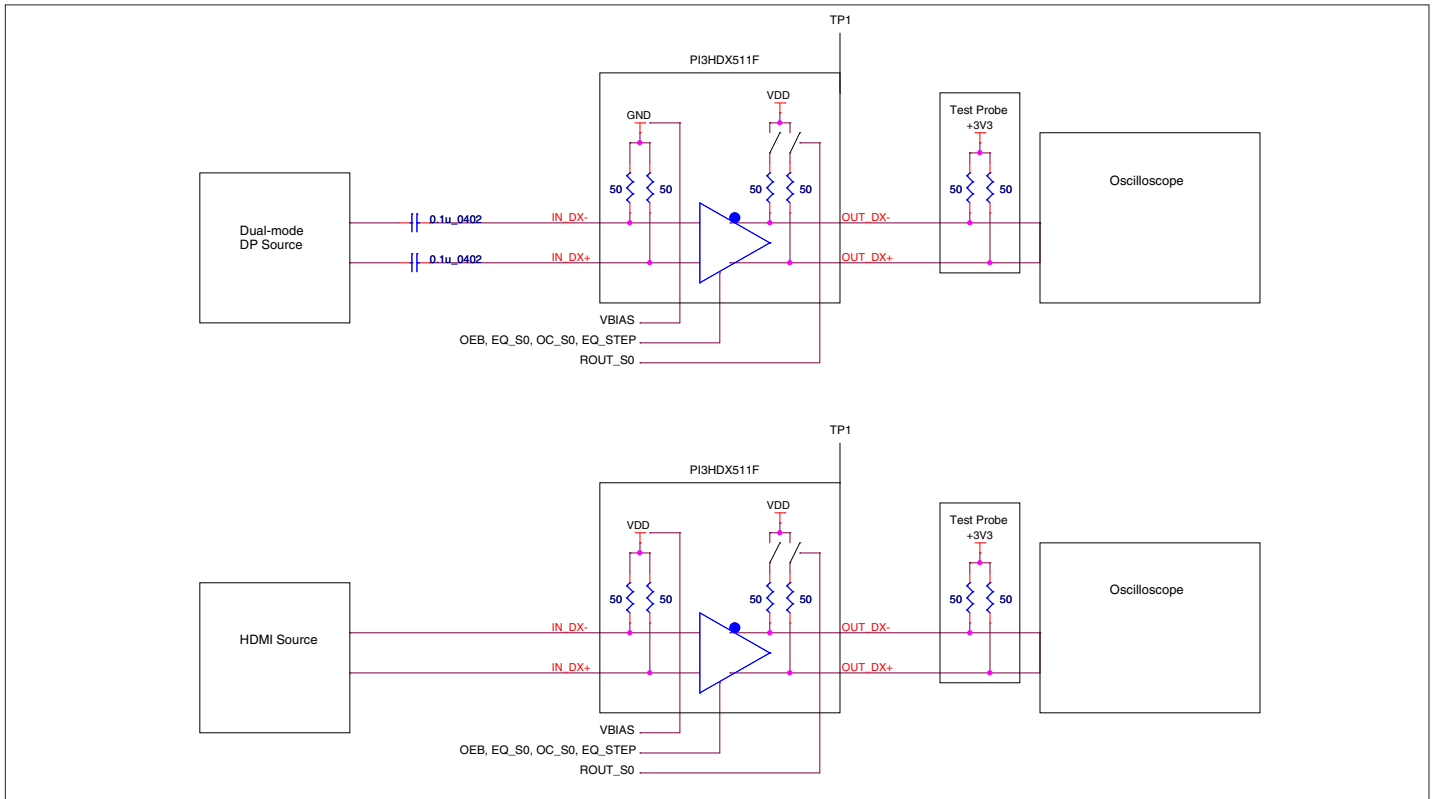


Figure 5-1 Electrical Characteristic Test Circuit

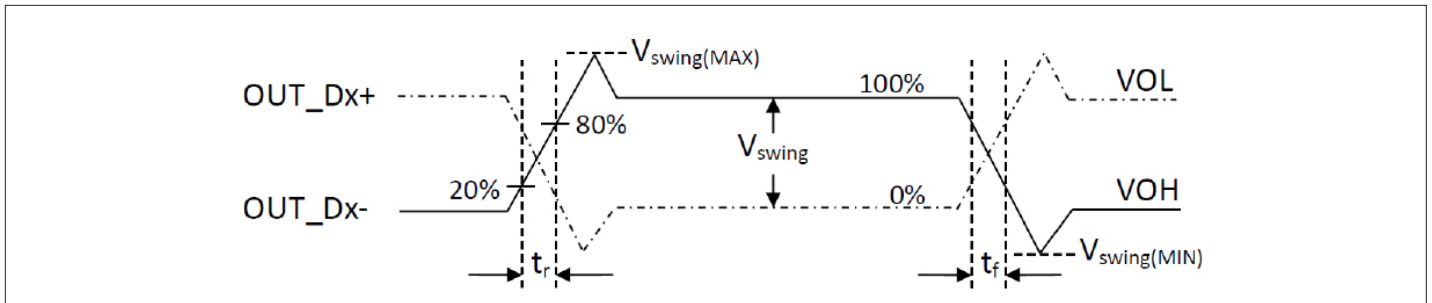


Figure 5-2 Vswing, tr/ta Definition

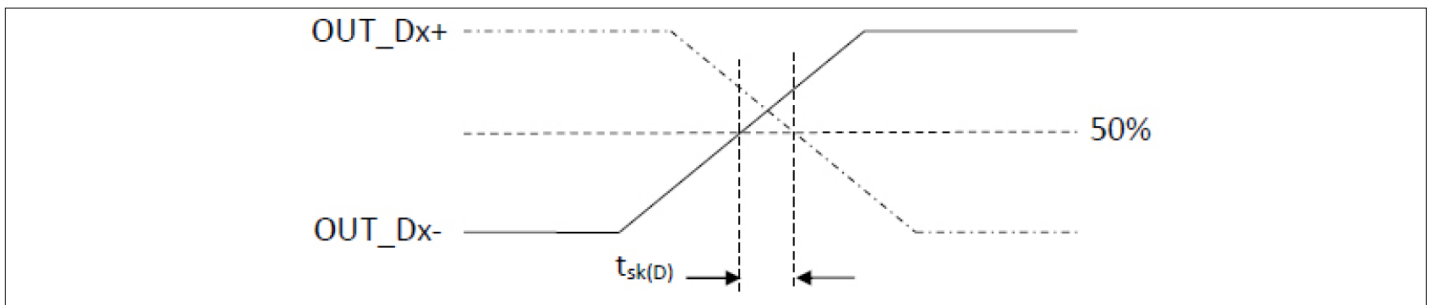
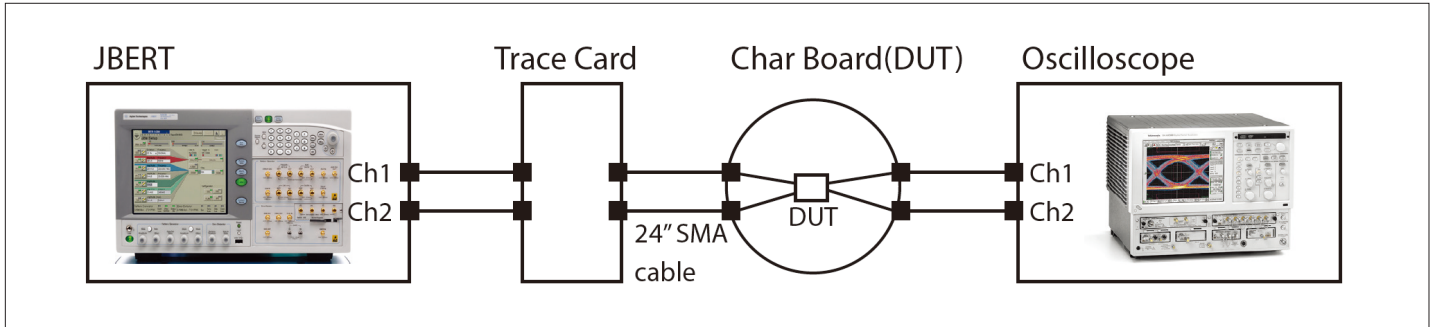


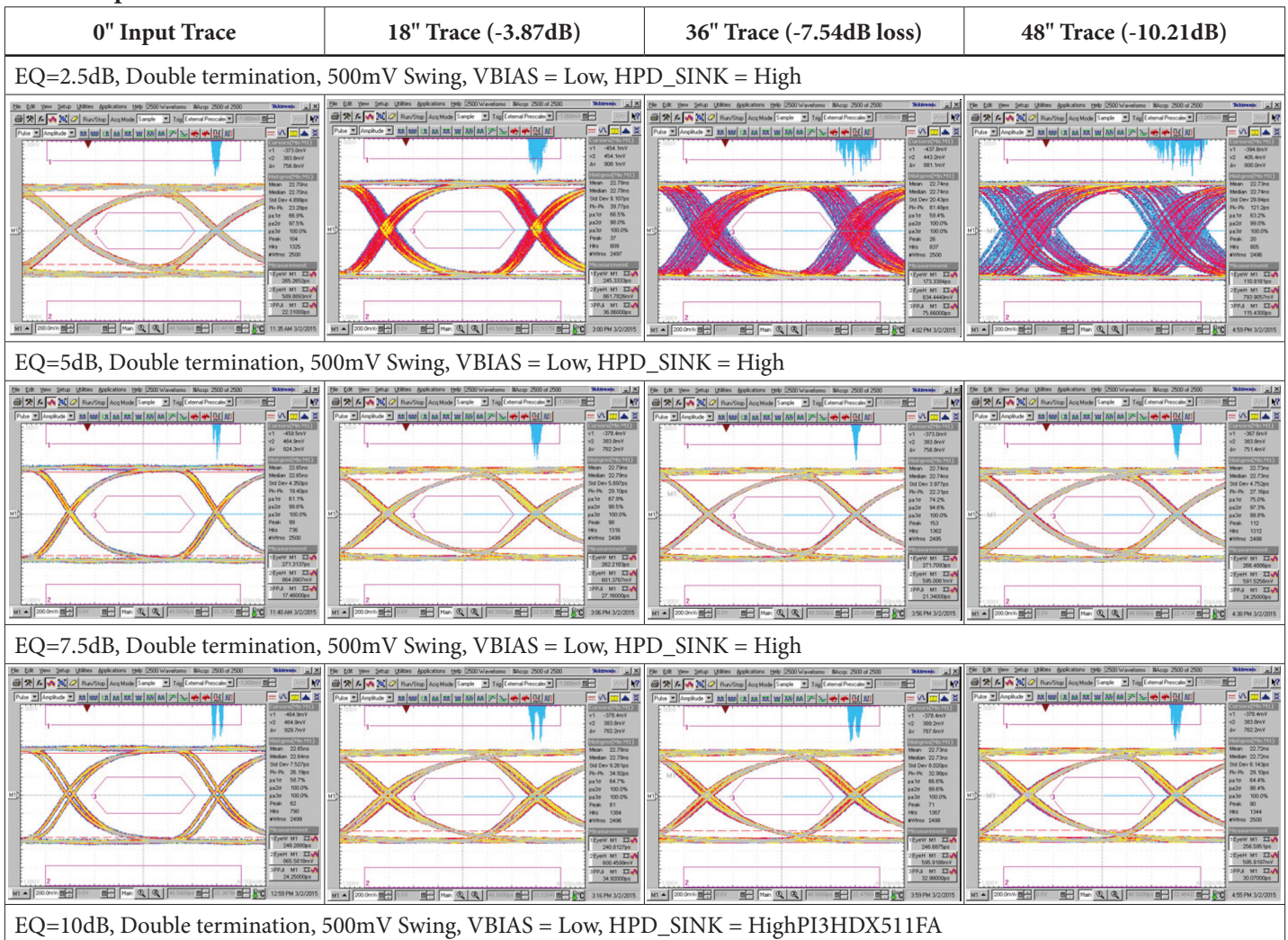
Figure 5-3 Intra-pair Skew($t_{sk(D)}$) Definition

5.4 Output Eye: EQ Settings and Input Trace Length (Informative)

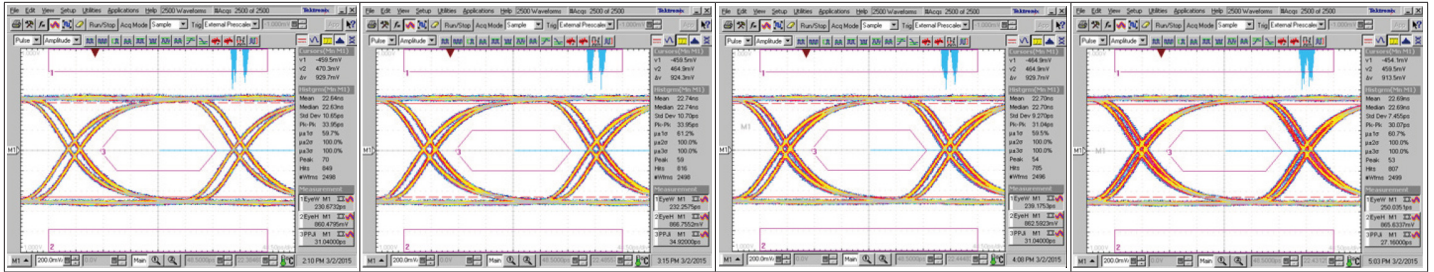
5.4.1 Test Setup



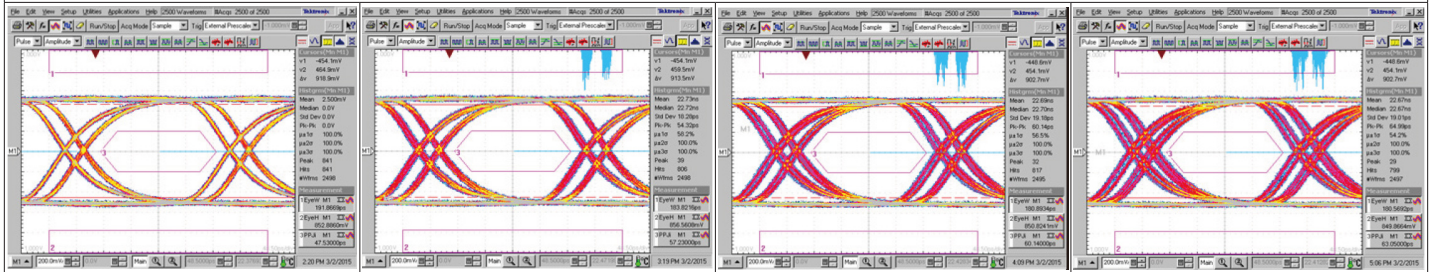
5.4.2 Output Waveforms



PI3HDX511F



EQ=15dB, Double termination 500mV Swing, VBIAS = Low, HPD_SINK = High

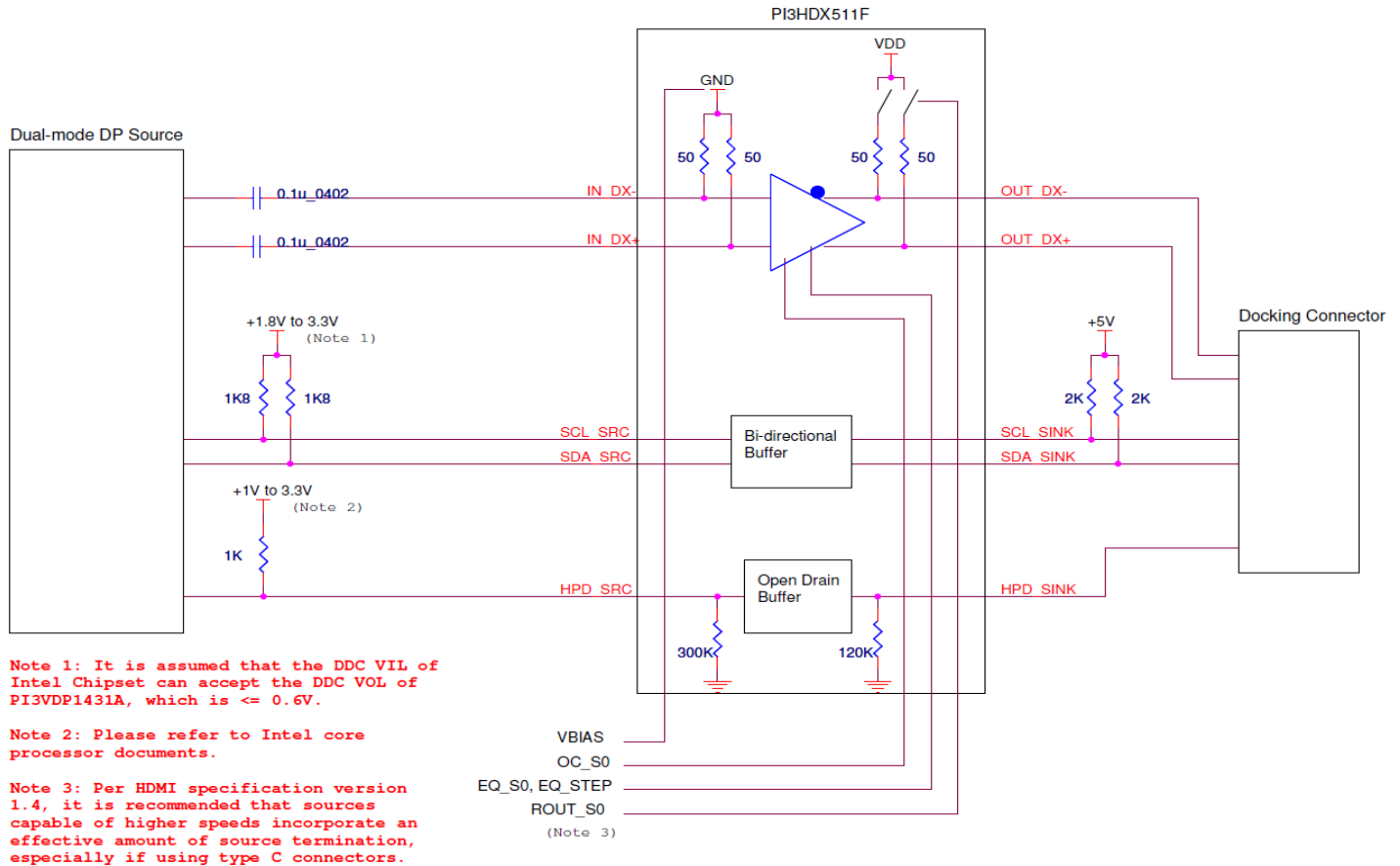


Note: For system designers reference, characterization trace board insertion Loss Informations and picture image are shown below.

Frequency @3.4Gbps	4-in	6-in	12-in	18-in	24-in	30-in	36-in	48-in	Unit
Insertion Loss	-0.9	-1.34	-2.54	-3.87	-5.17	-6.34	-7.54	-10.21	dB

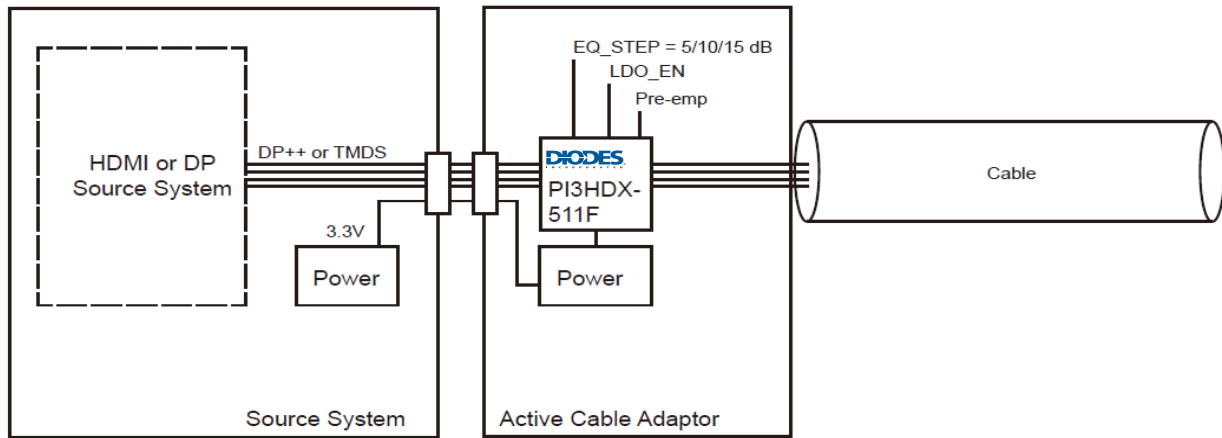
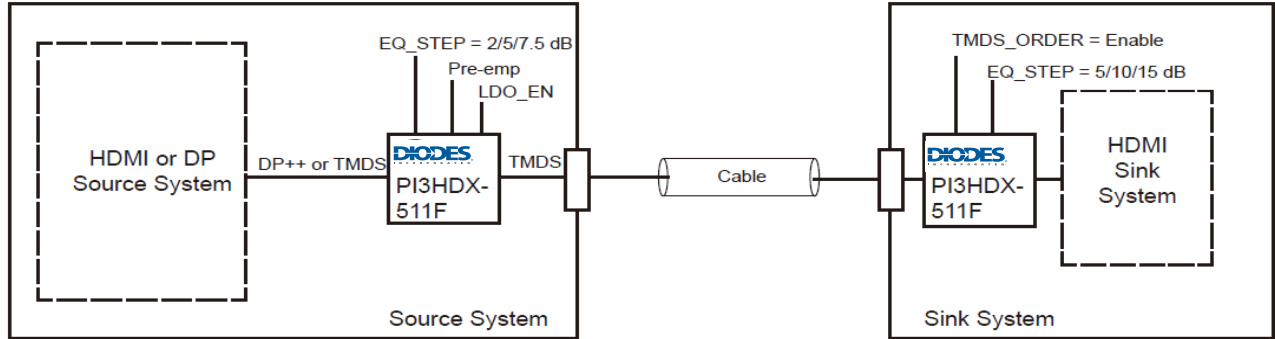
6. Applications

6.1 HDMI 1.8V DDC Buffer Usage Case



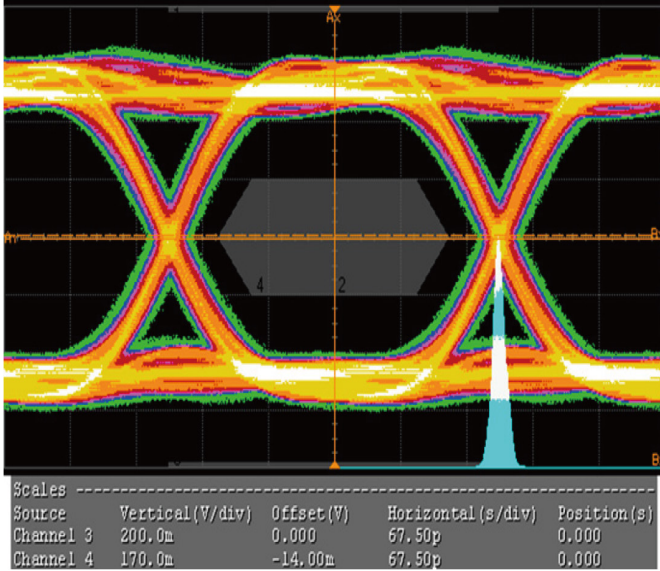
PI3HDX511F

6.2 Application Block Diagram

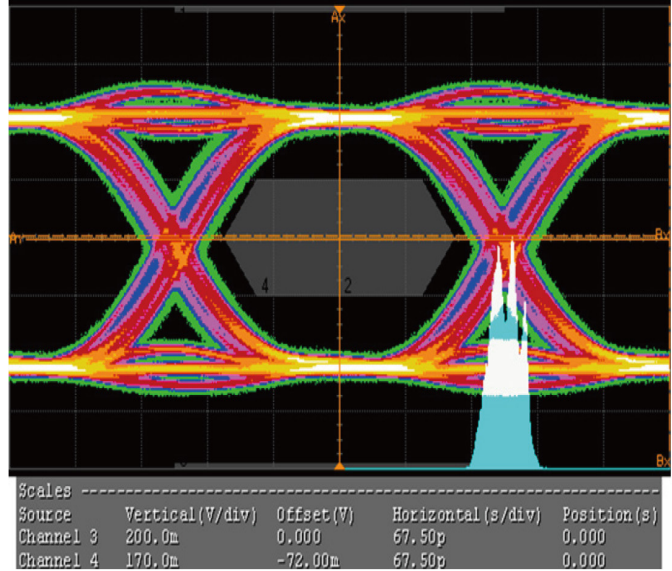


6.3 Output Eye Measurement Data

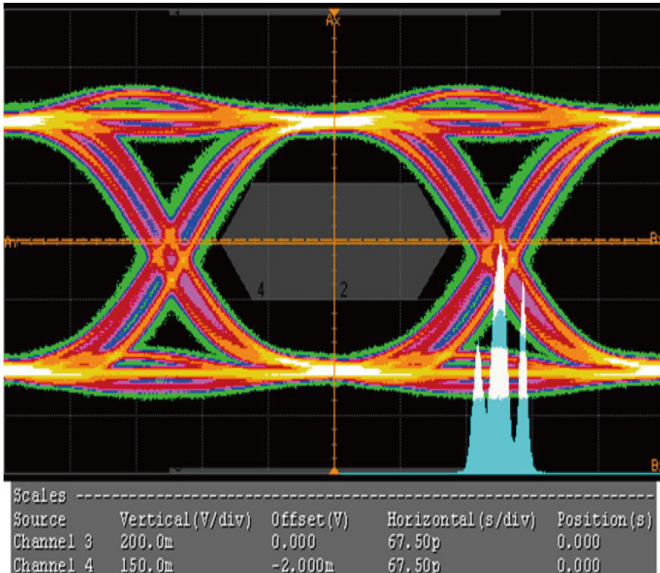
Sink Apps test set-up: Output Eye Diagram with different EQ settings of 1.5dB, 10dB and 15 dB. Trace Cards used with 24”, 48” and 84” with 2 meter HDMI Cable with proper pre-emphasis setting.



24” Input (-15.46dB loss) , EQ=2.5dB, 500mV Swing, Pre-emp =1.5dB, Rout_S0=1



48” Input, EQ=10dB, 500mV Swing, Pre-emp=0dB, Rout_S0=1



84” Input, EQ=15dB, 500mV Swing, Pre-emp=0dB, Rout_S0=1

Note: For system designers reference, AE-trace board information are shown below. Insertion loss is measured in the 3GHz (6.0 Gbps) speed.

FR4 trace length	0-in	6-in	12-in	18-in	24-in	30-in	36-in	Unit
Insertion Loss	-5.52	-9.35	-10.07	-12.66	-15.46	-16.57	-20.81	dB

6.4 Layout Guidelines

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

6.4.1 Power and Ground

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1 μ F decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7 μ F to 10 μ F should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

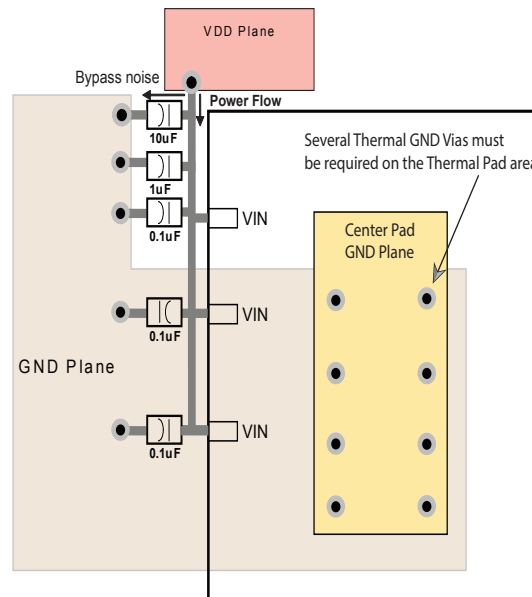
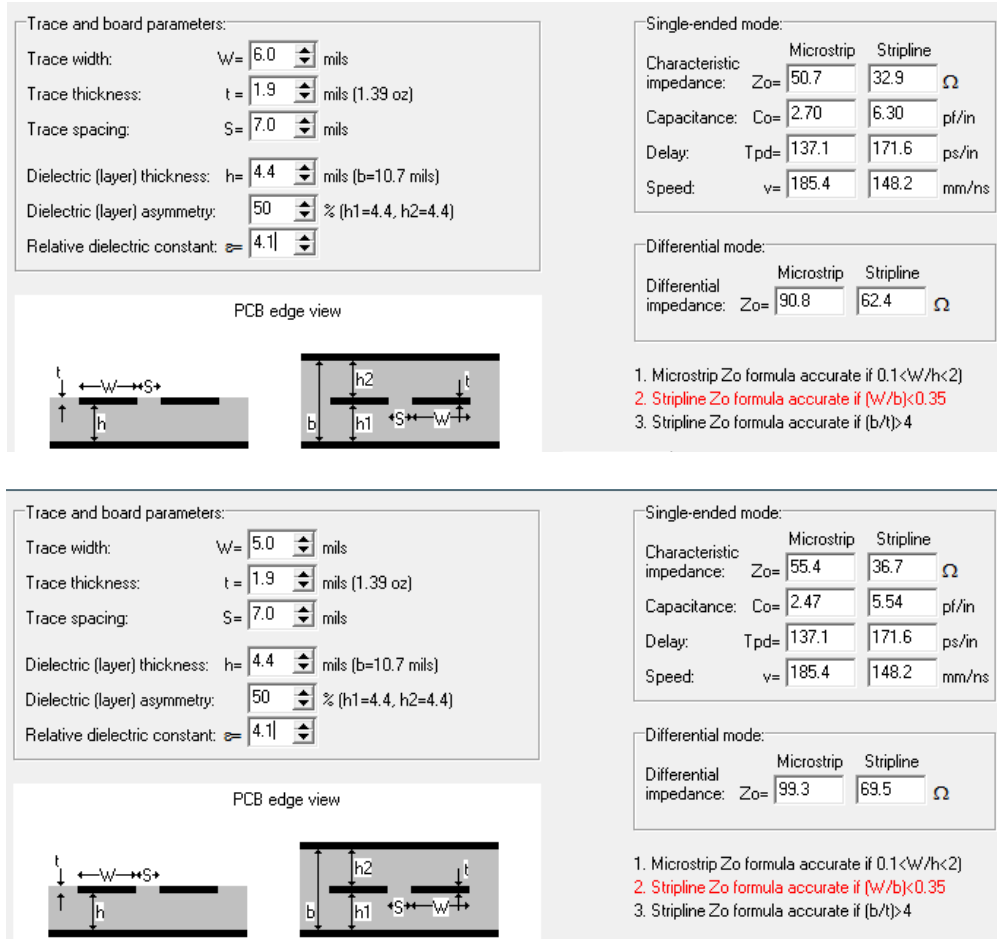


Figure 6-1 Decoupling Capacitor Placement Diagram

6.4.2 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.



- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

PI3HDX511F

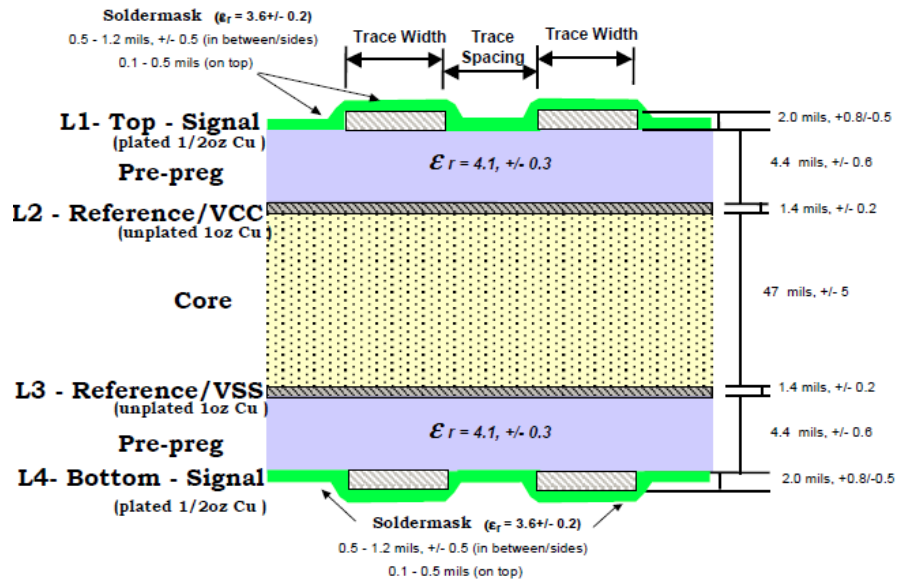


Figure 6-3 4-Layer PCB Stack-up Example

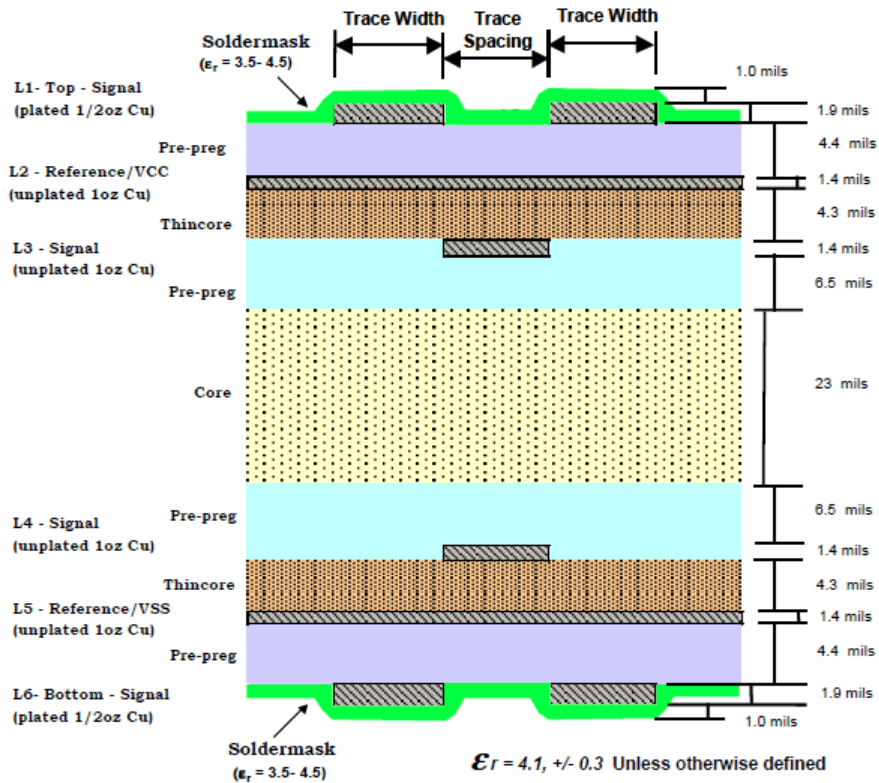


Figure 6-4 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

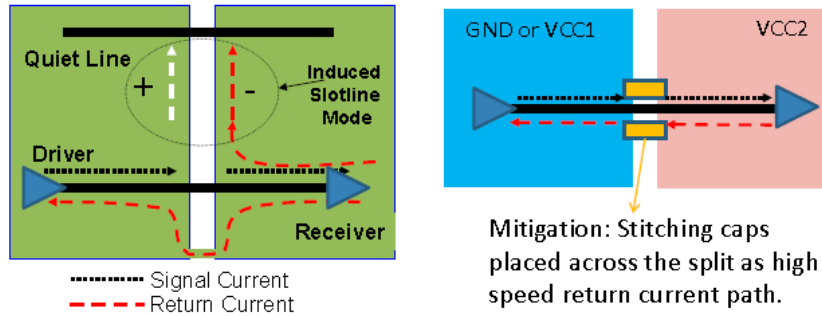


Figure 6-5 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.
- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

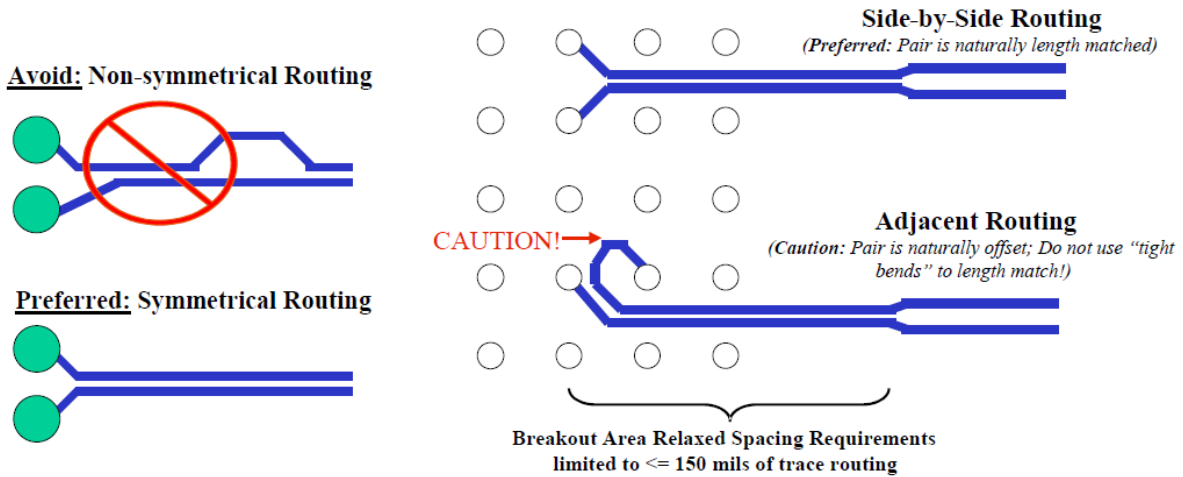


Figure 6-6 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

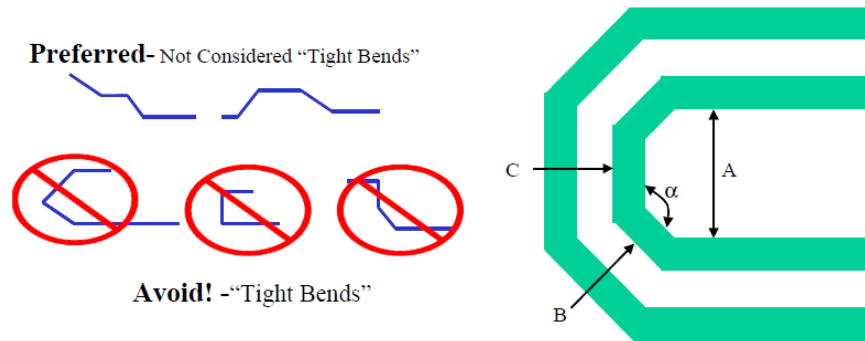


Figure 6-7 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

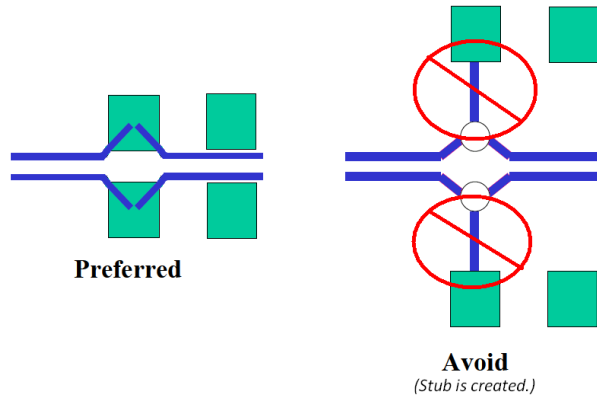


Figure 6-8 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

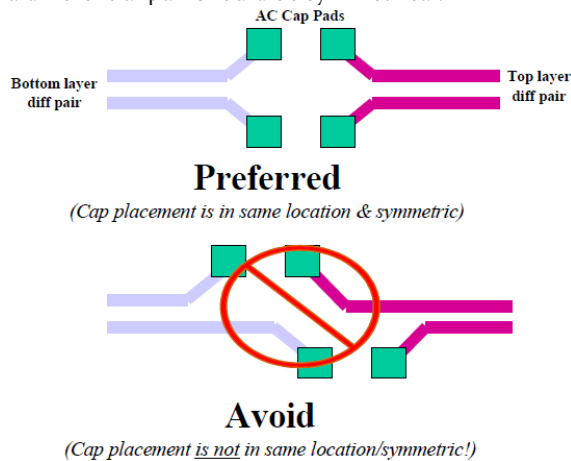


Figure 6-9 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

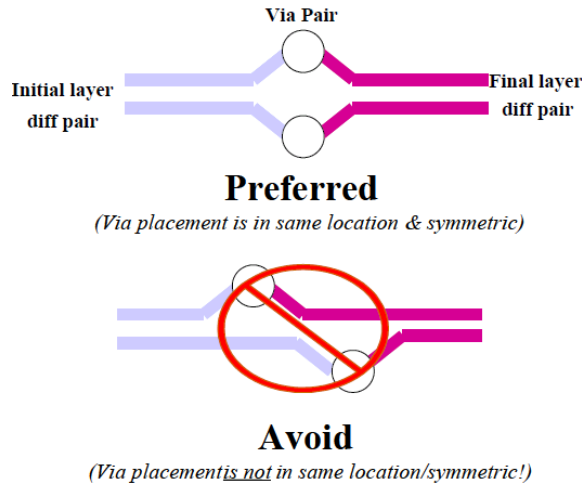


Figure 6-10 Layout Guidance of Stitching Via

6.5 HDMI 2.0 Compliance Test

6.5.1 HDMI 2.0 Compliance Test Set-up

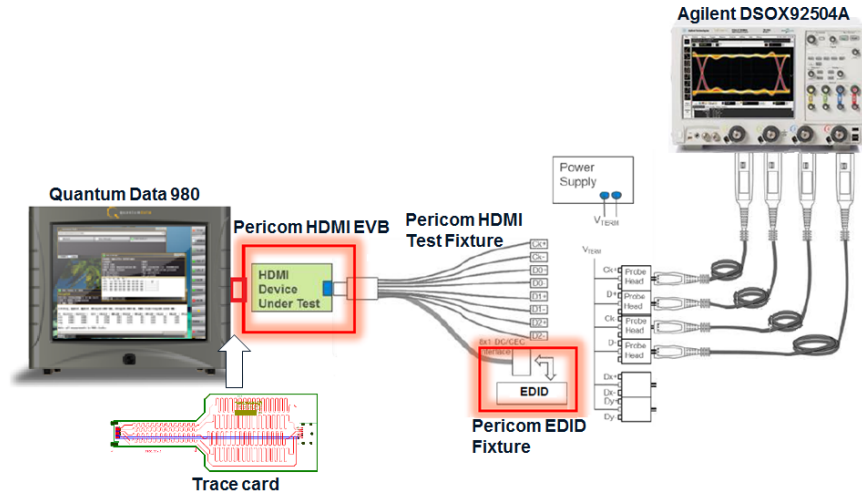


Figure 6-11 HDMI 2.0 CTS Test Setup*

Note: Application Trace Card Information

HDMI FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in	Unit
Insertion loss @ 3Gbps (estimated)	-2.96 dB	-4.88 dB	-5.24 dB	-6.53 dB	-7.94 dB	-8.49 dB	-10.60 dB	dB

6.5.2 HDMI Compliance Test Report: Pass

Test Setup : Pericom SMA-to-HDMI Test Fixture, 12” and 36” SMA Cables, Pericom 36” FR4 Trace Cards, 2m 28AWG HDMI Cable.

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.20.0013
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (18 FEB 2015 11:16:48), Using Cal Atten (5.7831E+000) Skew: Calibrated (18 FEB 2015 11:16:56), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (18 FEB 2015 11:19:29), Using Cal Atten (5.5882E+000) Skew: Calibrated (18 FEB 2015 11:13:57), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (18 FEB 2015 11:15:19), Using Cal Atten (5.7320E+000) Skew: Calibrated (18 FEB 2015 11:15:29), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (18 FEB 2015 11:11:30), Using Cal Atten (5.5123E+000) Skew: Calibrated (18 FEB 2015 11:12:12), Using Cal Skew
Last Test Date	2016-01-26 13:06:09 UTC +08:00

PI3HDX511F

Summary of Results

Test Statistics	
Failed	0
Passed	15
Total	15

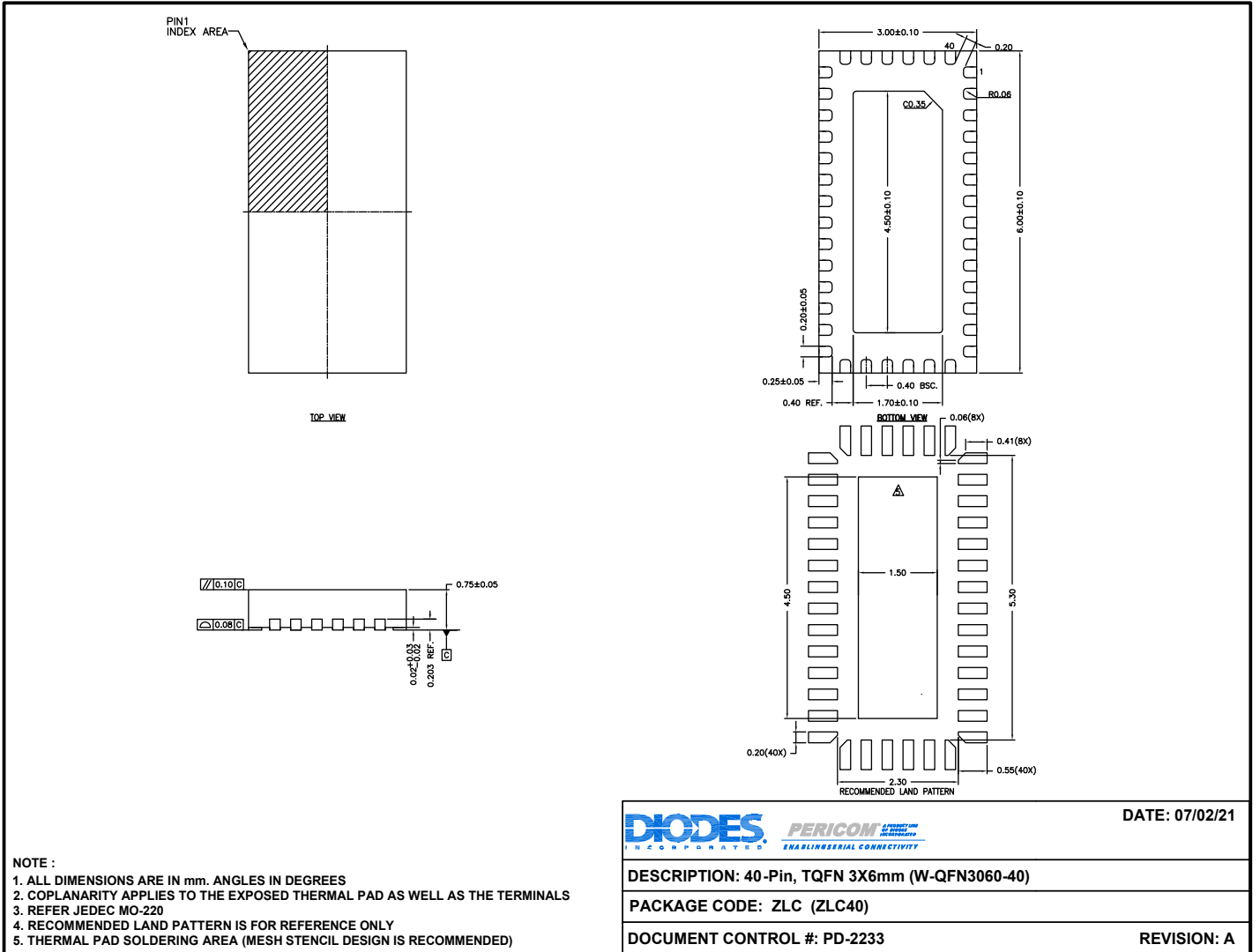
Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	<u>7-9: Clock Jitter</u>	144 mTbit	42.4 %	VALUE <= 250 mTbit
✓	0	1	<u>7-4: Clock Rise Time</u>	123.410 ps	64.5 %	VALUE >= 75.000 ps
✓	0	1	<u>7-4: Clock Fall Time</u>	122.160 ps	62.9 %	VALUE >= 75.000 ps
✓	0	1	<u>7-8: Clock Duty Cycle(Minimum)</u>	49.470	23.7 %	>=40%
✓	0	1	<u>7-8: Clock Duty Cycle(Maximum)</u>	50.130	16.5 %	<=60%
✓	0	1	<u>7-10: D0 Data Jitter</u>	249 m	17.0 %	<=0.3Tbit
✓	0	1	<u>7-4: D0 Rise Time</u>	104.503 ps	39.3 %	VALUE >= 75.000 ps
✓	0	1	<u>7-4: D0 Fall Time</u>	108.363 ps	44.5 %	VALUE >= 75.000 ps
✓	0	1	<u>7-2: VL Clock +</u>	2.853 V	15.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-2: VL Clock -</u>	2.845 V	18.3 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-7: Intra-Pair Skew - Clock</u>	115 mTbit	11.7 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	<u>7-2: VL D0+</u>	2.848 V	17.3 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-2: VL D0-</u>	2.853 V	15.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	<u>7-7: Intra-Pair Skew - Data Lane 0</u>	81 mTbit	23.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	<u>7-10: D0 Mask Test</u>	0.000	50.0 %	No Mask Failures

PI3HDX511F

7. Packaging Mechanical, Ordering Information

7.1 Packaging Mechanical Outline



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

21 1406

PI3HDX511F

7.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an “add mark” operation which places the speed code letter at the end of the complete part number.

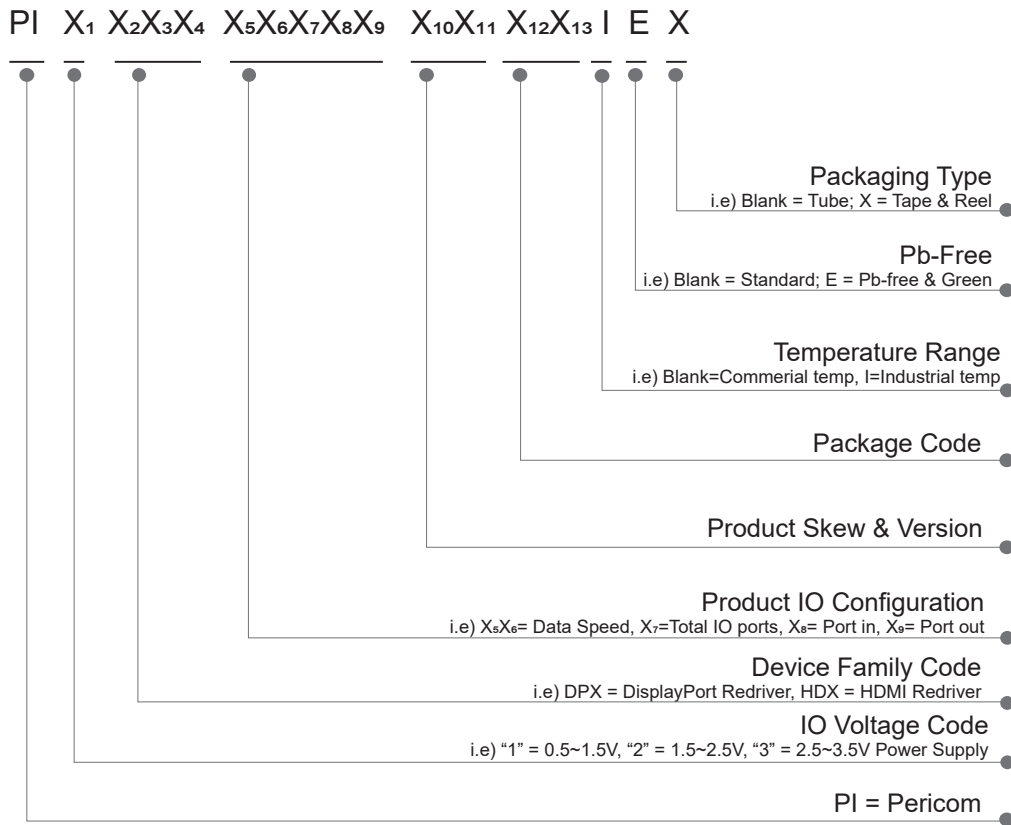


Figure 7-1 Part Naming Information

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Figure 7-2 Package Marking Information

7.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6 Ohm/sq maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 7-5 and 7-6 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7 Ohm/Sq . Minimum to 10^{11} Ohm sq maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 7-4). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 7-6) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7 Ohm/sq minimum to 10^{11} Ohm/sq max.

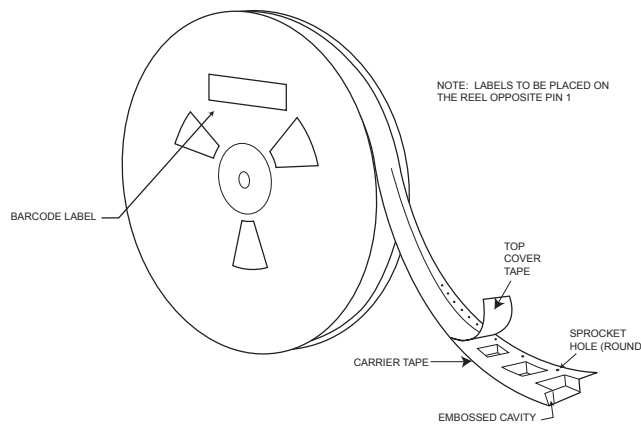


Figure 7-3 Tape & Reel Label Information

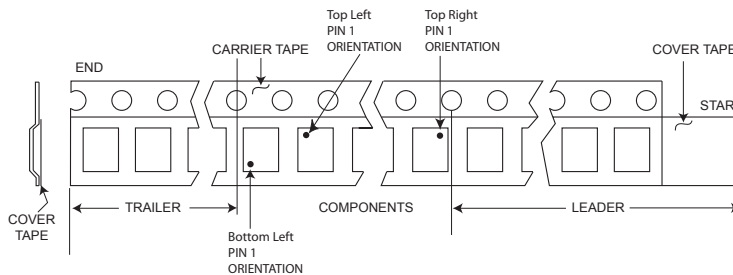


Figure 7-4 Tape Leader and Trailer Pin 1 Orientations

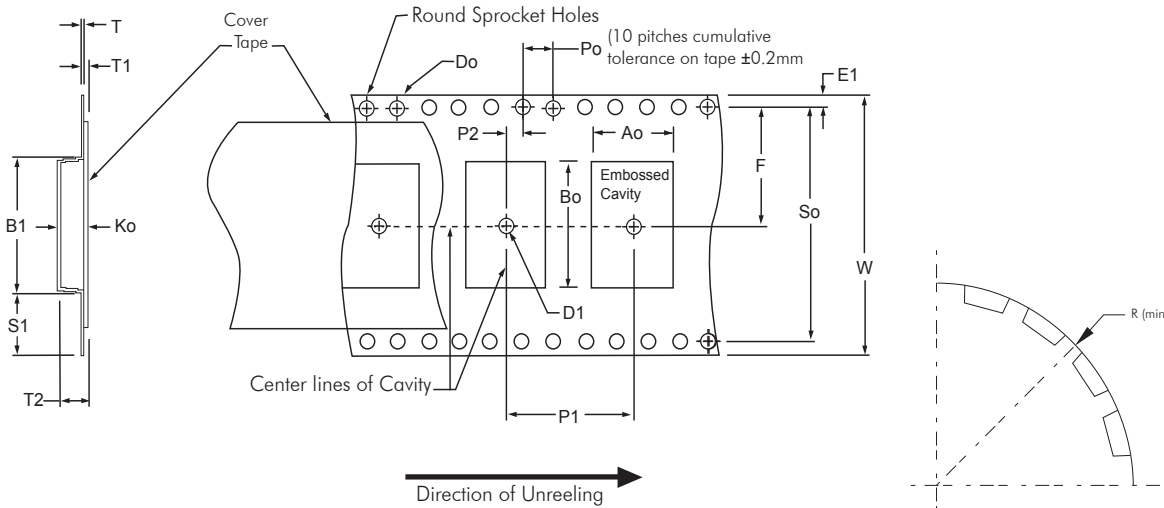


Figure 7-5 Standard Embossed Carrier Tape Dimensions

Table 7-1. Constant Dimensions

Tape Size	D0	D1 (Min)	E1	P0	P2	R (See Note 2)	S1 (Min)	T (Max)	T1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5			2.0 ± 0.1	30			
16mm									
24mm		2.0			2.0 ± 0.1	50	N/A (See Note 3)		
32mm									
44mm									

Table 7-2. Variable Dimensions

Tape Size	P1	B1 (Max)	E2 (Min)	F	So	T2 (Max.)	W (Max)	A0, B0, & K0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1	12.0	24.3		
32mm		23.0	N/A	14.2 ± 0.1		28.4 ± 0.1	32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:

- A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
- Tape and components will pass around reel with radius "R" without damage.
- S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
- So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

PI3HDX511F

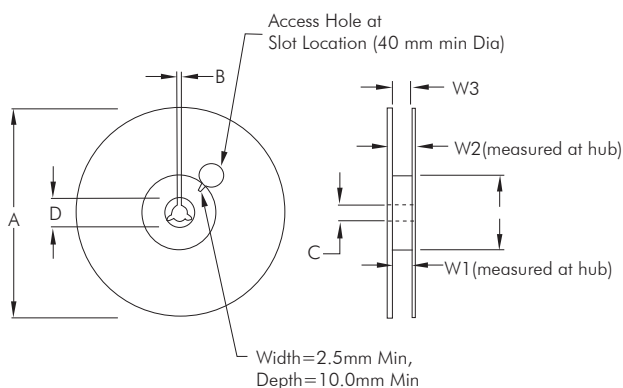


Figure 7-6 Reel Dimensions

Table 7-3. Reel dimensions by tape size

Tape Size	A	N (Min) See Note A	W1	W2(Max)	W3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:

A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min)) will be 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will be 100±2.0mm.

8. Important Notice

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at <https://www.diodes.com/about/company/terms-and-conditions/important-notice>

DIODES is a trademark of Diodes Incorporated in the United States and other countries.

The Diodes logo is a registered trademark of Diodes Incorporated in the United States and other countries.

© 2022 Diodes Incorporated. All Rights Reserved.

www.diodes.com