

# PDI1284P11

## 3.3 V parallel interface transceiver/buffer

Rev. 4 — 6 July 2021

Product data sheet

## 1. General description

The PDI1284P11 parallel interface chip is designed to provide an asynchronous, 8-bit, bidirectional, parallel interface for personal computers. The PDI1284P11 includes all 19 signal lines defined by the IEEE 1284 interface specification for Byte, Nibble, EPP, and ECP modes. The PDI1284P11 is designed for hosts or peripherals operating at 3.3 V to interface 3.3 V or 5.0 V devices.

The eight transceiver pairs (A/B 1 to 8) allow data transmission from the A-bus to the B-bus, or from the B-bus to the A-bus, depending on the state of the direction pin DIR.

The B-bus and the Y9 to Y13 lines have either totem pole or resistor pull-up outputs, depending on the state of the high drive enable pin HD. The A-bus has only totem pole style outputs. All inputs are TTL compatible with at least 400 mV of input hysteresis at  $V_{CC} = 3.3$  V.

## 2. Features and benefits

- Asynchronous operation
- 8-bit transceivers
- Six additional buffer/driver lines peripheral to cable
- Five additional control lines from cable
- 5 V tolerant
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Latch-up current protection exceeds 500 mA per JEDEC Std 19
- Input hysteresis
- Low-noise operation
- IEEE 1284 compliant level 1 and 2
- Overvoltage protection on B/Y side for off-state
- A side 3-state option
- B side active or resistive pull-up option
- Cable side supply voltage for 5 V or 3 V operation

## 3. Ordering information

Table 1. Ordering information

| Type number   | Package           |         |  | Version  |
|---------------|-------------------|---------|--|----------|
|               | Temperature range | Name    | Description  |          |
| PDI1284P11DGG | 0 °C to 70 °C     | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

### 4. Functional diagram

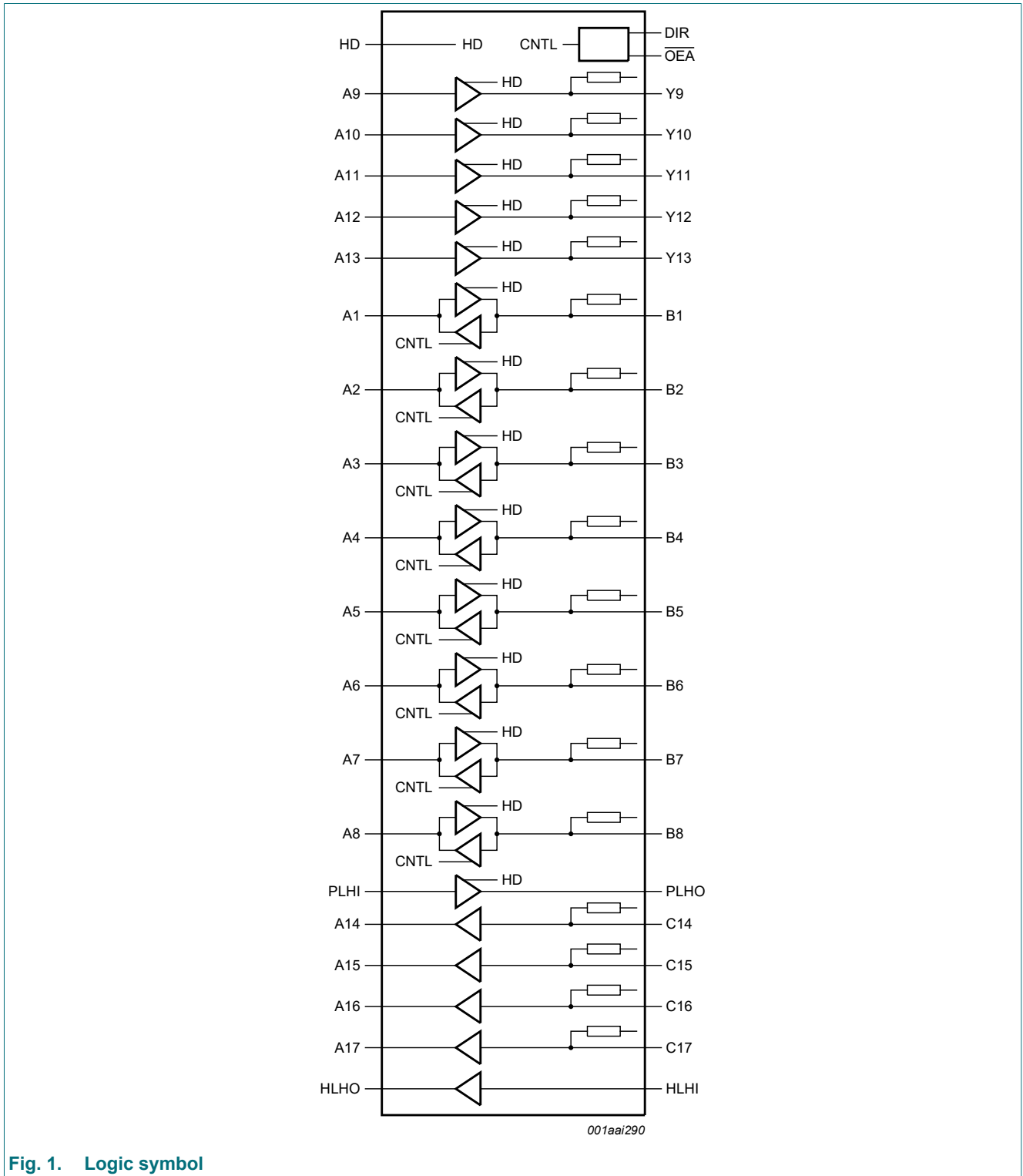


Fig. 1. Logic symbol

## 5. Pinning information

### 5.1. Pinning

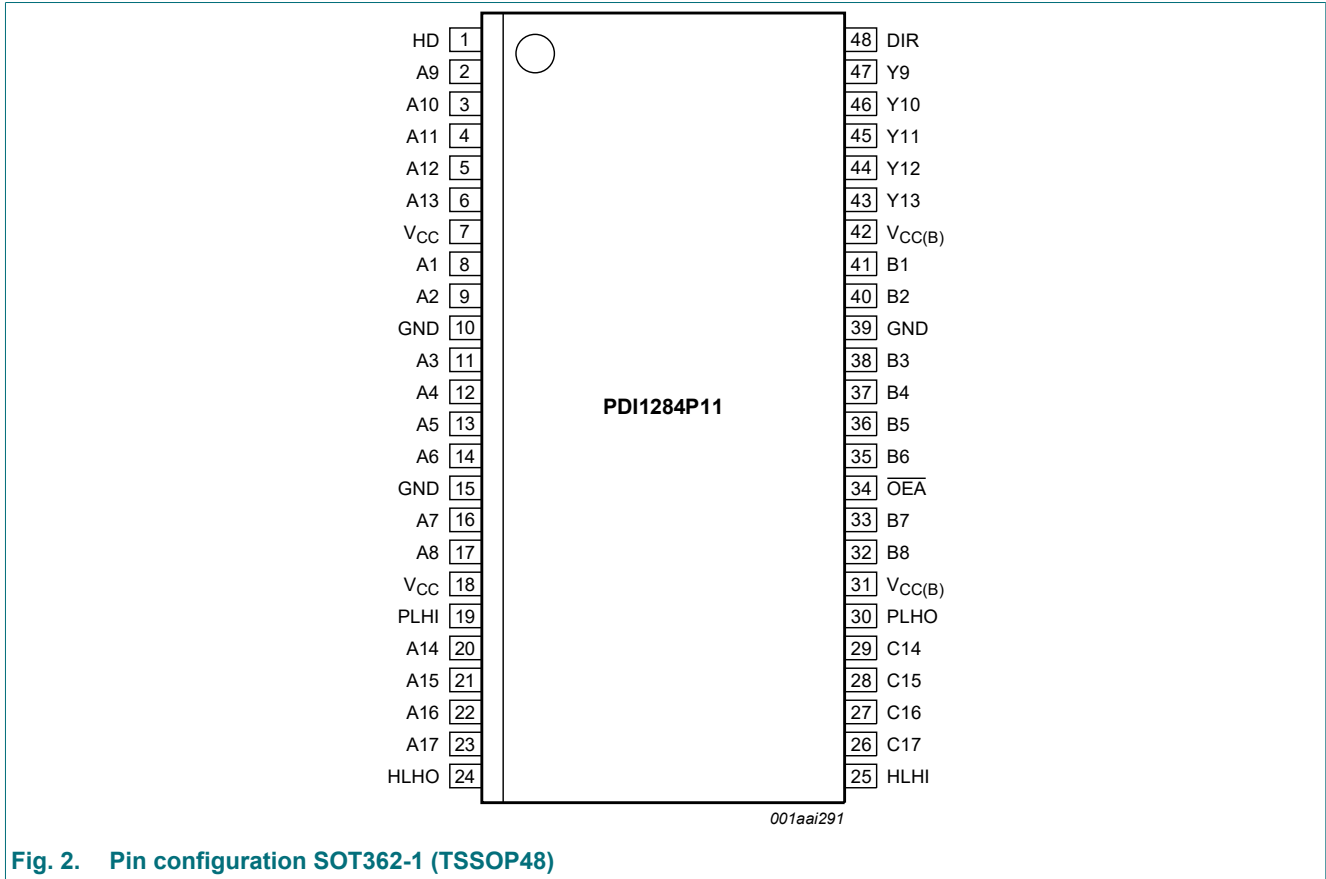


Fig. 2. Pin configuration SOT362-1 (TSSOP48)

### 5.2. Pin description

Table 2. Pin description

| Symbol                         | Pin                            | Description                         |
|--------------------------------|--------------------------------|-------------------------------------|
| HD                             | 1                              | high drive enable/disable input     |
| A1, A2, A3, A4, A5, A6, A7, A8 | 8, 9, 11, 12, 13, 14, 16, 17   | data input/output                   |
| B1, B2, B3, B4, B5, B6, B7, B8 | 41, 40, 38, 37, 36, 35, 33, 32 | IEEE 1284 standard output/input [1] |
| A9, A10, A11, A12, A13         | 2, 3, 4, 5, 6                  | data input                          |
| Y9, Y10, Y11, Y12, Y13         | 47, 46, 45, 44, 43             | IEEE 1284 standard output [1]       |
| C14, C15, C16, C17             | 29, 28, 27, 26                 | control input (cable) [1]           |
| A14, A15, A16, A17             | 20, 21, 22, 23                 | control output (peripheral)         |
| V <sub>CC</sub>                | 7, 18                          | supply voltage                      |
| GND                            | 10, 15, 39                     | ground (0 V)                        |

## 3.3 V parallel interface transceiver/buffer

| Symbol                  | Pin    | Description                              |
|-------------------------|--------|--|
| PLHI                    | 19     | peripheral logic high input (peripheral) |
| HLHO                    | 24     | host logic high output (cable)           |
| HLHI                    | 25     | host logic high input (cable)            |
| PLHO                    | 30     | peripheral logic high output (cable)     |
| V <sub>CC(B)</sub>      | 31, 42 | supply voltage B (cable side 3 V/5 V)    |
| $\overline{\text{OEA}}$ | 34     | A side output enable input (active LOW)  |
| DIR                     | 48     | direction selection input                |

[1] Pin with pull-up resistor to load cable.

## 6. Functional description

Table 3. Function table [1]

| DIR | OEA | HD | Input      | Output     | Output type |
|-----|-----|----|------------|------------|-------------|
| X   | X   | X  | C14 to C17 | A14 to A17 | TP          |
| X   | X   | X  | HLHI       | HLHO       | TP          |
| X   | X   | L  | A9 to A13  | Y9 to Y13  | RP          |
| X   | X   | H  | A9 to A13  | Y9 to Y13  | TP          |
| X   | X   | L  | PLHI       | PLHO       | OC          |
| X   | X   | H  | PLHI       | PLHO       | TP          |
| H   | X   | L  | A1 to A8   | B1 to B8   | RP          |
| H   | X   | H  | A1 to A8   | B1 to B8   | TP          |
| L   | L   | X  | B1 to B8   | A1 to A8   | TP          |
| L   | H   | X  | -          | A1 to A8   | Z [2]       |
| L   | H   | X  | B1 to B8   | -          | RP [2]      |

[1] An = side driving internal IC;

Bn = side driving external cable (bidirectional);

Cn = side receiving control signals from external cable;

H = HIGH voltage level;

L = LOW voltage level;

OC = Open Collector;

X = don't care (control signals in);

Yn = side driving external cable (unidirectional);

Z = high impedance (high-Z) or 3-state;

TP = totem pole output;

RP = resistive pull-up: 1.4 k $\Omega$  (nominal) on B/Y/C cable side and V<sub>CC</sub>. However, while a B/Y side output is LOW as driven by a LOW signal on the A side, that particular B/Y side resistor is switched off to stop current drain from V<sub>CC</sub> through it.

[2] When DIR = L and  $\overline{\text{OEA}}$  = H, the output signal is isolated from the input signal. Signals B1 to B8 maintain a resistive pull-up of 1.4 k $\Omega$  on the input for this mode.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol      | Parameter               | Conditions                            | Min  | Max            | Unit |
|-------------|-------------------------|---------------------------------------|------|----------------|------|
| $V_{CC}$    | supply voltage          | pins $V_{CC}$                         | -0.5 | +4.6           | V    |
| $V_{CC(B)}$ | supply voltage B        | pins $V_{CC(B)}$ ; cable side 3 V/5 V | -0.5 | +6.5           | V    |
| $I_{IK}$    | input clamping current  | $V_I < 0$ V                           | -    | $\pm 20$       | mA   |
| $I_{OK}$    | output clamping current | $V_O < 0$ V                           | -    | $\pm 50$       | mA   |
| $V_I$       | input voltage           | [1]                                   | -0.5 | +5.5           | V    |
| $V_O$       | output voltage          | B/Y side [1]                          | -0.5 | +5.5           | V    |
|             |                         | A side                                | -0.5 | $V_{CC} + 0.5$ | V    |
| $V_{trt}$   | transient voltage       | B/Y side; 40 ns transient [2]         | -2   | +7             | V    |
| $I_{CC}$    | supply current          |                                       | -    | 200            | mA   |
| $I_{GND}$   | ground current          |                                       | -200 | -              | mA   |
| $I_O$       | output current          | output HIGH or LOW                    | -    | $\pm 50$       | mA   |
| $T_{stg}$   | storage temperature     |                                       | -60  | +150           | °C   |
| $P_{tot}$   | total power dissipation | $T_{amb} = 0$ °C to +70 °C            | -    | 500            | mW   |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{trt}$  guarantees only that the PDI1284P11 will not be damaged by reflections in application so long as the voltage levels remain in the specified range.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

| Symbol      | Parameter                 | Conditions                            | Min  | Max      | Unit |
|-------------|---------------------------|---------------------------------------|------|----------|------|
| $V_{CC}$    | supply voltage            | pins $V_{CC}$                         | 3.0  | 3.6      | V    |
| $V_{CC(B)}$ | supply voltage B          | pins $V_{CC(B)}$ ; cable side 3 V/5 V | 3.0  | 5.5      | V    |
| $V_{IH}$    | HIGH-level input voltage  |                                       | 2.0  | -        | V    |
| $V_{IL}$    | LOW-level input voltage   |                                       | -    | 0.8      | V    |
| $V_O$       | output voltage            | pins Bn, Yn                           | -0.5 | +5.5     | V    |
|             |                           | pins An                               | 0    | $V_{CC}$ | V    |
| $I_{OH}$    | HIGH-level output current | pins Bn, Yn                           | -    | -14      | mA   |
| $I_{OL}$    | LOW-level output current  | pins Bn, Yn                           | -    | 14       | mA   |
| $T_{amb}$   | ambient temperature       | free-air                              | 0    | 70       | °C   |

## 9. Static characteristics

**Table 6. Static characteristics**
 $T_{amb} = 0\text{ }^{\circ}\text{C to }70\text{ }^{\circ}\text{C}$ ; ground = 0 V; unless specified otherwise.

| Symbol           | Parameter                 | Conditions  | Min  | Typ  | Max  | Unit |    |
|------------------|---------------------------|---|------|------|------|------|----|
| V <sub>IL</sub>  | LOW-level input voltage   | An, Bn, Cn and PLHI inputs; V <sub>CC</sub> = 3.0 V to 3.6 V  | -    | -    | 0.8  | V    |    |
|                  |                           | HLHI input; V <sub>CC</sub> = 3.0 V   | -    | -    | 1.55 | V    |    |
| V <sub>IH</sub>  | HIGH-level input voltage  | An, Bn, PLHI inputs; V <sub>CC</sub> = 3.0 V to 3.6 V   | 2.0  | -    | -    | V    |    |
|                  |                           | Cn inputs; V <sub>CC</sub> = 3.0 V to 3.6 V   | 2.3  | -    | -    | V    |    |
|                  |                           | HLHI input; V <sub>CC</sub> = 3.6 V   | 2.6  | -    | -    | V    |    |
| V <sub>H</sub>   | hysteresis voltage        | An, Bn inputs; V <sub>CC</sub> = 3.3 V; V <sub>IL</sub> = 0.8 V; V <sub>IH</sub> = 2.0 V  | [1]  | 0.4  | 0.47 | -    | V  |
|                  |                           | Cn inputs; V <sub>CC</sub> = 3.3 V  | [1]  | 0.8  | 0.47 | -    | V  |
| V <sub>OL</sub>  | LOW-level output voltage  | pins An, HLHO; I <sub>OL</sub> = 50 μA; V <sub>CC</sub> = 3.0 V   | -    | -    | 0.2  | V    |    |
|                  |                           | pins An, HLHO; I <sub>OL</sub> = 4 mA; V <sub>CC</sub> = 3.0 V  | -    | -    | 0.4  | V    |    |
|                  |                           | pins Bn, Yn; I <sub>OL</sub> = 14 mA; V <sub>CC</sub> = 3.0 V   | -    | -    | 0.77 | V    |    |
|                  |                           | pin PLHO; I <sub>OL</sub> = 500 μA; V <sub>CC</sub> = 3.0 V   | -    | -    | 0.8  | V    |    |
| V <sub>OH</sub>  | HIGH-level output voltage | pins An, HLHO; I <sub>OH</sub> = -500 μA; V <sub>CC</sub> = 3.0 V   | 2.8  | -    | -    | V    |    |
|                  |                           | pins An, HLHO; I <sub>OH</sub> = -4 mA; V <sub>CC</sub> = 3.0 V   | 2.4  | -    | -    | V    |    |
|                  |                           | pins Bn, Yn; I <sub>OH</sub> = -14 mA; V <sub>CC</sub> = 3.0 V  | 2.23 | -    | -    | V    |    |
|                  |                           | pin PLHO; I <sub>OH</sub> = 500 μA; V <sub>CC</sub> = 3.15 V  | 3.1  | -    | -    | V    |    |
| I <sub>CC</sub>  | supply current            | V <sub>I</sub> = 0 V or V <sub>CC</sub> ; I <sub>O</sub> = 0 A  | [1]  | -    | 5    | -    | μA |
|                  |                           | pins V <sub>CC</sub> and V <sub>CC(B)</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>CC(B)</sub> = 3.6 V to 5.5 V; V <sub>I</sub> = 0 V or V <sub>CC</sub> ; pins Bn = V <sub>CC(B)</sub> ; pins Cn = V <sub>CC(B)</sub> or floating | -    | 0.1  | 100  | μA   |    |
|                  |                           | pins V <sub>CC(B)</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V or V <sub>CC</sub> ; pins Cn = 0 V  | [2]  |      |      |      |    |
|                  |                           | pin DIR = 3.6 V; V <sub>CC(B)</sub> = 3.6 V   | -    | 10   | 15   | mA   |    |
|                  |                           | pin DIR = 3.6 V; V <sub>CC(B)</sub> = 5.5 V   | -    | 16   | 20   | mA   |    |
|                  |                           | pin DIR = 0 V; V <sub>CC(B)</sub> = 3.6 V; pins Bn = 0 V  | -    | 30   | 40   | mA   |    |
|                  |                           | pin DIR = 0 V; V <sub>CC(B)</sub> = 5.5 V; pins Bn = 0 V  | -    | 47   | 60   | mA   |    |
| I <sub>OFF</sub> | power-off leakage current | pins Bn, Cn, Yn; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V  |      |      |      |      |    |
|                  |                           | V <sub>CC(B)</sub> = 0 V  | -    | -    | ±100 | μA   |    |
|                  |                           | V <sub>CC(B)</sub> = 4.5 V  | -    | -    | ±100 | μA   |    |
| I <sub>I</sub>   | input leakage current     | V <sub>I</sub> = 0 V to V <sub>CC</sub>   | [3]  | -    | -    | ±1   | μA |
| I <sub>OZ</sub>  | OFF-state output current  | 3-state; V <sub>O</sub> = V <sub>CC</sub> or 0 V  | [3]  | -    | -    | ±20  | μA |
| R <sub>O</sub>   | output resistance         | V <sub>CC</sub> = 3.3 V; see Fig. 9   |      |      |      |      |    |
|                  |                           | V <sub>O</sub> = 1.65 V ± 0.1 V; B/Y side   | [1]  | 35   | 45   | 55   | Ω  |
| R <sub>PU</sub>  | pull-up resistance        | B/Y side; V <sub>CC</sub> = 3.3 V; output in high-Z with resistive pull-up  | [1]  | 1.15 | 1.4  | 1.65 | kΩ |

[1] Typical values at T<sub>amb</sub> = 25 °C.

[2] Includes extra I<sub>CC(B)</sub> current from pull-up resistors, i.e. I<sub>CC(B)</sub> = (total number of LOW inputs on B and C sides) × (V<sub>CC(B)</sub> / R<sub>PU</sub>).

[3] The pull-up resistor on the B side outputs makes it impossible to test I<sub>OZ</sub> on the B side. This applies to the input current on the C side inputs as well.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ;  $\text{ground} = 0\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 500\text{ }\Omega$ ;  $T_{amb} = 0\text{ }^\circ\text{C to }70\text{ }^\circ\text{C}$ ; unless specified otherwise.

| Symbol          | Parameter                     | Conditions  | Min  | Typ [1] | Max | Unit |
|-----------------|-------------------------------|---|------|---------|-----|------|
| $t_{PLH}$       | LOW to HIGH propagation delay | An to Bn or Yn; see Fig. 3 and Fig. 8                   | 0    | 12.5    | 20  | ns   |
| $t_{PHL}$       | HIGH to LOW propagation delay | An to Bn or Yn; see Fig. 3 and Fig. 8                   | 0    | 13.9    | 23  | ns   |
| $t_{pd}$        | propagation delay             | see Fig. 4 and Fig. 8 [2]                               |      |         |     |      |
|                 |                               | Bn to An  | 0    | -       | 12  | ns   |
|                 |                               | Cn to An  | -    | -       | 15  | ns   |
|                 |                               | PLHI to PLHO  | -    | -       | 20  | ns   |
|                 |                               | HLHI to HLHO  | -    | -       | 15  | ns   |
| SR              | slew rate                     | Bn/Yn; $R_L = 62\text{ }\Omega$ ; see Fig. 5 and Fig. 8 | 0.05 | 0.2     | 0.4 | V/ns |
| $t_{dis}$       | disable time                  | HD to Yn or Bn; see Fig. 6 and Fig. 8 [3]               | -    | -       | 20  | ns   |
|                 |                               | HD to PLHO; see Fig. 6 and Fig. 7 [3]                   | -    | -       | 20  | ns   |
|                 |                               | $R_L = 250\text{ }\Omega$ ; see Fig. 6 and Fig. 7 [3]   |      |         |     |      |
|                 |                               | DIR to Bn; TP load on B/Y side                          | -    | -       | 50  | ns   |
|                 |                               | DIR to An   | -    | -       | 15  | ns   |
|                 |                               | $\overline{OE}A$ to An                                  | -    | -       | 6   | ns   |
| $t_{en}$        | enable time                   | HD to Yn or Bn; see Fig. 6 and Fig. 7 [4]               | -    | -       | 20  | ns   |
|                 |                               | HD to PLHO; see Fig. 6 and Fig. 7 [4]                   | -    | -       | 20  | ns   |
|                 |                               | $R_L = 250\text{ }\Omega$ ; see Fig. 6 and Fig. 7 [4]   |      |         |     |      |
|                 |                               | DIR to Bn; TP load on B/Y side                          | -    | -       | 30  | ns   |
|                 |                               | DIR to An   | -    | -       | 50  | ns   |
|                 |                               | $\overline{OE}A$ to An                                  | -    | -       | 12  | ns   |
| $\Delta t_{PD}$ | propagation delay difference  | $t_{PZH} - t_{PHZ}$ ; HD to output                      | -    | -       | 10  | ns   |

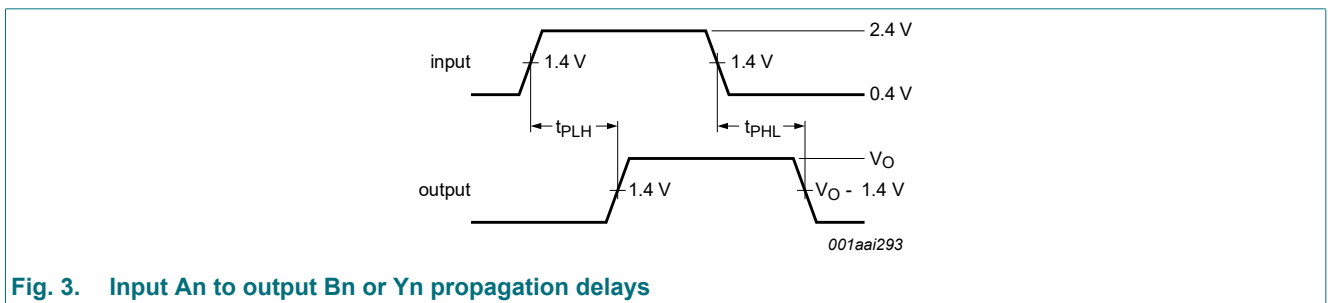
[1] Value at  $T_{amb} = 25\text{ }^\circ\text{C}$  and  $V_{CC} = 3.3\text{ V}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

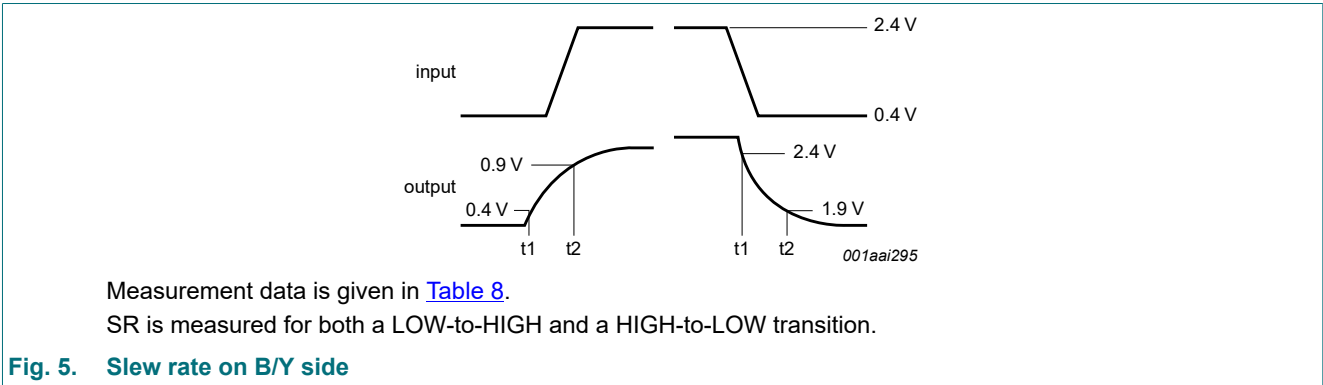
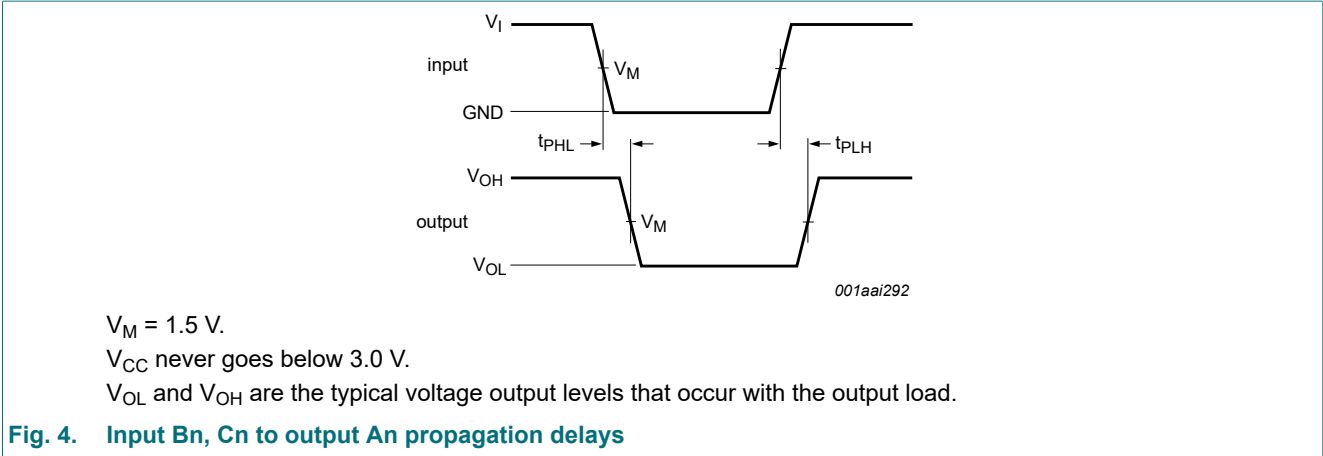
[3]  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[4]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

### 10.1. Waveforms and test circuit



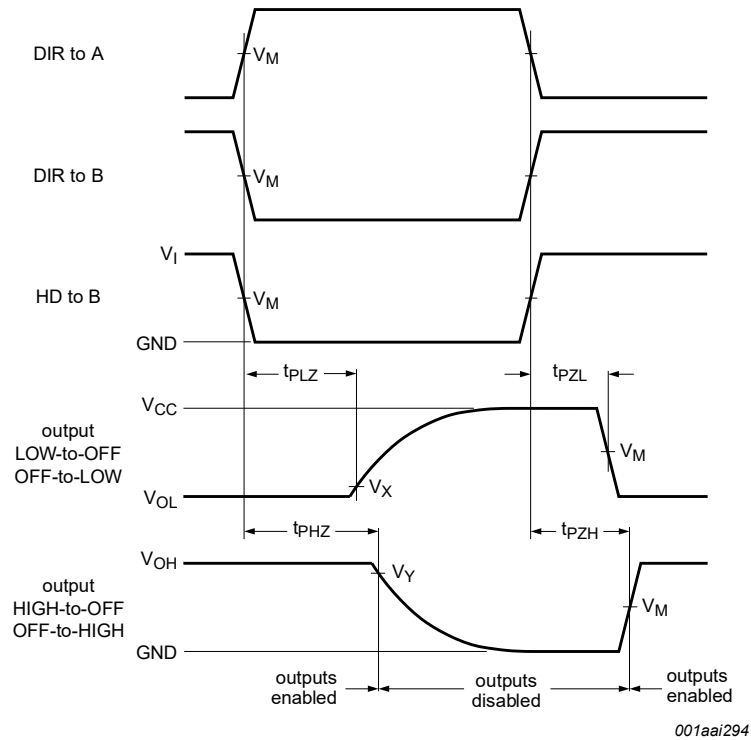
**Fig. 3. Input An to output Bn or Yn propagation delays**



**Table 8. Slew rate measurements**

| $t_r$ | $t_f$ | $t_w$                       | $R_L$       | $V_O$ transition (see <a href="#">Fig. 8</a> )    |   |
|-------|-------|-----------------------------|-------------|---|---|
|       |       |                             |             | Rising  | Falling   |
| 3 ns  | 3 ns  | 150 ns < $t_w$ < 10 $\mu$ s | 62 $\Omega$ | from $V_O = 0.4\text{ V}$ to $V_O = 0.9\text{ V}$ | from $V_O = 2.4\text{ V}$ to $V_O = 1.9\text{ V}$ |



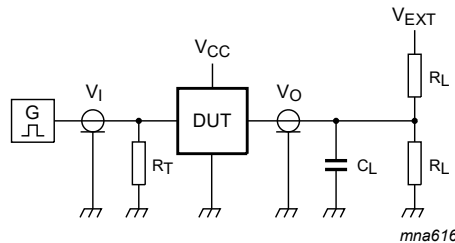


Test circuit is shown in Fig. 7.

Measurement points are given in Table 9.

$V_{OL}$  and  $V_{OH}$  are the typical voltage output levels that occur with the output load.

Fig. 6. Enable and disable times



Test conditions are given in Table 9.

Fig. 7. Test circuit for measuring enable and disable times

Table 9. Test data for test circuit measuring enable disable times Bn to An

| Parameter                     | $V_{CC}$       | Input    |       | Output |                    |                  | $V_{EXT}$          |                    |
|-------------------------------|----------------|----------|-------|--------|--------------------|------------------|--------------------|--------------------|
|                               |                | $V_I$    | $V_M$ | $V_M$  | $V_X$              | $V_Y$            | $t_{PZH}, t_{PHZ}$ | $t_{PZL}, t_{PLZ}$ |
| DIR to Bn, An;<br>OEĀ to An   | < 2.7 V        | $V_{CC}$ | 1.5 V | 1.5 V  | $V_{OL} \pm 0.3 V$ | $V_{OH} - 0.3 V$ | GND                | $2V_{CC}$          |
|                               | 2.7 V to 3.6 V | 2.7 V    | 1.5 V | 1.5 V  | $V_{OL} \pm 0.3 V$ | $V_{OH} - 0.3 V$ | GND                | $2V_{CC}$          |
| HD to Yn or Bn;<br>HD to PHLO | < 2.7 V        | $V_{CC}$ | 1.5 V | 1.5 V  | -                  | $V_{OH} - 0.3 V$ | open               | -                  |
|                               | 2.7 V to 3.6 V | 2.7 V    | 1.5 V | 1.5 V  | -                  | $V_{OH} - 0.3 V$ | open               | -                  |

3.3 V parallel interface transceiver/buffer

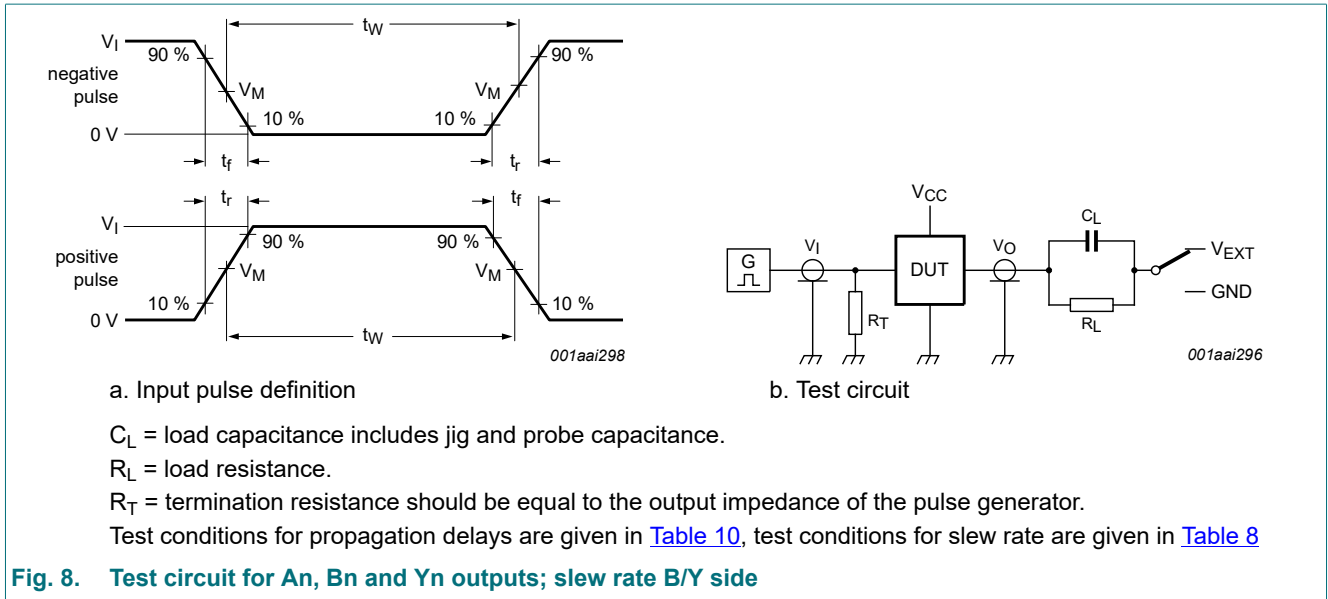
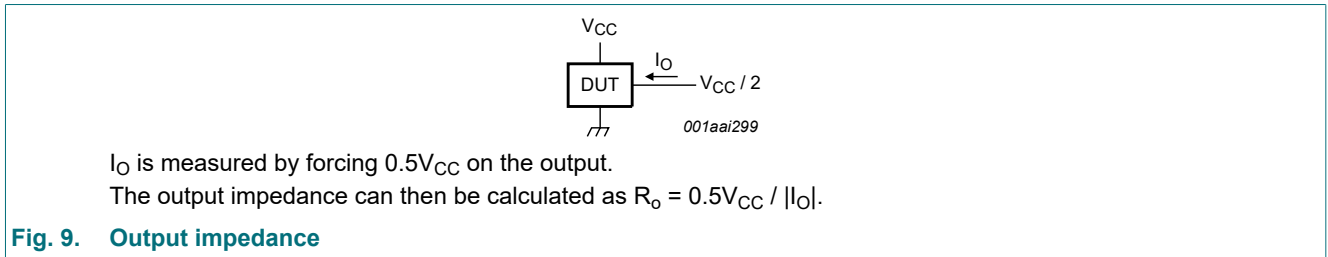


Table 10. Test conditions for An, Bn and Yn outputs

| Output | $V_I$ | $V_M$ | Repetition rate | $t_w$  | $t_r$ | $t_f$ | Switch position       |                       |
|--------|-------|-------|-----------------|--------|-------|-------|-----------------------|-----------------------|
|        |       |       |                 |        |       |       | $t_{PLH}$ , $t_{PZH}$ | $t_{PHL}$ , $t_{PHZ}$ |
| An     | 3.0 V | 1.5 V | 1 MHz           | 500 ns | 3 ns  | 3 ns  | GND                   | GND                   |
| Bn, Yn | 3.0 V | 1.5 V | 1 MHz           | 500 ns | 3 ns  | 3 ns  | GND                   | $V_{EXT} = 2.8 V$     |



# 11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

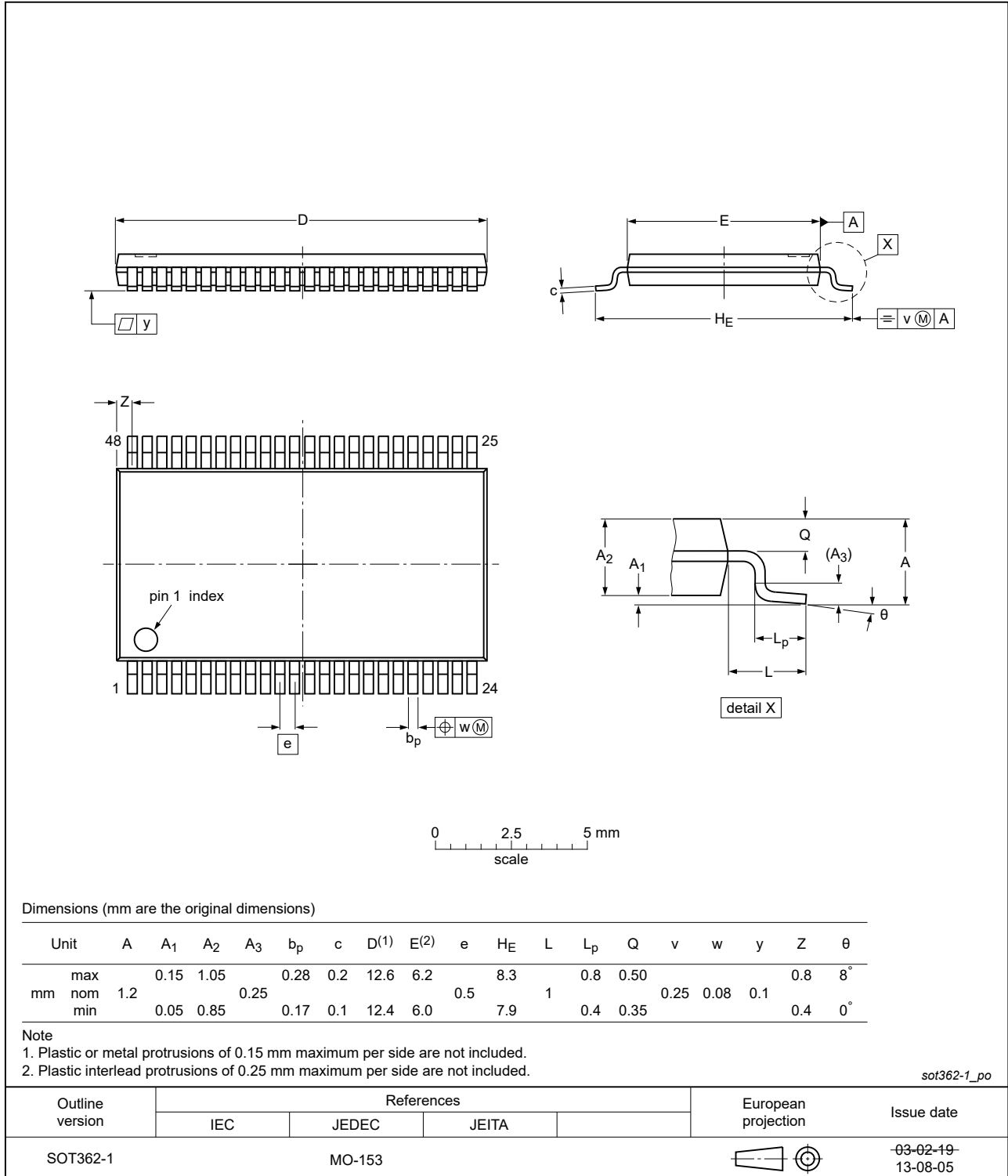


Fig. 10. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 11. Abbreviations

| Acronym | Description                                       |
|---------|---|
| CDM     | Charged Device Model                              |
| CMOS    | Complementary Metal-Oxide Semiconductor           |
| DUT     | Device Under Test                                 |
| ECP     | Extended Capability Port                          |
| EPP     | Enhanced Parallel Port                            |
| ESD     | ElectroStatic Discharge                           |
| HBM     | Human Body Model                                  |
| IEEE    | Institute of Electrical and Electronics Engineers |
| LSTTL   | Low-power Schottky Transistor-Transistor Logic    |
| MM      | Machine Model                                     |
| TTL     | Transistor-Transistor Logic                       |

## 13. Revision history

Table 12. Revision history

| Document ID    | Release date   | Data sheet status     | Change notice | Supersedes   |
|----------------|--|-----------------------|---------------|--------------|
| PDI1284P11 v.4 | 20210706   | Product data sheet    | -             | PDI1284P11_3 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number PDI1284P11DL (SOT370-1 / SSOP48) removed.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation removed.</li> <li><a href="#">Fig. 10</a>: Package outline drawing SOT362-1 (TSSOP48) updated.</li> </ul> |                       |               |              |
| PDI1284P11_3   | 20080825   | Product data sheet    | -             | PDI1284P11_2 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Quick reference table removed.</li> <li><a href="#">Table 7</a>, <math>t_{PHL}</math>: Maximum value of 20 ns replaced by 23 ns.</li> <li><a href="#">Table 11</a>: Abbreviations list added.</li> </ul>   |                       |               |              |
| PDI1284P11_2   | 19990917   | Product specification | -             | PDI1284P11_1 |
| PDI1284P11_1   | 19970915   | Product specification | -             | -            |

## 14. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
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| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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