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Freescale Semiconductor
Advance Information

Document Number: MC33389
Rev. 5.0, 3/2007

System Basis Chip with Low Speed Fault Tolerant CAN

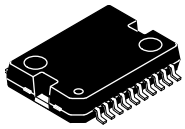
33389

SYSTEM BASIS CHIP

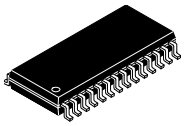
The 33389 is a monolithic integrated circuit combining many functions frequently used by automotive Engine Control Units (ECUs). It incorporates a low speed fault tolerant CAN transceiver.

Features

- Dual Low Drop Voltage Regulators, with Respectively 100 mA and 200 mA Current Capabilities, Current Limitation, and Over Temperature Detection with Pre-warning
- 5.0 V Output Voltage for V1 Regulator
- Three Operational Modes (Normal, Stand-by, and Sleep Modes) Separated from the CAN Interface Operating Modes
- Low Speed 125 kBaud Fault Tolerant CAN Interface, Compatible with 33388 Stand Alone Physical Interface
- V1 Regulator Monitoring and Reset Function
- Three External High Voltage Wake-Up Inputs, Associated with V3 V_{BAT} Switch
- 100 mA Output Current Capability for V3 V_{BAT} Switch Allowing Drive of External Switches or Relays
- Low Stand-by and Sleep Current Consumption
- V_{BAT} Monitoring and V_{BAT} Failure Detection Capabilities
- DC Operating Voltage up to 27 V
- 40 V Maximum Transient Voltage
- Programmable Software Window Watchdog and Reset
- Wake-Up Capabilities (CAN Interface, Local Programmable Cycle Wake
- INterface with the MCU through the SPI
- Pb-Free Packaging Designated by Suffix Codes VW and EG



DH SUFFIX
VW SUFFIX (PB-FREE)
PLASTIC PACKAGE
98ASH70273A
20-PIN HSOP



DW SUFFIX
EG SUFFIX (PB-FREE)
PLASTIC PACKAGE
98ASB42345B
28-PIN SOICW

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33389CDH/R2	-40 to 125°C	HSOP-20
MC33389CVW/R2		
MC33389CDW/R2		SO-28
MC33389DDW/R2		

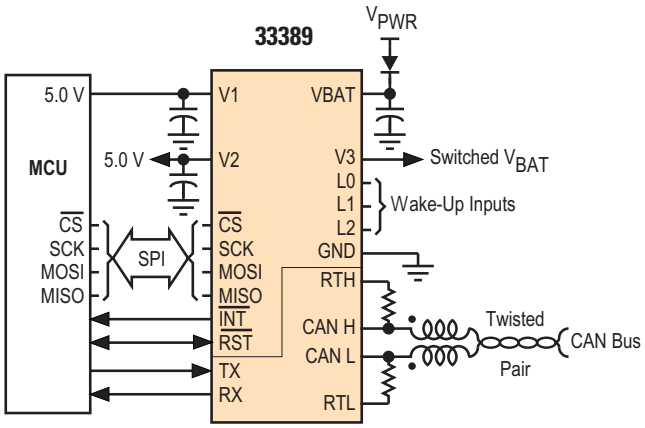


Figure 1. 33389 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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DEVICE VARIATIONS

Table 1. Device Variations

Freescale Part No.	V1 Undervoltage
MC33389CDH MC33389CVW MC33389CDW	In V1 undervoltage condition, device remains in permanent reset state until V1 returns to normal conditions. V1 is protected by overcurrent and overtemperature functions.
MC33389DDW	The sole difference between the C version and the D version is V1 Reset Threshold. Reference V1 Reset Threshold on V1 on page 9.

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INTERNAL BLOCK DIAGRAM

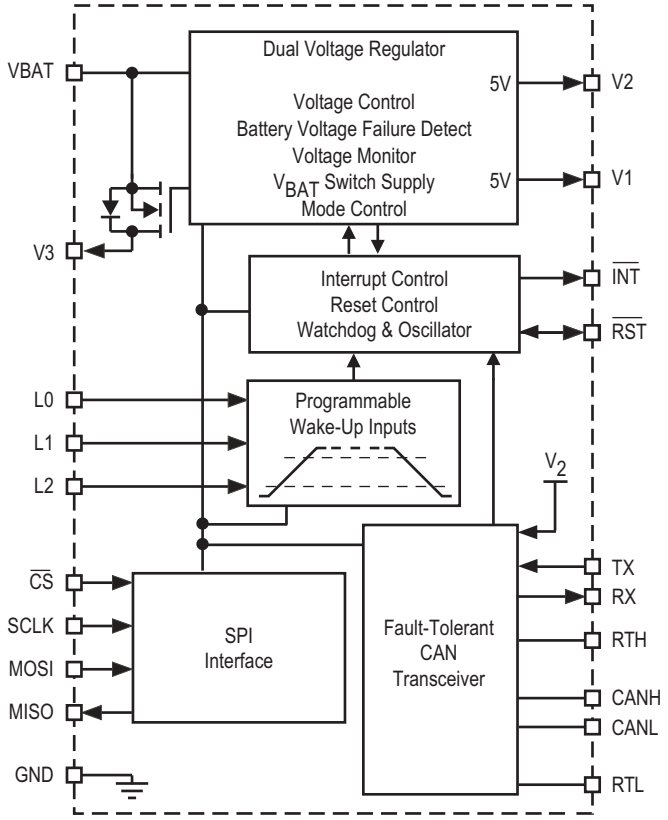

Figure 2. 33389 Simplified Internal Block Diagram

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PIN CONNECTIONS

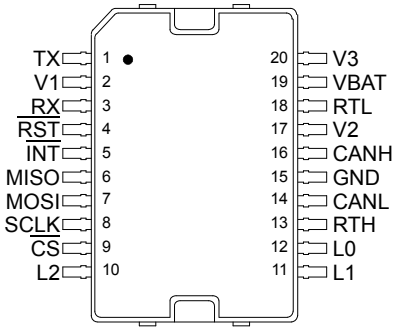

Figure 3. 33389 Pin Connections

Table 1. 33389 Pin Definitions: HSOSP 20-Lead

A functional description of each pin can be found in the Functional Pin Description section beginning on page 17.

Pin Number	Pin Name	Formal Name	Definition
1	TX	Transmitter Data	Transmitter input of the LS CAN interface
2	V1	Voltage Regulator One	This 5.0 V pin is a 3% low drop voltage regulator dedicated to the microcontroller supply.
3	RX	Receiver Data	Receiver output of the LS CAN interface
4	$\overline{RST}$	Reset	This is an Input/Output pin.
5	$\overline{INT}$	Interrupt Output	This output is asserted LOW when an enabled interrupt condition occurs.
6	MISO	Master In/Slave Out	This pin is the tri-state output from the shift register.
7	MOSI	Master Out/Slave In	This pin is for the input of serial instruction data.
8	SCLK	System Clock	This pin clocks the internal shift registers.
9	$\overline{CS}$	Chip Select	This pin communicates with the system MCU and enables SPI communication.
10 - 12	L0 - L2	Level 0 - 2 inputs (L0: L2)	Input interfaces to external circuitry. Levels at these pins can be read by SPI and input can be used as programmable wake-up input in Sleep or Stop mode.
13	RTH	RTH	Pin for the connection of the bus termination to CANH
14	CANL	CAN Low	CAN low input/output
15	GND	Ground	This pin is the ground of the integrated circuit.
16	CANH	CAN High	CAN high input/output
17	V2	Voltage Regulator Two	This 5.0 V pin is a low drop voltage regulator dedicated to the peripherals supply.
18	RTL	RTL	Pin for the connection of the bus termination to CANL
19	VBAT	Voltage Battery	This pin is voltage supply from the battery.
20	V3	Voltage Regulator Three	This pin is a 10 Ω switch to V_{BAT}, used to supply external contacts or relays.

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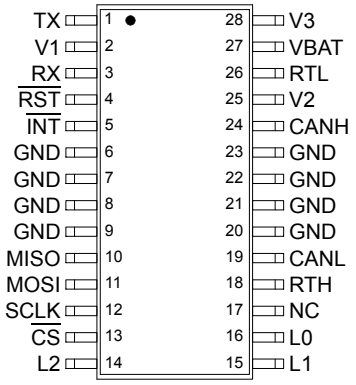

Table 2. 33389 Pin Definitions: SOICW 28-Lead

A functional description of each pin can be found in the Functional Pin Description section beginning on page 17.

Pin Number	Pin Name	Formal Name	Definition
1	TX	Transmitter Data	Transmitter input of the LS CAN interface
2	V1	Voltage Regulator One	This 5.0 V pin is a 3% low drop voltage regulator dedicated to the microcontroller supply.
3	RX	Receiver Data	Receiver output of the LS CAN interface
4	$\overline{RST}$	Reset	This is an Input/Output pin.
5	$\overline{INT}$	Interrupt	This output is asserted LOW when an enabled interrupt condition occurs.
6 -9 20 - 23	GND	Ground	These device ground pins are internally connected to the package lead frame to provide a 33389-to-PCB thermal path.
10	MISO	Master In/Slave Out	This pin is the tri-state output from the shift register.
11	MOSI	Master Out/Slave In	This pin is for the input of serial instruction data.
12	SCLK	System Clock	This pin clocks the internal shift registers.
13	$\overline{CS}$	Chip Select	This pin communicates with the system MCU and enables SPI communication.
14, 15, 16	L0: L2	Wake-up Input (L0: L2)	Input interfaces to external circuitry. Levels at these pins can be read by SPI and input can be used as programmable wake-up input in Sleep or Stop mode.
17	NC	No Connect	This pin does not connect.
18	RTH	Thermal Resistance High	Pin for the connection of the bus termination to CANH
19	CANL	CAN Low	CAN low input/output
24	CANH	CAN High	CAN high input/output
25	V2	Voltage Regulator Two	This 5.0 V pin is a low drop voltage regulator dedicated to the peripherals supply.
26	RTL	Thermal Resistance Low	Pin for the connection of the bus termination to CANL
27	VBAT	Voltage Battery	This pin is voltage supply from the battery.
28	V3	Voltage Regulator Three	This pin is a 10 Ω switch to V_{BAT}, used to supply external contacts or relays.

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ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
DC Voltage at VBAT Pin	V_{BAT}	-0.3 to 27	V
Transient Voltage at VBAT Pin t < 500 ms (load dump)	V_{BAT}	40	V
DC Voltage at Pins CANH and CANL	V_{BAT}	-20 to 27	V
Transient Voltage at Pins CANH and CANL 0.0 < V2 < 5.5, V_{BAT} > 0.0, t < 500 ms	V_{BAT}	-40 to 40	V
Coupled Transient Voltage at Pins CANH and CANL With 100 Ω Termination Resistors, Coupled Through 1.0 nF [(1)]	V_{BAT}	-100 to 100	V
DC Voltage at Pins V1 and V2	V_{BAT}	-0.3 to 6.0	V
DC Current at Output Pins RX, MISO, $\overline{RST}$, $\overline{INT}$	V_{BAT}	-20 to 20	mA
DC Voltage at Input Pins TX, MOSI, $\overline{CS}$, $\overline{RST}$	V_{BAT}	-0.3 to 6.0	V
DC Voltage at Pins L0, L1, L2 0.0 < V_{BAT} < 40 V	V_{BAT}	-0.3 to 40	V
Current at Pins L0, L1, L2	V_{BAT}	-15	mA
Transient Current at Pin V3	V_{BAT}	-30 to 20	mA
DC Voltage at pins RTH and RTL	V_{BAT}	-0.3 to 40	V
ESD Voltage on any Pin (HBM 100 pF, 1.5 K)	V_{BAT}	-2.0 to 2.0	kV
ESD Voltage on L0, L1, L2, CANH, CANL, VBAT	V_{BAT}	-2.0 to 2.0	kV
ESD Voltage on any Pin (MM 200 pF, 0 Ω)	V_{BAT}	-150 to 150	V
THERMAL RATINGS			
Operating Junction Temperature	T_J	-40 to 150	°C
Ambient Temperature	T_A	-40 to 125	°C
Storage Temperature	T_S	-55 to 165	°C

Notes
1. Pulses 1, 2, 3a, and 3b according to ISO7637.

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Table 3. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RESISTANCE			
RTH, RTL Termination Resistance	R_{RTHRTL}	500 to 16 k	Ω
Junction to Heatsink Thermal Resistance for HSOP-20 33% Power on V1, 66% on V2 (including CAN) [(2)]	R_{AJC}	3.1	°C/W
Junction to Pin Thermal Resistance for SO-28WD [(3)]	$R_{AS/P}$	17	°C/W
Thermal Shutdown Temperature	T_{SD}	165	°C
Peak Package Reflow Temperature During Reflow [(4)], [(5)]	T_{PPRT}	Note 5	°C

Notes

2. Refer to thermal management in device description section.
3. Refer to thermal management in device section. Ground pins 6, 7, 8, 9, 20, 21, 22, and 23 of SO28WB package.
4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
5. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

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STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions V_{BAT}, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VBAT)					
Nominal VBAT Operating Range	V_{BAT}	5.5	—	18	V
Functional VBAT Operating Range	V_{BAT}	5.5	—	27	V
V_{BAT} Threshold for BAT_{FAIL} Flag	BAT_{FAIL}	2.0	—	4.0	V
Delay for Signalling BAT_{FAIL}	TFAIL	—	150	400	µs
Overvoltage V_{BAT} Threshold	BAT_{HIGH}	18	20	22	V
Delay for Setting BAT_{HIGH} Flag	T_{HIGH}	4.0	18	50	µs
Supply Current in Sleep Mode Forced Wake-Up and Cyclic Sense Disabled V_{BAT} = 12 V, T_J = 25°C to 150°C	I_{SLEEP1}	—	75	125	µA
Supply Current in Sleep Mode Forced Wake-Up and Cyclic Sense Disabled V_{BAT} = 12 V, T_J = -40°C to 25°C	I_{SLEEP2}	—	—	210	µA
Supply Current in Sleep Mode Forced Wake-Up and Cyclic Sense Enabled V_{BAT} = 12 V, T_J = 25°C to 150°C	I_{SLEEP3}	—	105	155	µA
Supply Current in Sleep Mode Forced Wake-Up and Cyclic Sense Enabled V_{BAT} = 12 V, T_J = -40°C to 25°C	I_{SLEEP4}	—	—	250	µA
Supply Current in Sleep Mode Forced Wake-Up and Cyclic Sense Disabled V_{BAT} = 12 V, T_J = 25°C to 150°C	I_{SLEEP5}	—	—	300	µA
Supply Current in Stand-by Mode	I_{STB2}	—	0.5	1.0	mA
Supply Current in Normal Mode Normal Mode with I(V1) = 1 I(V2) = 0 Bus in Recessive State	I_{NREC}	—	3.5	7.0	mA
POWER OUTPUT					
V1 Output Voltage 0 mA < I_{OUT} < 100 mA 5.5 V < V_{BAT} < 27 V	$V1_{NOM}$	4.85	5.0	5.15	V
V1 Output Voltage I_{OUT} =< 100 mA 27 V < V_{BAT} < 40 V	V1	4.8	5.0	5.2	V
V1 Drop Voltage I_{OUT} =< 100 mA [(6)]	V1DROP	—	0.35	0.5	V

Notes
6. Measured when V1 has dropped 100mV below its nominal value

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT}, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
V1 Output Current Limitation $V1_{NOM}$ - 100 mV	I1MAX	130	170	200	mA
V1 Overtemperature Shut OFF Threshold Junction Temperature	TV1H	160	—	190	°C
V1 Pre-Warning Temperature Threshold Junction Temperature	TV1L	130	—	160	°C
V1 Temperature Threshold Difference	TV1H-TV1L	20	—	40	°C
V1 Reset Threshold on V1 5.5 V < V_{BAT} < 27 V (C Version) (D Version)	VR1	 4.1 V2 - 0.4	 4.3 V1 - 0.28	 4.8 V1 - 0.1	V
V1 Reset Active V1 Range	V1R	1.0	VR1	—	V
V1 Reverse Current from V1 to V_{BAT} and GND V1 = 4.9 V, 0 < V_{BAT} < 4.9 V	IREV	—	—	1.0	mA
V2 Output Voltage 0 mA < I_{OUT} < 200 mA 5.5 V < V_{BAT} < 40 V	V2NOM	4.75	5.0	5.25	V
V2 Drop Voltage I_{OUT} = 200 mA (7)	V2DROP	—	0.2	0.5	V
V2 Drop Voltage I_{OUT} = 20 mA (7)	V2DROP	—	0.05	0.15	V
V2 Output Current Limitation $V2_{NOM}$ -100 mV	$I1_{MAX}$	220	280	350	mA
V2 Threshold on V2 to Report V2 OFF V2 Nominal	V_{R2}	4.1	4.55	4.75	V
V_{R2} Delay Time	V_{R2}	20	—	70	µs
V2 Overtemperature Pre-Warning Threshold V2 Junction Temperature	T_{V2L}	130	—	160	°C
V2 Overtemperature Switch-OFF Threshold V2 Junction Temperature	T_{V2H}	155	—	185	°C
V2 Line Regulation 9.0 V < V_{BAT} < 16.5	$V2_{LR1}$	-15	—	+15	mV
V2 Load Regulation 4.0 mA < I_{LOAD} < 200 mA	$V2_{LR2}$	-75	—	+75	mV
V2 Line Ripple Rejection 100 Hz, 1.0 V_{PP} on V_{BAT} (8)	$V2_{LRR}$	30	55	—	dB

Notes
7. Measured when V1 has dropped 100mV below its nominal value
8. Guaranteed by design; however, it is not production tested

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT}, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
V2 Percentage Difference V2-V1 V_{BAT} > 9.0, I_{V1} = 20 mA, I_{V2} = 40 mA	$V2_{V2-V1}$	-3.0	—	3.0	%
V3 High Level Voltage Drop I_{V3} = -50 mA, 9.0 V < V_{BAT} < 40 V	$V3_{DROP}$	—	0.4	1.0	V
V3 High Level Voltage Drop I_{V3} = -50 mA, 6.0 V < V_{BAT} < 9.0 V	$V3_{DROP}$	—	—	1.5	V
V3 Leakage Output Limitation 5.5 V < V_{BAT} < 27 V	$I3_{LIM}$	100	150	250	mA
V3 Leakage Current V3 = 0 (V3 OFF)	$I3_{LEAK}$	—	—	15	µA
V3 Overtemperature Detection Junction Temperature	T_{V3}	155	—	185	°C
V3 Voltage with -30 mA (negative current for Relay Switch OFF) No Functional Error Allowed for t ≤ 100 ms	V_{V3}	0.3	—	0.5	V
CAN Transceiver V2 for Forced Bus Stand-by Mode (Fail Safe)	VRC2	3.0	3.9	4.7	V
CANH/L Differential Receiver, Threshold Voltage	V_{CANTH}	-3.2	—	-2.5	V
CANH/L Differential Receiver, Dominant to Recessive Threshold (Bus Failures 1, 2, and 5)	$V_{CANDRTH}$	-3.2	—	-2.5	V
CANH Recessive Output Voltage TX = High, R(RTH) < 4.0 k	V_{CANH}	—	—	0.2	V
CANL Recessive Output Voltage TX = High, R(RTH) < 4.0 k	V_{CANL}	V2-0.2	—	—	V
CANH Output Voltage, Dominant TX = 0 V, BusNormal Mode, I_{CANH} = - 40 mA	V_{CANH}	V2-1.4	—	—	V
CANL Output Voltage, Dominant TX = 0 V, Bus Normal Mode, I_{CANL} = - 40 mA	V_{CANL}	—	—	1.4	V
CANH Output Current Limit (V_{CANH} = 0.0 V, TX = 0)	I_{CANH}	50	75	100	mA
CANL Output Current Limit (V_{CANL} = 14 V, TX = 0)	I_{CANL}	50	95	130	mA
Detection Threshold for Short Circuit to Battery Voltage Bus Normal Mode	V_{CANH}-V_{CANL}	7.3	7.9	8.9	V
Detection Threshold for Short Circuit to Battery Voltage Bus Stand-by Mode	V_{CANH}	V_{BAT}/2+3	—	V_{BAT}/2+5	V
CANH Output Current, Failure 3 Bus Stand-by Mode V_{CANH} = 12 V	I_{CANHF3}	—	5.0	10	µA
CANL Output Current, Failure 4 Bus Stand-by Mode, V_{CANL} = 0.0 V, V_{BAT} = 12 V	I_{CANLF4}	—	0.0	2.0	µA

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT}, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
CANL Wake-Up Voltage Threshold Bus Stand-by Mode	V_{WAKEL}	2.5	3.3	3.9	V
CANH Wake-Up Voltage Threshold Bus Stand-by Mode	V_{WAKEH}	1.2	2.0	2.7	V
Wake-Up Threshold Difference	V_{WAKEL} - V_{WAKEH}	0.2	—	—	V
CANH Single Ended Receiver Threshold Failures 4, 6, and 7	V_{CANH}	1.5	1.85	2.15	V
CANL Single Ended Receiver Threshold Failures 3 and 8	V_{CANL}	2.8	3.05	3.4	V
CANL Pull-Up Current Bus Normal Mode	I_{CANLPU}	45	75	90	μA
CANH Pull Down Current Bus Normal Mode	I_{CANLPD}	45	75	90	μA
Receiver Differential Input Impedance CANH/CANL	R_{DIFF}	100	—	180	kΩ
Differential Receiver Common Mode Voltage Range	V_{COM}	-8.0	—	8.0	V
RTL to V2 Switch on Resistance I_{OUT} < -10 mA, Bus Normal Operating Mode	R_{RTL}	10	25	70	Ω
RTL to Battery Switch Series Resistance Bus Stand-by Mode	R_{RTL}	8.0	12.5	20	kΩ
RTH to Ground Switch on Resistance I_{OUT} < 10 mA, All Modes	R_{RTH}	—	25	70	Ω
CONTROL INTERFACE					
High Level Input Voltage	V_{IH}	0.7 V1	—	V1 + 0.3 V	V
$\overline{CS}$ Threshold for SPI Wake-Up SBC in Sleep Mode, V1 < 1.5 V	V_{CSTH}	—	2.2	—	V
$\overline{CS}$ Filter Time for SPI Wake-Up SBC in Sleep Mode, V1 < 1.0 V	t_{CSFT}	—	—	3.0	μs
Low Level Input Voltage	V_{IL}	-0.3	—	0.3 V1	V
High Level Input Current on $\overline{CS}$ V_I = 4.0 V	I_{CSH}	-100	—	-20	μA
Low Level Input Current on $\overline{CS}$ V_I = 1.0 V	I_{CSL}	-100	—	-20	μA
TX High Level Input Current V_I = 4.0 V	I_{TXH}	-200	-80	-25	μA
TX Low Level Input Current V_I = 1.0 V	I_{TXL}	-800	-320	-100	μA
SI, SCLK Input Current 0 < V_{IN} < V1	I_{SISLK}	-10	—	+10	μA

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT}, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE (CONTINUED)					
RX, $\overline{INT}$, MISO High Level Output Voltage I_0 = -250 µA	V_{OH}	V1 - 0.9	—	V1	V
RX, $\overline{INT}$, MISO Low Level Output Voltage I_0 = -1.5 mA	V_{OL}	0.0	—	0.9	V
RX, $\overline{INT}$, MISO Tri-Stated SO Output Current 0 V < V_{SO} < V1	I_Z	-2.0	—	+2.0	µA
$\overline{RST}$ High Level Input Voltage	V_{IH}	0.7 V1	—	V1 + 0.3 V	—
$\overline{RST}$ Low Level Input Voltage	V_{IL}	-0.3	—	-0.3 V1	V
$\overline{RST}$ High Level Output Current 1 0.0 < V_{OUT} < 0.5 V1	I_{RSTH1}	-50	-30	-10	µA
$\overline{RST}$ High Level Output Current 2 0.5 < V_{OUT} < V1	I_{RSTH2}	—	-300	—	µA
$\overline{RST}$ Low Level Output Voltage (I_0 = 1.5 mA) 1.0 V < V_{BAT} < 27 V	V_{RST}	0.0	—	0.9	V
LX/Wake-Up Positive Switching Threshold 6.0 V <V_{BAT} < 16 V	V_{WUP}	3.0	3.7	4.5	V
LX/Wake-Up Negative Switching Threshold 6.0 V <V_{BAT} < 16 V	V_{WUN}	2.5	3.0	3.8	V
LX/Wake-Up Hysteresis 6.0 V <V_{BAT} < 16 V	V_{HYS}	—	700	—	mA
LX/Wake-Up Leakage Current 0 < V_{WU} < V_{BAT}	I_{LXWU}	-5.0	—	+5.0	µA
LX Input Current at 40 V	V_{IN}	—	350	600	µA

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DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
MICROCONTROLLER INTERFACE					
AC CANL/CANH Slew Rates, Rising or Falling Edges, TX from Recessive to Dominant State C_{LOAD} - 10 nF, 133 Ω Termination Resistors	t_{CANRD}	3.5	5.0	10	V/µs
AC CANL/CANH Slew Rates, Rising or Falling Edges, TX from Dominant to Recessive State C_{LOAD} - 10 nF, 133 Ω Termination Resistors	t_{CANDR}	2.0	3.5	10	V/µs
AC Propagation Delay TX to RX Low C_{LOAD} - 10 nF, 133 Ω Termination Resistors	t_{DH}	—	1.2	2.0	µs
AC Propagation Delay TX to RX High C_{LOAD} - 10 nF, 133 Ω Termination Resistors	t_{DL}	—	2.0	3.0	µs
Wake-Up Filter Time	t_{WUFT}	8.0	20	38	µs
$\overline{RST}$ Duration after V1 High	t_{RES}	—	1.0	—	ms
SCLK Clock Period	t_{PSCLK}	500	—	—	ns
SCLK Clock High Time	t_{WSCLKH}	175	—	—	ns
SCLK Clock Low Time	t_{WSCLKL}	175	—	—	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	250	50	—	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LEAD}	250	50	—	ns
SI to Falling Edge of SCLK	t_{SISU}	125	25	—	ns
Falling Edge of SCLK to SI	$t_{SI(HOLD)}$	125	25	—	ns
SO Rise Time (C_L = 200 pF)	t_{RSO}	—	25	75	ns
SO Fall Time (C_L = 200 pF)	t_{FSO}	—	25	75	ns
SI, $\overline{CS}$, SCLK Incoming Signal Rise Time	t_{RSI}	—	—	200	ns
SI, $\overline{CS}$, SCLK Incoming Signal Fall Time	t_{FSI}	—	—	200	—
Time from Falling Edge of CS to SO Low Impedance High Impedance	 $t_{SO(EN)}$ $t_{SO(DIS)}$	—	—	 200 200	ns
Time from Rising Edge of SCLK to SO Data Valid 0.2 V1 or V2 ≤ SO ≥ 0.8 V1 or V2, C_L = 200 pF	t_{VALID}	—	50	125	—
Running Mode Oscillator Tolerance (Normal Request, Normal and Stand-by Modes [9])	RMOT	-12	—	+12	%
Software Watchdog Timing 1 [9]	t_{SW1}	4.4	5.0	5.6	ms
Software Watchdog Timing 2 [9]	t_{SW2}	8.8	10	11.2	ms
Software Watchdog Timing 3 [9]	t_{SW3}	17.6	20	22.4	ms
Software Watchdog Timing 4 [9]	t_{SW4}	28	32	36	ms

Notes

9. Software watchdog timing accuracy is based on the running mode oscillator tolerance

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Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
MICROCONTROLLER INTERFACE (CONTINUED)					
Software Watchdog Timing 5 (10)	t_{SW5}	44.8	51	58	ms
Software Watchdog Timing 6 (10)	t_{SW6}	65	74	83	ms
Software Watchdog Timing 7 (10)	t_{SW7}	88	100	112	ms
Software Watchdog Timing 8 (10).	t_{SW8}	167	190	213	ms
Sleep Mode Oscillator Tolerance (10)	SMOT	-30	—	+30	%
Cyclic Sense/FWU Timing 1 Sleep Mode (10)	t_{CY1}	22.4	32	46.6	ms
Cyclic Sense/FWU Timing 2 Sleep Mode (10)	t_{CY2}	44.8	64	83.2	ms
Cyclic Sense/FWU Timing 3 Sleep Mode (10)	t_{CY3}	89.6	128	166.4	ms
Cyclic Sense/FWU Timing 4 Sleep Mode (10)	t_{CY4}	179	256	333	ms
Cyclic Sense/FWU Timing 5 Sleep Mode (10)	t_{CY5}	358	512	665	ms
Cyclic Sense/FWU Timing 6 Sleep Mode (10).	t_{CY6}	717	1024	1331	ms
Cyclic Sense/FWU Timing 7 Sleep Mode (10)	t_{CY7}	1434	2048	2662	ms
Cyclic Sense/FWU Timing 8 Sleep Mode (10)	t_{CY8}	5734	8192	10650	ms
Ground Shift Threshold 1 (11) CAN Transceiver Active in Two Wire Operation	GS1	-1.0	-0.7	-0.3	V
Ground Shift Threshold 2 (11) CAN Transceiver Active in Two Wire Operation	GS2	-1.5	-1.2	-0.8	V
Ground Shift Threshold 3 (11) CAN Transceiver Active in Two Wire Operation	GS3	-2.0	-1.7	-1.3	V
Ground Shift Threshold 4 (11) CAN Transceiver Active in Two Wire Operation	GS4	-2.6	-2.2	-1.7	V
BUS TRANSMITTER					
AC Minimum Dominant Time for Wake-Up on CANL or CANH Bus Stand-by Mode, V_{BAT} = 12 V	t_{WAKE}	4.0	—	40	µs
AC Failure 3 Detection Time Bus Normal Mode	t_{AC3D}	10	—	60	µs
AC Failure 3 Recovery Time Bus Normal Mode	t_{AC3R}	10	—	60	µs
AC Failure 6 Detection Time Bus Normal Mode	t_{AC6D}	50	—	400	µs
AC Failure 6 Recovery Time Bus Normal Mode	t_{AC6R}	150	—	1000	µs
AC Failure 4, 7, and 8 Detection Time Bus Normal Mode	t_{AC478D}	0.75	—	4.0	ms

Notes
10. Cyclic sense and forced wake-up timing accuracy are based on the Sleep mode oscillator tolerance.
11. No overlap between two adjacent thresholds.

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Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER (CONTINUED)					
AC Failure 4, 7, and 8 Recovery Time Bus Normal Mode	t_{AC478R}	10	—	60	µs
AC Failure 3, 4, and 7 Detection Time Bus Stand-by Mode, V_{BAT} = 12 V	t_{AC347D}	0.8	—	8.0	ms
AC Failure 3, 4 and 7 Recovery Time Bus Stand-by Mode, V_{BAT} = 12 V	t_{AC347R}	—	2.5	—	ms
AC Edge Count Difference Between CANH/CANL for Failures 1, 2, 5 Detection Bus Normal Mode	CAN_{125D}	—	3.0	—	—
AC Edge Count Difference Between CANH/CANL for Failures 1, 2, 5 Recovery Bus Normal Mode	CAN_{125R}	—	3.0	—	—
TX Permanent Dominant Timer Disable Time Bus Normal and Failure Modes	t_{TXD}	0.75	—	4.0	ms
POWER INPUT TIMING					
V1 Reset Delay Time	t_D	2.0	—	20	µs
V1 Line Regulation 9.0 V < V_{BAT} < 16.5, I_{LOAD} = 10 mA	t_D	-15	2.0	+15	mV
V1 Line Regulation 5.5 V < V_{BAT} < 27 V I_{LOAD} = 10 mA	t_D	-50	10	+50	mV
V1 Load Regulation 1.0 mA < I_{LOAD} < 100 mA	t_D	-50	—	+50	mV
V1 Line Ripple Rejection 100 Hz, 1.0 V_{PP} on V_{BAT} = 12 V, I_{LOAD} = 100 mA (12)	t_D	30	55	—	dB
V1 Line Transient Response V_{BAT} from 12 V to 40 V in 1.0 µs, (10 µF, ESR = 3 Ω)	t_D	—	27	—	mV
V1 Load Transient Response I_{LOAD} from 10 µA to 100 mA in 1.0 µs (CLOAD = 10 µF, ESR = 3 Ω) (13)	t_D	—	400	—	mV
V1 Load Transient Response I_{LOAD} from 10 µA to 100 mA in 1.0 µs (CLOAD = 10 µF, ESR= 0.1 Ω)	t_D	—	16	—	mV

Notes
12. Guaranteed by design. Not production tested.
13. This condition does not produce a reset

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TIMING DIAGRAMS

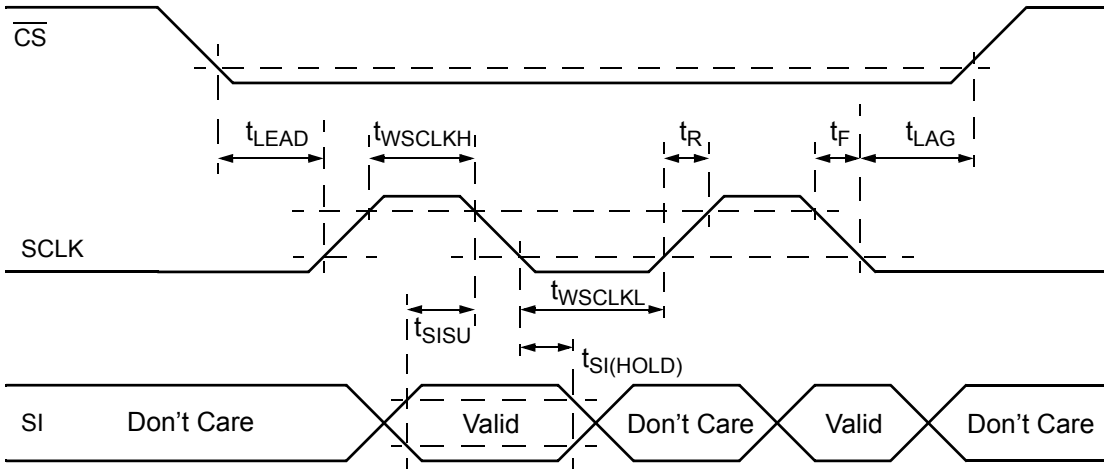

Figure 4. Input Timing Switch Characteristics

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FUNCTIONAL DESCRIPTION

INTRODUCTION

The System Basis Chip (SBC) is an integrated circuit dedicated to car body applications. It includes three main blocks:

1. A dual voltage regulator
2. Reset, watchdog, wake-up inputs, cyclic wake-up
3. CAN low speed fault tolerant physical interface

Supplies

Two low drop regulators and one switch to V_{BAT} are provided to supply the **ECU** microcontroller or peripherals, with independent control and monitoring through SPI.

FUNCTIONAL PIN DESCRIPTION

TRANSMIT AND RECEIVE DATA (TX AND RX)

The RX and TX pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TX is an input and controls the CANH and CANL line state (dominant when TX is LOW, recessive when TX is HIGH). RX is an output and reports the bus state.

VOLTAGE REGULATOR ONE AND TWO (V1 AND V2)

The V1 pin is a 3% low drop voltage regulator dedicated to the microcontroller supply (nominal 5V supply).

The V2 pin is a low drop voltage regulator dedicated to the peripherals supply (nominal 5V supply).

RESET ($\overline{\text{RST}}$)

The $\overline{\text{RST}}$ (reset) pin is an input/output pin. The typical reset duration from SBC to microcontroller is 1ms. If longer times are required, an external capacitor can be used. SBC provides two $\overline{\text{RST}}$ output pull-up currents. A typical 30µA pull up when Vreset is below 2.5V and a 300uA pull up when reset voltage is higher than 2.5V. $\overline{\text{RST}}$ is also an input for the SBC. It means the MC33389 is forced to Normal Request mode after $\overline{\text{RST}}$ is released by the microcontroller

INTERRUPT ($\overline{\text{INT}}$)

The Interrupt pin $\overline{\text{INT}}$ is an output that is set LOW when an interrupt occurs. $\overline{\text{INT}}$ is enabled using the Interrupt Register (INTR). When an interrupt occurs, $\overline{\text{INT}}$ stays LOW until the interrupt source is cleared.

$\overline{\text{INT}}$ output also reports a wake-up event.

GROUND (GND)

This pin is the ground of the integrated circuit.

MASTER IN/ SLAVE OUT (MISO)

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

MASTER OUT/ SLAVE IN (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

SYSTEM CLOCK (SCLK)

This pin clocks the internal shift registers for SPI communication.

CHIP SELECT ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ is the Chip Select pin of the serial peripheral interface (SPI). When this pin is LOW, the SPI port of the device is selected.

LEVEL 0-2 INPUTS (L0: L2)

The L0: L2 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by the SPI. These inputs can be used as wake-up events for the SBC.

NO CONNECT (NC)

No pin connection.

TERMINATION RESISTANCE (HIGH AND LOW?) (RTH AND RTL)

External CAN bus high and low termination resistance pins are connected to these pins.

CAN HIGH AND CAN LOW OUTPUTS (CANH AND CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TX input level, and the state of CANH and CANL is reported through RX output.

VOLTAGE BATTERY (VBAT)

This pin is the voltage supply from the battery.

VOLTAGE REGULATOR THREE (V3)

This pin is a 10 Ω switch to VBAT, which is used to supply external contacts or relays.

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FUNCTIONAL DEVICE OPERATION

Voltage Regulator V1

V1 is a 5.0 V, three percent low drop voltage regulator dedicated to the microcontroller supply. It can deliver up to 100 mA. It is totally protected against short-to-ground (current limitation) and over temperature. V1 is active in Normal Request, Normal, and Stand-by modes.

No forward parasitic diode exists from V1 to V_{BAT}. This means if V_{BAT} voltage drops below V1, high current flowing from V1 to V_{BAT} will not discharge the capacitor connected to V1. Its stored energy will only be used to supply the microcontroller and gives time to save all relevant data.

- Under Voltage Reset—V1 is monitored for under voltage (power-up, power down) and a reset is provided at $\overline{RST}$ output for 1 ms. This ensures proper initialization of the microcontroller at power-on or after supply is lost. Furthermore, a flag is set in the Reset Source Register (RSR) and can be read via the SPI.
- Over Temperature Protection—V1 internal ballast transistor is monitored for over temperature. Two detection thresholds are provided. A pre-warning threshold at 145°C and a shut-off threshold at 175°C. Once the first threshold is reached, a flag is set in the Over Temperature Status Register (OTSR). A maskable interrupt can be sent to the microcontroller. Once the second threshold is reached, a flag is set in the OTSR, a maskable interrupt is sent to the microcontroller and V1 is switched OFF.

Once the junction temperature is back to the pre-warning threshold, V1 regulator will be automatically switched ON.

Table 6. V1 Control

Conditions for V1 ON	Conditions for V1 OFF
Normal Request Mode (at V1 Power ON)	Sleep Mode (via SPI)
Normal Mode (via SPI)	Shut-Off Temperature Threshold Reached
Stand-by Mode (via SPI)	No V_{BAT} Power Supply (cold start)
V1 Below Pre-Warning Temperature Threshold	Emergency Mode
During Rest	—

Note: Current capability of V1, V2 and V3 depends upon the thermal management. Over temperature shutdown might be reached and lead to turn OFF of V1, V2, and V3 for output current below their maximum current capability.

Voltage Regulator V2

V2 is a 5.0 V low drop voltage regulator dedicated to peripherals supply. It can deliver up to 200 mA and is protected against short to ground (current limitation) and over temperature. V2 is active in Normal mode.

- Under Voltage Detection—V2 is monitored for under voltage and a flag is set in the Voltage Supply Status Register (VSSR).
- Over Temperature Protection—V2 internal ballast transistor is monitored for overtemperature. Two detection thresholds are provided. A pre-warning threshold at 140°C and a shut-off threshold at 165°C. Once the first threshold is reached, a flag is set in the readable OTSR register. A maskable interrupt can be sent to microcontroller.

Once the second threshold is reached, a flag is set in the OTSR register, V2 is switched OFF. It can only be switched on again via the SPI.

Table 7. V2 Control

Conditions for V2 ON	Conditions for V2 OFF
Normal Mode (via SPI) and V2 Below Shut-Off Temperature Threshold	Sleep, Stand-by, Normal Request, or Emergency Modes (via SPI)
—	Shut-Off Temperature Threshold Reached
—	V1 Disabled (for any reason)

Switch V3

V3 is a 10 Ω switch to V_{BAT}. It can be used to supply external contacts or relays. A great flexibility is given for the different possible ways for its control. It is protected against short to ground (current limitation).

- Over Temperature Protection—V3 output transistor is monitored for over temperature. Once the threshold is reached, a flag is set in the VSSR register, V3 is switched OFF. It will be automatically switched ON once the junction temperature is back to the pre-warning threshold.

Table 8. V3 Control

Conditions For V3 ON	Conditions For V3 OFF
Permanently in Normal Mode if Configured via SPI	Permanently in Normal Mode if Configured
Permanently in Stand-by Mode if Configured via SPI	Normal Request Mode
In Sleep Mode, During Enable Time of Cyclic Sense if Configured	Permanently in Stand-by Mode if Configured
—	Permanently in Sleep Mode if Configured

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Table 8. V3 Control

—	In Sleep Mode, During Disable Time of Cyclic Sense if Configured
—	Over Temp Threshold Reached
—	V1 Disabled (for any reason)
—	V2 Over Temperature Shutdown

Supply and V_{BAT} Block

- **V_{BAT}** Monitoring—V_{BAT} is the main power supply coming from the battery voltage after an external protection diode (for reverse battery). V_{BAT} is monitored for under voltage and over voltage.
- **V_{BAT}** Under Voltage—V_{BAT} is monitored for under voltage if it is below 4.0 V the BatFail flag is set in the VSSR register and a maskable interrupt is sent to the microcontroller.
- **V_{BAT}** Over Voltage— When V_{BAT} is > 20 V, the BatHigh flag is set in the VSSR register. A maskable interrupt is sent to the microcontroller. No specific action is taken to reduce current consumption (to limit power dissipation). This is to allow the entire flexibility to the microcontroller for a decision.

CAN Transceiver

The device incorporates a low speed 125 kBaud CAN physical interface. Its electrical parameters for the CANL, CANH, RTL,RTH, RX, and TX pins are identical to the 33388, stand alone CAN physical interface.

The mode control for the CAN transceiver (Normal, V_{BAT} Stand-by, Sleep, etc.) are selectable through the 33389 SPI interface.

- Baud Rate up to 125 kBit/s
- Supports unshielded bus wires
- Short-circuit proof to battery and ground in 12 V powered systems
- Supports single-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single wire mode in case of bus failures
- Automatic reset to differential mode if bus failure is removed
- Low Electromagnetic Interference (EMI) due to built-in slope control and signal symmetry
- Fully integrated receiver filters
- Thermally protected
- Bus lines protected against automotive transients
- Low current Bus Stand-by mode with wake-up capability via the bus
- An unpowered node does not disturb the bus lines

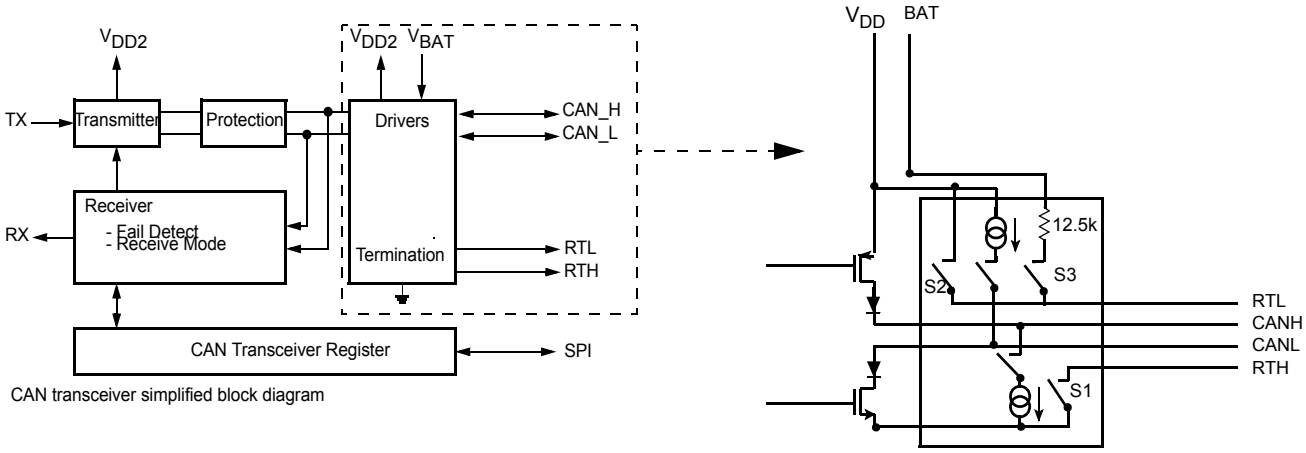

Figure 5. CAN Simplified Block Diagram

CONSEQUENCE OF FAILURE DETECTIONS

S1 is the switch from RTH to Ground

S2 is the switch from RTL to V2 and

S3 is the switch from RTL to V_{BAT}

Each failure type provides data concerning which switch is open and which driver is disabled.

Failure 1: Nothing done

Failure 2: Nothing done

Failure3: S1 open. Driver CANH is disabled

Failure4: S2 and S3 open. Driver CANL is disabled

Failure5: Nothing done

Failure6: S2 and S3 open. Driver CANL disabled

Failure7: S2 and S3 open. Driver CANL disabled

Failure8: S1 Open. CANH driver disable

CAN Transceiver Description

The CAN transceiver is an interface between CAN protocol controller and the physical bus. It is intended for low

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speed applications up to 125 kBit/s in passenger cars. It provides differential transmission capability, but will switch in error condition to single wire transmitter and/or receiver.

The rise and fall slopes are limited to reduce radio frequency interference (RFI). This provides use of an unshielded twisted pair or a parallel pair of wires for the bus. It supports transmission capability on either bus wire if one of the bus wire is corrupted. The logic failure detection automatically selects a suitable transmission mode.

In a normal operation (no wiring failures), the differential bus state is the output to RX. The differential receiver inputs are connected to CANH and CANL through integrated filters. The filtered inputs signals are also used for the single wire receivers. The CANH and CANL receivers have threshold voltages, assuring maximum noise margin in single wire modes. In the RX Only mode, the transmitter is disabled; however, the receive part of the transceiver remains active. In this mode, RX reports bus and TX activity ($\overline{RX}$ = $\overline{TX}$ or Bus dominant). Failure detection and management is the same as the Bus Normal mode.

Failure Detector

The failure detector is active in RXTX and RX Only operation modes. The detector recognizes the following single bus failures and switches to an appropriate mode.

1. CANH wire interrupted
2. CANL wire interrupted or shorted to 5.0 V
3. CANH short-circuit to battery
4. CANL short-circuit to ground
5. CANH short-circuit to ground
6. CANL short-circuit to battery
7. CANL mutually shorted to CANH
8. CANH to V2 (5.0 V)

Note: Shorts-circuit failures are detected for 0 to 50 Ω shorts.

The differential receiver (CANH-CANL) threshold is set at -2.8 V, this assures a proper reception in the normal operating modes. In case of failures 1, 2, and 5 the on-going message is not destroyed due to noise margin.

Failures 3 and 6 are detected by comparators respectively connected to CANH and CANL. If the comparator threshold is exceeded for a certain time (T_{AC3D}, T_{AC6D}), the reception is switched to single wire mode. This time is required to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain **(T_{AC3R}, T_{AC6R})** time-out (filtering).

Failures 4 and 7 initially result in a permanent dominant level at RX. After a time-out, the CANL driver and the RTL pins are switched OFF. Only a weak pull-up at CANL remains. Reception continues by switching to Single Wire mode through CANH. When Failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold for a certain **(T_{AC478R})** time, reception and transmission switch back to the Differential mode.

If any of the eight wiring failure occurs, a flag is set in the TESRH and TESRL Status registers. Eight different types of errors are distinguished out of these eight errors. They are separately stored in these register. Please refer to the Tables 35 and 36. A maskable interrupt is sent to the microcontroller. On error recovery, the corresponding flag is reset after read-out operation.

During all single wire transmissions, the EMC performance (both immunity and emission) is worse than in the Differential mode. Integrated receiver filters suppress any high frequency noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and high frequency suppression. In the Single Wire mode, low frequency noise can not be distinguished from the expected signal.

In the event of a permanent dominant TX state (for more than 2.0 ms) the output drivers are disabled. That assures the operation of the complete system in case of a permanent dominant TX state of one control unit. The CAN interface of a defective ECU, which has TX permanently low, will automatically be set to the receive only mode and therefore will not lock the complete CAN bus.

Protection

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage. If the junction temperature exceeds a maximum value, the transmitter output stages are disabled. Because the transmitter is responsible for a part of the power dissipation, this results in a reduced power dissipation resulting in a lower chip temperature. All other parts of the transceiver will remain operating. The CANH and CANL inputs are protected against electrical transients, and may occur in an automotive environment.

Thermal Management

The 33389 is proposed in two different packages:

1. HSOP-20 for high power applications
2. SO28WB with eight pins to the lead frame for medium power applications

HSOP20 Package

For such a package, the heat flow is mainly vertical and each heat source (dissipating element) can be seen as an independent thermal resistance to the Heatsink. The thermal network can be roughly depicted in Figure 6.

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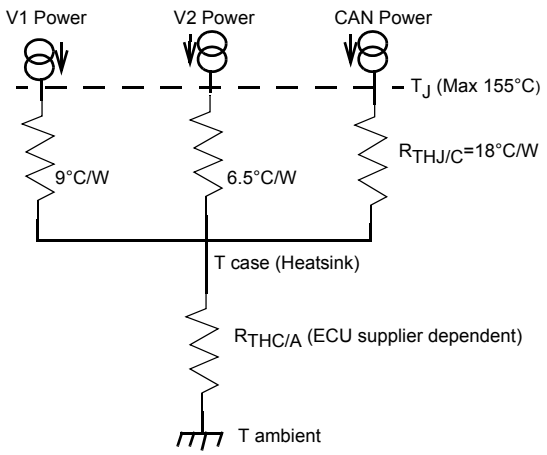

Figure 6. HSOP-20 Simplified Thermal Model

Example

Assuming I_{V1} = 100 mA at V_{BAT} = 16 V,
I_{V2} =150 mA at V_{BAT} = 16 V (Excluding CAN consumption).
I_{CAN} = 50 mA at V_{BAT} =16 V, we have:
P_{V1} = 1. 1 W, P_{V2} = 1.65 W, P_{CAN} = 0.55 W

System assumptions:
If T_{AMB}= 85°C and $R_{THC/A}$ = 18°C/W, this gives:
$T_{CASE} = T_{AMB}+R_{THC/A}$ x 3.3 W = 85 + 18 x 3.3 = 145°C
and $T_JV1 = T_JV2 = T_{JCAN}$=155°C.

This example represents the limit for the maximum power dissipation with a HSOP20.

SO28WB Package

The case (pin) to junction R_{TH} is represented here by only one thermal resistance for the total power because the three power sources strongly interact on the silicon for such a package.

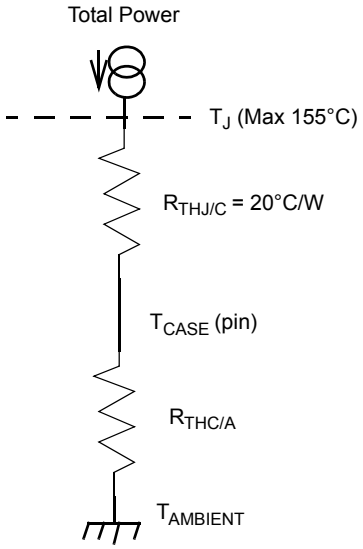

Figure 7. SO28WB Simplified Thermal Model

Example

Assuming I_{V1} = 45 mA at V_{BAT} = 16 V,
I_{V2} = 45 mA at V_{BAT} = 16 V (Excluding CAN consumption).
I_{CAN} = 50 mA at V_{BAT} = 16 V, we have:
P_{V1} = 0.5 W, P_{V2} =0.5 W, P_{CAN} =0.55 W thus P_{TOTAL} =1.55W

System assumptions:
If T_{AMB} = 85°C and $R_{THC/A}$ = 25°C/W, this gives:
$T_{CASE} = T_{AMB} + R_{THC/A}$ x 1.55 W = 85+25 x 1.55 = 124°C
and T_JV1 = 124 + 20 x 1.55 = 155°C.

DIFFERENT DEVICE VERSIONS

The MC33389 is proposed in several package versions, and also offers slight differences in term of functionalities. The device version is identified in the device part number by the first letter after the 389 number. The package identification is done by the last two letters of the part number (DW for SO28 wide body, DH for power SO20).

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OPERATIONAL MODES

CAN Transceiver Modes

The CAN transceiver has its own functioning modes: RXTX mode, Term V_{BAT}/Term V_{CC} mode, and RX Only mode. They are controlled by the Transceiver Control/Status Register (TCR).

- RXTX mode—Full transmitting and receiving capabilities are enabled. Full failure detection is enabled.

Note: Standard/RXTX and Extended/RXTX are equivalent.

- RX Only mode—The transmitter is disabled but the receive portion of the transceiver remains active. In this mode, RX reports bus and TX activity ($\overline{RX}$ = $\overline{TX}$ or Bus dominant).

Note: Standard/RX Only and Extended/RX Only are equivalent.

- Bus Stand-by mode—Is the Low Power mode for the CAN transceiver. The driver and receivers are disabled. Wake-up capability on both bus lines as well as Failure 3, 4, 7, and 8 detection are enabled. RTL termination is set to V_{BAT} in the Bus Stand-by mode.

Low Power Modes

The transceiver provides a Low Power mode, entered and exited by a SPI command. This is the Bus Stand-by mode having the lowest power consumption for the transceiver. CANL is biased to the battery voltage via the RTL output and the pull-up current source on CANL and pull down current source on CANH are disabled. Wake-up requests are recognized by the transceiver when a dominant state is detected on either bus wake-up lines. On a Bus wake-up request, the SBC will activate the $\overline{INT}$ output or, if it is in the Sleep mode, switch to the Normal Request mode. This event is stored in the Wake-Up Input Status Register (WUISR).

To prevent a false wake-up resulting from transients or (RF) fields, wake-up threshold levels have to be maintained for a certain time. While in the Transceiver Low Power mode, failure detection circuit remains partly active preventing increased power consumption in cases of error 3, 4, 7, and 8.

Power-On

After the VBAT supply is switched ON, the SBC is in Normal Request mode. Bus Stand-by is the corresponding mode for the CAN transceiver.

The CAN transceiver is supplied by V2. As long as V2 is below its under voltage threshold, the transceiver is forced to Bus Stand-by mode (fail safe property).

SBC MODES

Global Power Save Concept

The SBC minimizes power consumption of the ECU. Several operating modes are available to go to low power consumption when the full activity is not required. Several possibilities are provided to wake-up the ECU. This permits peripherals or the microcontroller to be switched OFF when no activity on the ECU is required.

Two switchable independent supply voltages (V1 and V2) are provided for optimum ECU power management.

Generalities

The SBC can be operated in four modes:

1. Sleep
2. Stand-by
3. Normal
4. Emergency

After reset, the 33389 is automatically initialized to the temporary mode, Normal Request, while waiting for microcontroller configuration.

Reset Mode

This mode is entered after SBC power-up, or if an incorrect software watchdog trigger occurs. The minimum duration for reset mode is 1.0 ms typical, and unless there is a V1 failure condition, the SBC enters the Normal Request mode after reset.

In the case of a V1 failure condition leading to V1 low (ex: short to ground), the SBC switches to the Reset mode. If V1 is still below the reset threshold after 100 ms, the behavior depends upon the device version A or C:

- C version: The 33389CDW and the 33389CDH will remain in the reset mode.
- D version: The 33389DDW and the 33389DEG will remain in the reset mode. Note that the reset mode threshold for the D version is slightly higher than the C version.

Normal Request Mode

The Normal Request mode is the Default mode after 33389 reset. V1 is active, while V2 and V3 are passive. The SBC is not configured. The default values are set in the registers. The SBC awaits data configuration via the SPI.

If no SPI data is received 75 ms after the Reset is released, the SBC switches itself into the Sleep mode.

The software timing word (in SWCR) provides the data the SBC must receive to consider when the microcontroller begins the configuration sequence. Once received, this software timing word, and the watchdog timer, become active. Any other control data can then be sent from the microcontroller to SBC.

The watchdog is not active in the Normal Request mode before the software timing word is programmed into the SBC. In this mode, neither V2 nor the CAN transmitter are active.

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Table 9. Normal Request: V1 Active and V2/V3 Passive

Entering Normal Request	Leaving Normal Request
SBC Reset Just Released	When First Receiving the SW Timing Word, SBC goes to Normal
—	If Time-out Without Receiving SPI Commands (75ms), SBC goes to Seep

SBC Normal Mode

In this mode, V1 and V2 are active, V3 can be set active or passive via the SPI. Therefore, the whole ECU can be operated. Normal mode is entered by a SWCR configuration in the Normal Request mode.

Table 10. SBC Normal Mode: V1/V2 Active While V3 is Active or Passive

Entering Normal Mode	Leaving Normal Mode
By SPI command	By SPI command, going to any other mode
After SWCR register configuration in Normal Request mode	Watchdog time-out, going to Normal Request after activat-ing Reset
—	V1 undervoltage detection, going to Normal Request mode after activating Reset

SBC Stand-by Mode

In this mode V1 is active and V2 is passive. V3 can be either permanently active or permanently passive. This is a low power mode with V1 active in order to have a fast reaction time in case of any wake-up.

For Stand-by mode, the S Bus Circuit (SBC) monitors the software. It means the microcontroller runs, is monitored, and must serve as a watchdog trigger.

Table 11. Stand-by: V1 Active, V2 Passive, V3 Active or Passive, Watchdog is Active

Entering Stand-by	Leaving Stand-by
—	If SW Timeout Going to Normal Request After Microcontroller Reset
By SPI Command	By SPI Command Going to any Other Mode

Table 11. Stand-by: V1 Active, V2 Passive, V3 Active or Passive, Watchdog is Active

Entering Stand-by	Leaving Stand-by
—	V1 Under Voltage Detection, Going to Normal Request Mode After Activating Reset
—	External Activation of the $\overline{\text{RST}}$ Pin

S Bus Circuit Sleep Mode

This is a low power consumption mode. V1 and V2 are disabled. V3 can be permanently disabled or cyclically active.

Table 12. SBC Sleep Mode: V1/V2 are Passive, V3 is Passive or Cyclic

Entering Sleep Mode	Leaving Sleep Mode
If SW Timing Not Configured 75 ms After Entering Normal Request Mode	CAN Wake-Up, Going to Normal Request
By SPI Command	If a Wake-Up is Detected with Cyclic Sense
For 33389ADW Only: If V1 is Below V1 Reset for More Than 100 ms	If a Wake-Up is Detected with Wake-Up Not Connected to V3 (permanent sense)
—	Forced Wake-Up (See Forced Wake-Up Section)
—	SPI Wake-Up (See Wake-Up by SPI Section)

Emergency Mode

In case the microcontroller detects the ECU or the system is no longer under control, it may decide to switch the SBC to the Emergency mode. V1, V2, and V3 become passive and wake-ups are not detected. The only way to leave this mode is to disconnect the ECU from the battery voltage (BatFail detection).

Table 13. SBC Emergency Mode: V1:V3 are Passive

Entering Emergency Mode	Leaving Emergency Mode
By SPI Command	SBC BatFail Detection (Discon-nection of the Battery Voltage)

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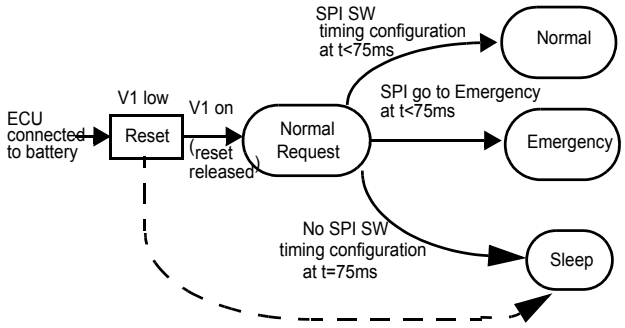

Figure 8. Typical Behavior at Power-On

Note: In the Normal Request mode, if a SPI command is received before the software timing configuration (SWCR register), it will not be taken into account by the SBC (except for the go-to Emergency mode).

Correspondence Between SBC and CAN Transceiver Modes

Table 14 provides different possible CAN transceiver modes versus SBC modes.

Table 14. CAN Modes vs. SBC Modes

When SBC Is In The Following Mode	CAN Transceiver Can Be In
Reset Condition	Bus Stand-by Mode
Normal Request	Bus Stand-by Mode
Normal	RXTX or RXOnly or BusStand-by
Stand-by	Bus Stand-by
Sleep	Bus Stand-by
Emergency	Bus Stand-by
Normal and V2 OFF (over load) In case V2 is turned OFF either by SPI command (Stand-by mode) or by the SBC itself due to V2 over load condition (V2 short to ground or V2 over temperature) the CAN is automatically set into the Bus Stand-by mode and does not return to TXRX mode automatically when V2 is back to 5.0 V. The CAN must be re configured to TXRX or RX Only mode after a V2 turn OFF	Bus Stand-by

Watchdog

The software window watchdog function monitors the microcontroller operation in the Normal and Stand-by modes.

The window watchdog timing is derived from the SBC clock. The desired watchdog timing must be first transmitted during the SBC configuration, in the Normal Request mode, via SPI to SWCR. It can also be changed later on. Selectable watchdog timings are 5.0 ms, 10 ms, 20 ms, 33 ms, 50 ms, 75 ms, 100 ms and 200 ms. These timings correspond to the full disable window plus full enable window.

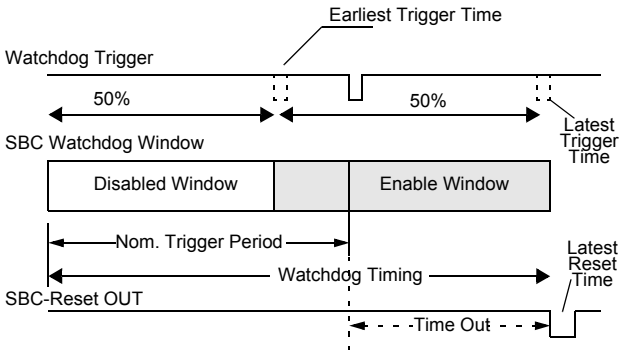

Figure 9. Window Watchdog Timing

As soon as the watchdog trigger is received in the Enable Window, the internal counter is reset and begins a new disable window. The SBC triggers the watchdog word at $\overline{CS}$ low-to-high transition. Any watchdog trigger outside the Enable Window leads to an SBC reset.

- Normal and Stand-by Modes— The SBC get the watchdog word from the microcontroller via SPI in the Normal mode. In case of a trigger time failure (no trigger or trigger outside the Enable Window) the SBC reset is switched to active.
- Normal Request, Sleep, and Emergency Mode— Watchdog is not active in these modes.

WAKE-UP CAPABILITIES

Several wake-up capabilities are available.

Forced Wake-Up

The forced wake-up is enabled and disabled by SPI in the V3 register. It is used to automatically wake-up the system by supplying V1 with proper reset in the Sleep mode. This corresponds to jump into the Normal Request mode. If the SBC is not properly configured within 75 ms, it switches back to the Sleep mode until the next wake-up. If both Cyclic Sense and Forced Wake-Up are enabled by the SPI while in the Sleep mode, only Cyclic Sense is active.

The period of Forced Wake-Up are 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms, and 8192 ms chosen by SPI in the Cyclic Timing Control Register (CYTCR).

Wake-Up Inputs (Local Wake-Up)/Cyclic Sense

SBC provides three wake-up inputs to monitor external events such as closing/opening of switches. The wake-up feature is available in Normal, Stand-by, and Sleep modes.

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The switches can be directly connected to V_{BAT} or to V3. The SBC must be properly configured by setting the bit WI2V3 in the V3 register. In this case, wake-ups are only detected when V3 is ON. It can take advantage of the V3 Cyclic Sense feature. If both Cyclic Sense and Forced Wake-Up are enabled by the SPI in the Sleep mode, only Cyclic Sense will be active.

Options for Wake Input

Different conditions for wake-up can be chosen for wake-up input pins (via SPI in the Wake-Up Input Control Register (WUICR).

- No Wake-Up— Wake-ups are not detected whatever occurs on wake-up inputs.
- High-State—If the input pin voltage is above the detection threshold during more than a 20 µs filter time, a wake-up is detected. A flag is set in the WUISR.
- Low-State—If the input pin voltage is below the detection threshold during more than a 20 µs filter time, a wake-up is detected. A flag is set in the WUISR.
- Change of state—Each change of the wake-up input pin is considered as a wake-up if it lasts more than a 20µs filter time. The first reference state (no wake-up) is the wake-up input state when the SBC is programmed to this option. A flag is set in the WUISR.
- Multiple Sampling Events—When wake-up inputs are used with V3 in Cyclic Sense in the Sleep mode.

For positive edge sensitivity, two samples Low followed by two samples High are necessary to validate the wake-up condition.

For negative edge sensitivity, two samples High followed by two samples Low are necessary to validate the wake-up condition.

For both edge sensitivity, two samples at a given state followed by two samples in the opposite state are necessary to validate the wake-up condition.

Wake-Up Inputs with Cyclic Sense

Connecting the external switches to V3 allows power saving because V3 can be programmed to be active, passive, or cyclic (Cyclic Sense). This provides great flexibility reducing total power consumption while allowing full wake-up capabilities. Cyclic Sense is available only in the Sleep mode.

The period of the Cyclic Sense can be chosen out of eight different timings: 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms, and 8192 ms programmable via SPI in the CYTCR register. Once activated, V3 remains ON during 400 µs. The wake-up inputs states are sampled at 300 µs.

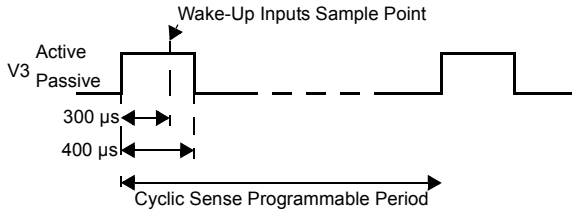

Figure 10. V3 Timing

Note: In Sleep mode, the Cyclic Sense feature 'EXCLUSIVE OR' the forced Wake-Up is chosen (not both).

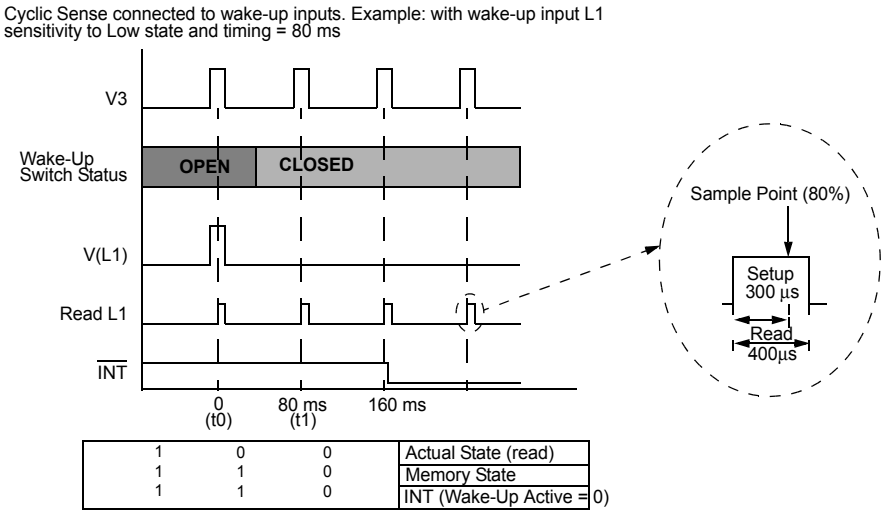

Figure 11. Cyclic Sense Timing

Wake-Up Inputs with Permanent Sense

Wake-up detection can also be accomplished in a permanent way in Normal and Stand-by modes. If the contacts are connected to V3, wake-ups are only detected if V3 is ON.

Wake-ups are also detected in a permanent way in the Sleep mode if the contacts are directly connected to V_{BAT} (if they are connected to V3, only Cyclic Sense is available in Sleep mode).

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Local Wake-Up Consequences

In Normal or Stand-by modes, the real time state of each wake-up input pin is stored in the readable Wake-Up Input Control Register (WUIRTI). Wake-ups are detected according to the selected option. A flag is set in the WUISR. A maskable interrupt is then sent via $\overline{INT}$ output.

In the Sleep mode, a local wake-up leads to a jump to Normal Request mode (via proper reset of the microcontroller). A flag is set in the WUISR.

Table 15. SBC Mode vs. Local Wake-Up Behavior

SBC Modes	Local Wake-Up Behaviour
Normal Request	No Detection
Normal and Stand-by	Detection Active According to the Option. The Event is Stored in WUISR. The SBC may Activate $\overline{INT}$ Output. Real Time State of Each Wake-Up Input Pin Available in WUIRTI Register
Sleep	Detection Active According to the Option. The Event is Stored in WUISR. The SBC Switches to Normal Request Mode
Emergency	No Detection

Wake-Up By SPI

In some applications, the microcontroller might be supplied by an external V_{DD}, remaining powered in SBC Sleep mode. In this case, a feature is provided making possible to wake-up the SBC by SPI activity.

After V1 is totally switched OFF in the Sleep mode (V1< 1.5 V), if a falling edge occurs on $\overline{CS}$ (crossing 2.5 V threshold), a wake-up by SPI is detected, the SBC switches to the Normal Request mode. A flag is set in ISR2.

Interrupt Output

The $\overline{INT}$ output may be activated in the following cases:

- V_{BAT} overvoltage (BatHigh)
- V_{BAT} undervoltage (BatFail)
- High temperature on V1 or V2
- Pre-warning temperature on V1 or V2
- CAN bus failure
- SPI error
- Local wake-up (can be used for low battery detection)
- Bus wake-up

All these interrupts are maskable. Please see the SPI Registers Descriptions on page 34.

Reset Input/Output

The Reset ($\overline{RST}$) pin is an input/output pin. The typical reset duration from SBC to microcontroller is 1 ms. If extended times are required, an external capacitor can be used. SBC provides two $\overline{RST}$ output pull-up currents.

A typical 30 µA pull up when Vreset is below 2.5 V and a 300 µA pull up when reset voltage is higher than 2.5 V.

$\overline{RST}$ is also an input for the SBC. It means the 33389 is forced to the Normal Request mode after $\overline{RST}$ is released by the microcontroller.

GROUND SHIFT DETECTION

When normally working in a two-wire operating mode, the CAN transmission can afford some ground shift between different nodes without trouble. Nevertheless, in case of bus failure, the transceiver switches to single-wire operation, therefore working with less noise margin. The affordable ground shift is decreased in this case.

The SBC is provided with a ground shift detection for diagnosis purpose. Four ground shift levels (GSL) are selectable and the detection is stored in the GSL register, accessible via the SPI.

Detection Principle

The ground shift to detect is selected via the SPI from four different values (-0.7 V, -1.2 V, -1.7 V, -2.2 V). The CANH voltage is sensed at each TX falling edge (end of recessive state). If it is detected to be below the selected ground shift threshold, the bit SHIFT is set at one in the GSL register. No filter is implemented. Required filtering for reliable detection should be achieved by software (e.g. several trials).

Figure 12. SBC Operation Mode

Mode	V1 & V2 Regulators, V3 Switch	Wake-Up Capabilities (if enabled)	Reset Pin ($\overline{RST}$)	Interrupt Pin $\overline{INT}$	Software Watchdog	CAN Cell
Reset State	V1: ON (Unless Failure Condition) V2: OFF V3:OFF	—	Low (Duration 1 ms)	—	—	Term V_{BAT}
Normal Request	V1: ON (75 ms Timeout) V2: OFF V3: OFF	—	High (Active Low -go to Reset State if V1 Under Voltage Occurs)	—	—	Term V_{BAT}

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Mode	V1 & V2 Regulators, V3 Switch	Wake-Up Capabilities (if enabled)	Reset Pin ($\overline{RST}$)	Interrupt Pin $\overline{INT}$	Software Watchdog	CAN Cell
Normal	V1: ON V2: ON V3: ON/OFF	—	High (Active Low -go to Reset State if W/D or V1 Under Voltage Occurs)	If Enabled, Signal Failure Condition or L0, L1, L2 Inputs State Change	Running	Tx/Rx, or Rx Only, or Term V_{BAT}
Stand-by	V1: ON V2: OFF V3: ON/OFF	—	Same as Normal Mode	Same as Normal Mode	Running	Term V_{BAT}
Sleep	V1: OFF V2: OFF V3: OFF/Cyclic	• CAN • SPI • L0,L1,L2 • Cyclic Sense • Forced Wake-Up	Low	Not Active	Not Running	Term V_{BAT} + Wake-Up Capability
Emergency	V1: OFF V2: OFF V3: OFF	None	Low	Not Active	Not Running	Term V_{BAT}

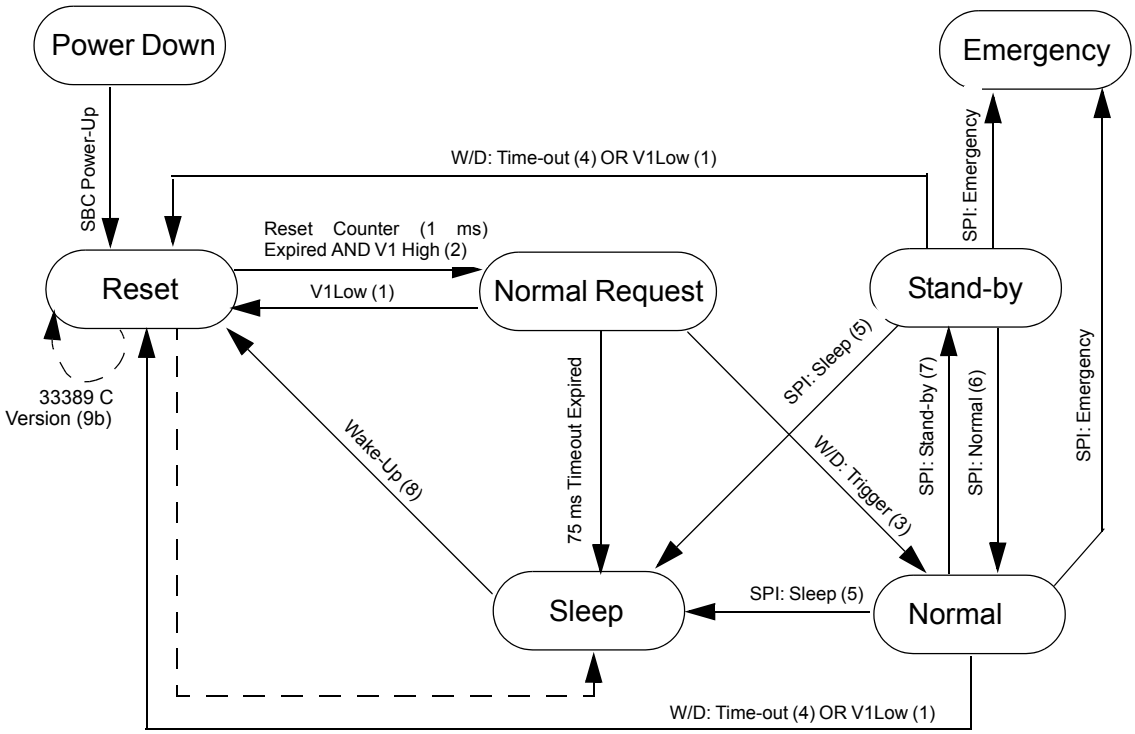

Figure 13. State Machine

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1. V1 Low = V1 below reset threshold
2. V1 High = V1 above reset threshold
3. W/D: Trigger = SCWR register write operation during Normal Request mode
4. W/D: Time-out = SWCR register not written before W/D time-out period expired, or W/D written in incorrect time window. In normal request mode time out is 75ms
5. SPI: Sleep = SPI write command to MCR and MCVR registers, data sleep
6. SPI: Normal = SPI write command to MCR and MCVR registers, data normal
7. SPI: Stand-by = SPI write command to MCR and MCVR registers, data stand-by
8. Wake-Up = one of the following events occur: CAN wake-up, Forced wake-up, Cyclic sense wake-up, Direct LX wake-up, or SPI $\overline{CS}$ wake-up
9. V1Low > 100 ms = V1 below reset threshold for more than 100 ms
   a. This condition leads to SBC in Sleep mode only for the 33389ADW (SO28 package)
   b. V1 Low for > 100 ms does not lead to Sleep mode for the 33389CDW (SO28WB package) and for the 33389CDH (HSOP20 package)

Figure 14. State Machine Legend

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Sleep Mode Activation

Once in the Sleep mode, the SBC turns the V1 and V2 regulator OFF . Thus the microcontroller can not run any mode.

In order to have the microcontroller run again, the SBC should enable and turn ON V1. This is achieved by an SBC wake-up event.

Several options are available to wake-up the SBC and the application and have the microcontroller in Run mode.

Some wake-ups are selectable; some are always active in Sleep mode:

- Wake-up from CAN interface and wake-up from SPI ($\overline{CS}$) are always active.
- Wake-up from L0,L1, and L2 inputs, with and without cyclic sense and the forced wake-up (FWU) are selectable. The selection must be done while the SBC is in Normal or Stand-by mode, and prior to enter Sleep mode.

General Condition to Enter Sleep Mode

All previous wake-up conditions must be cleared, assuring the SBC enters the Sleep mode, and Write operations into the MCR and MCVR. To clear a wake-up condition requires reading the appropriate register.

Once the SBC has powered-up from *zero* (battery power-up or cold start), the following registers must be read:

- WUICR—possible wake-up event report from CAN bus
- RSR—report a V1 under voltage
- VSSR—reports a V_{BAT} fail flag

Once these read operations are completed, the wake-up conditions, or flags are reset.

The VBSR0 bit in the VSSR can be used to determine if the SBC has experienced a loss of battery voltage.

Once the SBC is awakened from *Sleep mode* the following registers indicate the wake-up source. They must be cleared to allow the SBC to enter Sleep mode again:

- WUICR—wake-up event report for CAN or SPI buses
- WUISR— wake-up event report for the L0,L1, and L2 inputs
- RSR—report a V1 under voltage
- VSSR—reports a V_{BAT} fail flag
- etc.

The ensuing paragraphs describe the write operation to be accomplished for the several Sleep modes and Wake-up control options.

In addition to FWU, cyclic sense and direct wake-up, the CAN and SPI wake will always be activated.

Sleep Mode with CAN and SPI Wake-Up

To enter the Sleep mode and activate the only CAN or SPI wake-up, there is no dedicated wake-up condition to be completed. The SBC has CAN and SPI wake-up sources always active in the Sleep mode. To enter the Sleep mode in this case, while the SBC is in Normal or Stand-by mode:

- Write to V3R—data 0000 (this clears the WI2V3 bit, is set to1after reset)
- Write to MCR—data SLEEP (100)
- Write to MCVR—data SLEEP (100)

The SBC then enters the Sleep mode.

Sleep Mode Enter with Forced Wake-Up

To enter the Sleep mode and activate the forced wake-up, write to the following registers:

- Write to V3R (data 0100) this set the FWU bit to 1
- Write the desired wake-up time to CYTCR. (This sets the time the SBC will stay in the Sleep mode).
- Write to MCR–data SLEEP (100)
- Write to MCVR– data SLEEP (100)

The SBC then enters the Sleep mode. It will wake-up after the time period is selected in the CYTCR.

Sleep Mode Enter with Cyclic Sense

To enter the Sleep mode and activate the cyclic sense wake-up the following registers must be written:

- Write to V3R (data 1010) this sets the VI2V3 and CYS bits to 1
- Write to CYTCR the desired cyclic sense period. (This sets the time the SBC will wait in the Sleep mode to turn on V3 and sense the LX inputs)
- Write to WUICR bits 0 and 1 to select the edge sensitivity for the LX inputs
- Write to MCR—data SLEEP (100)
- Write to MCVR—data SLEEP (100)

The SBC then enters the Sleep mode. It will periodically turn on V3 and while V3 is on, sample the level of the Ls inputs.

If any of the 3 LX inputs is in the correct state for two consecutive samples, SBC will wake-up. If not, it will stay in the Sleep mode. Refer to device description for detail.

Sleep Mode Enter With Direct LX Input Wake-Up

To enter the Sleep mode and activate the direct wake-up from the LX inputs, the following registers must be written:

- Write to V3R (data 0000) this clear VI2V3 bit
- Write to WUICR bits 0 and 1 to select the edge sensitivity for the LX inputs
- Write to MCR—data SLEEP (100)
- Write to MCVR—data SLEEP (100)

The SBC then enters the Sleep mode. It will wake-up as soon as any of the LX input read the correct state.

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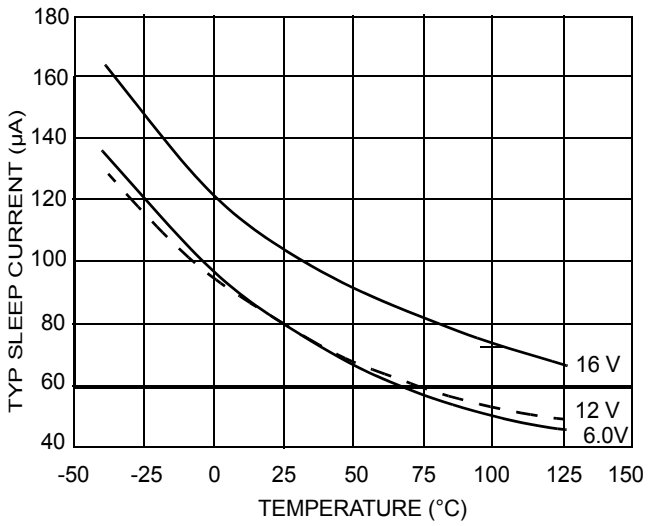

Figure 15. Current vs Temp and Batt Voltage

LOGIC COMMANDS AND REGISTERS

SPI Introduction

This SPI system is flexible enough to communicate directly with numerous standard peripherals and MCUs available from Motorola and other semiconductor manufacturers. SPI reduces the number of pins necessary for input/output on the 33389. The SPI system of communication consists of the MCU transmitting, and in return, receiving one data bit of information per clock cycle. Data bits of information are simultaneously transmitted by one pin, Microcontroller Out Serial In (MOSI), and received by another pin, Microcontroller In Serial Out (MISO), of the MCU. Figure 16 illustrates the basic SPI configuration between an MCU and one 33389. The SPI serial operation is guaranteed to 2.0 MHz.

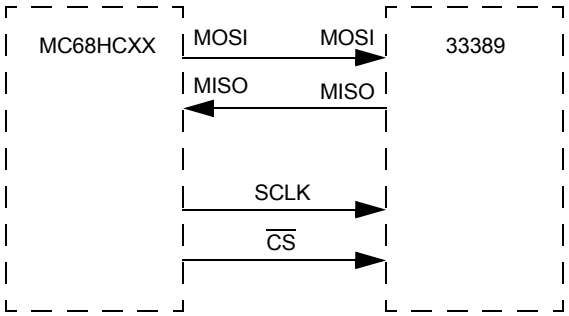

Figure 16. SPI Interface with Microcontroller

$\overline{\text{CS}}$ PIN

The system MCU selects the MC33389 to be communicated with, through the use of the $\overline{\text{CS}}$ pin. Whenever the pin is in logic low state, data can be transferred from the MCU to the MC33389 and vice versa. Clocked-in data from the MCU is transferred from the MC33389 shift register and latched into the addressed registers on the rising edge of the $\overline{\text{CS}}$ signal if the read/write bit is set and the parity check was successful.

The $\overline{\text{CS}}$ pin controls the output driver of the serial output pin. Whenever the $\overline{\text{CS}}$ pin goes to a logic low state, the MISO pin output driver is enabled allowing information to be transferred from the MC33389 to the MCU. To avoid any spurious data, it is essential that the high-to-low transition of the $\overline{\text{CS}}$ signal occur only when SCLK is in a logic low state.

SCLK PIN

The system clock pin (SCLK) clocks the internal shift registers of the MC33389. The serial input pin (MOSI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (MISO) shifts data information out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select bar pin ($\overline{\text{CS}}$) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin be kept in a low logic state as long as the device is not accessed ($\overline{\text{CS}}$ in logic high state). When $\overline{\text{CS}}$ is in a logic high state, any signal at the SCLK and MOSI pin is ignored and MISO is tristated (high impedance).

MOSI PIN

This pin is for the input of serial instruction data. MOSI information is read in on the falling edge of SCLK. To program the MC33389 by setting appropriate programming registers, an sixteen bit serial stream of data is required to be

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entered the MOSI pin starting with Bit15, followed by Bit14, Bit13, etc., to Bit0. For each fall of the SCLK signal, with $\overline{CS}$ held in a logic low state, a data bit is loaded into the shift register per the tidbit MOSI state.The shift register is full after sixteen bits of information have been entered.

MISO PIN

The serial output (MISO) pin is the tri-stateable output from the shift register. The MISO pin remains in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. The MISO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. The MOSI/MISO shifting of data follows a first-in-first-out protocol with both input and output words transferring the MSB first.

Module Address Map, the module address map is shown in table.

Table 16. Module Address Map

Address	Register	Register Name
$000	Mode Control Register	MCR
$003	Mode Control Validation RegisterMCVR	MCVR
$005	V3 control register	V3R
$006	Cyclic timing control register	CYTCR
$009	Software watchdog control register	SWCR
$00A	Ground shift level register	GSLR
$00C	Wake-up input control register	WUICR
$00F	Wake-up input status register	WUISR
$011	Wake up input real time information	WUIRTI
$012	Overtemperature status regist	OTSR
$014	Transceiver error status register for CANH	TESRH
$017	Transceiver error status register for CANL	TESRL
$018	Reset source register	RSR
$01B	Voltage supply status regist	VSSR
$01D	Interrupt mask control register 1	IMR1
$01E	Interrupt mask control register 2	IMR2
$021	Interrupt source register 1	ISR1
$022	Interrupt source register 2	ISR2

Table 16. Module Address Map

Address	Register	Register Name
$024	Transceiver control register	TCR

Control and Status Reporting of the 33389

The MCU is responsible for the control data transfer to the 33389, while the 33389 reports its status to the MCU. Major data for control and status reporting are summarized here:

- SPI initialization during start up
- 33389 control during operation
- Watchdog triggering
- Reading status registers of the 33389

Control Data

The control data are transferred from the MCU to the 33389. A control word includes an address of a control register and the appropriate data (see Figure 17). Basically, the following data will be transferred. Please see SPI Registers Descriptions on page 34.

- 33389 mode control
- Supply control
- Forced wake-up timing
- Cyclic sense control
- Watchdog control
- Transceiver control

Status Data

The status data are transmitted from the 33389 to the MCU. After receiving a valid register address from the MCU, the 33389 returns the appropriate status. Some of the major status data are listed below:

- Current operation mode status
- Wake-up sources
- Reset status
- Error status
- Over temperature status
- Transceiver status

Data Transfer

The data to and from the 33389 are transferred in form of two bytes.The structure of the transferred information is the same as for control and status reporting. The address field A5 to A0 (Bit 15 to Bit 10) contains the address of a control or status register in the 33389. RW (Bit 9 and Bit 8) contains the read/write flag for the data field. The parity field is located at P3 to P0 (Bit 7 to Bit 4). The data field D3 to D0 (Bit 3 to Bit 0) is part of the two-byte data word. Please see Figure 17.

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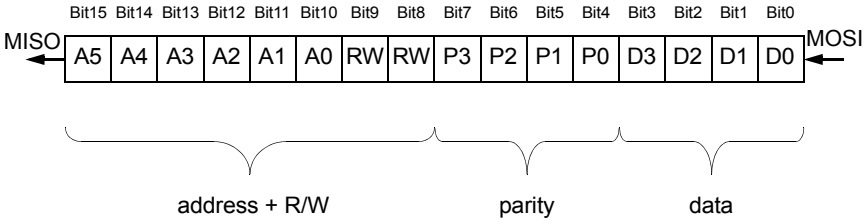

Figure 17. SPI Communication Format

The SBC is accessible via the SPI interface in the Normal Request mode, Normal mode, and Stand-by mode. In all other modes (Sleep mode, Emergency mode), the voltage supply for the microcontroller in permanently switched OFF and the SBC input logic for MISO, MOSI, $\overline{CS}$ and SCLK isn't working (except SPI wake-up function in the Sleep mode).

Writing Data

To write data in a SPI register there are two, one-byte transmissions to be performed. The first byte contains the address of the register (MSB first) and the read/write bits must be set to one. The second byte contains the new data addressed by the previous byte (MSB first) and the parity information. The calculation of the parity field P3-P0 has to follow the equations:

$$P3 = D3 \oplus D0 \qquad \text{(EX - OR)}$$

$$P2 = D3 \oplus D2$$

$$P1 = D2 \oplus D1$$

$$P0 = D1 \oplus D0$$

Note: During the transmission of the two bytes the $\overline{CS}$ pin remains 0. Please see Figure 18

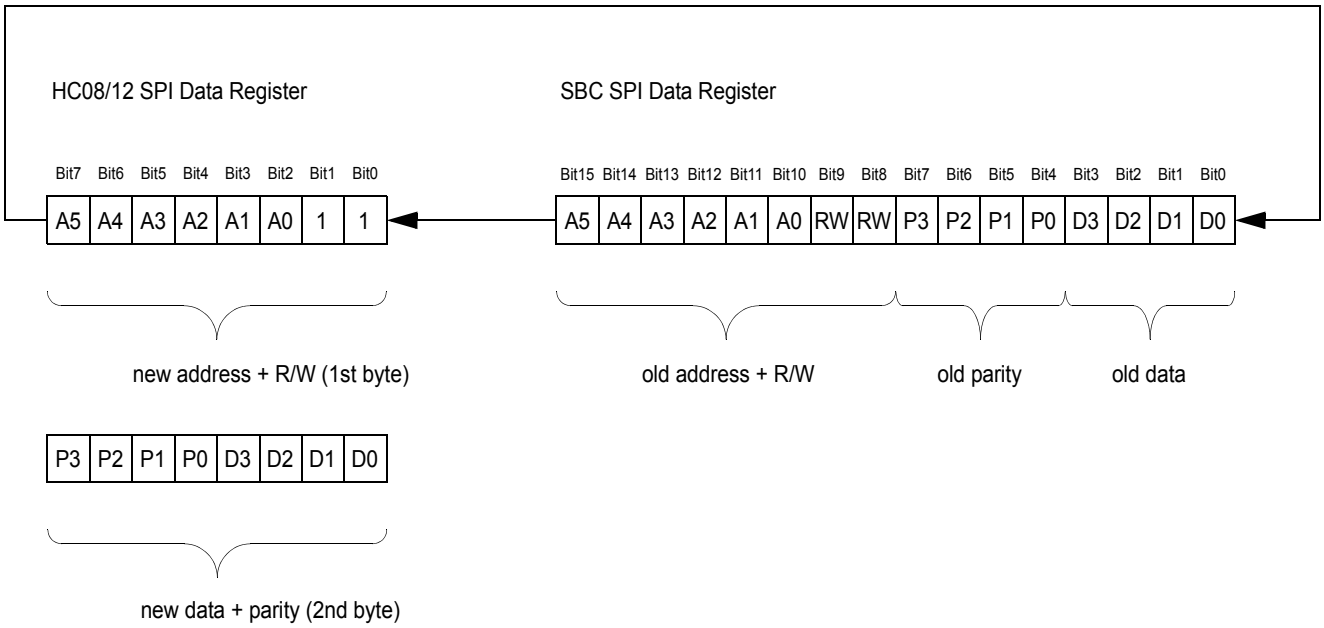

Figure 18. Microcontroller SPI Writing Data

The SBC sends back the old address, R/W, parity, and data information from a previous transmission. This data contains no useful information (e.g. status). It shouldn't be used.

In case of a wrong address field or parity mismatch, an interrupt will be issued and the SBC retains the old state.

Reading Data

To read data from a dedicated register two, one-byte transmissions have to be performed. The first byte contains the address of the register (MSB first) and the read/write flags setting to zero. The second byte needn't contain valid data, nevertheless, the parity calculation has to performed to avoid an interrupt caused by a parity mismatch.

During a read operation the SBC sends back the old address and R/W bits and the new data addressed by the first transmitted byte starting with P3 after the last valid read/write bit has been received.

Note: During the transmission of the two bytes the $\overline{CS}$ pin remains zero.

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Figure 19 illustrates content of the HC08/12 SPI Data Register and the SBC SPI Data Register before the transmission. The new address and R/W bits are already in the SPI Data Register while the new data and parity bits are still in an appropriate microcontroller register or memory. This second byte has to be loaded into the HC08/12 SPI Data Register after the first byte was transmitted to the SBC.

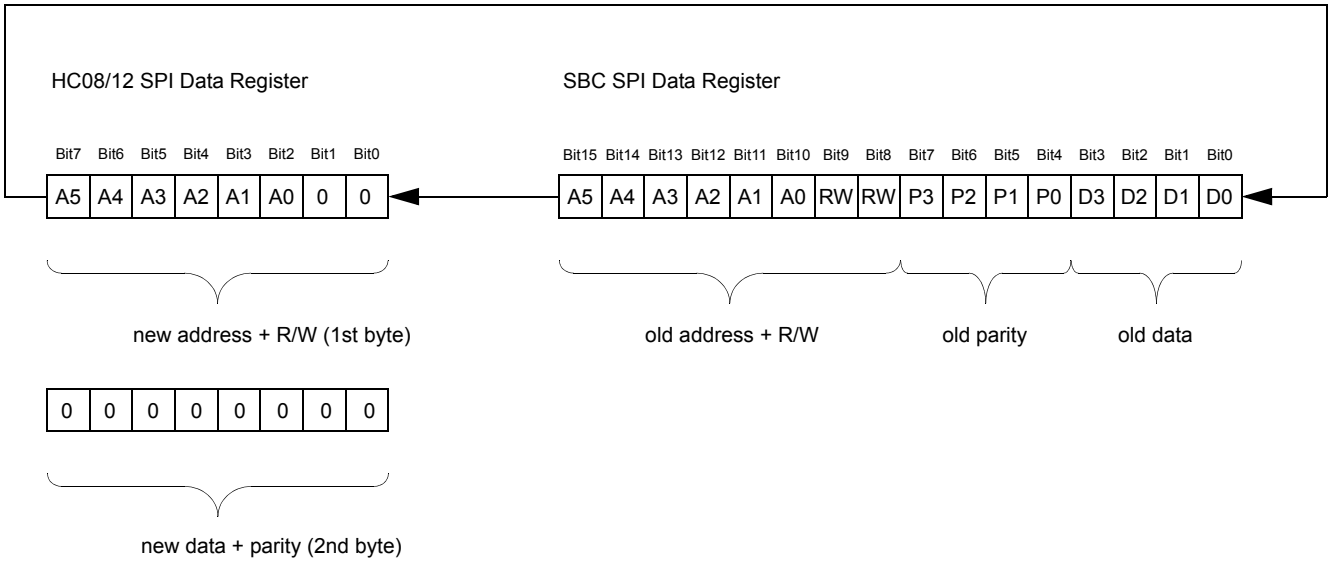

Figure 19. Microcontroller SPI Reading Data - Sequence A

After transmission of the first byte, the HC08/12 SPI read buffer contains the old address and R/W bits received from the SBC. An appropriate operation in the microcontroller loads the new data and parity into the HC08/12 SPI Data Register (second byte). In the SBC the internal logic loads P3-P0 and D3-D0 to the location of Bit 15 to Bit 8 in the SBC SPI Data Register, shifting this data within the remaining eight clock cycles. Please see Figure 20.

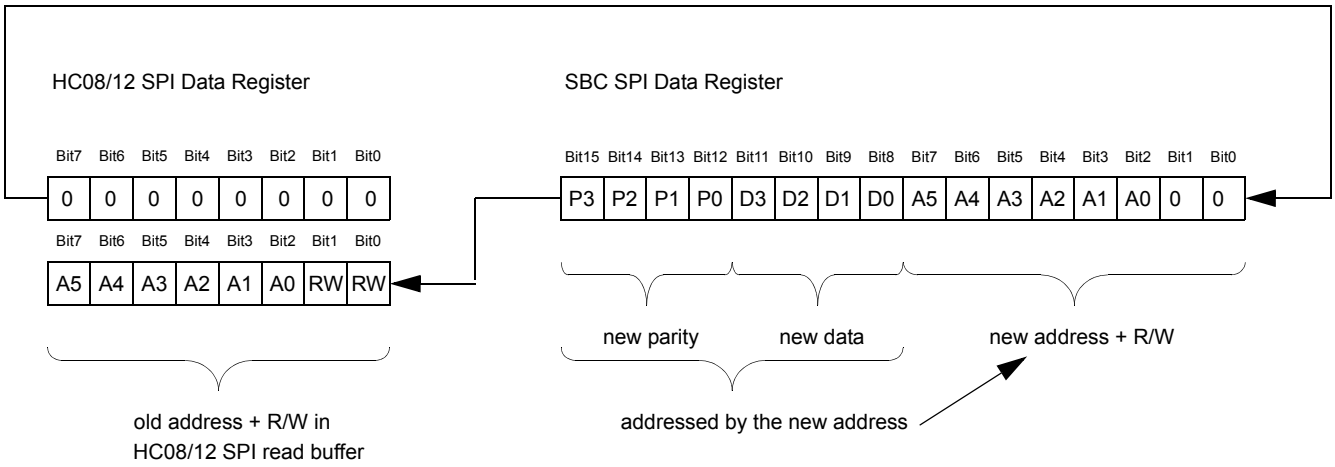

Figure 20. Microcontroller SPI Reading Data - Sequence B

After sixteen clock cycles, the microcontrollers read buffer contains the new parity, and data and is now ready for the next transmission. Please see Figure 21.

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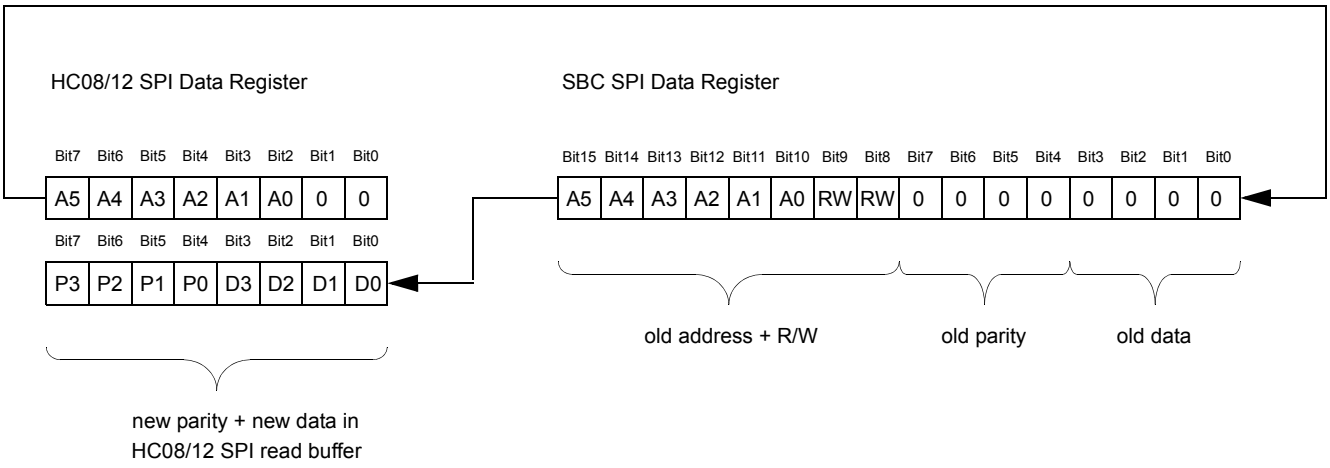

Figure 21. Microcontroller SPI Reading Data - Sequence C

Safety Concept

Because the SPI interface is an on-board interface without any data fault detection capabilities, the SPI interface of the 33389 provides built-in fail save functions.

Address coding is based on increasing the Hamming distance, parity check, and parity generation for data.

For the address and the read/write bits, only codes with a Hamming distance < 2 will be used. So, any single bit failure caused by disturbances will be recognized and handled. When one bit toggles in the address field during the transmission, no misbehavior occurs.

Additionally, validation registers are implemented to confirm safety critical settings in the 33389, e.g. the Mode Control Register MCR has its validation register, MCVR. To change the appropriate settings, both registers must have the same content to switch to another mode.

To increase data integrity, a parity check is used. A parity module in the 33389 ascertains the parity of the data field and compares the result with the received parity. When the parity check is successfully passed, data will be written into the addressed registers. The parity bits P3 to P0 results from the logic following equations:

$$P3 = D3 \oplus D0 \quad \text{(EX - OR)}$$

$$P2 = D3 \oplus D2$$

$$P1 = D2 \oplus D1$$

$$P0 = D1 \oplus D0$$

In case of error detection, the incoming data is not taken in the SBC and an error flag is set in an SPI register.

SPI REGISTERS DESCRIPTIONS

Registers MCR and MCVR control the SBC mode. To change the operating mode of the SBC, both registers must have the same content. The order of writing the registers has to be taken into account. To properly set the SBC mode, MCR must be written first followed by the MCVR write. A write operation sets the MCR and MCVR registers.

The Emergency mode is a regular mode.

A reset of both MCR and MCVR registers occurs when $\overline{RST}$ = low and the SBC is set to Normal Request mode.

Table 17. Mode Control Register (MCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCR $000	R						MSR2	MSR1	MSR0
	W						MCR2	MCR1	MCR0
RESET		—	—	—	—	—	0	0	0

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Table 18. Mode Control Validating Register (MCVR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCVR $003	R						MSVR2	MSVR1	MSVR0
	W						MCR2	MCR1	MCR0
RESET		—	—	—	—	—	0	0	0

Table 19. MCR and MCVR Bit Definition

MC(V)R2	MC(V)R1	MC(V)R0	—	MSR2	MSR1	MSR0
Automatically Entered After Reset			Normal Request	0	0	0
0	0	1	Normal	0	0	1
0	1	0	Stand-by	0	1	0
1	0	0	Sleep	1	0	0
1	1	1	Emergency	1	1	1

This register configures the state of V3 high-side switch in Normal and Stand-by modes, and the V3 operation and the Forced wake-up or the cyclic sense option for the sleep mode operation.

Table 20. V3 Control Register (V3R)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
V3R $005	R					WI2V3	FWU	CYS	V3R0
	W								
RESET		—	—	—	—	1	0	0	0

Table 21. V3R Bit Definition

WI2V3	FWU	CYS	V3R0	—	Comments
x	0	0	0	V3 OFF	Only in Normal and Stand-by Mode Available
x	0	0	1	V3 ON	
x	x	1	x	Cyclic Sense ON	—
x	1	0	x	Forced Wake-Up ON	Only in Sleep Mode Available
1	x	x	x	Wake-Up Inputs Linked to V3	

In low power modes, cyclic sense has priority. A reset of the register occurs when $\overline{RST}$ = low.

Table 22. Cyclic Timing Control Register (CYTCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CYTCR $006	R						CYTCR2	CYTCR1	CYTCR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to select the cyclic sense or force wake-up timing.

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Table 23. CYTCR Bit Definition

CYTCR2	CYTCR1	CYTCR0	Comments	t(ms) Typical
0	0	0	Timer ON, t1 (Default)	32
0	0	1	Timer ON, t2	64
0	1	0	Timer ON, t3	128
0	1	1	Timer ON, t4	256
1	0	0	Timer ON, t5	512
1	0	1	Timer ON, t6	1024
1	1	0	Timer ON, t7	2048
1	1	1	Timer ON, t8	8192

Note: A reset of the register occurs when $\overline{RST}$ = Low.

Table 24. Software Watchdog Control Register (SWCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCR $009	R						SWCR2	SWCR1	SWCR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to select the window watchdog time period. Open window of the selected period is only the second half of the selected period.

Table 25. SWCR Bit Definition

SWCR2	SWCR1	SWCR0	Comments	t(ms) Typical
0	0	0	Timer ON, t1 (Default)	5
0	0	1	Timer ON, t2	10
0	1	0	Timer ON, t3	20
0	1	1	Timer ON, t4	33
1	0	0	Timer ON, t5	50
1	0	1	Timer ON, t6	75
1	1	0	Timer ON, t7	100
1	1	1	Timer ON, t8	200

Note: The software watchdog is only running in Normal and Stand-by modes. A reset of this register occurs when $\overline{RST}$ = Low.

Table 26. Ground Shift Level Register (GSLR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GSLR $00A	R					TXDOM	SHIFT	GSLR1	GSLR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to monitor the ground shift of the vehicle network.

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Table 27. GSLR Bit Definition

GSLR1	GSLR0	Typical Ground Shift Level
0	0	0.7 V
0	1	-1.2 V
1	0	-1.7 V
1	1	-2.2 V

SHIFT

1 = Ground shift above the threshold selected by GSLR1 and GSLR2
0 = No ground shift
The SHIFT information is latched until a read operation of the GSLR register occurs. The GSLR register is set to 0 after power-ON reset. A reset of GSLR1 and GSLR0 occurs when $\overline{RST}$ = Low.

TXDOM

0 = No failure on TX
1 = TX permanent dominant

Table 28. Wake-Up Input Control Register (WUICR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUICR $00C	R					SPIWU	BUSWU	WUCR1	WUICR0
	W								
RESET		—	—	—	—	0	0	0	0

This register configures the wake-up level for the L0, L1, and L2 inputs. It reports the CAN wake-up and SPI ($\overline{CS}$) wake-up events during the Read operation.

Table 29. WUICR Bit Definition

WUICR1	WUICR0	Description
0	0	Wake-Up Inputs Disabled
0	1	Positive Edge Sensitive
1	0	Negative Edge Sensitive
1	1	Positive and Negative Sensitive

Table 30. WUICR Bit Definition

SPIWU	BUSWU	Description
0	0	No Wake-Up Events
0	1	Wake-Up Event on CAN Bus
1	0	Wake-Up Event on SPI Bus

The information is SPIWU and BUSWU is latched. Bits SPIWU and BUSWU will be reset by a read operation of the WUICR register and are set to 0 after a power-ON reset. A reset of WUICR1 and WUICR0 occurs when $\overline{RST}$ = Low.

Table 31. Wake-Up Input Status Register (WUISR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUISR $00F	R						WUISR2	WUISR1	WUISR0
	W								
RESET		—	—	—	—	—	0	0	0

This register reads back the wake input (L0, L1, L2) causing the SBC to wake-up.

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Table 32. WUISR Bit Definition

WUISR2	WUISR1	WUISR0	Description
0	0	0	No Event on Wake-Up Inputs
x	x	1	Event on L0
x	1	x	Event on L1
1	x	x	Event on L2

In case of a wake-up event, the appropriate bit is set to 1. The bits will be reset by a Read operation of the register. After power-ON reset, all bits are set to 0.

Table 33. Wake-Up Input Real Time Information (WUIRTI)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUIRTI $011	R						WUIRTI2	WUIRTI1	WUIRTI0
	W								
RESET		—	—	—	—	—	0	0	0

This register reports the real time information on the state; (High or Low) of the L0, L1, and L2 inputs. The bits WUIRT1 2:0 contain the real time logic value coming from the wake-up inputs (0 means input below threshold, 1 means input above threshold. Typical threshold is 3.5 V).

Table 34. Over Temperature Status Register (OTSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTSR $012	R					OPWV2	OPWV1	OPTV2	OTV1
	W							OTV2C	
RESET		—	—	—	—	0	0	0	0

This register reads back the over temperature status for the V1 and V2 regulators. It is used to turn V2 ON after a V2 over temperature shutdown occurred in the Write mode.

OTV1: 1 = V1 over temperature shutdown, 0 = V1 no over temperature
OTV2: 1 = V2 over temperature shutdown, 0 = V2 no over temperature
OPWM1: 1 = V2 over temperature pre-warning, 0 = V2 normal temperature
OPWV2: 1 = V2 over temperature pre-warning, 0 = V2 normal temperature

In case of V1 or V2 over temperature, the appropriate voltage regulators are switched OFF automatically, and the over temperature flags are set (latched). The flags can be reset by a Read operation of the register OTSR. Once V2 is switched OFF because of over temperature (OTV2 = 1) it can only be switched ON again by forcing OTV2C = 0 by a Write operation.
The V1 and V2 pre-warning flags are set as long as the first over temperature exists. The flags disappear, when the temperature is below the threshold. An over temperature of the V2 power supply will also switch OFF V3. After a power-ON reset, all bits of the register are set to 0.

Table 35. Transceiver Error Status Register for CANH (TESRH)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TESRH $014	R					TESRH3	TESRH2	TESRH1	TESRH0
	W								
RESET		—	—	—	—	0	0	0	0

This register reports the CANH failure status.

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Table 36. TESRH Bit Definition

TESRH3	TESRH2	TESRH1	TESRH0	Description
0	0	0	0	No Failure on CANH
0	x	0	1	CANH Wire Interruption
x	x	1	x	CANH Short Circuit to V_{BAT}
0	1	0	x	CANH Short Circuit to Ground
1	x	0	x	CANH Short Circuit to V_{CC}

In case of CANH line failures, the appropriate bit(s) are set according to **Table 36**. This information is latched. The register can be reset by a Read operation. After power-ON is reset, all bits are set to 0.

Table 37. Transceiver Error Status Register for CANL and Tx (TESRL)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TESRL $017	R					TESRL3	TESRL2	TESRL1	TESRL0
	W								
RESET		—	—	—	—	0	0	0	0

This register reports the CANL and Tx permanent failure status

Table 38. TESRL Bit Definition

TESRL3	TESRL2	TESRL1	TESRL0	Description
0	0	0	0	No Failure
0	x	0	1	CANL Wire Interruption
0	1	0	x	CANL Short Circuit to Ground/CANH mutually shorted to CANL
x	x	1	x	CANL Short Circuit to V_{BAT}
1	x	0	x	CANL Short Circuit to V_{DD}

In case of CANL line failures, the appropriate bit(s) are set according to **Table 38**. This information is latched. The register can be reset by a Read operation. After power-ON is reset, all bits are set to 0.

Table 39. Reset Source Register (RSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR $018	R						RSR2	RSR1	RSR0
	W								
RESET		—	—	—	—	—	1	0	1

This register reports the source of a reset already occurred.

RSR0: 1 = > V_{DD1} under voltage occurred (RSR2 = 1 in this case), 0 = > no over voltage on V occurred
RSR1: 1 = > Software watchdog reset occurred (RSR 2 = 1 in this case), 0 = > no SW watchdog reset occurred
RSR2: 1 = > External reset occurred (RSR0 = RSR1= 0 in this case), 0 = > no external reset occurred
Events related to the bits in register RSR are latched. All bits can be reset by a Read operation of the register. After a power-ON reset, RSR2 and RSR0 are set to 1. Therefore, the first read out of the register after power-ON delivers RSR[2:0] = [101].

Table 40. Voltage Supply Status Register (VSSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VSSR $01B	R					V3SR	V2SR	VBSR1	VBSR0
	W								
RESET		—	—	—	—	0	0	—	—
POR		—	—	—	—	0	0	0	1

This register monitors the status of the V2, V3, and V_{BAT} voltage level.

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Table 41. VBSR1 VBSR0

VBSR1	VBSR0	Description
0	0	No Failure on VBAT
x	1	Under Voltage (BATFail)
1	x	Over Voltage (BATHigh)

V2SR: 1 = V2 ON, 0 = V2 OFF
V3SR: 1 = V3 over temperature, 0 = V3 no over temperature
VBSR1 is real time information. It cannot be reset. Bits V3SR, V2SR, and VBSR0 are latched and can be reset by a Read operation of the register.

The next two registers (IMR1 and IMR2) mask the interrupt function.

Table 42. Interrupt Mask Control Register 1 (IMR1)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR1 $01D	R					HV	HTPW	MTPW	BATU
	W								
RESET		—	—	—	—	0	0	0	0

Table 43. Interrupt Mask Control Register 2 (IMR2)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR2 $01E	R						BUSF	SPIE	WU
	W								
RESET		—	—	—	—	—	0	0	0

To enable the appropriate interrupt, the mask bit has to be set to 1. To disable the interrupt the bit, it must be cleared to 0. After a power-ON reset or $\overline{RST}$ = Low, the bits are cleared to 0. All interrupts are disabled. Explanation for the abbreviations:
HV = V_{BAT} High voltage
HT = High temperature on V1 or V2
MTPW = Medium temperature pre-warning on V1 or V2
BATU = Battery under voltage (BATFail)
BUSF = CAN bus failure
SPIE = SPI error
WU = Wake-up

The next two registers (ISR1 and ISR2) read the interrupt source. All bits in registers ISR1 and ISR2 are copies of the appropriate bits in different SPI registers. For a faster read-out, these bits are merged in ISR1 and ISR2. A reset cannot be completed for registers ISR1 and ISR2.

Table 44. Interrupt Source Register 1 (ISR1)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR $021	R					HV	HTPW	MTPW	BATU
	W								
RESET		—	—	—	—	0	0	0	0

Table 45. Interrupt Source Register 2 (ISR2)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR $022	R						BUSF	SPIE	WU
	W								
RESET		—	—	—	—	—	0	0	0

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Table 46. Transceiver Control/Status Register (TCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR $024	R					TOT	TSR2	TSR1	TSR0
	W						TCR2	TCR1	TCR0
RESET		—	—	—	—	0	0	0	0

This register controls the state of the CAN transceiver (CAN transceiver is also dependent upon the SBC mode). When it is read, this register reports the CAN transceiver state and a CAN over temperature condition.

Table 47. TCR / TSR Data

TCR2	TCR1	TCR0	Description	TSR2	TSR1	TSR0
0	0	0	Standard/Term V_{BAT}	0	0	0
0	1	0	Standard/Rx Only	0	1	0
0	1	1	Standard/RxTx	0	1	1

TOT
1 = > Transceiver over temperature
0 = > Normal temperature
The MODE bit selects between the standard and extended physical layer mode. Any conditions forcing the transceiver to Term VBAT lead to reset of TCR0 and TCRO1 bits. After power-ON reset all bits of the register are set to 0. The information TOT is latched. Reset TOT by reading the TCR. In case of $\overline{RST}$ = Low, the register content remains unchanged.

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TYPICAL APPLICATIONS

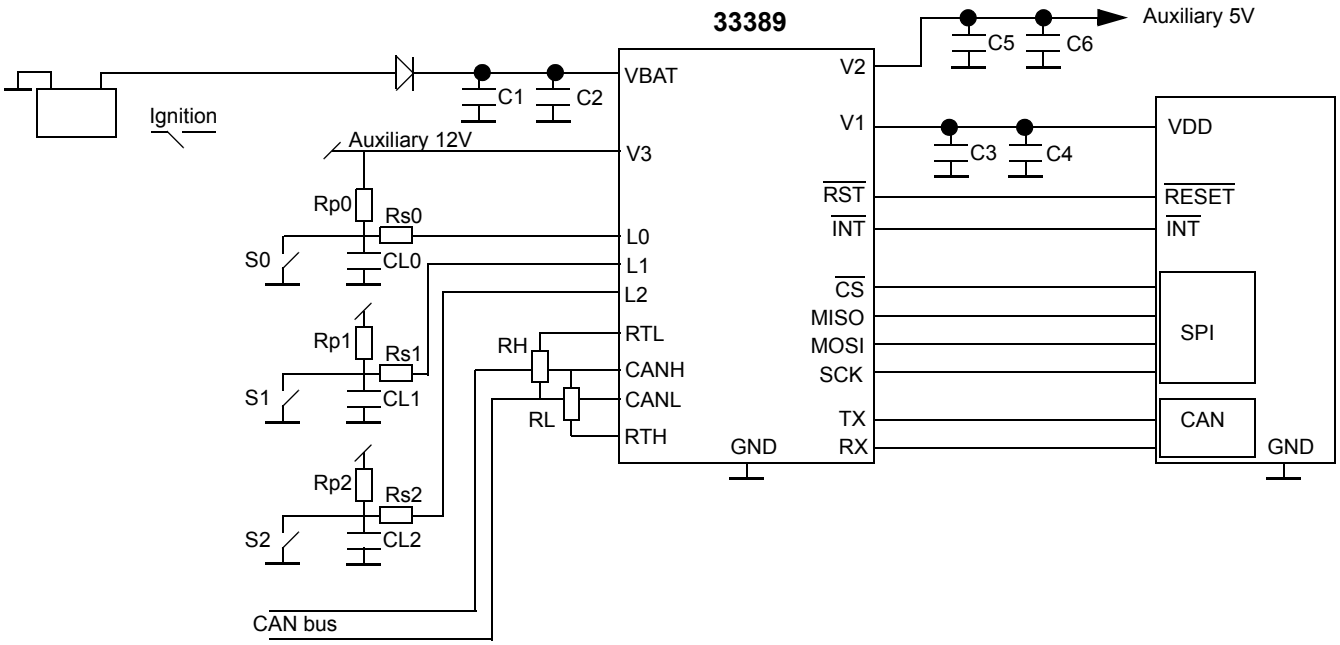

Figure 22. Typical Application Schematic 1

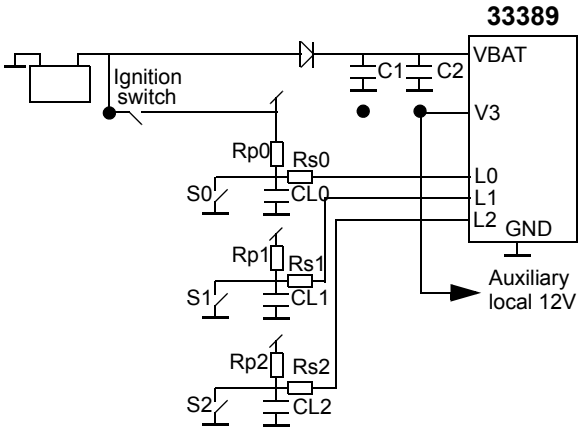

Figure 23. Typical Application: V3 Used as Auxiliary ECU Supply

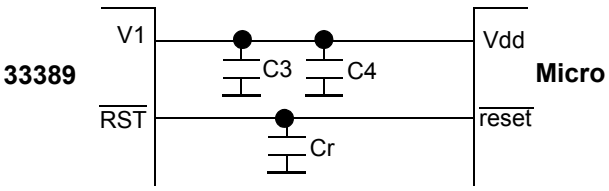

Figure 24. Reset Duration Extension

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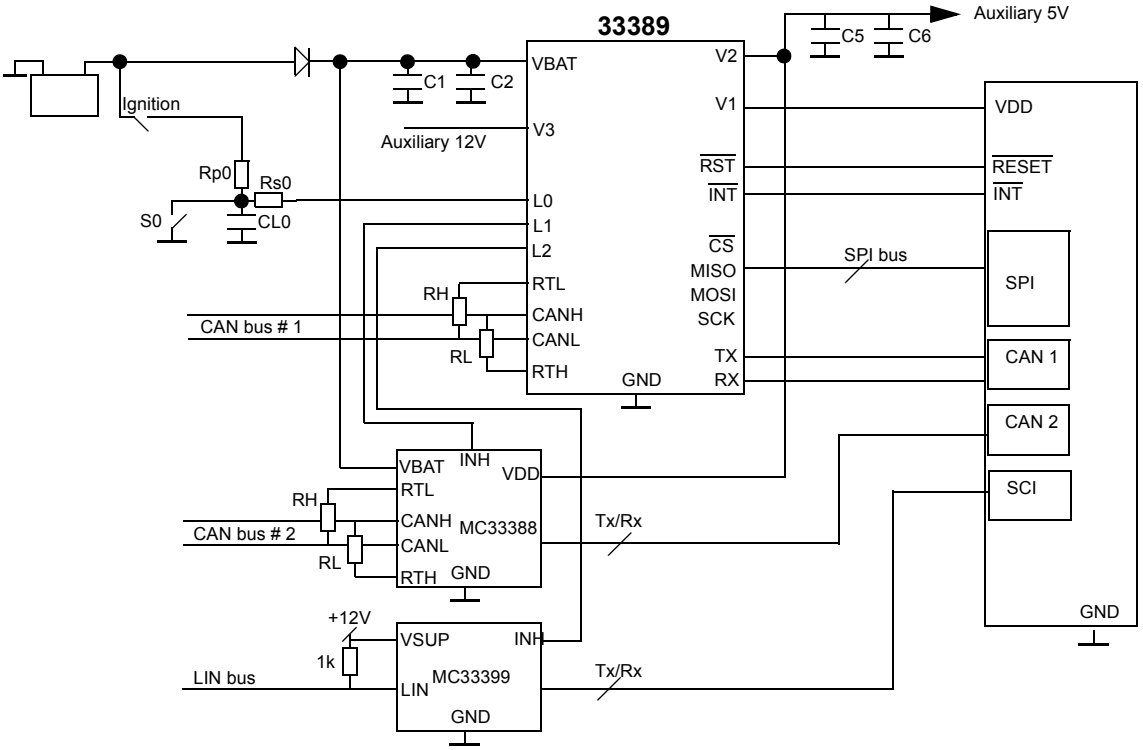

(Wake-up input linked to peripheral circuits: (ex: low speed CAN or LIN transceivers).

Figure 25. Typical Application Schematic 2

The SBC offers several capabilities to help users debug their application.

- External bias of V1 and reset pin
- Turn OFF software watchdog in the Stand-by mode
- Special debug samples with software watchdog disable at power-up (contact local Motorola representative)

DEBUG AND PROGRAM DOWNLOAD INTO FLASH MEMORY

While the SBC is powered, it enters Normal Request mode and expects during the 75 ms time period in the NR mode, an SPI trigger word (to enter Normal mode and select the watchdog time period). If this does not occur, the SBC enters the Sleep mode and turns off V1.

When the software is debugged, and when using development tools, it is not always easy to make sure these events happen properly. It is thus possible to externally power the V1 line with an external 5.0 V supply, and to force the Reset pin to V1 or to and external 5.0 V. These can be done at nominal voltage and temperature. By doing this, 5.0 V is provided to the MCU V_{DD} and reset lines.

Under this condition the SBC is not operational. However, the reset pin is pulled low and is sinking 5 mA to ground. This means, the external circuitry driving reset must have a current capability higher than 5 mA in order to drive the reset in the high-state.

DISABLE OF SOFTWARE WATCHDOG IN STAND-BY MODE

The software watchdog can be disable in Stand-by mode only. In order to disable it the following operation must be done:

- Write to MCR register–data 011 (bit 2, bit 1, bit 0)
- Write to MCVR register–data 011 (bit 2, bit 1, bit 0)

Then the SBC enters the Stand-by mode without software watchdog. However the V2 can not be turn on, and the CAN cell can not be used.

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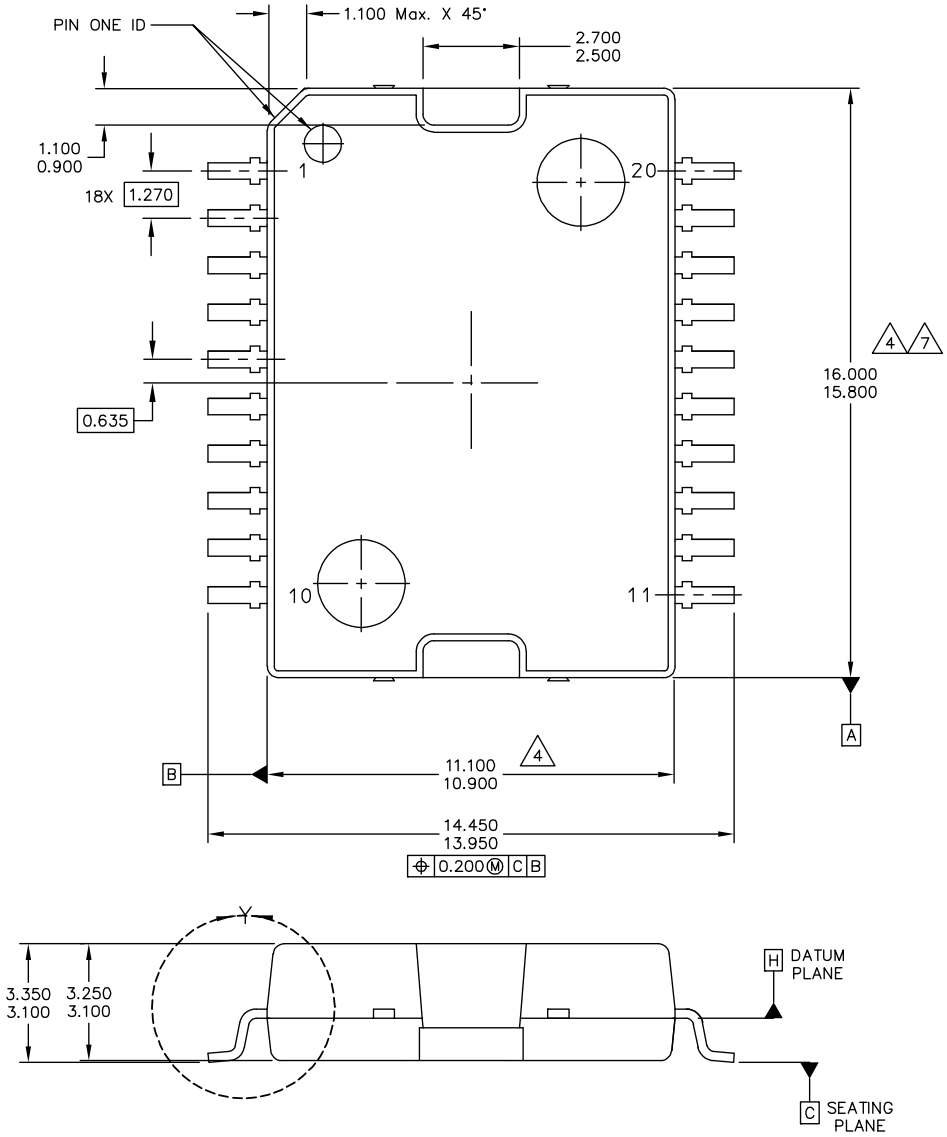
PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98ASH70273A listed below.



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TITLE: 20 LEAD HSOP	DOCUMENT NO: 98ASH70273A	REV: E
	CASE NUMBER: 979–04	19 MAY 2005
	STANDARD: NON–JEDEC	

DH SUFFIX
VW SUFFIX (Pb-FREE)
20 PIN
PLASTIC PACKAGE
98ASH70273A
ISSUE E

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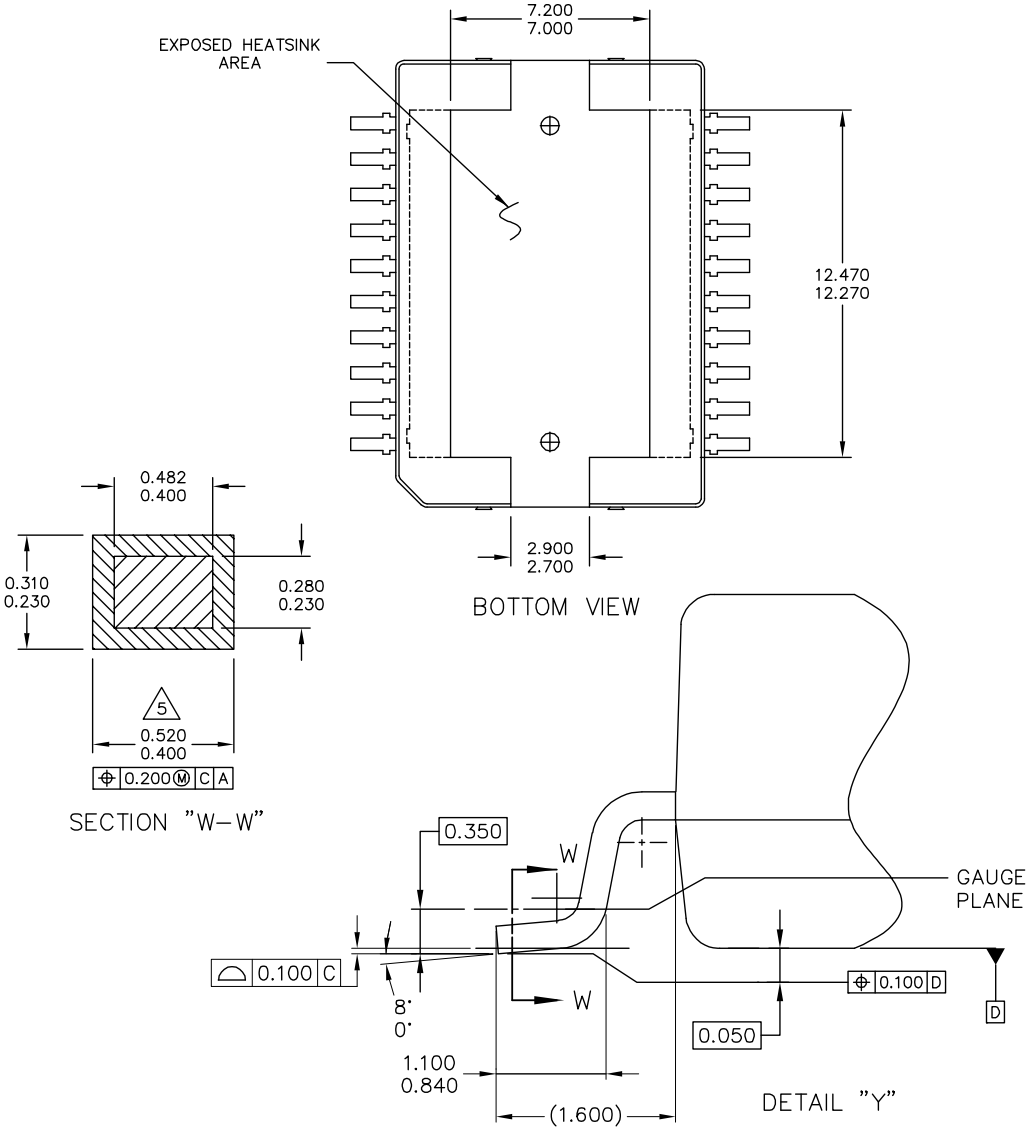

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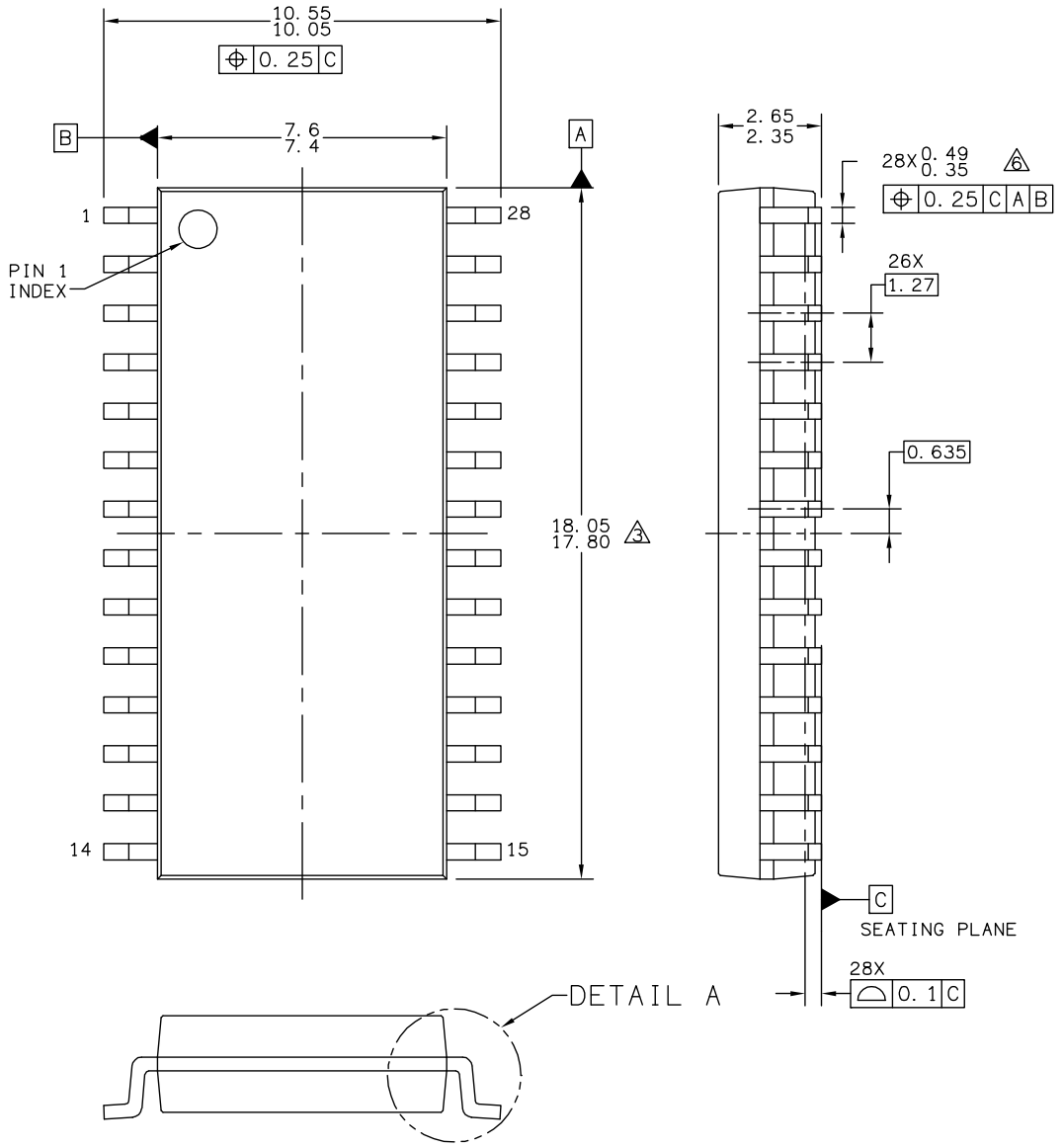

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TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	

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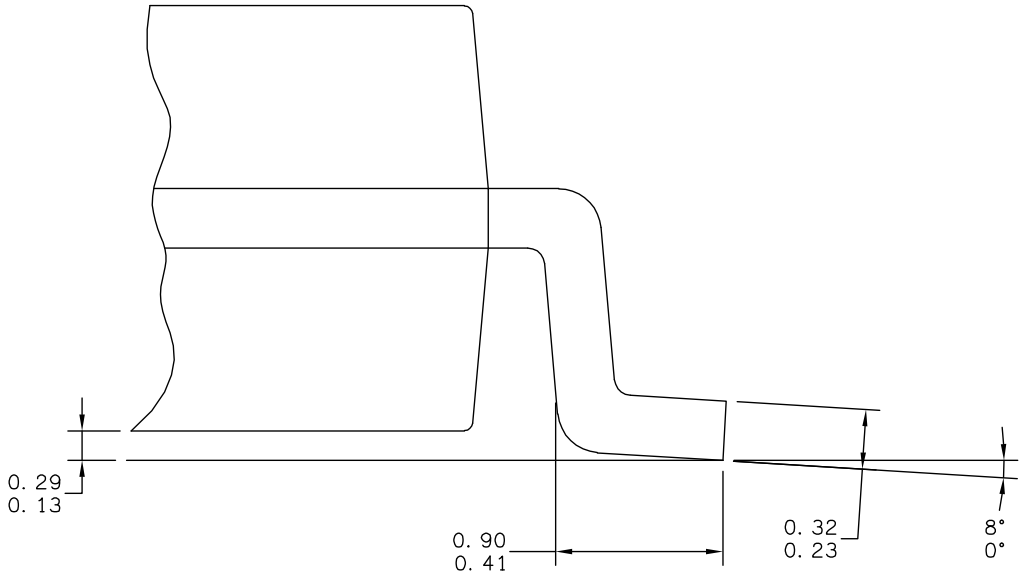

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TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B		REV: G
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DW SUFFIX
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REVISION HISTORY

	DATE	DESCRIPTION OF CHANGES
5.0	3/2007	• Added Revision History • Converted to the prevailing Freescale form and style • Entire document was edited for wording, labels, and technical accuracy. • Added the Pb-FREE package types VW and EG to the ordering information • Updated the package drawings • Added Peak Package Reflow Temperature During Reflow (4), (5) on page 7 • Added notes (4) and (5) • Removed all references to MC33389ADW/R2, MC33389ADH/R2, MC33389CEG/R2, and MC33389DEG/R2 from the data sheet. • Restated MC33389DDW in the Device Variations on page 2

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