



# PCA9545A

4-channel I<sup>2</sup>C-bus switch with interrupt logic and reset

Rev. 10 — 27 September 2022

Product data sheet

## 1 General description

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The PCA9545A is a quad bidirectional translating switch controlled via the I<sup>2</sup>C-bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs, INT<sub>0</sub> to INT<sub>3</sub>, one for each of the downstream pairs, are provided. One interrupt output, INT, acts as an AND of the four interrupt inputs.

An active LOW reset input allows the PCA9545A to recover from a situation where one of the downstream I<sup>2</sup>C-buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I<sup>2</sup>C-bus state machine and causes all the channels to be deselected as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V<sub>DD</sub> pin can be used to limit the maximum high voltage which is passed by the PCA9545A. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

## 2 Features and benefits

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- 1-of-4 bidirectional translating switches
- I<sup>2</sup>C-bus interface logic; compatible with SMBus standards
- Four active LOW interrupt inputs
- Active LOW interrupt output
- Active LOW reset input
- Two address pins allowing up to four devices on the I<sup>2</sup>C-bus
- Channel selection via I<sup>2</sup>C-bus, in any combination
- Power-up with all switch channels deselected
- Low R<sub>on</sub> switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant Inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up protection exceeds 100 mA per JESD78
- Three packages offered: SO20, TSSOP20, and HVQFN20



### 3 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9545ABS	9545A	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 × 5 × 0.85 mm	SOT662-1
PCA9545AD	PCA9545AD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCA9545APW	PA9545A	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

#### 3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9545ABS	PCA9545ABS,118	HVQFN20	Reel 13" Q1/T1 *standard mark SMD	6000	T <sub>amb</sub> = -40 °C to +85 °C
PCA9545AD	PCA9545AD,112	SO20	Standard marking * IC's tube - DSC bulk pack	1520	T <sub>amb</sub> = -40 °C to +85 °C
	PCA9545AD,118	SO20	Reel 13" Q1/T1 *standard mark SMD	2000	T <sub>amb</sub> = -40 °C to +85 °C
PCA9545APW	PCA9545APW,112	TSSOP20	Standard marking * IC's tube - DSC bulk pack	1875	T <sub>amb</sub> = -40 °C to +85 °C
	PCA9545APW,118	TSSOP20	Reel 13" Q1/T1 *standard mark SMD	2500	T <sub>amb</sub> = -40 °C to +85 °C

4 Block diagram

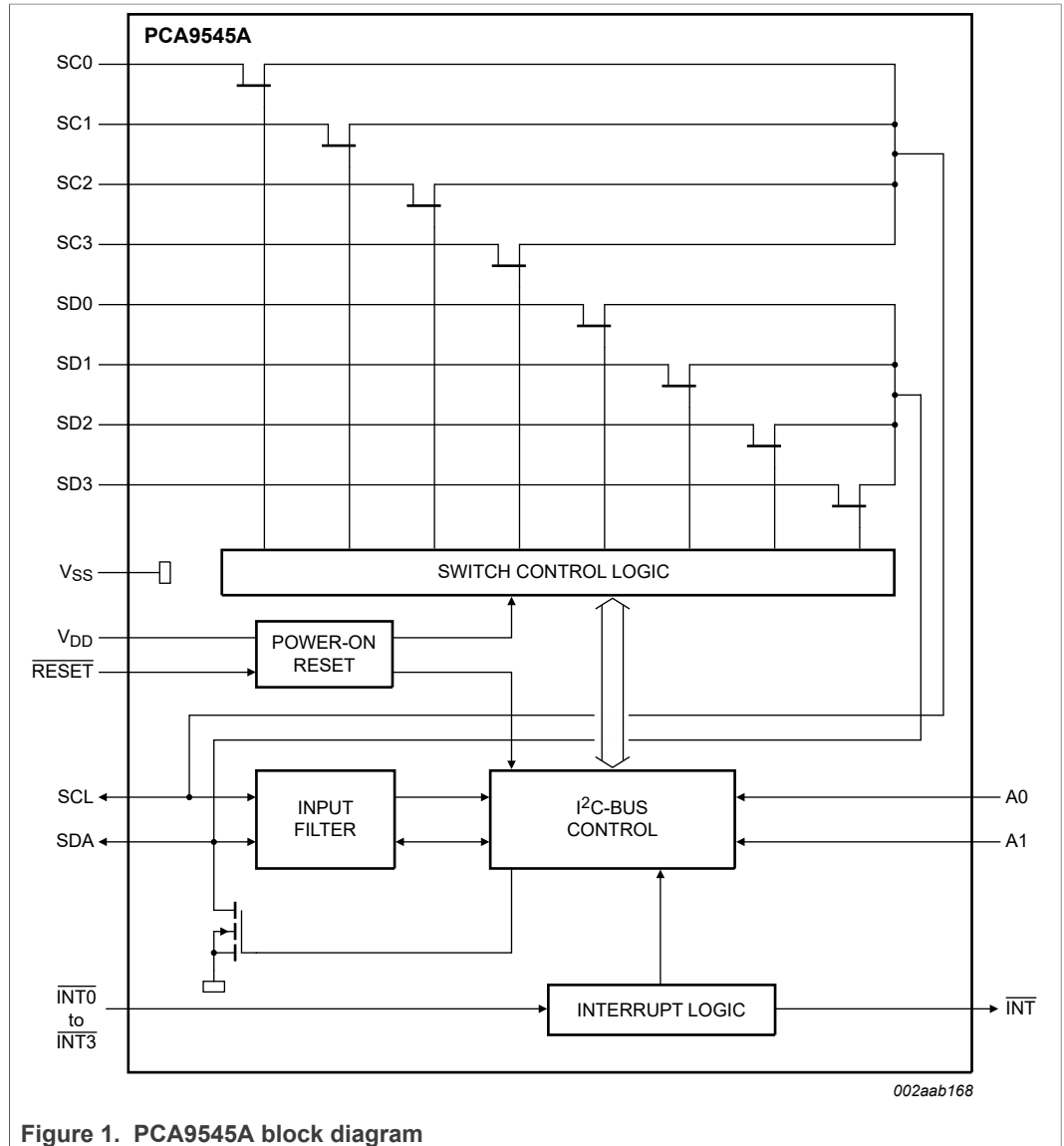


Figure 1. PCA9545A block diagram

5 Pinning information

5.1 Pinning

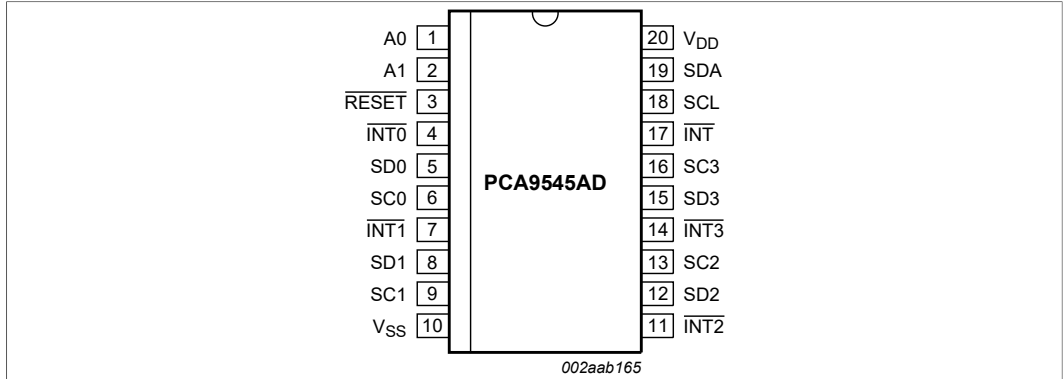


Figure 2. Pin configuration for SO20

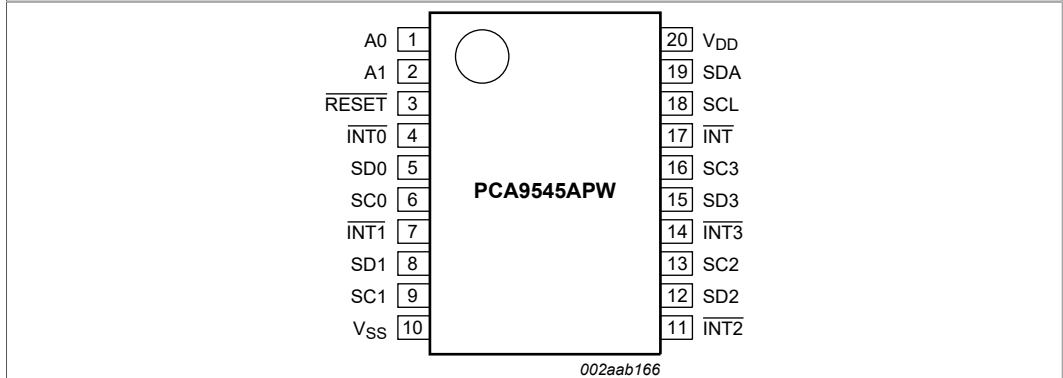


Figure 3. Pin configuration for TSSOP20

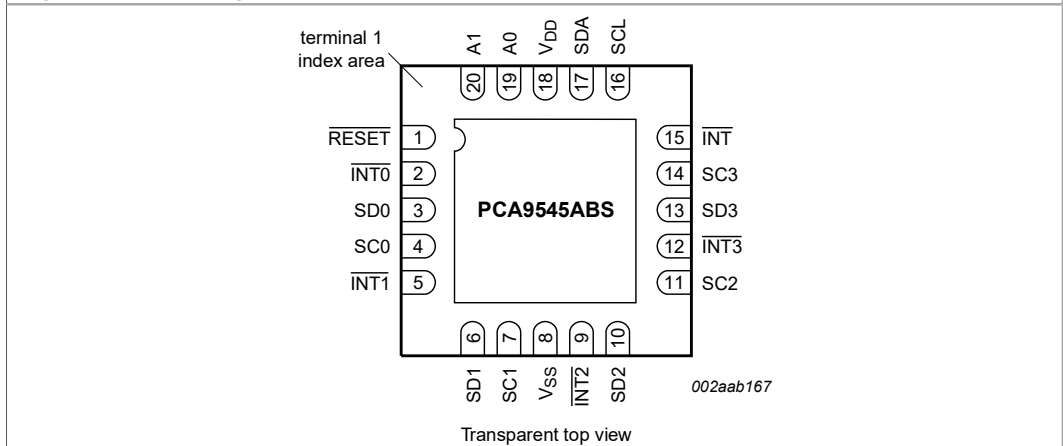


Figure 4. Pin configuration for HVQFN20 (transparent top view)

## 5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO20, TSSOP20	HVQFN20	
A0	1	19	address input 0
A1	2	20	address input 1
RESET	3	1	active LOW reset input
INT0	4	2	active LOW interrupt input 0
SD0	5	3	serial data 0
SC0	6	4	serial clock 0
INT1	7	5	active LOW interrupt input 1
SD1	8	6	serial data 1
SC1	9	7	serial clock 1
V <sub>SS</sub>	10	8 <sup>[1]</sup>	supply ground
INT2	11	9	active LOW interrupt input 2
SD2	12	10	serial data 2
SC2	13	11	serial clock 2
INT3	14	12	active LOW interrupt input 3
SD3	15	13	serial data 3
SC3	16	14	serial clock 3
INT	17	15	active LOW interrupt output
SCL	18	16	serial clock line
SDA	19	17	serial data line
V <sub>DD</sub>	20	18	supply voltage

[1] HVQFN20 package die supply ground is connected to both the V<sub>SS</sub> pin and the exposed center pad. The V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias must be incorporated in the PCB in the thermal pad region.

## 6 Functional description

Refer to [Figure 1](#).

### 6.1 Device address

Following a START condition, the bus controller must output the address of the target it is accessing. The address of the PCA9545A is shown in [Figure 5](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

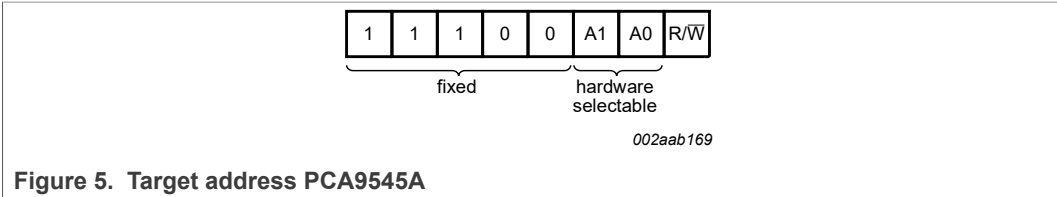


Figure 5. Target address PCA9545A

The last bit of the target address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

### 6.2 Control register

Following the successful acknowledgement of the target address, the bus controller sends a byte to the PCA9545A, which is stored in the control register. If multiple bytes are received by the PCA9545A, it saves the last byte received. This register can be written and read via the I<sup>2</sup>C-bus.

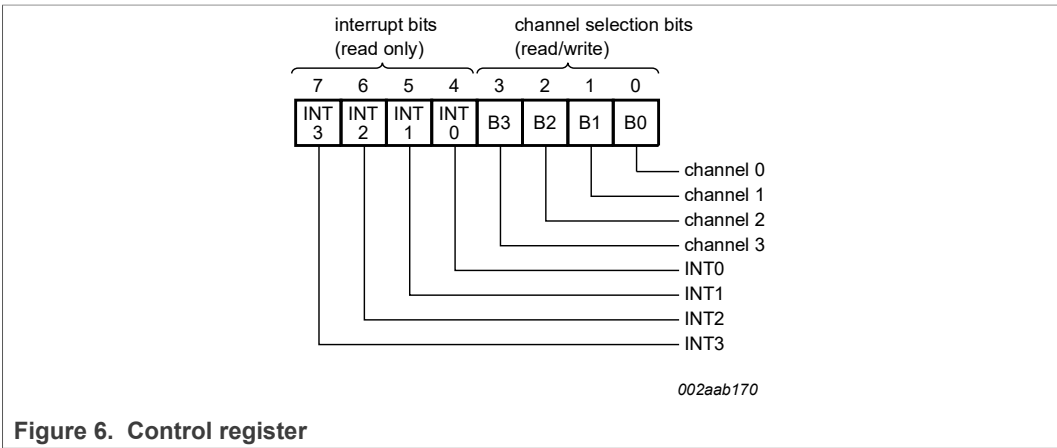


Figure 6. Control register

#### 6.2.1 Control register definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9545A has been addressed. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I<sup>2</sup>C-bus. This ensures that all SCx/SDx lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 4. Control register: write (channel selection); read (channel status)

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
								1
X	X	X	X	X	0	X	X	channel 2 disabled
								1
X	X	X	X	0	X	X	X	channel 3 disabled
								1
0	0	0	0	0	0	0	0	no channel selected; power-up/reset default state

**Remark:** Several channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and channel 3 are disabled and channel 1 and channel 2 are enabled. Care should be taken not to exceed the maximum bus capacity.

### 6.2.2 Interrupt handling

The PCA9545A provides four interrupt inputs, one for each channel, and one open-drain interrupt output. When an interrupt is generated by any device, it is detected by the PCA9545A and the interrupt output is driven LOW. The channel does not need to be active for detection of the interrupt. A bit is also set in the control register.

Bit 4 through bit 7 of the control register corresponds to channel 0 through channel 3 of the PCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The controller can then address the PCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The controller can then reconfigure the PCA9545A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the controller to ensure that all devices on a channel are interrogated for an interrupt.

If the interrupt function is not required, the interrupt inputs may be used as general-purpose inputs.

If unused, interrupt inputs must be connected to V<sub>DD</sub> through a pull-up resistor.

Table 5. Control register: Read — interrupt

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	0	X	X	X	X	no interrupt on channel 0
			1					interrupt on channel 0
X	X	0	X	X	X	X	X	no interrupt on channel 1
		1						interrupt on channel 1

Table 5. Control register: Read — interrupt...continued

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	0	X	X	X	X	X	X	no interrupt on channel 2
	1							interrupt on channel 2
0	X	X	X	X	X	X	X	no interrupt on channel 3
								1

**Remark:** Several interrupts can be active at the same time. Example: INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0, means that there is no interrupt on channel 0 and channel 3, and there is interrupt on channel 1 and channel 2.

### 6.3 RESET input

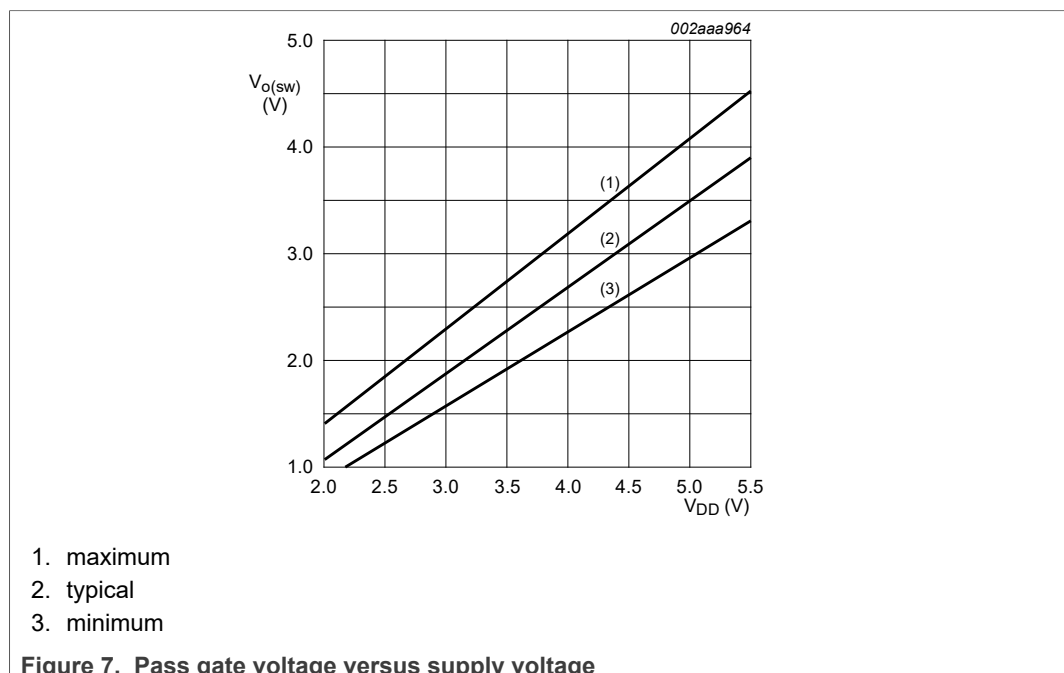
The  $\overline{\text{RESET}}$  input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of  $t_{w(\text{rst})L}$ , the PCA9545A resets its registers and I<sup>2</sup>C-bus state machine and deselects all channels. The  $\overline{\text{RESET}}$  input must be connected to  $V_{DD}$  through a pull-up resistor.

### 6.4 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9545A in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At this point, the reset condition is released and the PCA9545A registers and I<sup>2</sup>C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter,  $V_{DD}$  must be lowered below 0.2 V for at least 5  $\mu\text{s}$  in order to reset the device.

### 6.5 Voltage translation

The pass gate transistors of the PCA9545A are constructed such that the  $V_{DD}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C-bus to another.





[Figure 7](#) shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in [Section 11](#) of this data sheet). In order for the PCA9545A to act as a voltage translator, the  $V_{o(sw)}$  voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then  $V_{o(sw)}$  should be equal to or below 2.7 V to clamp the downstream bus voltages effectively. Looking at [Figure 7](#), we see that  $V_{o(sw)(max)}$  is at 2.7 V when the PCA9545A supply voltage is 3.5 V or lower, so the PCA9545A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see [Figure 14](#)).

More Information can be found in Application Note AN262: *PCA954X family of I<sup>2</sup>C/SMBus multiplexers and switches*.

## 7 Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see [Figure 8](#)).

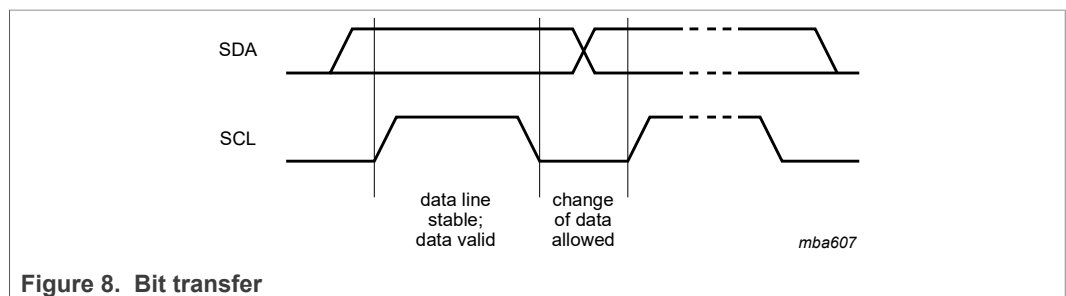


Figure 8. Bit transfer

### 7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 9](#)).

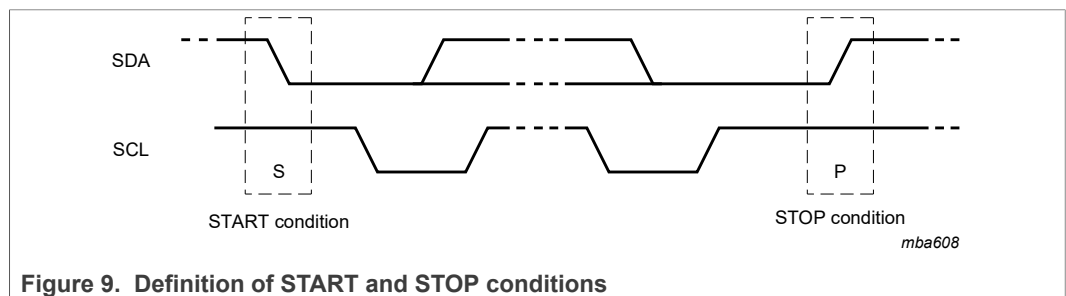
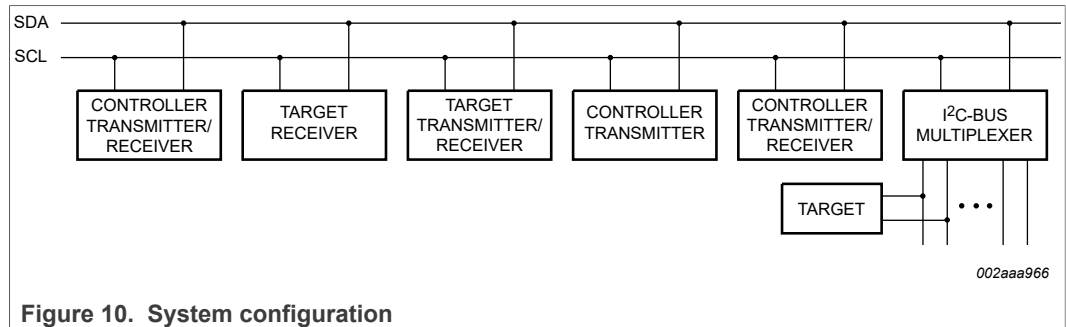


Figure 9. Definition of START and STOP conditions

### 7.3 System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'controller' and the devices which are controlled by the controller are the 'targets' (see [Figure 10](#)).

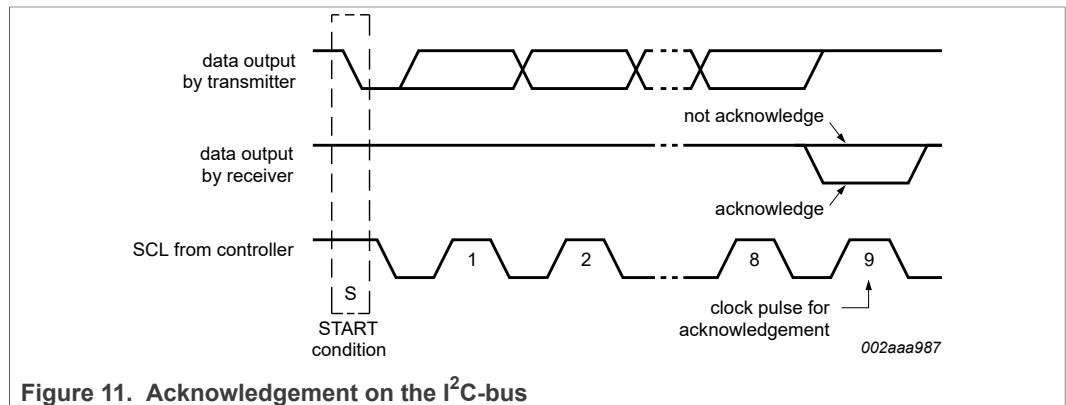


7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the controller generates an extra acknowledge related clock pulse.

A target receiver which is addressed must generate an acknowledge after the reception of each byte. Also a controller must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.



7.5 Bus transactions

Data is transmitted to the PCA9545A control register using the Write mode as shown in [Figure 12](#).

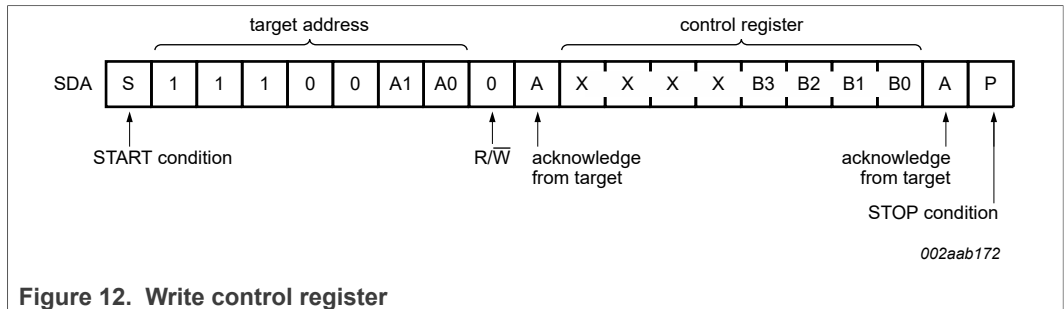


Figure 12. Write control register

Data is read from PCA9545A using the Read mode as shown in [Figure 13](#).

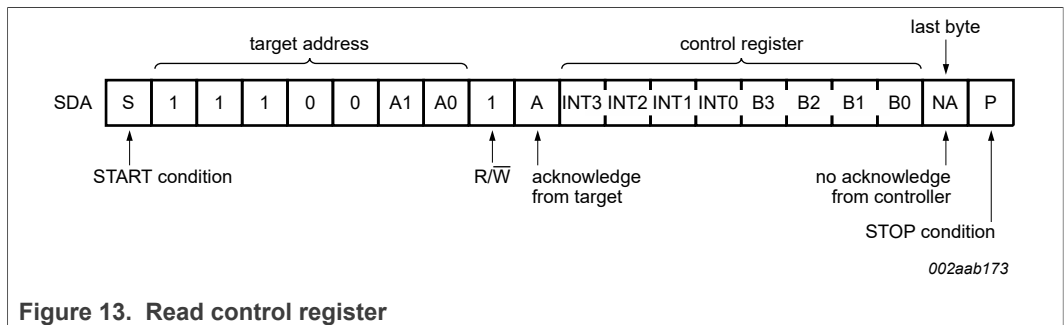
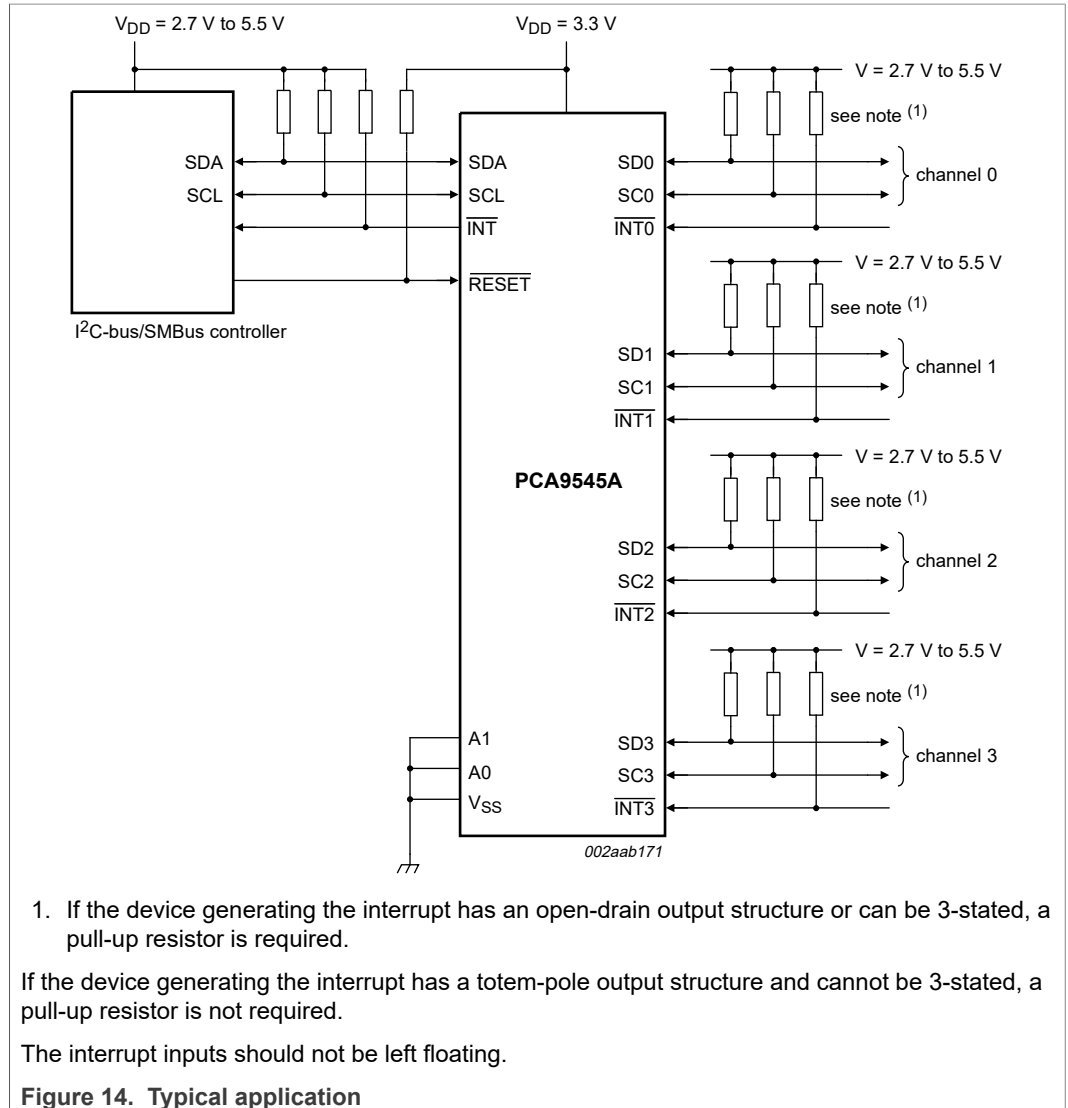


Figure 13. Read control register

8 Application design-in information



9 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V<sub>SS</sub> (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>I</sub>	input current		-	±20	mA
I <sub>O</sub>	output current		-	±25	mA
I <sub>DD</sub>	supply current		-	±100	mA
I <sub>SS</sub>	ground supply current		-	±100	mA
P <sub>tot</sub>	total power dissipation		-	400	mW
T <sub>j(max)</sub>	maximum junction temperature	[1]	-	125	°C
T <sub>stg</sub>	storage temperature		-60	+150	°C
T <sub>amb</sub>	ambient temperature	operating	-40	+85	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

10 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	HVQFN20 package	32	°C/W
		SO20 package	90	°C/W
		TSSOP20 package	146	°C/W

11 Static characteristics

Table 8. Static characteristics at V<sub>DD</sub> = 2.3 V to 3.6 V

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. See Table 9 for V<sub>DD</sub> = 4.5 V to 5.5 V<sup>[1]</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
V <sub>DD</sub>	supply voltage		2.3	-	3.6	V
I <sub>DD</sub>	supply current	Operating mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	-	10	30	µA
I <sub>stb</sub>	standby current	Standby mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	0.1	1	µA
V <sub>POR</sub>	power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	[2]	1.6	2.1	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V

Table 8. Static characteristics at V<sub>DD</sub> = 2.3 V to 3.6 V...continuedV<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. See Table 9 for V<sub>DD</sub> = 4.5 V to 5.5 V<sup>[1]</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	6	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	7	-	mA
		V <sub>OL</sub> = 0.6 V	6	10	-	mA
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	10	13	pF
<b>Select inputs A0, A1, INT0 to INT3, RESET</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	6	V
I <sub>LI</sub>	input leakage current	pin at V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	1.6	3	pF
<b>Pass gate</b>						
R <sub>on</sub>	ON-state resistance	V <sub>DD</sub> = 3.6 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 15 mA	5	11	30	Ω
		V <sub>DD</sub> = 2.3 V to 2.7 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 10 mA	7	16	55	Ω
V <sub>O(sw)</sub>	switch output voltage	V <sub>i(sw)</sub> = V <sub>DD</sub> = 3.3 V; I <sub>o(sw)</sub> = -100 μA	-	1.9	-	V
		V <sub>i(sw)</sub> = V <sub>DD</sub> = 3.0 V to 3.6 V; I <sub>o(sw)</sub> = -100 μA	1.6	-	2.8	V
		V <sub>i(sw)</sub> = V <sub>DD</sub> = 2.5 V; I <sub>o(sw)</sub> = -100 μA	-	1.5	-	V
		V <sub>i(sw)</sub> = V <sub>DD</sub> = 2.3 V to 2.7 V; I <sub>o(sw)</sub> = -100 μA	1.1	-	2.0	V
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>io</sub>	input/output capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	3	5	pF
<b>INT output</b>						
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	-	-	mA
I <sub>OH</sub>	HIGH-level output current		-	-	+10	μA

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] V<sub>DD</sub> must be lowered to 0.2 V for at least 5 μs in order to reset part.Table 9. Static characteristics at V<sub>DD</sub> = 4.5 V to 5.5 VV<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. See Table 8 for V<sub>DD</sub> = 2.3 V to 3.6 V<sup>[1]</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
V <sub>DD</sub>	supply voltage		4.5	-	5.5	V
I <sub>DD</sub>	supply current	Operating mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	-	25	100	μA

4-channel I<sup>2</sup>C-bus switch with interrupt logic and reset

Table 9. Static characteristics at V<sub>DD</sub> = 4.5 V to 5.5 V...continued

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. See Table 8 for V<sub>DD</sub> = 2.3 V to 3.6 V<sup>[1]</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>stb</sub>	standby current	Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	0.3	1	μA
V <sub>POR</sub>	power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	<sup>[2]</sup> -	1.7	2.1	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	6	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	-	-	mA
		V <sub>OL</sub> = 0.6 V	6	-	-	mA
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>SS</sub>	-1	-	+1	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	10	13	pF
<b>Select inputs A0, A1, INT0 to INT3, RESET</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	6	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	2	5	pF
<b>Pass gate</b>						
R <sub>on</sub>	ON-state resistance	V <sub>DD</sub> = 4.5 V to 5.5 V; V <sub>O</sub> = 0.4 V; I <sub>O</sub> = 15 mA	4	9	24	Ω
V <sub>o(sw)</sub>	switch output voltage	V <sub>i(sw)</sub> = V <sub>DD</sub> = 5.0 V; I <sub>o(sw)</sub> = -100 μA	-	3.6	-	V
		V <sub>i(sw)</sub> = V <sub>DD</sub> = 4.5 V to 5.5 V; I <sub>o(sw)</sub> = -100 μA	2.6	-	4.5	V
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	-	+1	μA
C <sub>io</sub>	input/output capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	3	5	pF
<b>INT output</b>						
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	-	-	mA
I <sub>OH</sub>	HIGH-level output current		-	-	+10	μA

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] V<sub>DD</sub> must be lowered to 0.2 V for at least 5 μs in order to reset part.

## 12 Dynamic characteristics

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
t <sub>PD</sub>	propagation delay	from SDA to SDx, or SCL to SCx	-	0.3 <sup>[1]</sup>	-	0.3 <sup>[1]</sup>	ns
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	kHz



Table 10. Dynamic characteristics...continued

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t <sub>HD,STA</sub>	hold time (repeated) START condition		[2] 4.0	-	0.6	-	μs
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t <sub>SU,STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>SU,STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	μs
t <sub>HD,DAT</sub>	data hold time		0 <sup>[3]</sup>	3.45	0 <sup>[3]</sup>	0.9	μs
t <sub>SU,DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	20 + 0.1C <sub>b</sub> <sup>[4]</sup>	300	ns
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	20 + 0.1C <sub>b</sub> <sup>[4]</sup>	300	ns
C <sub>b</sub>	capacitive load for each bus line		-	400	-	400	pF
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
t <sub>VD,DAT</sub>	data valid time	HIGH-to-LOW	[5] -	1	-	1	μs
		LOW-to-HIGH	[5] -	0.6	-	0.6	μs
t <sub>VD,ACK</sub>	data valid acknowledge time		-	1	-	1	μs
<b>INT</b>							
t <sub>v(INTnN-INTN)</sub>	valid time from INTn to INT signal		-	4	-	4	μs
t <sub>d(INTnN-INTN)</sub>	delay time from INTn to INT inactive		-	2	-	2	μs
t <sub>w(rej)L</sub>	LOW-level rejection time	INTn inputs	1	-	1	-	μs
t <sub>w(rej)H</sub>	HIGH-level rejection time	INTn inputs	0.5	-	0.5	-	μs
<b>RESET</b>							
t <sub>w(rst)L</sub>	LOW-level reset time		4	-	4	-	ns
t <sub>rst</sub>	reset time	SDA clear	500	-	500	-	ns
t <sub>REC,STA</sub>	recovery time to START condition		0	-	0	-	ns

[1] Pass gate propagation delay is calculated from the 20 Ω typical R<sub>on</sub> and the 15 pF load capacitance.  
 [2] After this period, the first clock pulse is generated.  
 [3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH(min)</sub> of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.  
 [4] C<sub>b</sub> = total capacitance of one bus line in pF.  
 [5] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

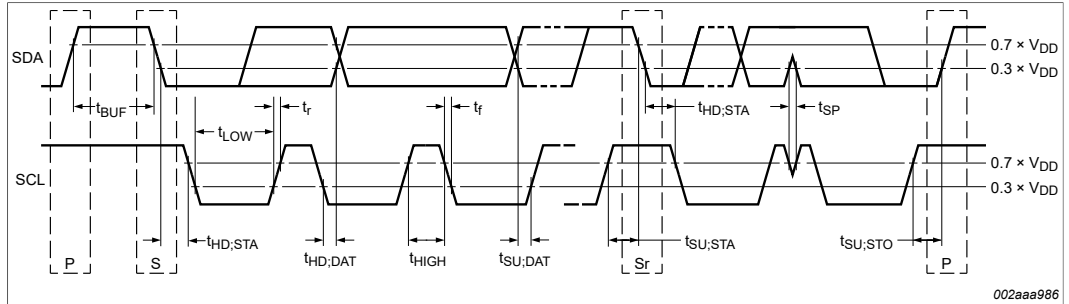


Figure 15. Definition of timing on the I<sup>2</sup>C-bus

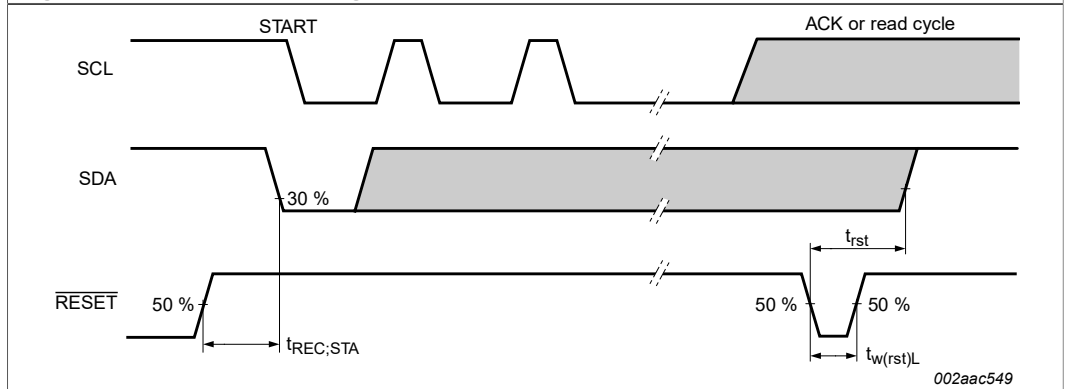
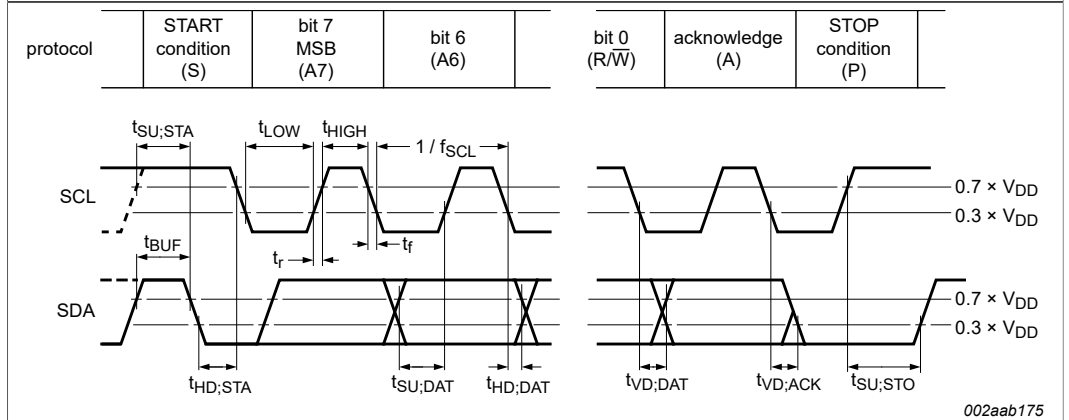


Figure 16. Definition of RESET timing



Rise and fall times refer to  $V_{IL}$  and  $V_{IH}$ .

Figure 17. I<sup>2</sup>C-bus timing diagram

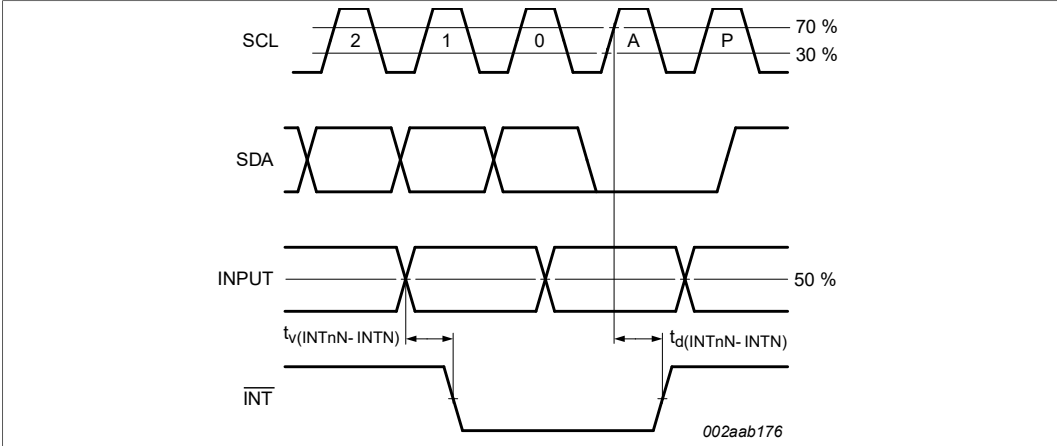
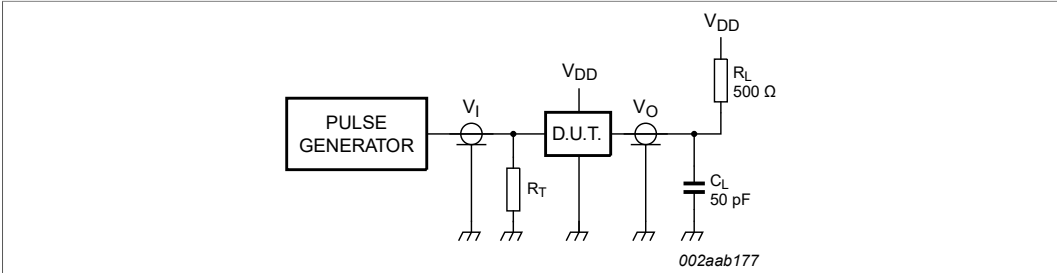


Figure 18. Expanded view of read input port register

13 Test information

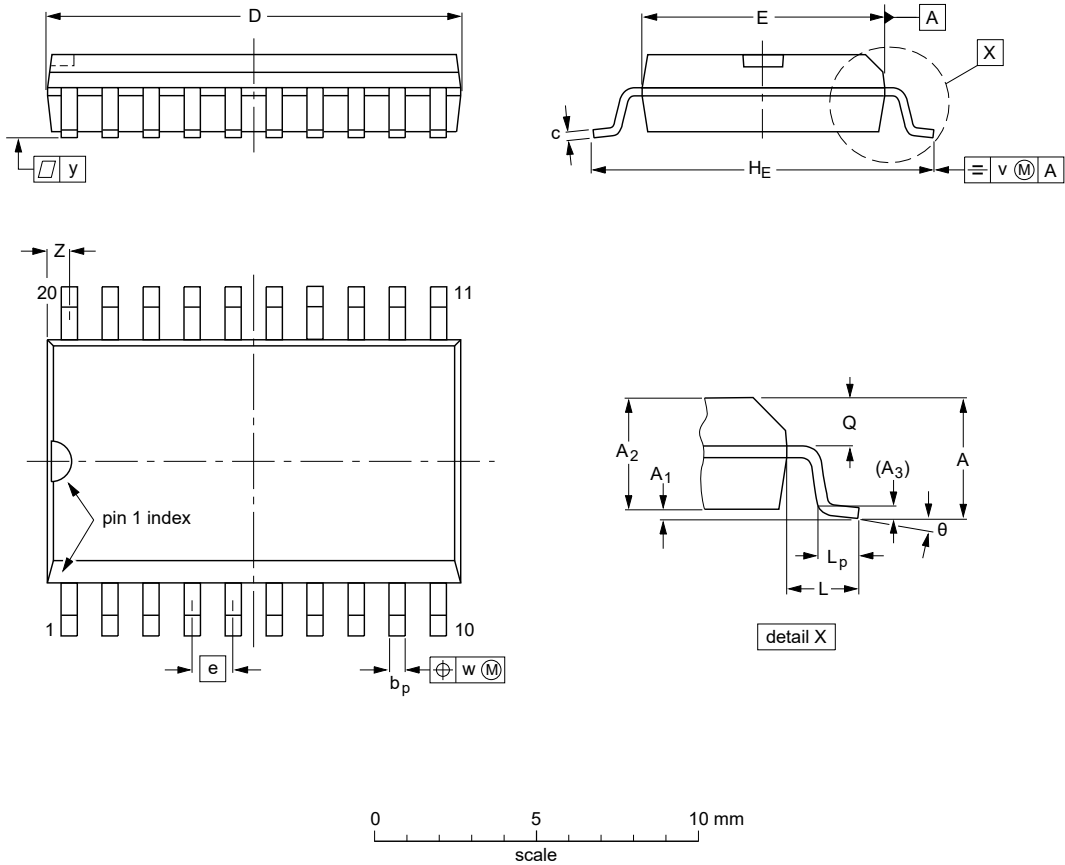


**Definitions test circuit:**  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.  
**Figure 19. Test circuitry for switching times**

14 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

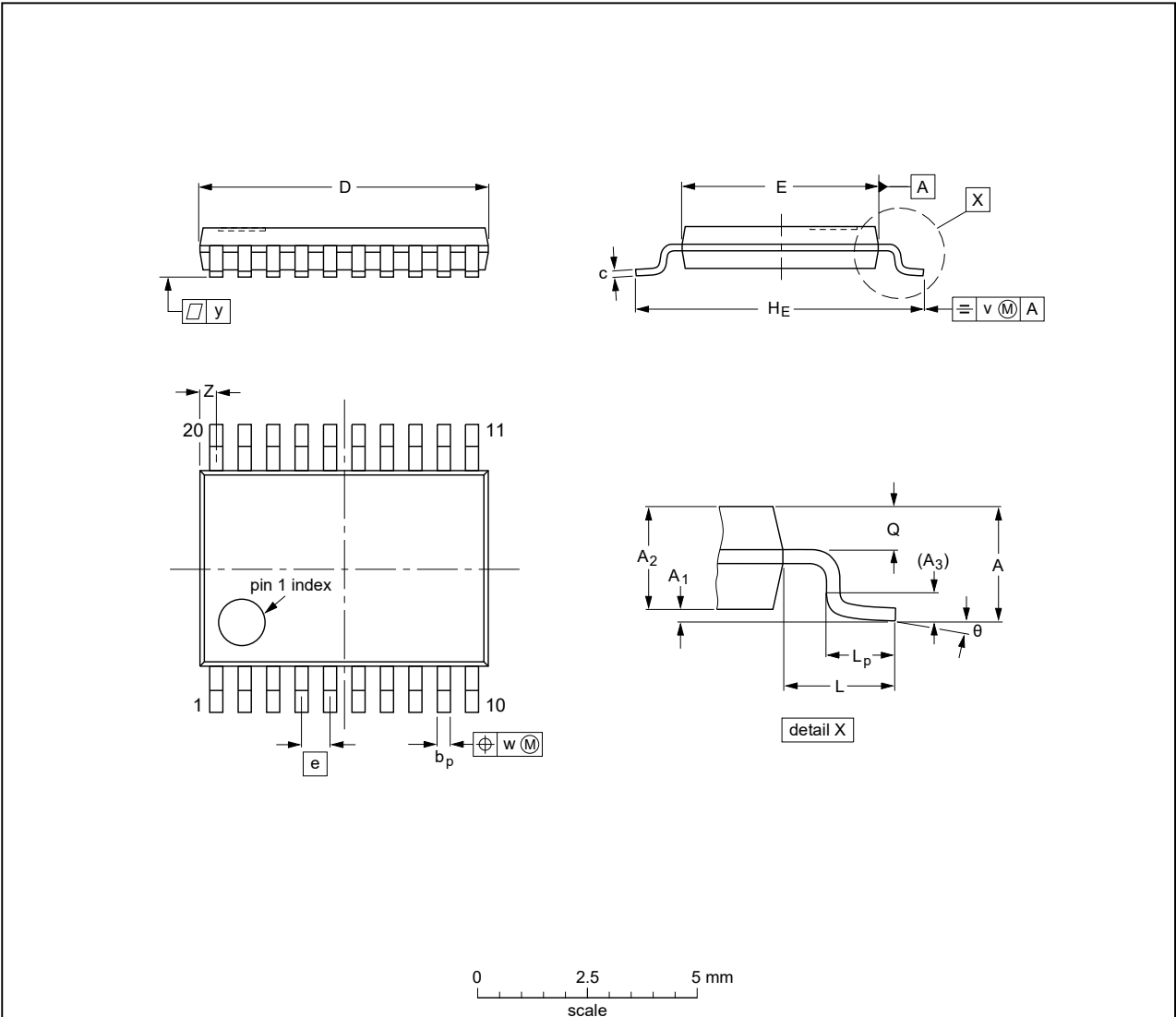
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Figure 20. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

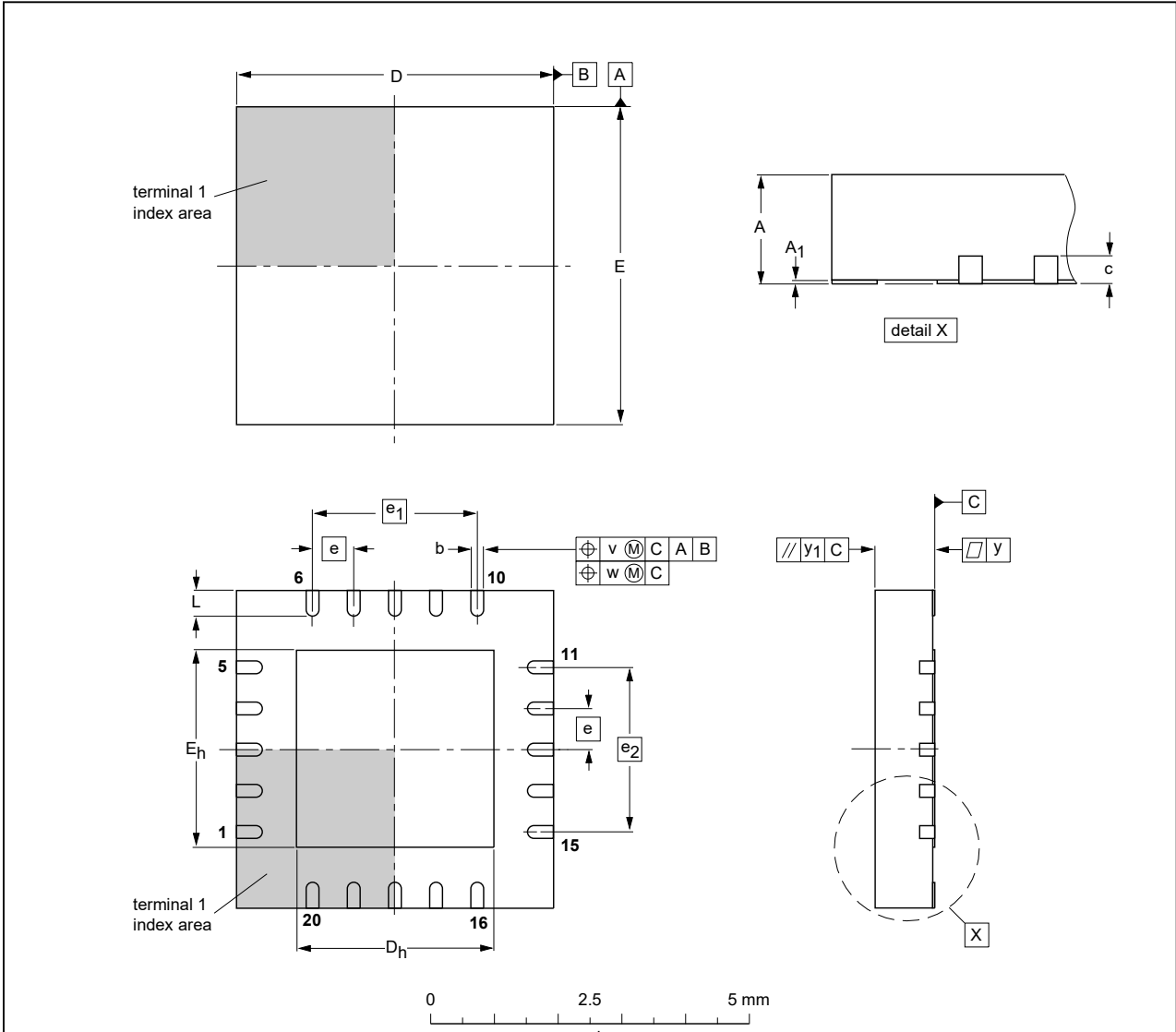
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				99-12-27 03-02-19

Figure 21. Package outline SOT360-1 (TSSOP20)

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads;  
20 terminals; body 5 x 5 x 0.85 mm

SOT662-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	e <sub>2</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

**Note**  
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT662-1	---	MO-220	---		-01-08-08- 02-10-22

Figure 22. Package outline SOT662-1 (HVQFN20)

## 15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 23](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 11](#) and [Table 12](#)

**Table 11. SnPb eutectic process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

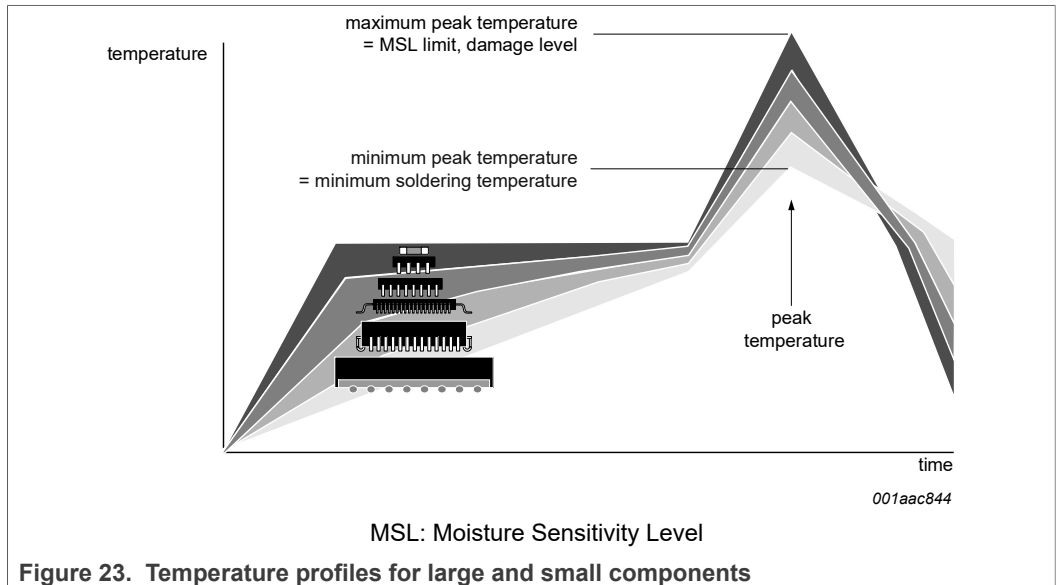
**Table 12. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

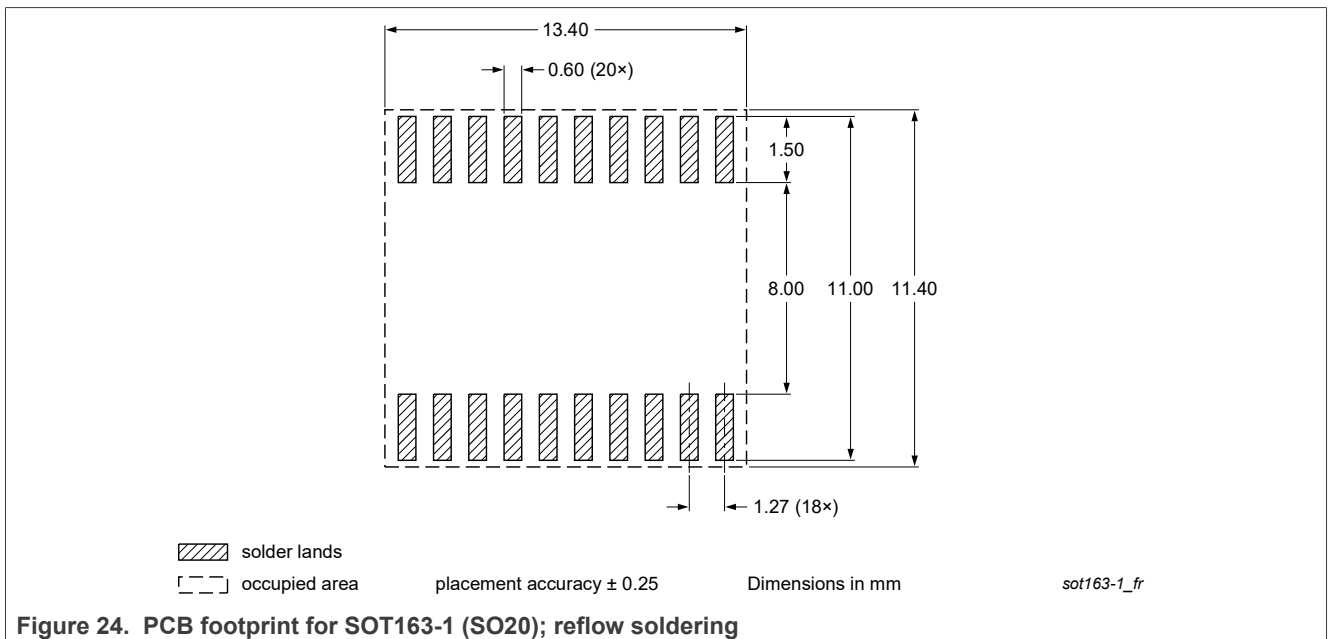
Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 23](#).

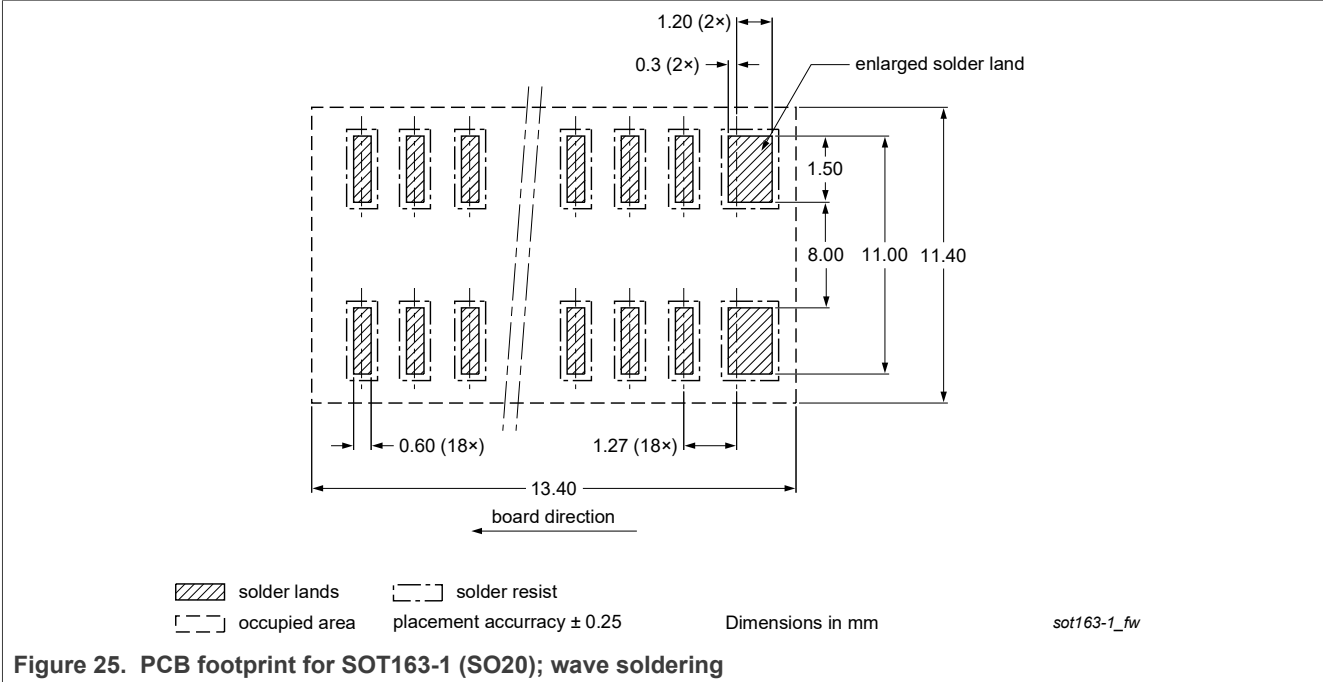




For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 16 Soldering: PCB footprints





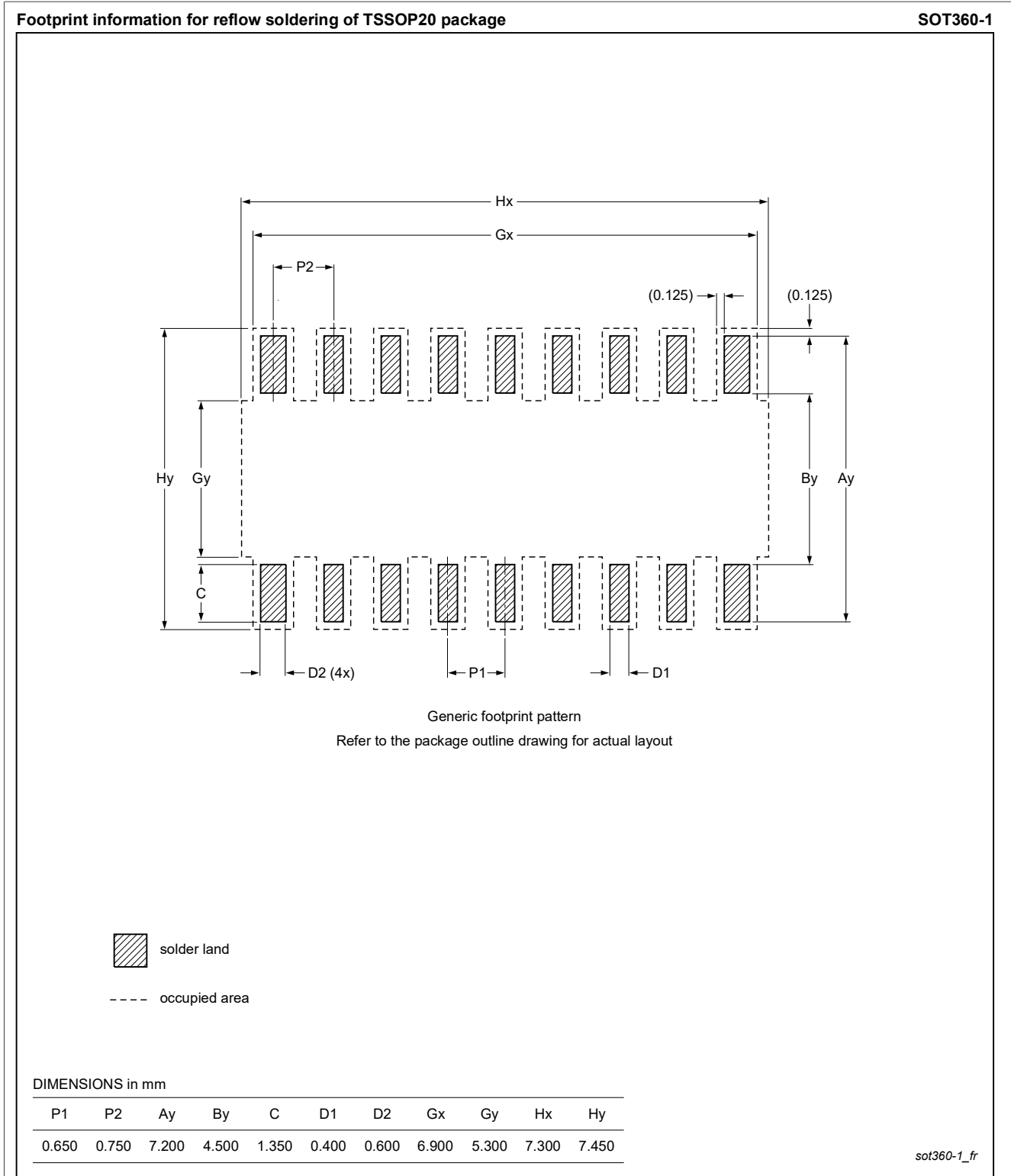


Figure 26. PCB footprint for SOT360-1 (TSSOP20); reflow soldering

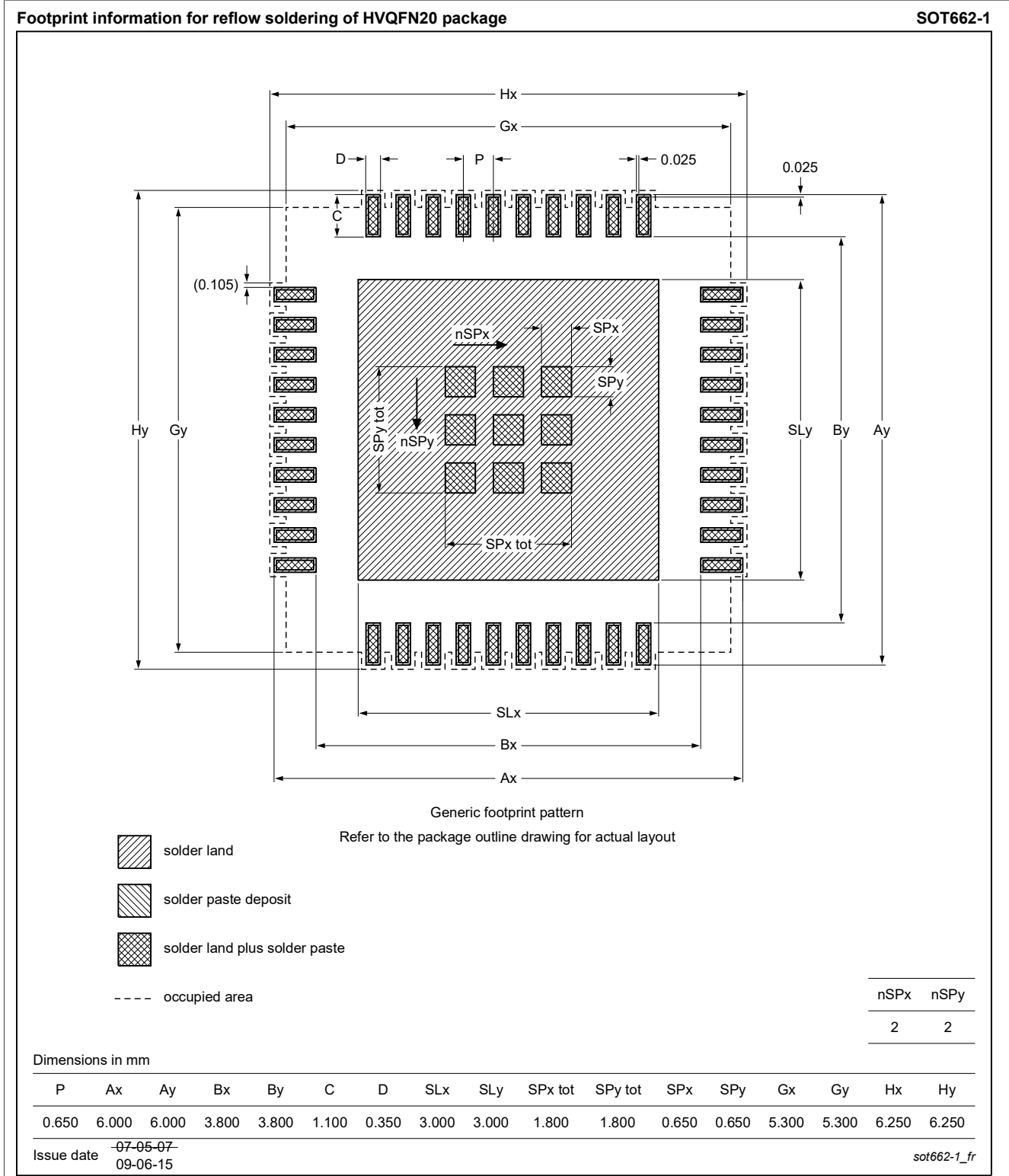


Figure 27. PCB footprint for SOT662-1 (HVQFN20); reflow soldering

## 17 Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
IC	Integrated Circuit
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus

## 18 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9545A v.10	20220927	Product data sheet	-	PCA9545A_45B_45C v.9
Modifications:	<ul style="list-style-type: none"> <li>PCA9545B and PCA9545C are identical to PCA9545A but with alternate fixed address and were removed. PCA9545B address is 11010A1A0R/W and was in Discontinuation Notice 202106032DN and PCA9545C address is 10110A1A0R/W and was in Discontinuation Notice 201905028DN.</li> <li>The terms "master" and "slave" are deprecated and have been replaced by "controller" and "target" respectively.</li> </ul>			
PCA9545A_45B_45C v.9	20140505	Product data sheet	-	PCA9545A_45B_45C v.8
PCA9545A_45B_45C v.8	20130514	Product data sheet	-	PCA9545A_45B_45C v.7
PCA9545A_45B_45C v.7	20090619	Product data sheet	-	PCA9545A_45B_45C v.6
PCA9545A_45B_45C v.6	20070319	Product data sheet	-	PCA9545A_45B_45C v.5
PCA9545A_45B_45C v.5	20061017	Product data sheet	-	PCA9545A v.4
PCA9545A v.4	20060925	Product data sheet	-	PCA9545A v.3
PCA9545A v.3	20050303	Product data sheet	-	PCA9545A v.2
PCA9545A v.2	20040929	Objective data sheet	-	PCA9545A v.1
PCA9545A v.1	20040728	Objective data sheet	-	-

## 19 Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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