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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:

30 June 1987

AMSC N/A

PREPARED BY Ray Monnin

CHECKED BY DA DiCenzo

APPROVED BY MEHauda

SIZE A

CODE IDENT. NO. 14933

REV

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, MULTIMODE DMA CONTROLLER, N-CHANNEL MOS, MONOLITHIC SILICON

DWG NO. 5962-87575

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5962-E361

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87575	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	9517A	Multimode DMA controller
02	9517A-4	Multimode DMA controller

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead 9/16" x 2 1/16") dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.5 W
Lead temperature (soldering, 5 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	(See MIL-M-38510, appendix C)
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	5.0 V dc ±10%
Minimum high level input voltage (V_{IH}) (other than CLK)	2.2 V dc
Minimum high level input voltage for CLK (V_{IH} CLK)	2.35 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc
Minimum low level input voltage (V_{IL})	-0.5 V dc
Maximum high level input voltage (V_{IH})	V_{CC} +0.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V & 5.5 V	1,2,3	All		.7	V
Input high voltage	V_{IH}	V_{CC} = 4.5 V & 5.5 V	1,2,3	All	2.2		V
Input high voltage	V_{IH} (CLK)	V_{CC} = 4.5 V & 5.5 V (CLK only)	1,2,3	All	2.35		V
Low level output voltage	V_{OL}	V_{CC} = 5.5 V I_{OL} = 3.2 mA	1,2,3	All		0.45	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = 200 µA	1,2,3	All	2.4		V
HREQ High level output voltage	V_{OH} (HREQ)	V_{CC} = 4.5 V I_{OH} = -200 µA I_{OH} = -100 µA HREQ only	1,2,3 1,2,3	All All	2.4 3.3		V V
Input load current	I_{LI}	V_{CC} = 5.5 V V_{IN} = 5.5 V & 0 V	1,2,3	All	-10	+10	µA
Output leakage current	I_{LOL} I_{LOH}	V_{CC} = 5.5 V V_{OUT} = 5.5 V & 0.40 V	1,2,3	All	-10	+10	µA
V_{CC} supply current	I_{CC}	V_{CC} = 5.5 V Outputs not loaded. Dynamic 1/	1,2,3	All		150	mA
Output capacitance	C_O	Fc = 1 MHz See 4.3.1d	4	All		20	pF
Input capacitance	C_{IN}	Fc = 1 MHz See 4.3.1d	4	All		15	pF
I/O capacitance	$C_{I/O}$	See 4.3.1d Unmeasured pins returned to V_{SS} V_{CC} = 0 V	4	All		18	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Functional tests		See 4.3.1c	7,8				
AEN HIGH from CLK LOW (S1) delay time	t_{AEL}	See figure 5 2/ 3/	9,10,11	01		300	ns
				02		225	ns
AEN LOW from CLK HIGH (S1) delay time	t_{AET}		9,10,11	01		200	ns
				02		150	ns
ADR active to float delay from CLK HIGH 4/	t_{AFAB}		9,10,11	01		150	ns
				02		120	ns
$\overline{READ}$, $\overline{WRITE}$ float delay from CLK HIGH 4/	t_{AFC}		9,10,11	01		150	ns
				02		120	ns
DB active to float delay from CLK HIGH 4/	t_{AFDB}		9,10,11	01		250	ns
				02		190	ns
ADR from $\overline{READ}$ HIGH hold time	t_{AHR}		9,10,11	All	$t_{CY}-100$		ns
D3 from ADSTB LOW hold time	t_{AHS}		9,10,11	All	30		ns
ADR from $\overline{WRITE}$ HIGH hold time	t_{AHW}		9,10,11	All	$t_{CY}-50$		ns
DACK valid from CLK LOW delay time	t_{AK}		9,10,11	01		280	ns
				02		220	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{EOP}$ HIGH from CLK HIGH delay and $\overline{EOP}$ LOW to CLK HIGH delay time 5/	t_{AK}	See figure 5 2/ 3/	9,10,11	01		250	ns
				02		190	ns
ADR stable from CLK HIGH	t_{ASM}		9,10,11	01		250	ns
				02		190	ns
DB to ADSTB LOW setup time	t_{ASS}		9,10,11	All	100		ns
Clock high time (transitions $\le$ 10 ns)	t_{CH}		9,10,11	01	120		ns
				02	100		ns
Clock low time (transitions $\le$ 10 ns)	t_{CL}		9,10,11	01	150		ns
				02	110		ns
CLK cycle time	t_{CY}		9,10,11	01	320		ns
				02	250		ns
CLK HIGH to $\overline{READ}$,$\overline{WRITE}$ LOW delay 6/	t_{DCL}		9,10,11	01		270	ns
				02		200	ns
$\overline{READ}$ HIGH from CLK HIGH (S4) delay time 6/	t_{DCTR}		9,10,11	01		270	ns
				02		210	ns
$\overline{WRITE}$ HIGH from CLK HIGH (S4) delay time 6/	t_{DCTW}		9,10,11	01		200	ns
				02		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
HREQ valid from CLK HIGH delay time 7/	t_{DQ1}	See figure 5 2/ 3/	9,10,11	01		160	ns
				02		120	ns
HREQ valid from CLK HIGH delay time 7/	t_{DQ2}		9,10,11	01		$2t_{CY}$ +250	ns
				02		$2t_{CY}$ +190	ns
$\overline{EOP}$ LOW from CLK LOW setup	t_{EPS}		9,10,11	01	60		ns
				02	45		ns
$\overline{EOP}$ pulse width	t_{EPW}		9,10,11	01	300		ns
				02	225		ns
ADR float to active delay from CLK HIGH	t_{FAAB}		9,10,11	01		250	ns
				02		190	ns
$\overline{READ}$, $\overline{WRITE}$ active from CLK HIGH	t_{FAC}		9,10,11	01		200	ns
				02		150	ns
DB float to active delay from CLK HIGH	t_{FADB}		9,10,11	01		300	ns
				02		225	ns
HACK valid to CLK HIGH setup	t_{HS}		9,10,11	01	100		ns
				02	75		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input data from $\overline{MEMR}$ HIGH hold time	t_{IDH}	See figure 5 2/ 3/	9,10,11	All	0		ns
Input data to $\overline{MEMR}$ HIGH setup time	t_{IDS}		9,10,11	01	250		ns
				02	190		ns
Output data from $\overline{MEMW}$ HIGH hold time	t_{ODH}		9,10,11	All	20		ns
Output data valid to $\overline{MEMW}$ HIGH 8/	t_{ODV}		9,10,11	01	200		ns
				02	125		ns
DREQ to CLK LOW (S1, S4) setup time	t_{QS}		9,10,11	01	0		ns
				02	0		ns
CLK to READY LOW hold time	t_{RH}		9,10,11	All	20		ns
READY to CLK setup time	t_{RS}		9,10,11	01	100		ns
				02	60		ns
ADSTB HIGH from CLK HIGH delay time	t_{STL}		9,10,11	01		200	ns
				02		150	ns
ADSTB LOW from CLK HIGH delay	t_{STT}		9,10,11	01		140	ns
				02		110	ns
DREQ from DACK valid hold time	t_{QH}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
HREQ to HACK delay time	t_{RQHA}	See figure 5 2/ 3/	9,10,11	All	1		CLK
ADR valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	t_{AR}		9,10,11	All	50		ns
ADR valid to $\overline{WRITE}$ HIGH setup time	t_{AW}		9,10,11	01	200		ns
				02	150		ns
$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH setup time	t_{CW}		9,10,11	01	200		ns
				02	150		ns
Data valid to $\overline{WRITE}$ HIGH setup time	t_{DW}		9,10,11	01	200		ns
				02	150		ns
ADR or $\overline{CS}$ hold from $\overline{READ}$ HIGH	t_{RA}		9,10,11	All	0		ns
Data access from $\overline{READ}$ LOW 9/	t_{RDE}		9,10,11	01		300	ns
				02		200	ns
DB float delay from $\overline{READ}$ HIGH 4/	t_{RDF}		9,10,11	01	20	150	ns
				02	20	100	ns
Power supply HIGH to reset LOW setup	t_{RSTD}		9,10,11	All	500		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device types	Limits		Unit
					Min	Max	
RESET to first $\overline{IOWR}$	t_{RSTS}	See figure 5 2/ 3/	9,10,11	All	$2t_{CY}$		ns
RESET pulse width	t_{RSTW}		9,10,11	All	300		ns
$\overline{READ}$ width	t_{RW}		9,10,11	01	300		ns
				02	250		ns
ADR from $\overline{WRITE}$ HIGH hold time	t_{WA}		9,10,11	All	20		ns
$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH hold time	t_{WC}		9,10,11	All	20		ns
Data from $\overline{WRITE}$ HIGH hold time	t_{WD}		9,10,11	All	30		ns
Write width	t_{WWS}		9,10,11	All	200		ns
Data access from ADR valid $\overline{CS}$ LOW 10/	t_{AD}	See figure 5	9,10,11	All		300	ns

See footnotes on next page.

1/ I_{CC} is measured in a dynamic condition with outputs in a worst case state having no loads applied.

2/ Test conditions: V_{CC} = 4.5 V & 5.5 V, see figure 4
V_{IL} = 0.45 V V_{IH} = 2.4 V
V_{OL} = 0.8 V V_{OH} = 2.0 V
I_{OL} = 3.2 mA I_{OH} = -200 µA
Capacitive output loading = 100 ±20 pF

3/ Clock rise and fall times are controlled by the test equipment. Measurement of typical signals generated $t_R = t_F$ = 5 ns.

4/ V_{OL} level to float level specification values are tested.
V_{OH} level to float level specification value is not tested.

5/ $\overline{EOP}$ HIGH from CLK HIGH delay time.
$\overline{EOP}$ LOW to CLK HIGH delay time.

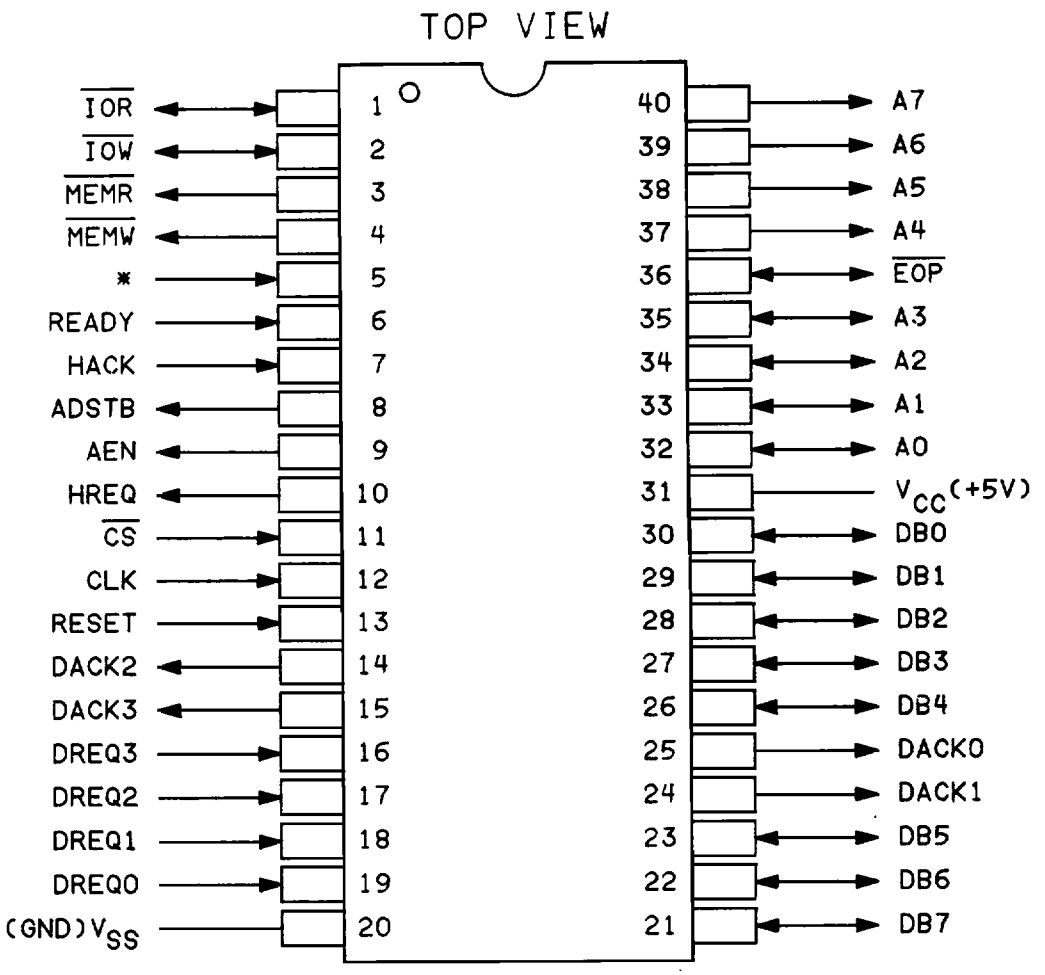
6/ The new $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal WRITE will be t_{CY}-100 ns and for extended WRITE will be $2t_{CY}$-100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal READ will be $2t_{CY}$-50 ns and for compressed READ will be t_{CY}-50 ns.

7/ t_{DQ} is specified for two different output HIGH levels. t_{DQ1} is measured at 2.0 V. t_{DQ2} is measured at 3.3 V. The value for t_{DQ2} assumes an external 3.3 kΩ pull-up resistor connected from HREQ to V_{CC}.

8/ If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by $N(t_{CY})$.

9/ Successive READ or WRITE operations by the external processor to program or examine the controller must be timed to allow at least 600 ns for the 01 device and at least 450 ns for the 02 device as recovery time betweeen active READ or WRITE.

10/ t_{AD} is tested indirectly and is equal to $t_{AR} + t_{RDE}$.



* Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. Alternately, pin 5 may be tied to V_{CC}.

FIGURE 1. Terminal connections.

Register and function addressing

Interface signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read status register
1	0	0	0	1	0	Write command register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write request register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write single mask register bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write mode register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear byte pointer flip-flop
1	1	0	1	0	1	Read temporary register
1	1	0	1	1	0	Master clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear mask register
1	1	1	1	0	1	Illegal
1	0	1	1	1	0	Write all mask register bits

FIGURE 2. Truth tables.

Channel	Register	Operation	Signals							Internal flip-flop	Data bus DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base & current address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base & current word count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current word count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base & current address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base & current word count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current word count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base & current address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base & current word count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current word count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base & current address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base & current word count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current word count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

Word count and address register command codes

FIGURE 2. Truth tables - Continued.

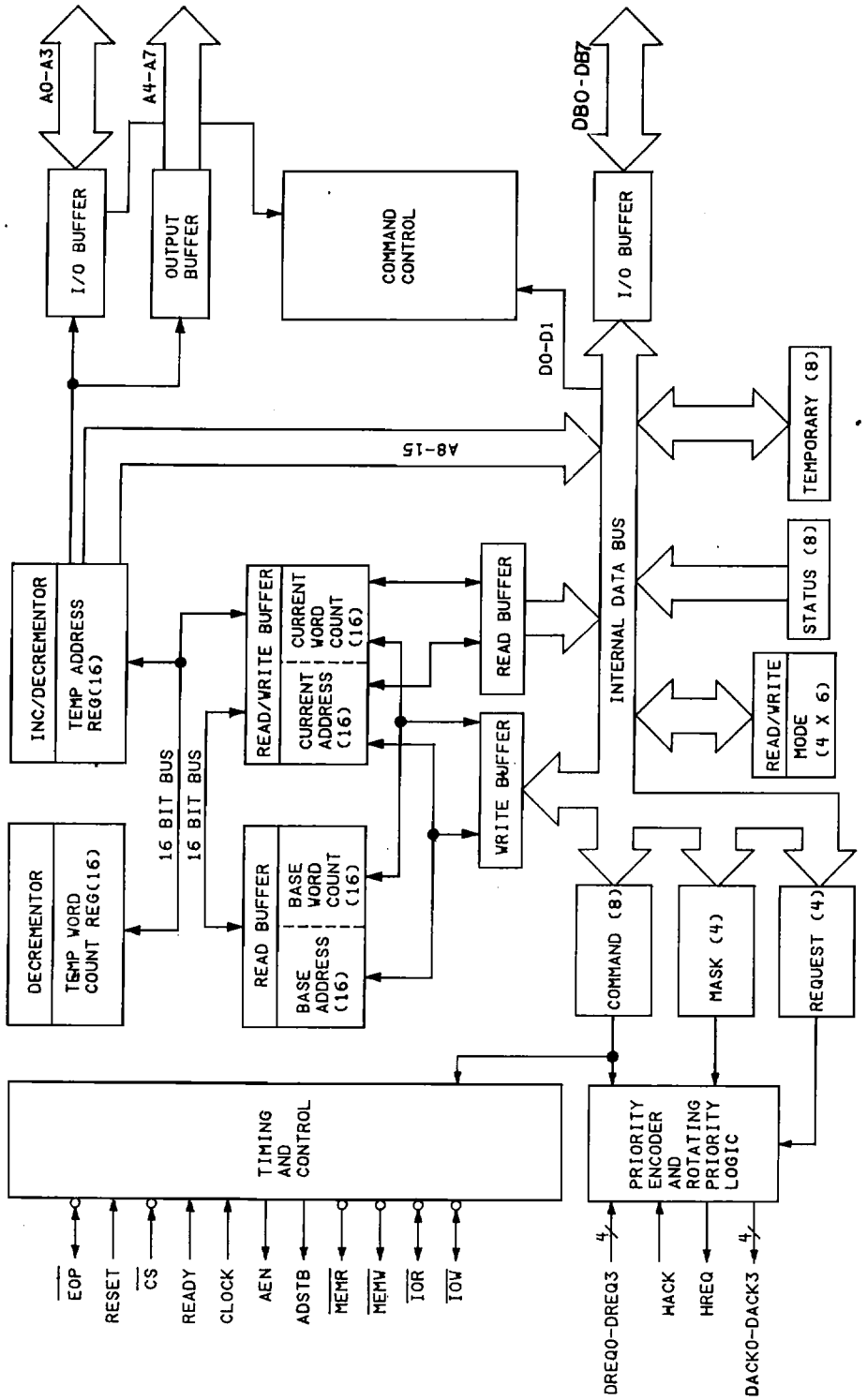
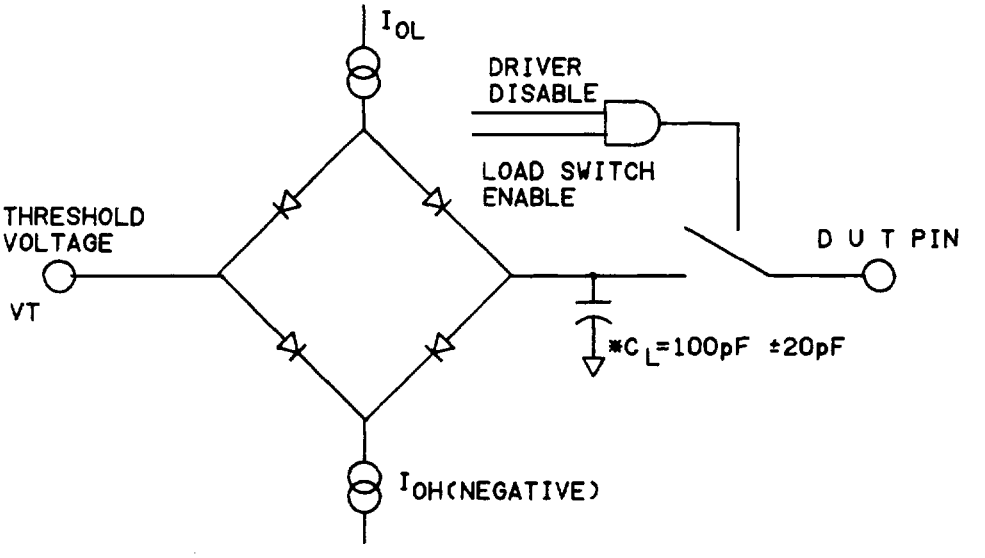


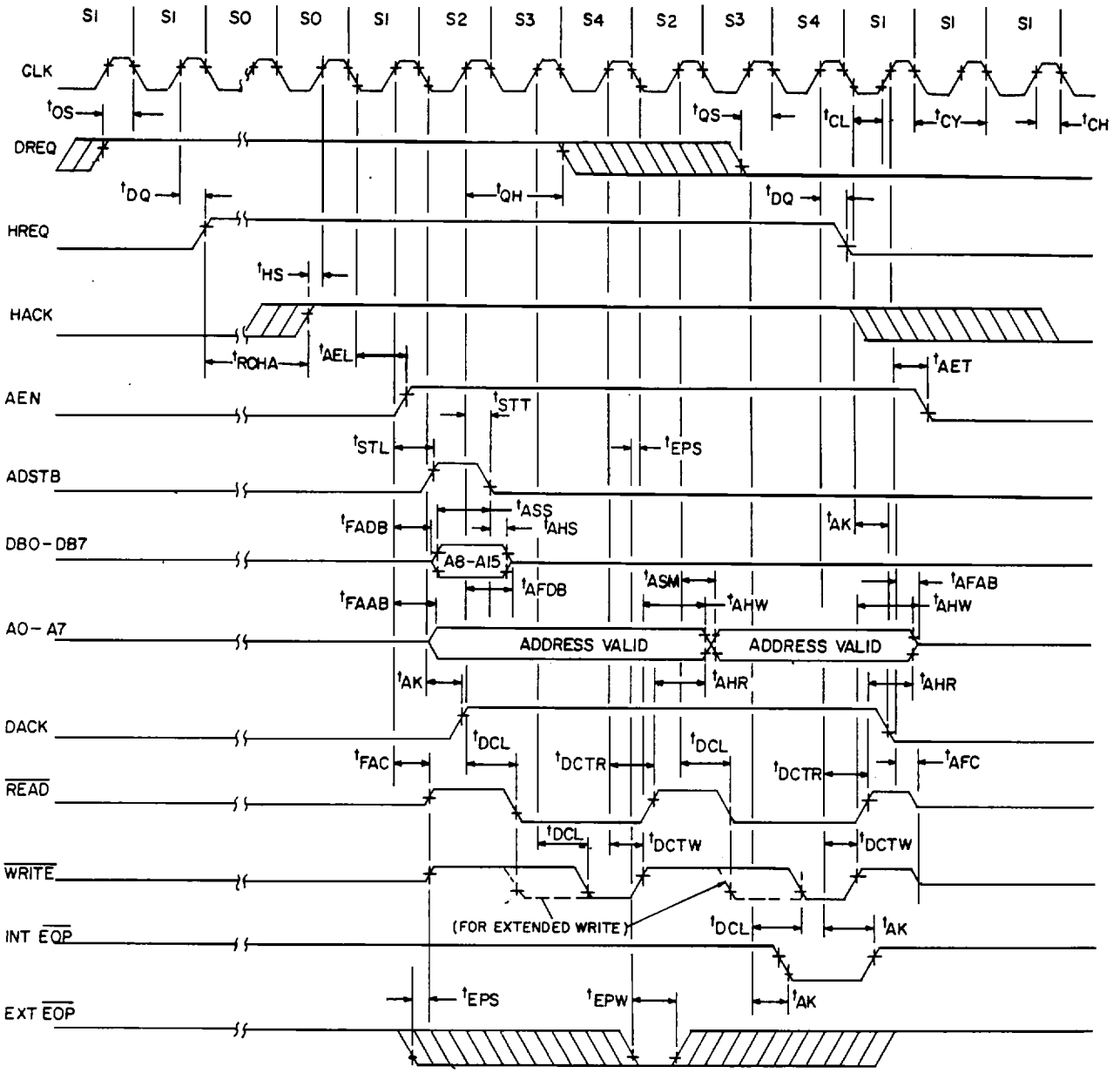
FIGURE 3. Block diagram.



* C_L = teradyne channel capacitance including device interface board

FIGURE 4. Dynamic load circuit.

Active cycle timing diagram



NOTE: $\overline{EOP}$ must precede AEN in single transfer mode.

FIGURE 5. Switching waveforms.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-87575
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DESC FORM 193A
FEB 86

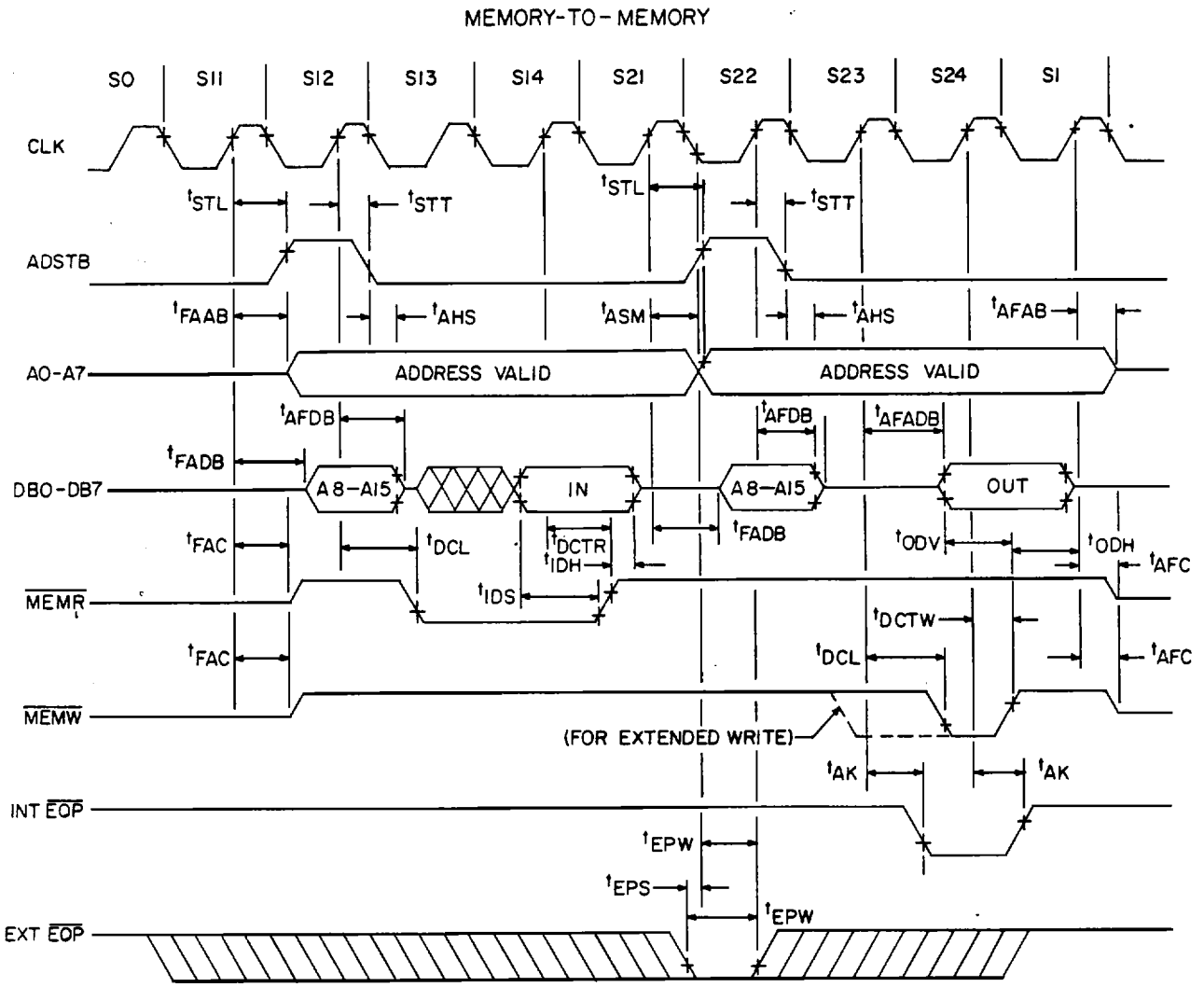

FIGURE 5. Switching waveforms - Continued.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-87575
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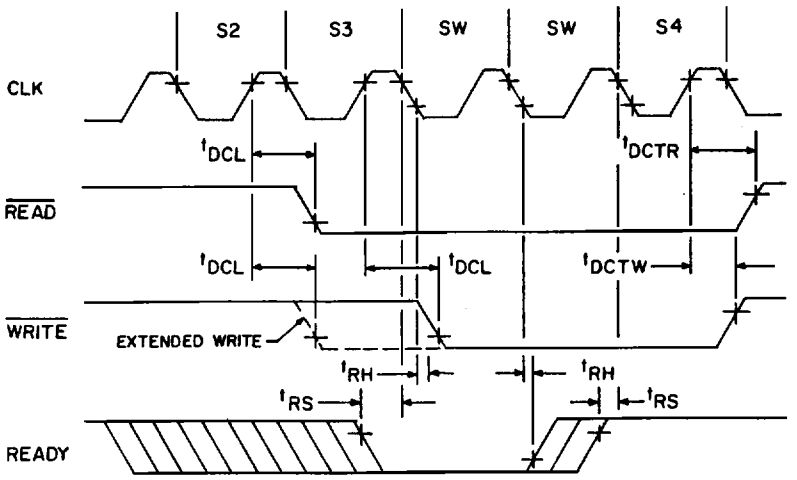
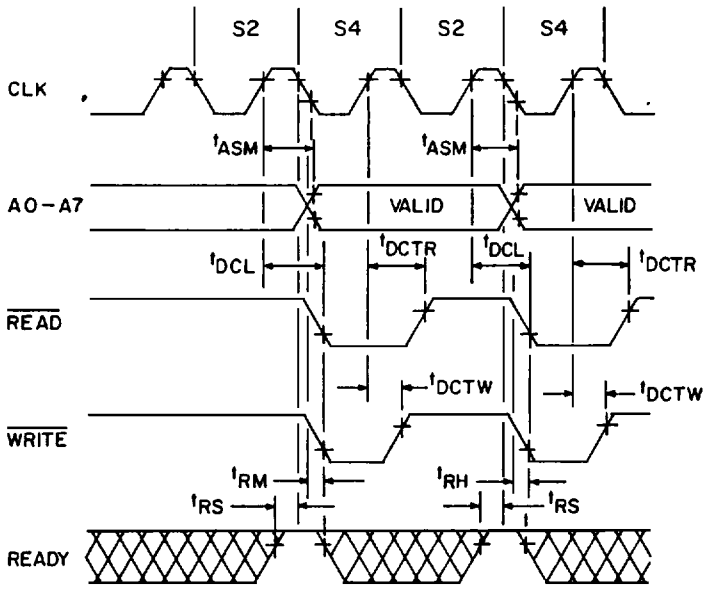
DESC FORM 193A
FEB 86

READY TIMING



COMPRESSED TIMING



RESET TIMING

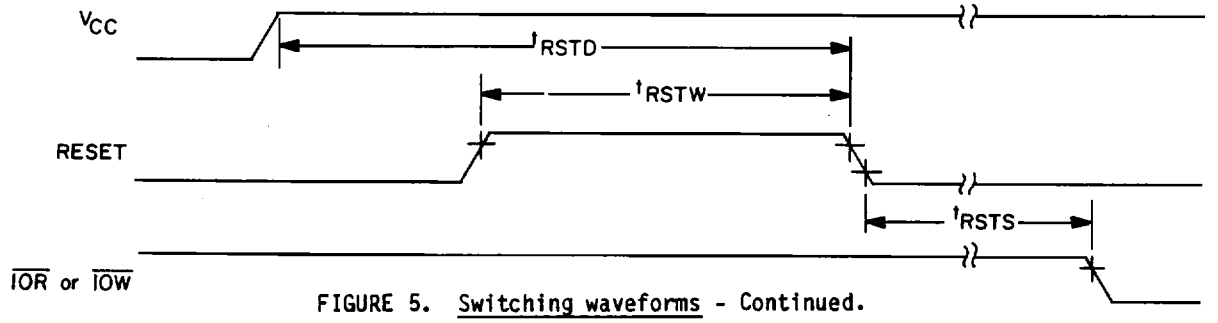
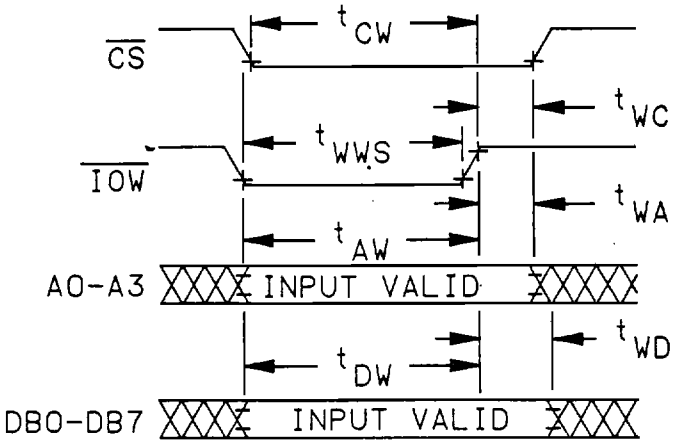
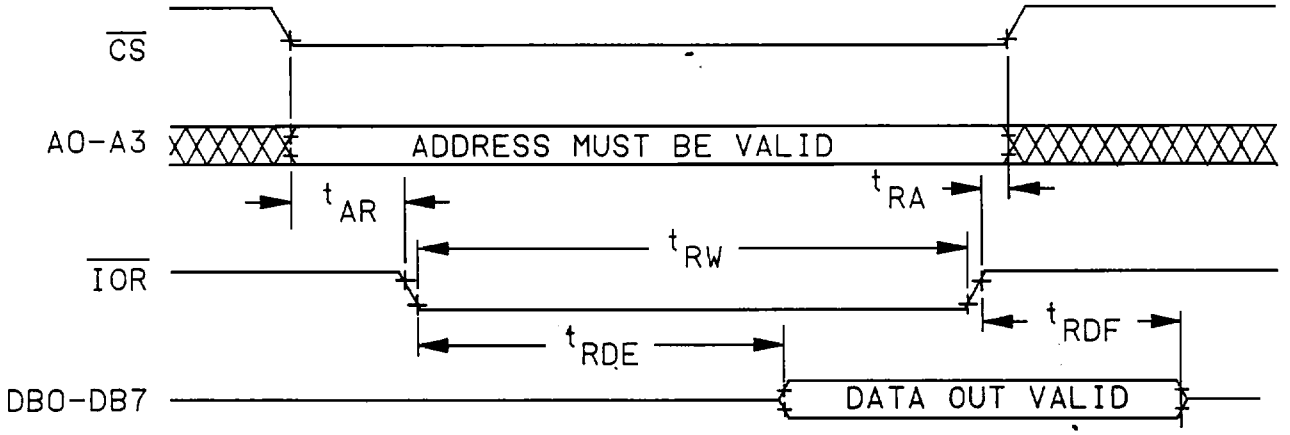


FIGURE 5. Switching waveforms - Continued.

Program Condition Write Timing



Program Condition Read Cycle



Note: t_{AD} is tested indirectly and is equal to $t_{AR} + t_{RDE}$.

FIGURE 5. Switching waveforms - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 test sufficiently to verify the truth tables.

d. Subgroup 4 (C_{IN}, C_{OUT} and $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Initial electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8,9, 10,11
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Pin description:

PIN NO.	NAME	I/O	DESCRIPTION
31	V_{CC}		Power: +5 volt supply.
20	V_{SS}		Ground.
12	CLK	I	Clock Input: Clock Input controls the internal operations of the device and its rate of data transfers. The input may be driven at up to 3 MHz for the 01 device and up to 5 MHz for the 02 device.
11	$\overline{CS}$	I	Chip Select: Chip Select is an active low input used to select the device as an I/O device during the idle cycle. This allows CPU communication on the data bus.
13	RESET	I	Reset: Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the First/Last Flip/Flop and sets the Mask register. Following a Reset the device is in the idle cycle.
6	READY	I	Ready: Ready is an input used to extend the memory read and write pulses from the device to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
7	HACK	I	Hold Acknowledge: The active high Hold acknowledge from the CPU indicates that it has relinquished control of the system buses.
19-16	DREQ0-DREQ3	I	DMA Request: The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.

6.3 Pin description: - Continued

PIN NO.	NAME	I/O	DESCRIPTION
30-26, 23-21	DB0-DB7	I/O	DATA Bus. The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the device control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the device on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
1	$\overline{IOR}$	I/O	I/O Read: I/O Read is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the device to access data from a peripheral during a DMA Write transfer.
2	$\overline{IOW}$	I/O	I/O Write: I/O Write is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to load information into the device. In the active cycle, it is an output control signal used by the device to load data to the peripheral during a DMA read transfer.
36	$\overline{EOP}$	I/O	End of Process: End of Process is an active low bidirectional open-drain signal. Information concerning the completion of DMA service is available at the bidirectional $\overline{EOP}$ pin. The device allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an exteral $\overline{EOP}$ signal. The device also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ Line. The reception of $\overline{EOP}$, either internal or external, will cause the device to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.

6.3 Pin description: - Continued

PIN NO.	NAME	I/O	DESCRIPTION
32-35	A0-A3	I/O	Address: The four least significant address lines are bidirectional three-state signals. In the idle cycle, they are inputs and are used by the CPU to address the the registers to be loaded or read. In the active cycle, they are outputs and provide the lower 4 bits of the output address.
37-40	A4-A7	O	Address: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during DMA service.
10	HREQ	O	Hold Request: This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the device to issue the HRQ. After HRQ goes active, at least one clock cycle (t_{CY}) must occur before HLDA goes active.
25,24 14,15	DACK0-DACK3	O	DMA Acknowledge: DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
9	AEN	O	Address Enable: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable in other system bus drivers during DMA transfers. AEN is active high.
8	ADSTB	O	Address Strobe: The active high Address Strobe is used to strobe the upper address byte into an external latch.
3	$\overline{\text{MEMR}}$	O	Memory Read: The Memory read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
4	$\overline{\text{MEMW}}$	O	Memory Write: The Memory Write signal is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-87575 01QX	34335	AM9517A/BQA	
5962-87575 02QX	34335	AM9517A-4/BQA	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Inc. 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088

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