

## High-Speed, Quad, Industrial Digital Input with Parallel Output

**MAX22193**

### Product Highlights

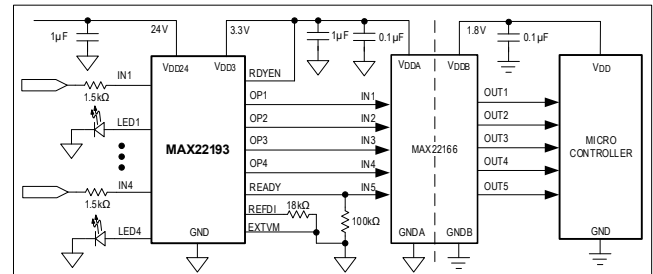
- High-Speed, Industrial Digital Inputs
  - 300ns Maximum Propagation Delay
  - 40ns Maximum Channel-to-Channel Skew
  - Parallel Output for Simultaneous Signal Delivery
- High Integration Reduces BOM and Space
  - Operates Directly from Field Supply (7V to 65V)
  - Compatible with 3.3V or 5V Logic
  - 4mm x 4mm, 20-TQFN Package
- Low Power and Low Heat Dissipation
  - 1.2mA (max) Quiescent Current with 3.3V Supply
  - Accurate Input Current-Limiters
  - Energyless Field-Side LED Drivers
- Fault Tolerant with Built-In Diagnostics
  - Integrated Field-Side Supply Monitor
  - Integrated Over-Temperature Monitor
  - Current-Setting Resistor Monitor
- Configurability Enables Wide Range of Applications
  - Configurable IEC 61131-2 Types 1, 2, 3 Inputs
  - Input Current Limiting from 1.18mA to 7.01mA
- Robust Design for Industrial Environments
  - $\pm 2$ kV Surge Tolerant using 470 $\Omega$  Resistor (min)
  - $\pm 8$ kV Contact ESD and  $\pm 15$ kV Air Gap ESD Using 470 $\Omega$  Resistor (min)
  - -40°C to +125°C Ambient Operating Temperature

### Key Applications

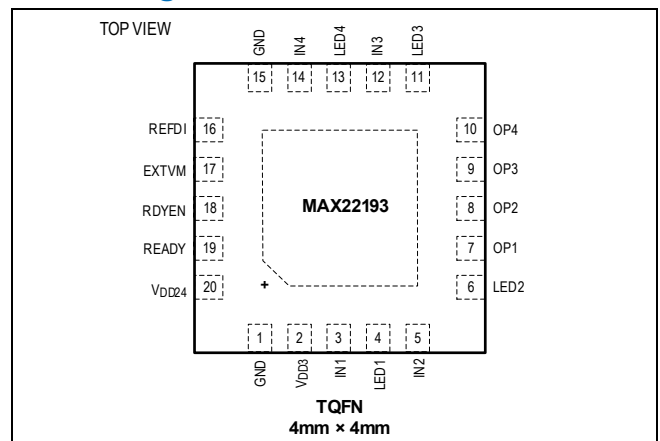
- Programmable Logic Controllers (PLC)
- Distributed Control System (DCS)
- Motor Control
- Industrial Automation
- Process Automation

The MAX22193 translates four 24V industrial digital inputs to four CMOS-logic-compatible, parallel outputs. Propagation delay from input-to-output is less than 300ns for all four channels. Current-limiter on each digital input greatly reduces power dissipation compared to traditional resistive input. The accuracy of these current-limiters minimizes power dissipation while ensures compliance with the IEC 61131-2 standard. A current-setting resistor allows the MAX22193 to be configured for Type 1, Type 2 or Type 3 digital inputs. Additionally, the MAX22193 has energyless field-side LED drivers to meet the indicator light requirement of IEC 61131-2 with no additional power dissipation.

### Simplified Application Diagram



### Pin Configuration



The MAX22193 provides a 3.3V integrated voltage regulator. The internal LDO accepts the field supply  $V_{DD24}$  from 7V to 65V. The internal LDO output can supply up to 25mA of current in addition to powering the basic MAX22193 requirements. This LDO can be used to power digital isolators and other field-side circuits. Alternatively, the MAX22193 can be powered from an external 3.0V to 5.5V supply at  $V_{DD3}$ .

The MAX22193 includes an open-drain READY output that asserts high to indicate the MAX22193 is functional. If the  $V_{DD24}$  field-side supply voltage is too low, or a fault in the current-setting resistor is detected, or the device reaches an over-temperature condition, the READY signal is set to high-impedance.

**Ordering Information** appears at end of data sheet.

**Absolute Maximum Ratings**

V<sub>DD3</sub> to GND ..... -0.3V to +6V  
 V<sub>DD24</sub> to GND ..... -0.3V to +70V  
 OP1-OP4 to GND ..... -0.3V to (V<sub>DD3</sub>+0.3)V  
 IN1-IN4 to GND ..... -40V to +40V  
 REFDI to GND ..... -0.3V to (V<sub>DD3</sub>+0.3)V  
 READY, RDYEN to GND ..... -0.3V to +6V  
 EXTVM to GND ..... -0.3V to +6V  
 LED1-LED4 to GND ..... -0.3V to +6V

Single-layer Board (derate 16.90mW/°C above T<sub>A</sub> = +70°C)  
 ..... 1355.90mW  
 Multilayer Board (derate 25.60mW/°C above T<sub>A</sub> = +70°C)  
 ..... 2051.30mW

**Continuous Power Dissipation (T<sub>A</sub> = +70°C)**

**Temperature Ratings**

Operating Temperature Range ..... -40°C to +125°C  
 Maximum Junction Temperature ..... +150°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (soldering, 10s) ..... +300°C  
 Soldering Temperature (reflow) ..... +260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Package Information**

**20-TQFN**

Package Code	T2044+3C
Outline Number	<a href="#">21-0139</a>
Land Pattern Number	<a href="#">90-0037</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	59°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	6°C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	39°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	6°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

## Electrical Characteristics

( $V_{DD3} = +3.0V$  to  $+5.5V$ ,  $C_L$  on  $OP\_$  = 15pF,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD24} = +24V$ , field inputs  $V_{IN\_} = +24V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLIES</b>						
Supply Voltage	$V_{DD24}$	Normal Operation	7		65	V
	$V_{DD3}$	Powered from an external power supply	3.0		5.5	
Supply Current Powered from $V_{DD24}$	$I_{DD24}$	$V_{DD24} = 24V$ , $V_{IN\_} = 0V$ , $LED\_ = GND$ , no load on $OP\_$		0.6	1.2	mA
Supply Current Powered from $V_{DD3}$	$I_{DD3}$	$V_{DD3} = 3.3V$ , $V_{DD24}$ floating, $V_{IN\_} = 0V$ , $LED\_ = GND$ , no load on $OP\_$		0.6	1.2	mA
$V_{DD3}$ Undervoltage-Lockout Threshold	$V_{UVLO3}$	Powered from $V_{DD3}$ , $V_{DD3}$ rising, $V_{DD24}$ floating	2.4		2.9	V
$V_{DD3}$ Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST3}$			0.07		V
$V_{DD24}$ READY Threshold	$V_{READY\_24VR}$	$V_{DD24}$ rising, $EXTVM = GND$	13.8	14.6	15.4	V
	$V_{READY\_24VF}$	$V_{DD24}$ falling, $EXTVM = GND$	13.3	14.1	15.0	
$V_{DD24}$ Undervoltage-Lockout Threshold	$V_{UVLO24}$	$V_{DD24}$ rising	6.0		6.8	V
$V_{DD24}$ Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST24}$			0.45		V
Regulator Output Voltage	$V_{DD3}$	$I_{LOAD} = 1mA$ , $V_{DD24} = 7V$ to $65V$	3.0	3.3	3.6	V
Line Regulation	d $V_{DDLIN}$	$I_{LOAD} = 1mA$ , $V_{DD24} = 12V$ to $24V$		0		mV
Load Regulation	d $V_{DDLAD}$	$I_{LOAD} = 1mA$ to $10mA$ , $V_{DD24} = 12V$		1		mV
Short-Circuit Current Limit	$I_{DD24\_SC}$	$I_{DD24}$ when $V_{DD3}$ short to GND, $V_{DD24} = 12V$	28	37.5	50	mA
<b>EXTVM MONITOR</b>						
EXTVM Glitch Filter				3		$\mu s$
EXTVM Threshold Off-to-On	$V_{24TH\_OFF\_ON}$	$V_{DD24}$ rising	0.77	0.81	0.84	V
EXTVM Threshold On-to-Off	$V_{24TH\_ON\_OFF}$	$V_{DD24}$ falling	0.74	0.79	0.82	V
External EXTVM Selection Threshold	$EXTVM\_SEL$			0.3		V
External EXTVM Selectable $V_{DD24}$ Threshold	$EXTVM\_VDD24$		10		30	V
EXTVM Leakage Current	$I_{EXTVM\_L}$		-1		+1	$\mu A$
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown Threshold	$T_{SHDN}$	$V_{DD3}$ internal regulator off		165		$^\circ C$

( $V_{DD3} = +3.0V$  to  $+5.5V$ ,  $C_L$  on  $OP_- = 15pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD24} = +24V$ , field inputs  $V_{IN} = +24V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Threshold Hysteresis	$T_{SHDN\_HYS}$			10		$^\circ C$
<b>REFDI SETTINGS</b>						
REFDI Voltage	$V_{REFDI}$			0.61		V
Current-Limit Setting Resistance	$R_{REFDI}$		6	18	36	k $\Omega$
REFDI Pin Short	$REFDI\_S$	Increasing current at REFDI pin		550		$\mu A$
		Decreasing current at REFDI pin		548		
<b>IC INPUTS (TYPE 1, 2, 3)</b>						
Negative Input Current		$-40V < V_{IN\_} < 0V$ , $V_{IN\_}$ at the pin		100		$\mu A$
LED On-State Current	$I_{LED\_ON}$	$R_{REFDI} = 18k\Omega$ , $V_{LED} = 3V$	1.5			mA
DI Leakage, Current Sources Disabled	$I_{DI\_LEAK}$	$V_{IN\_} = 28V$ , REFDI floating	40	58	84	$\mu A$
Input Threshold Low-to-High	$V_{THP+}$	$V_{IN\_}$ at the pin, $R_{REFDI} = 18k\Omega$	5.2	5.6	6	V
Input Threshold High-to-Low	$V_{THP-}$	$V_{IN\_}$ at the pin, $R_{REFDI} = 18k\Omega$	4.4	4.7	5.0	V
Input Threshold Hysteresis	$V_{INPHYST}$	$V_{IN\_}$ at the pin, $R_{REFDI} = 18k\Omega$		0.9		V
<b>FIELD INPUTS TYPE 1, 3: (EXTERNAL SERIES RESISOR <math>R_{IN} = 1.5k\Omega</math>, <math>R_{REFDI} = 18k\Omega</math>)</b>						
Field Input Current Limit	$I_{INLIM}$	$6V (V_{THP+} MAX) \leq V_{IN\_}$ at the pin $\leq 28V$ , LED on, $R_{REFDI} = 18k\Omega$	2.05	2.39	2.75	mA
Field Input Threshold Low-to-High	$V_{INF+}$	$R_{REFDI} = 18k\Omega$ , 1.5k $\Omega$ external series resistor			10	V
Field Input Threshold High-to-Low	$V_{INF-}$	$R_{REFDI} = 18k\Omega$ , 1.5k $\Omega$ external series resistor	8			V
<b>FIELD INPUTS TYPE 2: (EXTERNAL SERIES RESISOR <math>R_{IN} = 470\Omega</math>, <math>R_{REFDI} = 6k\Omega</math>)</b>						
Field Input Current Limit	$I_{INLIM}$	$6V (V_{THP+} MAX) \leq V_{IN\_}$ at the pin $\leq 28V$ , LED on, $R_{REFDI} = 6k\Omega$	6	7	8.9	mA
Field Input Threshold Low-to-High	$V_{INF+}$	$R_{REFDI} = 6k\Omega$ , 470 $\Omega$ external series resistor			10.2	V
Field Input Threshold High-to-Low	$V_{INF-}$	$R_{REFDI} = 6k\Omega$ , 470 $\Omega$ external series resistor	7.2			V
<b>LOGIC INPUT (RDYEN)</b>						
Input Logic-High Voltage	$V_{IH}$		0.7 x $V_{DD3}$			V
Input Logic-Low Voltage	$V_{IL}$				0.3 x $V_{DD3}$	V
Input Pulldown Resistance	$R_{PD}$			199		k $\Omega$
<b>LOGIC OUTPUTS (<math>OP_-</math>, READY)</b>						

( $V_{DD3} = +3.0V$  to  $+5.5V$ ,  $C_L$  on  $OP\_ = 15pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD24} = +24V$ , field inputs  $V_{IN\_} = +24V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic-High Voltage	$V_{OH}$	$I_{OUT} = -4mA$ Source	$V_{DD3} - 0.4$			V
Output Logic-Low Voltage	$V_{OL}$	$I_{OUT} = 4mA$ Sink			0.4	V
Output Leakage Current	$I_{OL}$		-1		+1	$\mu A$
<b>DYNAMIC CHARACTERISTICS (OP_)</b>						
Propagation Delay Low-to-High (Figure 1)	$t_{PDLH}$	$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 11V$ (Note 2)		85	280	ns
		$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 36V$ (Note 2)		85	280	
Propagation Delay High-to-Low (Figure 1)	$t_{PDHL}$	$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 11V$ (Note 2)		150	235	ns
		$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 36V$ (Note 2)		150	235	
Propagation Delay Skew Channel-to-Channel (Figure 1)	$t_{PDSKEW\_CH}$	$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 11V$ (Note 2)	-20		+20	ns
		$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 36V$ (Note 2)	-20		+20	
Propagation Delay Skew Part-to-Part (Figure 1)	$t_{PDSKEW\_PT}$	$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 11V$ , all conditions are the same between parts (Note 2)	-200		+200	ns
		$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 36V$ , all conditions are the same between parts (Note 2)	-200		+200	
Detectable Pulse Width (Figure 1)	$t_{PW}$	$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 11V$ (Note 2)			200	ns
		$IN\_ to OP\_ , R_{IN} = 470\Omega , V_{INF\_} = 36V$ (Note 2)			200	
Pulse Width Distortion	PWD	$ t_{PDLH} - t_{PDHL}  , V_{INF\_} = 11V$ (Note 2)	0	65	180	ns
		$ t_{PDLH} - t_{PDHL}  , V_{INF\_} = 36V$ (Note 2)	0	65	180	

**Note 1:** All parts are production tested at  $T_A = +25^\circ C$ . Specifications over temperature are guaranteed by design.

**Note 2:**  $V_{INF\_}$  is the voltage measured at the field input;  $V_{IN\_}$  is the voltage measured at the pin.

EMC Characteristics

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Surge		IEC 61000-4-5, 1.2/50µs pulse, 42Ω/0.5µF, minimum 470Ω resistor in series with IN1–IN4	Line-to-Line		±2		kV
			Line-to-Ground		±2		
		V <sub>DD24</sub>			±1		
ESD		All pins	Human Body Model		±2		kV
			IEC 61000-4-2, minimum 470Ω resistor in series with IN1–IN4	Contact Discharge		±8	
			Air-Gap Discharge		±15		

Timing Diagram

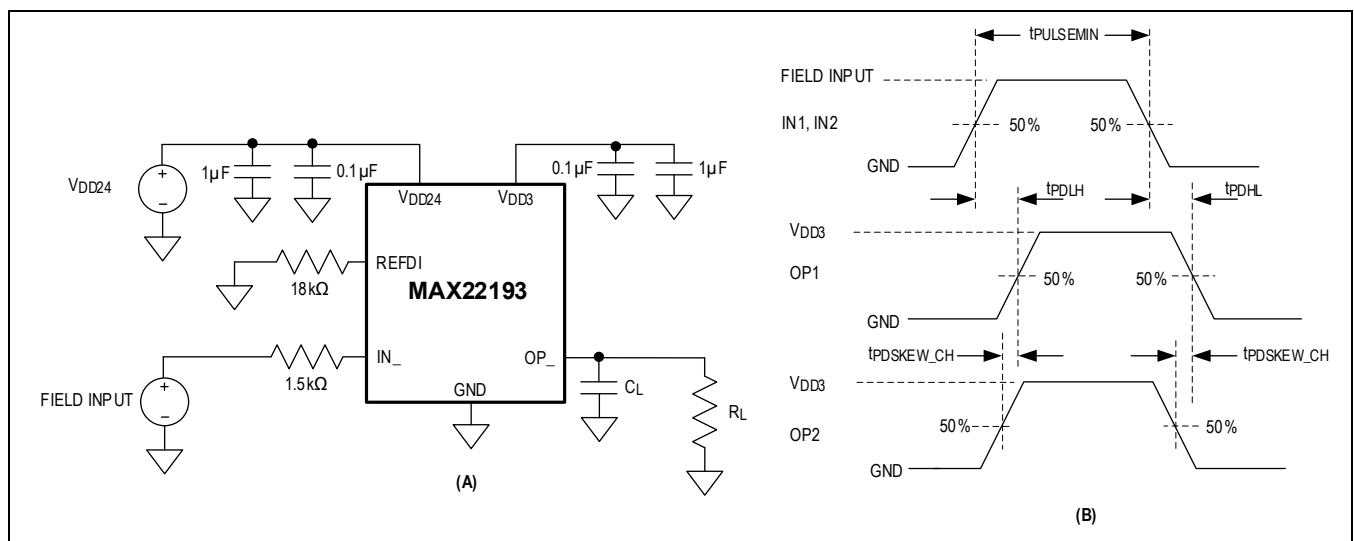
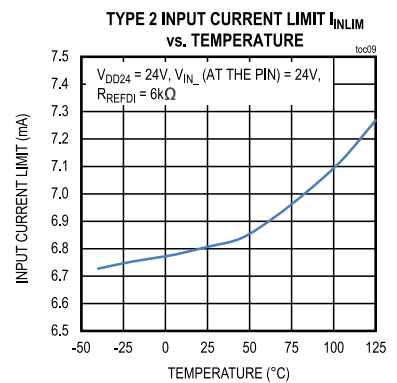
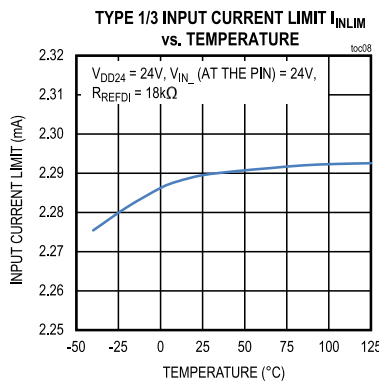
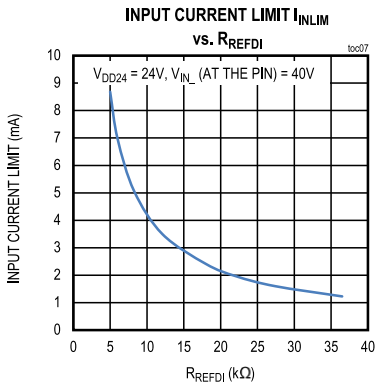
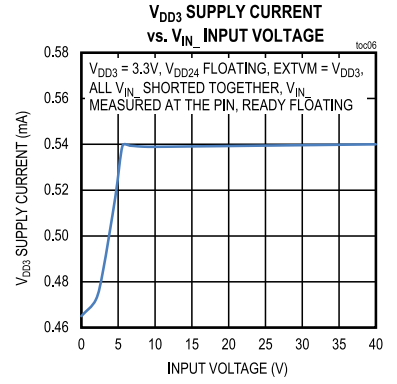
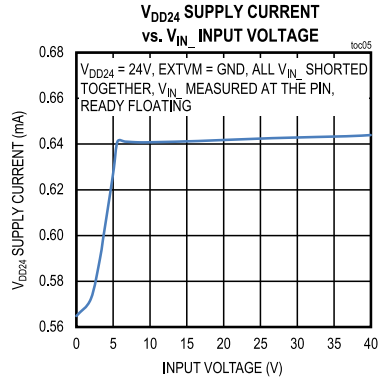
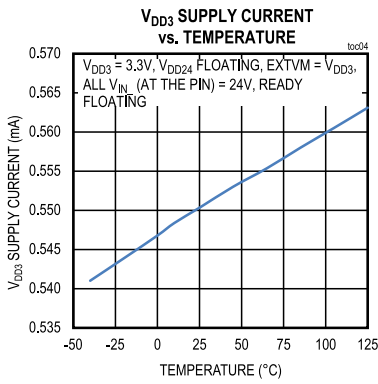
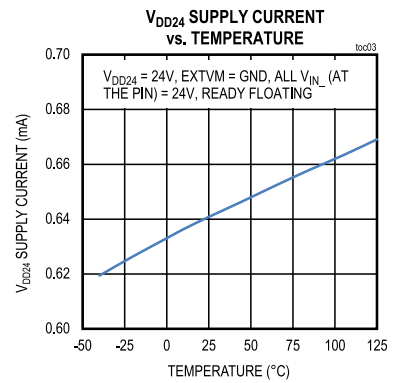
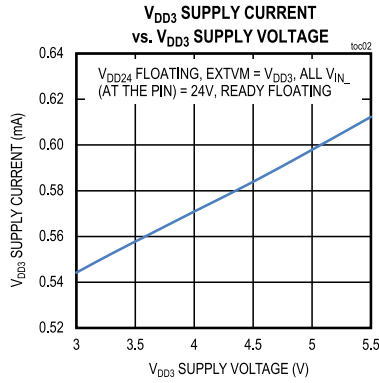
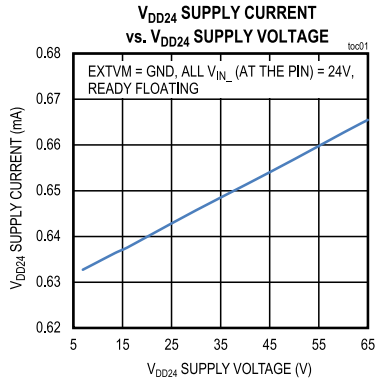


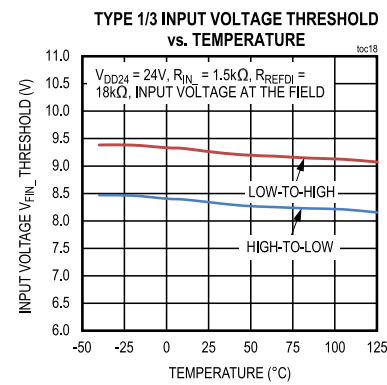
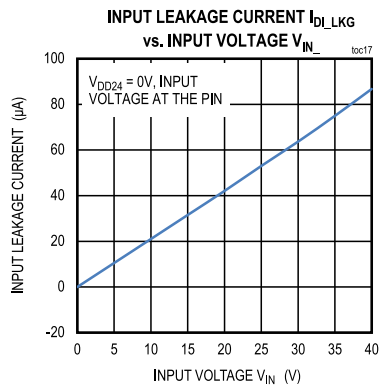
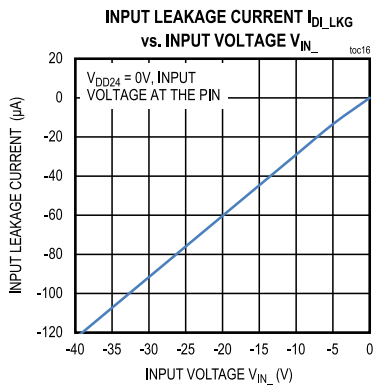
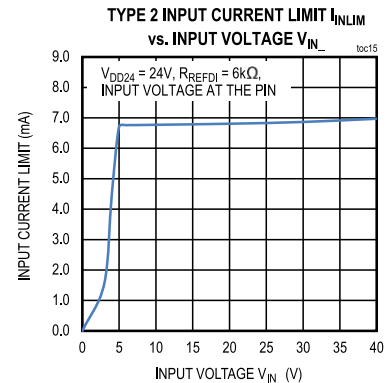
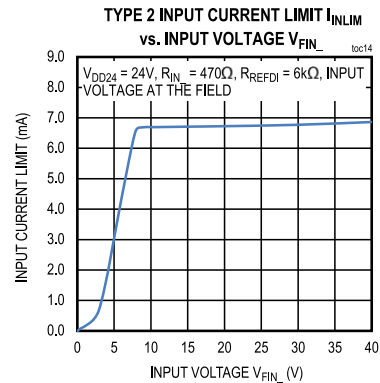
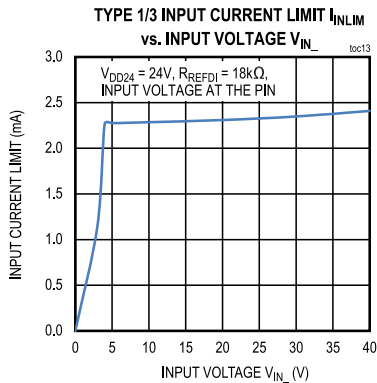
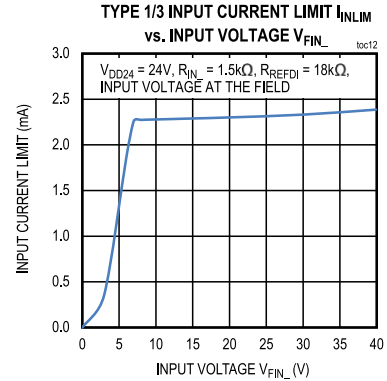
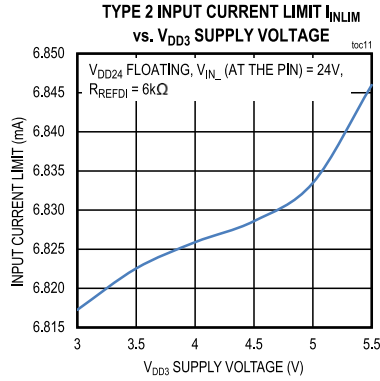
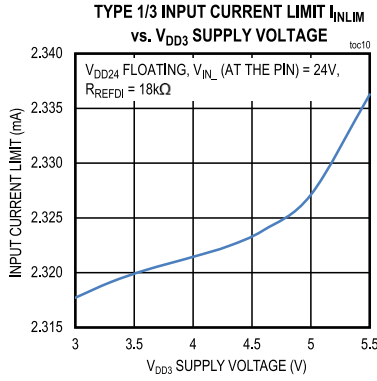
Figure 1. Test Circuit (A) and Timing Diagram (B)

Typical Operating Characteristics

( $V_{DD24} = 24V$ ,  $V_{DD3} = 3.3V$ ,  $T_A = +25^\circ C$ ,  $R_{REFDI} = 18k\Omega$  or  $6k\Omega$ ,  $R_{IN} = 1.5k$  or  $470\Omega$ , unless otherwise noted.)

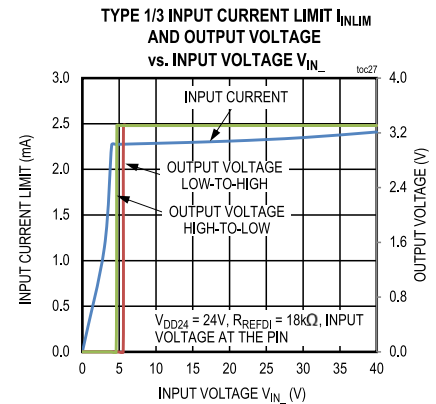
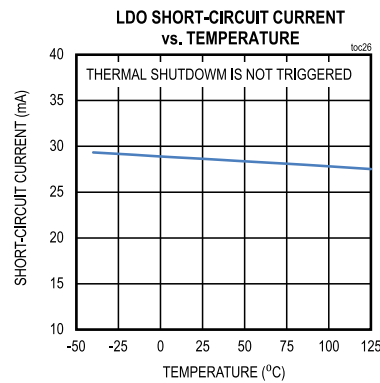
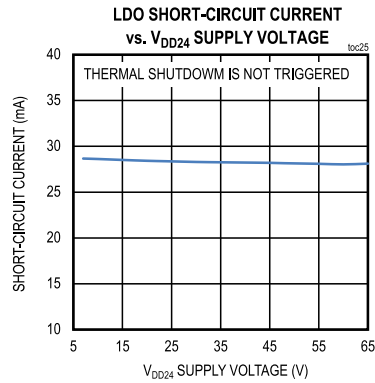
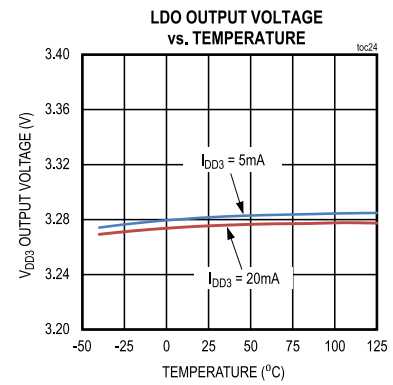
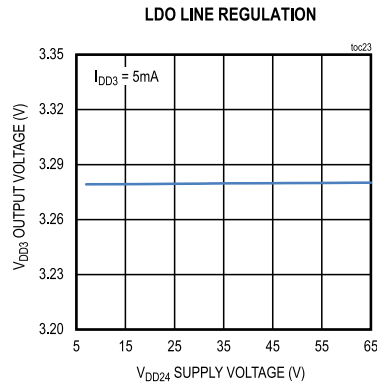
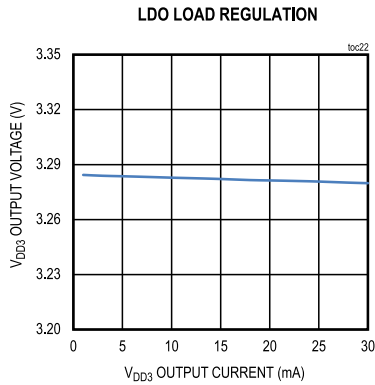
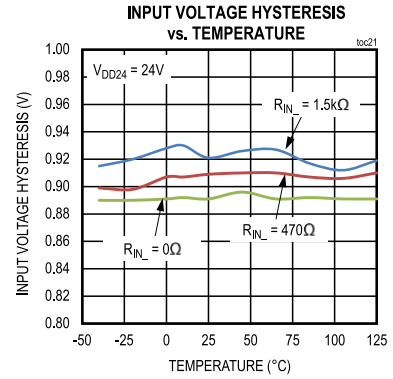
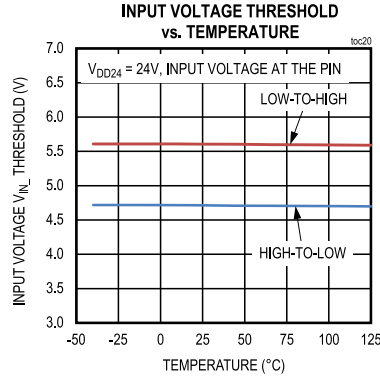
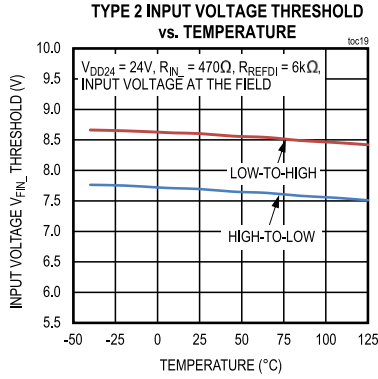


( $V_{DD24} = 24V$ ,  $V_{DD3} = 3.3V$ ,  $T_A = +25^\circ C$ ,  $R_{REFDI} = 18k\Omega$  or  $6k\Omega$ ,  $R_{IN} = 1.5k$  or  $470\Omega$ , unless otherwise noted.)

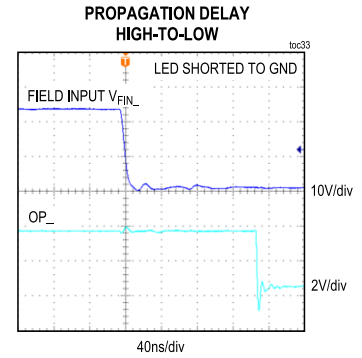
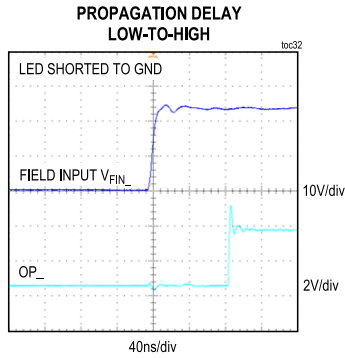
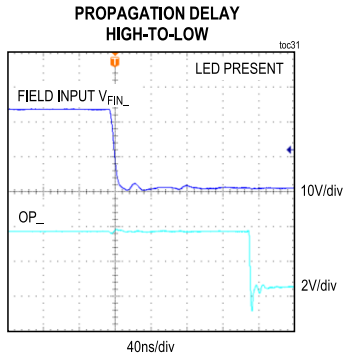
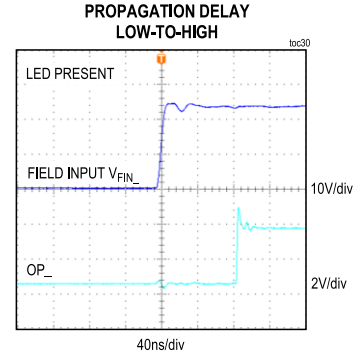
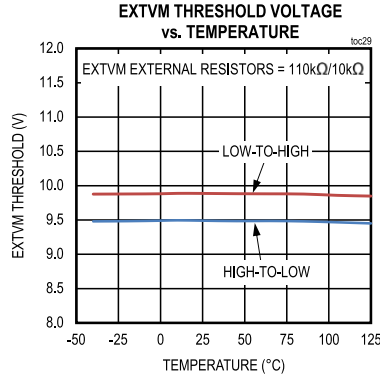
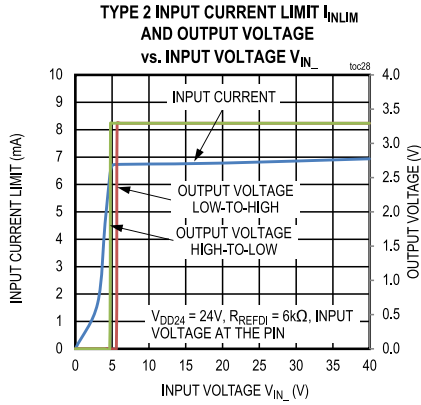




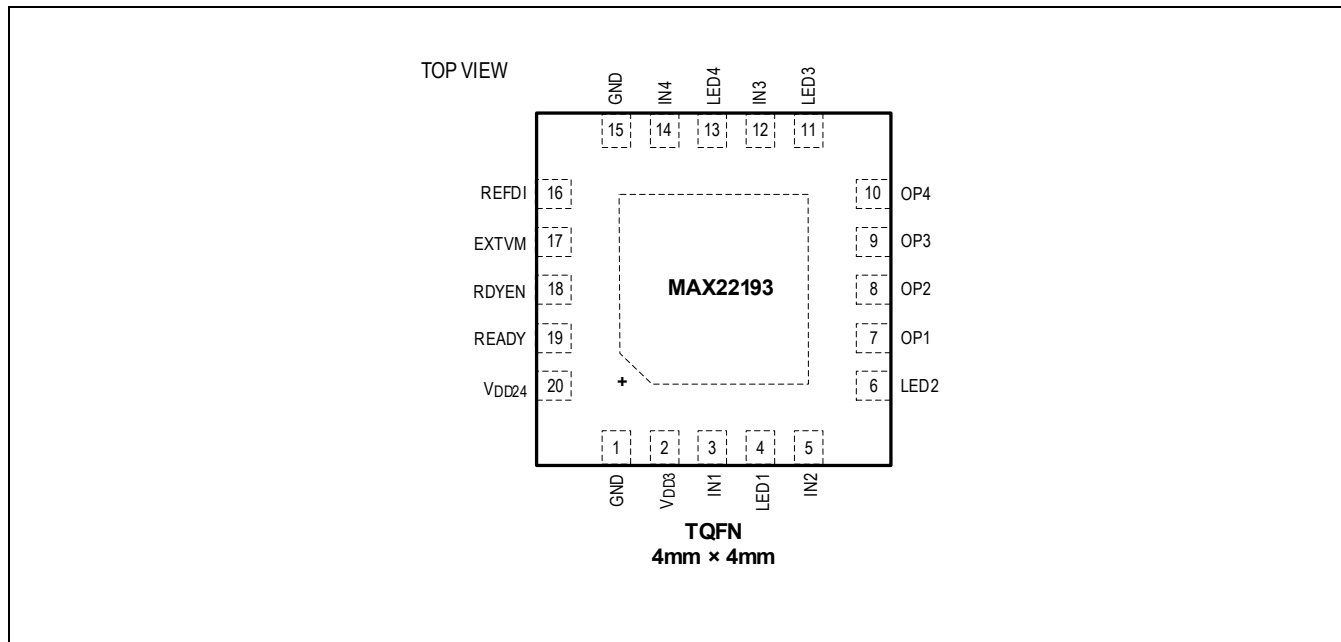
( $V_{DD24} = 24V$ ,  $V_{DD3} = 3.3V$ ,  $T_A = +25^\circ C$ ,  $R_{REFDI} = 18k\Omega$  or  $6k\Omega$ ,  $R_{IN} = 1.5k$  or  $470\Omega$ , unless otherwise noted.)



( $V_{DD24} = 24V$ ,  $V_{DD3} = 3.3V$ ,  $T_A = +25^\circ C$ ,  $R_{REFDI} = 18k\Omega$  or  $6k\Omega$ ,  $R_{IN} = 1.5k$  or  $470\Omega$ , unless otherwise noted.)



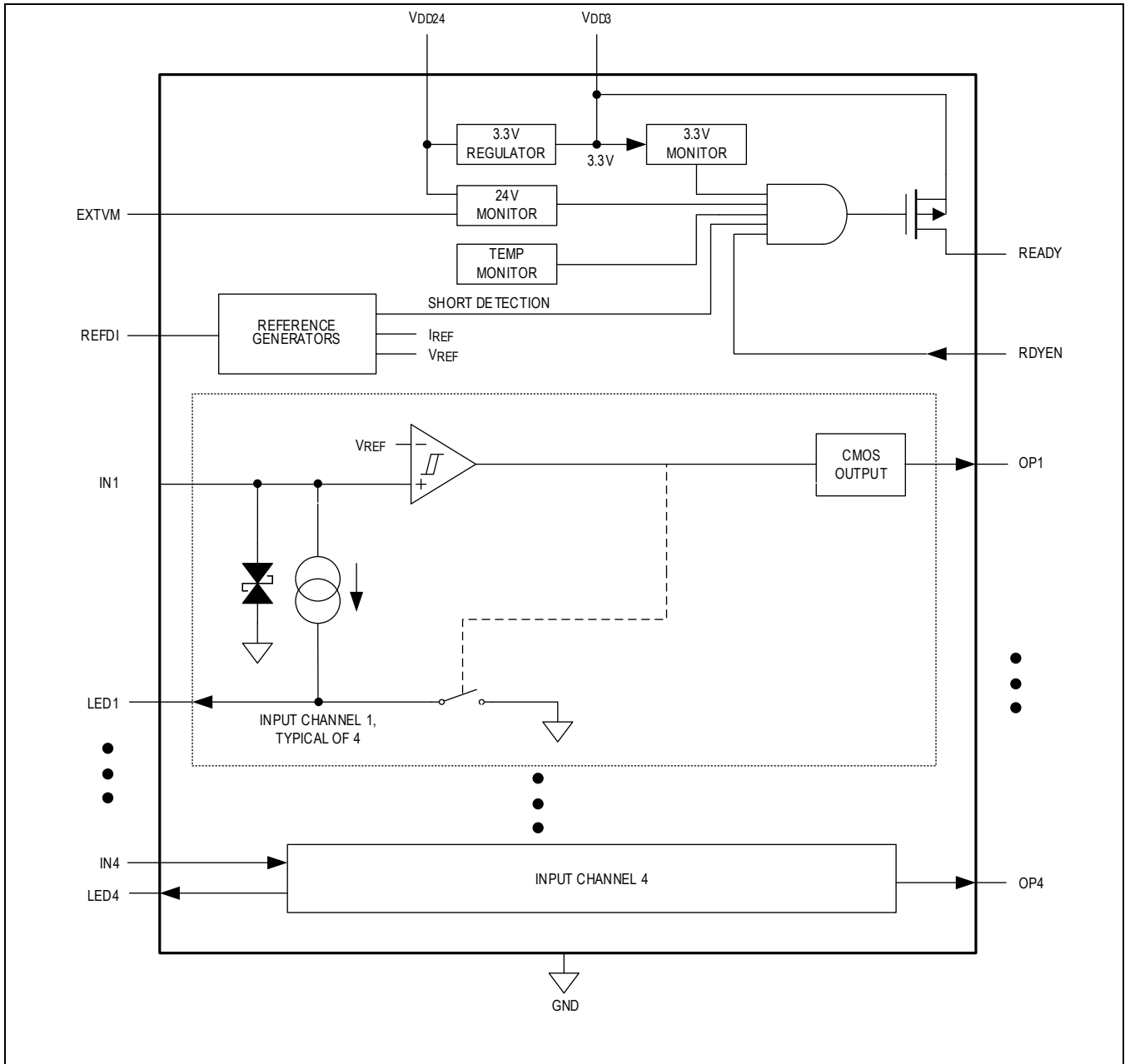
Pin Configuration



## Pin Descriptions

PIN	NAME	FUNCTION
<b>POWER SUPPLY</b>		
20	V <sub>DD24</sub>	24V Field Supply. Bypass to GND with 0.1μF capacitor in parallel with 1μF capacitor. If powering V <sub>DD3</sub> from an external supply, leave V <sub>DD24</sub> floating.
2	V <sub>DD3</sub>	3.3V output from integrated LDO when powered from V <sub>DD24</sub> , or 3.0 - 5.5V supply input when V <sub>DD24</sub> not driven. Bypass to GND with 0.1μF capacitor in parallel with 1μF capacitor. If powering V <sub>DD3</sub> from an external supply, leave V <sub>DD24</sub> floating. V <sub>DD3</sub> output is turned off during thermal shutdown.
1, 15	GND	Ground Return for All Signals and the Power Supplies.
EP	-	Exposed Pad. Connect to GND. Solder entire exposed pad area to ground plane with multiple vias for best thermal performance.
<b>ANALOG PINS</b>		
17	EXTVM	Connect EXTVM to GND to use internal thresholds (14V, typ) for V <sub>DD24</sub> voltage monitoring. Connect EXTVM to external resistive divider to set external thresholds for V <sub>DD24</sub> voltage monitoring. Connect EXTVM to V <sub>DD3</sub> to disable V <sub>DD24</sub> voltage monitoring at READY pin if the device is powered by V <sub>DD3</sub> .
16	REFDI	Digital Input Current Limiting Reference Resistor. For 24V type 1/3 inputs, place an 18kΩ resistor to GND. For type 2 inputs, place a 6kΩ resistor.
<b>FIELD INPUT PINS</b>		
3, 5, 12, 14	IN1 to IN4, respectively	Field Inputs. For 24V type 1/3 inputs, place a 1.5kΩ resistor between the field input and the IN_ pin. For type 2 inputs, place a 470Ω resistor. Capacitors for filtering should not be connected to the IN_ pins. See the <a href="#">Surge Protection of Field Inputs section</a> for more information.
4, 6, 11, 13	LED1 to LED4, respectively	Energiless LED Driver Outputs. Connect to GND if LEDs are not used.
<b>LOGIC PINS</b>		
7, 8, 9, 10	OP1 to OP4, respectively	Logic Outputs. Indicate the state (high or low) of IN1 to IN4, respectively. High level is V <sub>DD3</sub> . Low level is GND. If thermal shutdown is triggered, OP1 to OP4 are high-impedance.
18	RDYEN	Ready Enable. Has a weak internal pulldown. Assert high to enable the READY output. Cascade the READY signal of multiple devices through a single isolator or a microcontroller input pin by connecting the READY output of each device to the RDYEN input of the next device in the chain. READY from the last device in the chain drives the isolator input, or the microcontroller GPI.
19	READY	Open-drain Output. Connect a pulldown resistor between READY and GND pin. Assert high to indicate the device is functional and the outputs are valid. The following conditions must be met for READY to assert high: <ol style="list-style-type: none"> <li>V<sub>DD3</sub> is above the UVLO threshold.</li> <li>REFDI is not shorted to GND.</li> <li>MAX22193 is not in thermal shutdown.</li> <li>RDYEN is high.</li> <li>V<sub>DD24</sub> is valid if the device is powered by V<sub>DD24</sub> and EXTVM is not connected to V<sub>DD3</sub>.</li> </ol>

Functional Diagram



### Detailed Description

The MAX22193 senses the state (on, high or off, low) of each input (IN1 to IN4). The voltages at the IN\_ input pins are compared against internal references to determine whether the sensor is on (logic 1) or off (logic 0). Placing an 18kΩ current-setting resistor between REF<sub>DI</sub> and GND, and a 1.5kΩ resistor in series with each input ensures that the current at the on and off trip points as well as the voltage at the trip points satisfy the requirements of IEC 61131-2 for Type 1/3 inputs ([Figure 2](#)). The current sunk by each input pin rises linearly with input voltage until the level set by the current-limiter is reached; any voltage increase beyond this point does not increase the input current. Limiting the input current ensures compliance with IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs.

The current-setting resistor R<sub>REFDI</sub> can be calculated using this equation:

$$R_{REFDI} \text{ (k}\Omega, \text{typ)} = 42 / (I_{INLIM} \text{ (mA)} - V_{IN} / 517 \text{ (V/k}\Omega))$$

where V<sub>IN</sub> is 5.6V at the input pin during production test for the typical value of Type 1/3, and Type 2 current limits.

### RDYEN and READY Monitor

The READY output is used to signal a logic-side controller that the field-side circuit is working. This allows the controller to distinguish from a valid reading of four low inputs or an invalid reading caused by a field-side fault such as loss of power. The READY output is asserted high when the following five conditions are met: the UVLO voltage threshold for V<sub>DD3</sub> is exceeded; the V<sub>DD24</sub> field supply requirement is met as set by internal thresholds or EXTVM external thresholds if enabled; the device is not in thermal shutdown; the current through the REF<sub>DI</sub> pin is in a normal range; and the RDYEN is high.

Ready Enable RDYEN is used to cascade other READY signals through to a single digital isolation channel or a microcontroller GPI pin. Connect the READY output of one device to the RDYEN input of the next device in the chain. Connect the final READY output to a digital isolator or a microcontroller GPI pin. All READY signals must be high for the final READY signal to go high. READY is an open-drain output, driven to V<sub>DD3</sub> for a high output and set at high-impedance for a low output. Refer to [Typical Application Circuits](#) section for details.

Outputs OP1 to OP4 are high-impedance only when thermal shutdown is triggered.

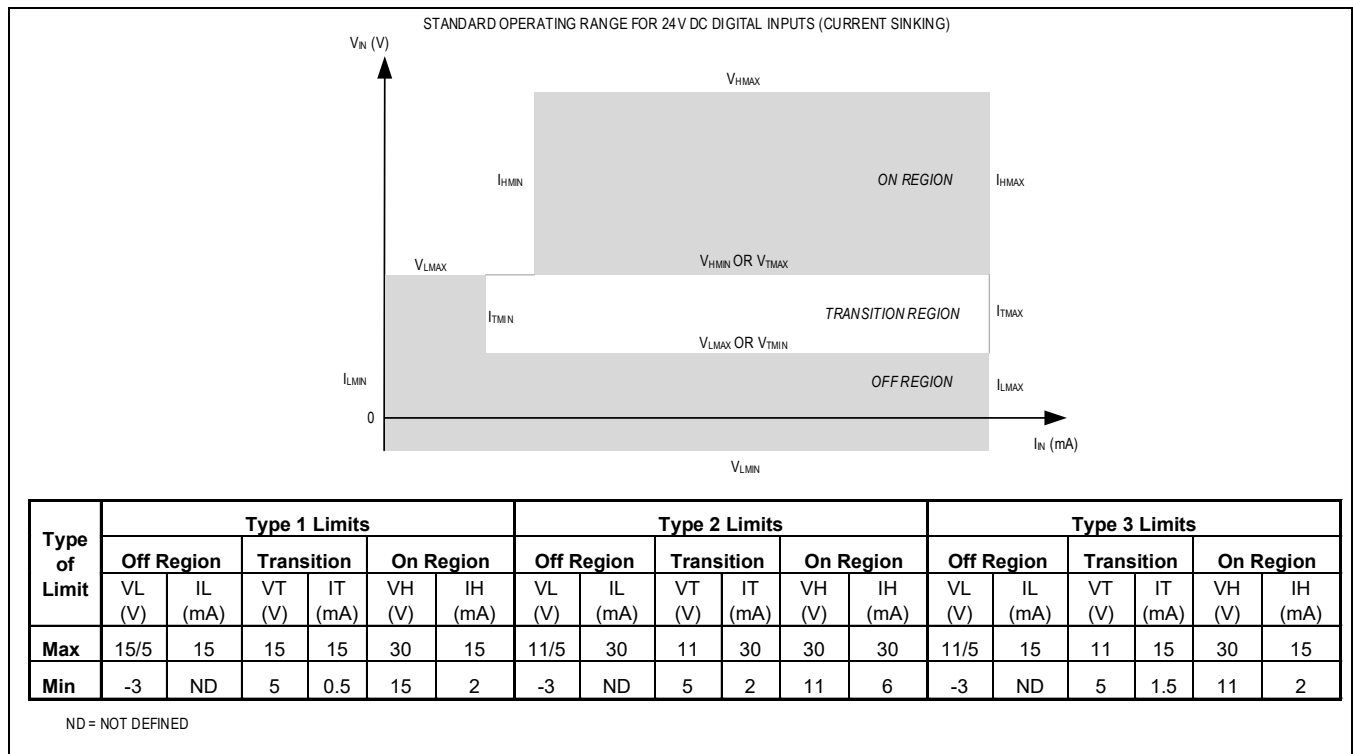


Figure 2. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24VDC Digital Inputs

### External V<sub>DD24</sub> Voltage Monitor

The EXTVM input controls how the V<sub>DD24</sub> field supply affects the READY output. When EXTVM is connected to V<sub>DD3</sub>, the status of the V<sub>DD24</sub> field supply becomes a don't-care in the decision to assert READY. This is useful when the MAX22193 is being powered directly from a 3.3V supply on V<sub>DD3</sub> and V<sub>DD24</sub> is not in use. When EXTVM is connected to GND, the V<sub>DD24</sub> must be above the nominal 14V threshold before READY asserted high. To use a user-defined V<sub>DD24</sub> supply voltage threshold, use an external resistive divider to apply an analog voltage directly to EXTVM. The voltage at EXTVM must be greater than the threshold, 0.81V (V<sub>24TH\_OFF\_ON</sub>) nominal, before READY asserted high. [Figure 3](#) shows an example of the V<sub>DD24</sub> being monitored with the use of external resistive divider to set a nominal threshold before READY asserted high. Use the following equation to determine the threshold:

$$V_{DD24} = V_{REF} \times (1 + (R2/R1))$$

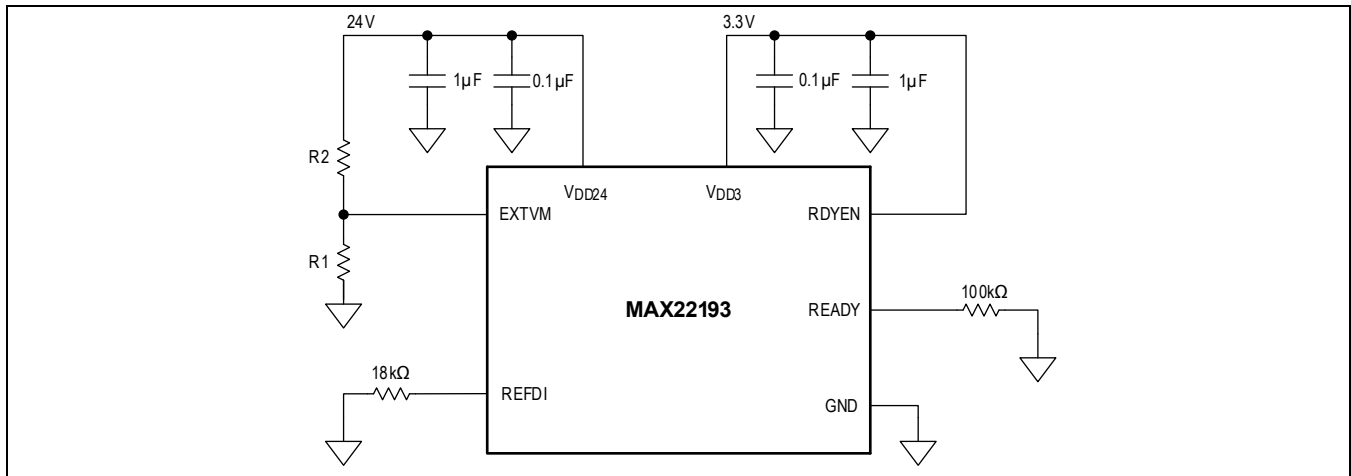


Figure 3. User-Defined V<sub>DD24</sub> Threshold Set by EXTVM and External Resistive Divider

### Short Detection at REFDI Pin

Short detection at REFDI pin is implemented by monitoring the current set by the resistor at the REFDI pin. When more than 550µA (typ) current is detected, meaning a short at REFDI, the 2mA minimum input current is not guaranteed; field input low-to-high and high-to-low thresholds are changed, and the READY pin is not asserted.

### Energiless LED Drivers

When IN<sub>n</sub> is determined to be on, its input current is diverted to the LED<sub>n</sub> pin and flows from that pin to GND. Placing an LED between LED<sub>n</sub> and GND provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LED<sub>n</sub> to GND.

### Type 2 Sensor Inputs

Each channel of the MAX22193 supports the higher current of Type 2 inputs (6mA, min) and the associated power dissipation. The current of the input channel is set to a nominal 7mA by placing a 6kΩ resistor from REFDI to GND. The proper voltage drop across the input resistor is maintained by reducing the resistance from 1.5kΩ to 470Ω ([Figure 4](#)).

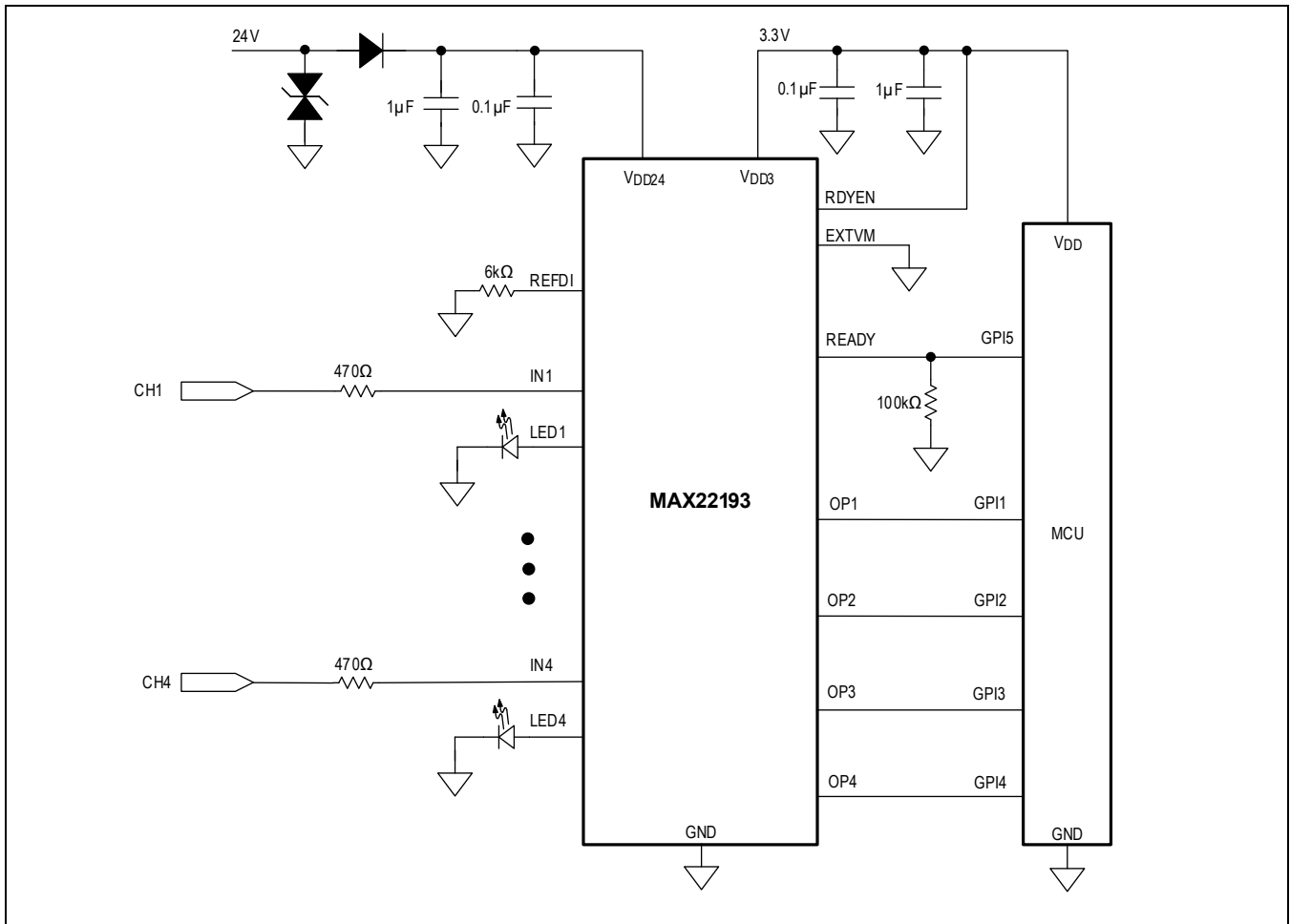


Figure 4. Implementing Type 2 Digital Inputs with MAX22193

**Thermal Considerations**

The MAX22193 will operate at an ambient temperature of 125°C on a properly designed multilayer PC board. Operating at higher voltages, or with heavy output loads such as optical isolators will increase power dissipation and reduce the maximum allowable operating temperature. See [Package Information](#) and [Absolute Maximum Ratings](#) for safety operation temperature and maximum power dissipation.

The MAX22193 is in thermal shutdown when the thermal shutdown temperature threshold is exceeded. During thermal shutdown, the internal voltage regulator, input channels, REFDI circuitry are all turned off, and outputs OP1 to OP4 are high-impedance.



## Applications Information

### Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass  $V_{DD24}$  and  $V_{DD3}$  with a  $0.1\mu\text{F}$  low-ESR ceramic capacitor in parallel with  $1\mu\text{F}$  ceramic capacitor to GND, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

### Powering MAX22193 with $V_{DD3}$

The MAX22193 can alternatively be powered using a 3.0–5.5V supply connected to the  $V_{DD3}$  pin. In this case, a 24V supply is no longer needed, the  $V_{DD24}$  pin must be left unconnected and EXTVM pin is connected to  $V_{DD3}$  to disable the  $V_{DD24}$  voltage monitoring, see [Typical Application Circuits](#) for details. This configuration has lower power consumption and heat dissipation since the on-chip LDO voltage regulator is disabled (the  $V_{DD24}$  undervoltage lockout is below threshold and automatically disables the LDO).

### PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias on the signals to make low-inductance paths.
- Have a solid ground plane underneath the entire exposed pad (EP) area with multiple thermal vias for best thermal performance.
- In order to achieve the highest EFT performance, it is recommended to have the GND plane around the REFDI traces, and isolate the REFDI traces from all input traces, especially IN4, as much as possible. For example, route input traces and REFDI traces on two different layers and have a GND plane on the inner layers in between.

### IEC 61131-2 EMC Requirements

The MAX22193 is required to operate reliably in harsh industrial environments. The device can meet the transient immunity requirements as specified in IEC 61131-2, including Electrostatic Discharge (ESD) per IEC 61000-4-2 and Surge Immunity per IEC 61000-4-5. Analog Devices' proprietary process technology provides robust input channels and field supply with internal ESD structures and high [Absolute Maximum Ratings](#), but external components are also required to absorb excessive energy from ESD and surge transients. The circuit with external components shown in [Figure 5](#) allows the device to meet and exceed the transient immunity requirements as specified in IEC 61131-2 and related IEC 61000-4-x standards. The system shown in [Figure 5](#), using the components shown in [Table 1](#), is designed to be robust against ESD and Surge specifications as listed in [Table 2](#). In all these tests, the part or DUT is soldered onto a properly designed application board (e.g., the MAX22193EVKIT#) with necessary external components.

**Table 1. Recommended Components for EMC Compliance**

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED
C1	$1\mu\text{F}$ , 100V ceramic capacitor	Required
C2	$0.1\mu\text{F}$ , 100V low-ESR ceramic capacitor	Required
C3	$1\mu\text{F}$ , 10V ceramic capacitor	Required
C4	$0.1\mu\text{F}$ , 10V low-ESR ceramic capacitor	Required
C5	$3.3\text{nF}$ , safety rated Y capacitor (2220)	Recommended
D1	Bi-directional TVS diode SMAJ33CA (42 $\Omega$ ) or SM30T39CAY (2 $\Omega$ )	Recommended
D2	Bi-directional TVS diode SMAJ33CA (42 $\Omega$ ) or SM30T39CAY (2 $\Omega$ )	Required to pair with R4
D3	Low forward voltage Schottky diode	Recommended
R1	Minimum 470 $\Omega$ , 2512, 2W pulse withstanding resistor	Required
R2	Minimum 470 $\Omega$ , 0603, 0.1W resistor	Required
All other resistors	0603, 0.1W resistors	Required
All LEDs	LEDs for visual input status indication	Recommended

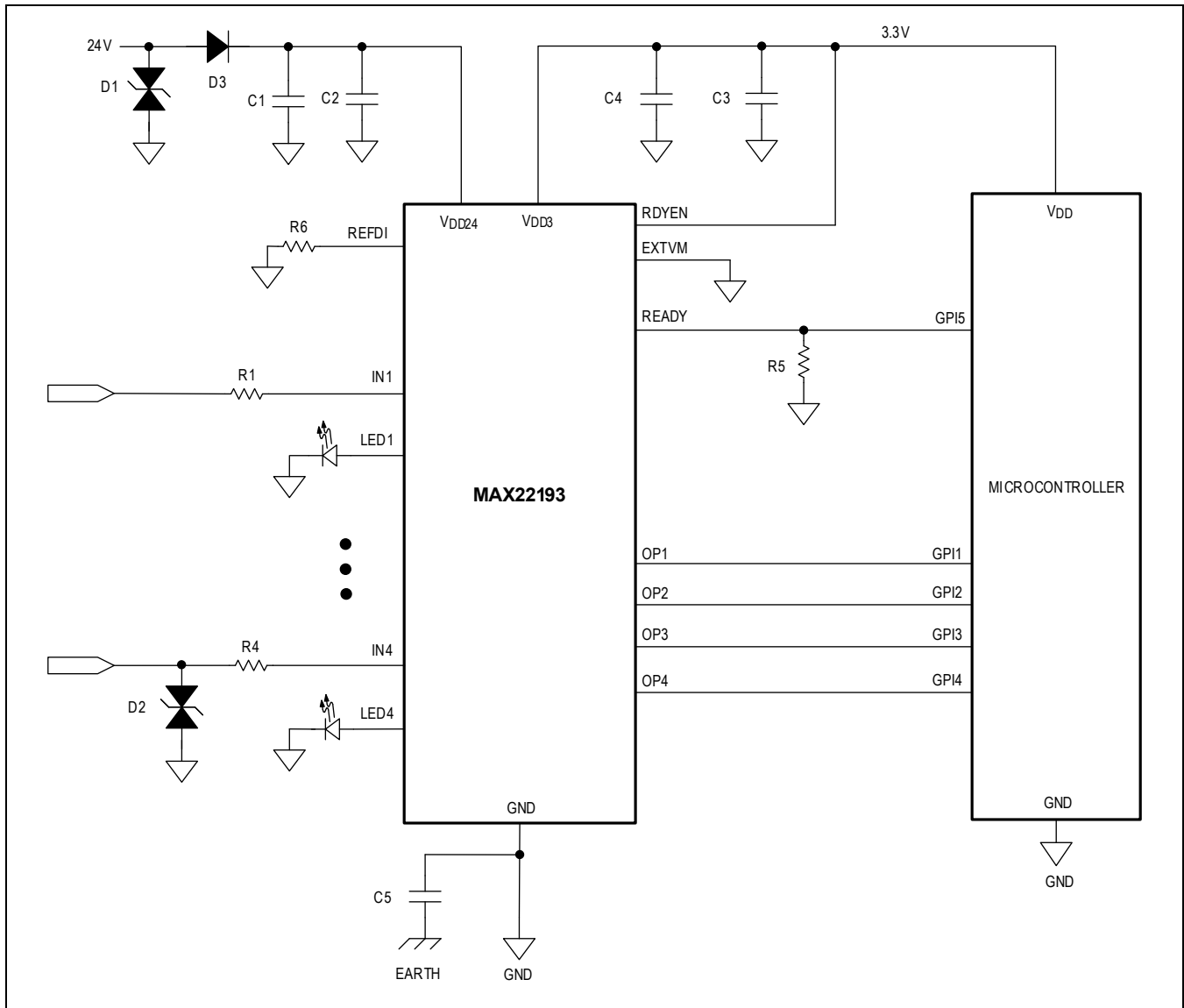


Figure 5. Typical EMC Protection Circuit for the MAX22193

### ESD Protection of Field Inputs

The input resistor limits the energy into the MAX22193 IN\_ pins and protects the internal ESD structure from excessive transient energy. An input series resistor is required and should be rated to withstand such ESD levels. The MAX22193 input channels can withstand up to  $\pm 8\text{kV}$  ESD contact discharge and  $\pm 15\text{kV}$  ESD air-gap discharge with an input series resistor of  $470\Omega$  or larger. The input resistor value shifts the field voltage switching threshold scaled by the input current; thus, it determines the input characteristics of the application. The package of the resistor should be large enough to prevent the arcing across the two resistor pads. Arcing depends on the ESD level applied to the field input and the application pollution degree.

### Surge Protection of Field Inputs

In order to protect the IN\_ pins against  $\pm 2\text{kV}/42\Omega$ ,  $1.2/50\mu\text{s}$  surges ([Figure 6](#) and [Figure 7](#)), two options exist. The first option is to use a series pulse-withstanding resistor as shown in the various application diagrams in the data sheet. The pulse resistor should support dissipation of the surge energy. For Type 1/3 digital inputs with  $1.5\text{k}\Omega$  series resistors, it is recommended to use CRCW-IF or CRCW-HP thick film resistor, or similar, to protect against up to  $\pm 2\text{kV}$  surges. For Type 2 digital inputs with  $470\Omega$  series resistors, it is recommended to use CRCW-IF or CRCW-HP thick film resistor, or similar,

to protect against up to  $\pm 1\text{kV}$  surge. Use the CMB0207 MELF resistor for  $\pm 2\text{kV}$  surge protections. Capacitors for filtering should not be connected to the IN\_ pins.

The second option, which can result in a smaller overall footprint, is to use a bidirectional TVS to GND at the field input with a low-power series resistor, greater or equal to  $470\Omega$ . The TVS must be able to absorb the surge energy and has the function of limiting the peak voltage so that the resistor only sees a low differential voltage. Suitable TVS with a small footprint are SMAJ33CA, offering protection against  $\pm 2\text{kV} / 42\Omega$  surges.

**Surge Protection of 24V Supply**

In order to protect the  $V_{DD24}$  pin against  $\pm 1\text{kV}/42\Omega$ ,  $1.2/50\mu\text{s}$  surges (Figure 6), an SMAJ33CA TVS can be applied to the  $V_{DD24}$  pin, along with a series Schottky diode for reverse current protection. To protect against  $\pm 1\text{kV}/2\Omega$ ,  $1.2\mu\text{s}/50\mu\text{s}$  surges, an SM30T39CAY TVS can be applied to the  $V_{DD24}$  pin.

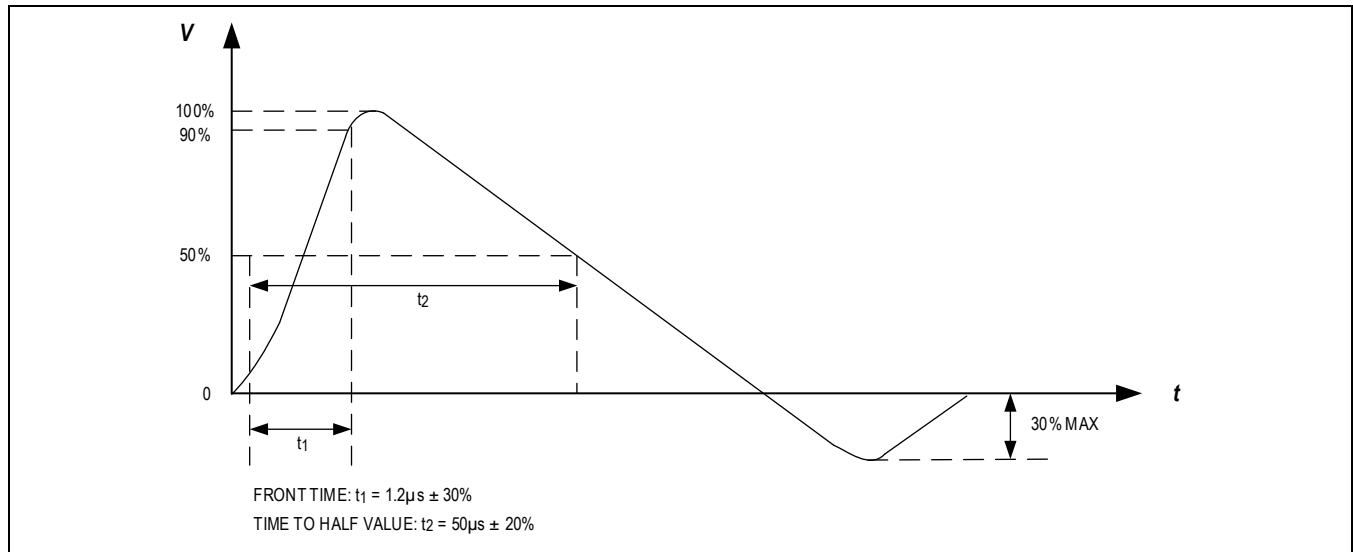


Figure 6. 1.2/50µs Surge Voltage Waveform

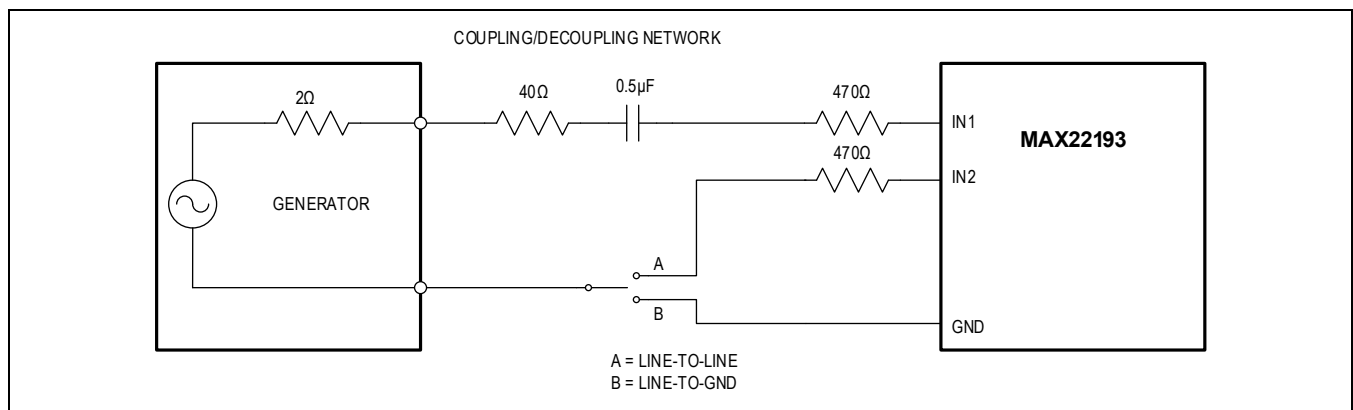
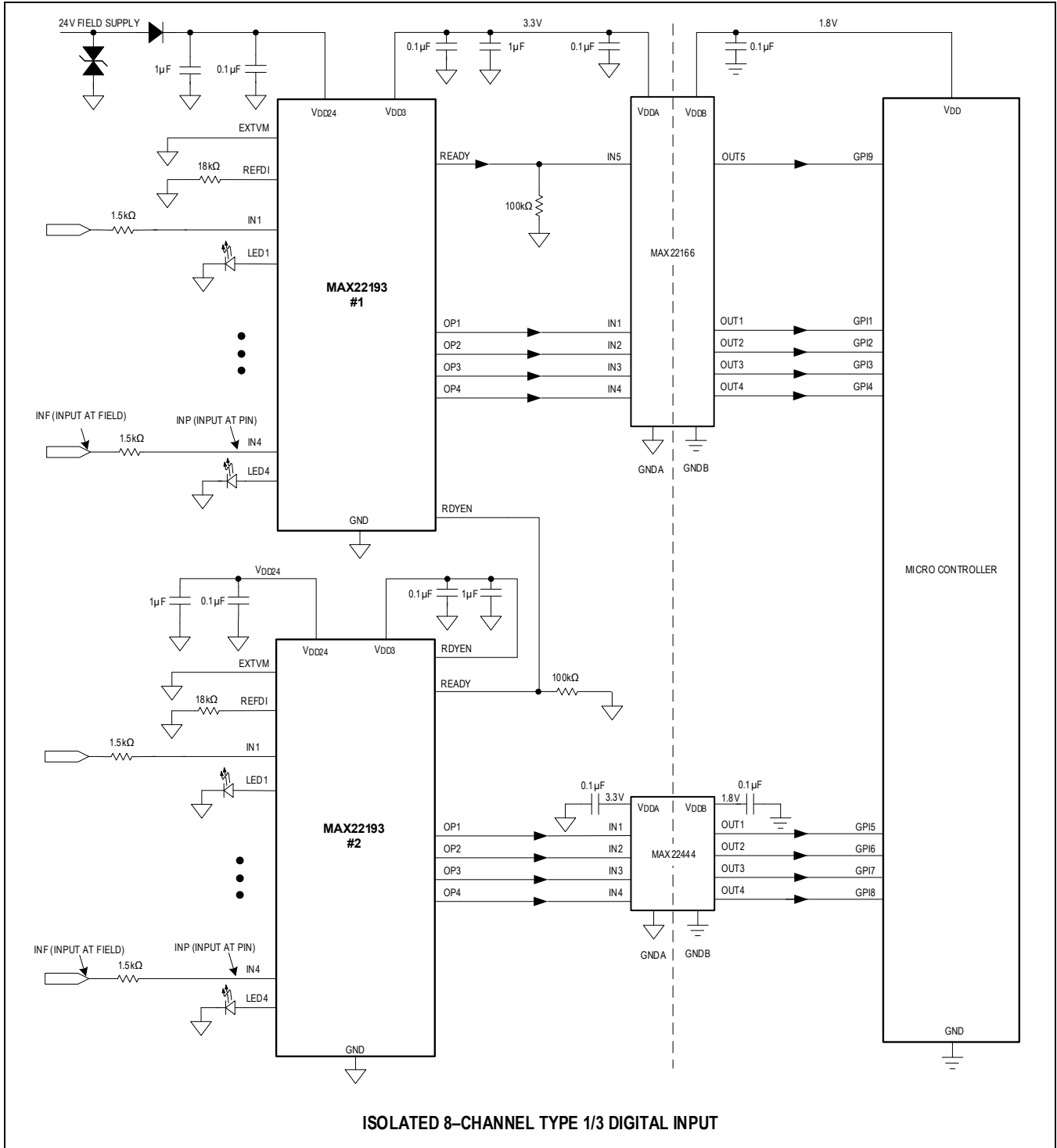


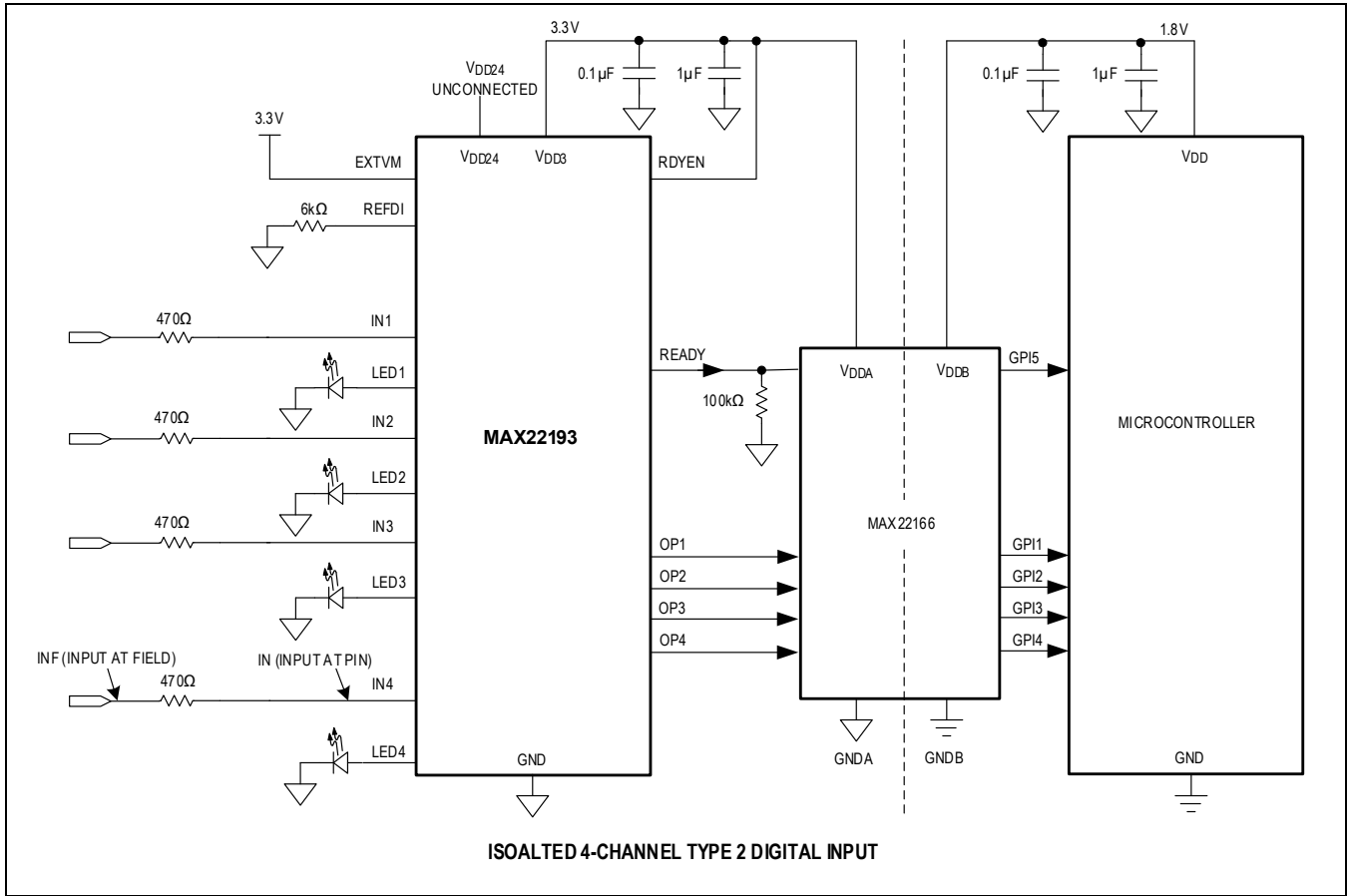
Figure 7. Surge Testing Method

**Table 2. Transient Immunity Test Results**

TEST		RESULT
IEC 61000-4-2 Electrostatic Discharge (ESD)	Contact ESD	$\pm 8\text{kV}$
	Air-Gap ESD	$\pm 15\text{kV}$
IEC 61000-4-5 Surge Immunity	Line-to-Ground	$\pm 2\text{kV}$
	Line-to-Line	$\pm 2\text{kV}$
	Power Supply	$\pm 1\text{kV}$

Typical Application Circuits





**Ordering Information**

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22193ATP+	-40°C to +125°C	20-TQFN
MAX22193ATP+T	-40°C to +125°C	20-TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and Reel.

**Chip Information**

PROCESS: BiCMOS

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	06/22	Release for Market Intro	—

