FEATURES

- **On-chip clock ÷4 and ÷8**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **2.5Gb/s data rate capability**
- **Differential clock and serial inputs**
- **V_{BB} output for single-ended use**
- **Asynchronous data synchronization**
- **Mode select to expand to 8 bits**
- **Internal 75kΩ input pull-down resistors**
- **Fully compatible with Motorola MC10E/100E445**
- **Available in 28-pin PLCC package**

PIN NAMES

Pin	Function
SINA, $\overline{SINA}$	Differential Serial Data Input A
SINB, $\overline{SINB}$	Differential Serial Data Input B
SEL	Serial Input Select Pin
SOUT, $\overline{SOUT}$	Differential Serial Data Output
Q0–Q3	Parallel Data Outputs
CLK, $\overline{CLK}$	Differential Clock Inputs
CL/4, $\overline{CL/4}$	Differential ÷4 Clock Output
CL/8, $\overline{CL/8}$	Differential ÷8 Clock Output
MODE	Conversion Mode 4-bit/8-bit
SYNC	Conversion Synchronizing Input
RESET	Input, Resets the Counters
V_{CCO}	V_{CC} to Output

DESCRIPTION

The SY10/100E445 are integrated 4-bit serial-to-parallel data converters. The devices are designed to operate for NRZ data rates of up to 2.5Gb/s. The chip generates a divide-by-4 and a divide-by-8 clock for both 4-bit conversion and a two-chip 8-bit conversion function. The conversion sequence was chosen to convert the first serial bit to Q_0, the second to Q_1, etc.

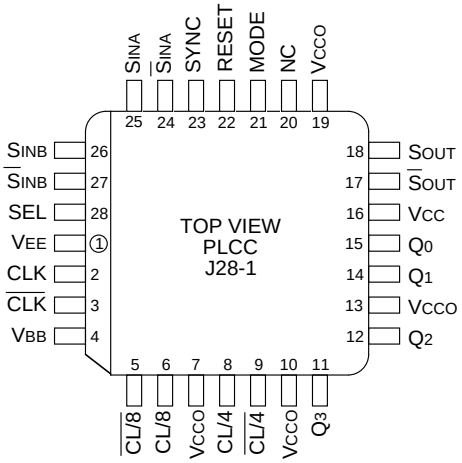
Two selectable serial inputs provide a loopback capability for testing purposes when the device is used in conjunction with the E446 parallel-to-serial converter.

The start bit for conversion can be moved using the SYNC input. A single pulse, applied asynchronously for at least two input clock cycles, shifts the start bit for conversion from Q_n to Q_{n-1} by one bit. For each additional shift required, an additional pulse must be applied to the SYNC input. Asserting the SYNC input will force the internal clock dividers to "swallow" a clock pulse, effectively shifting a bit from the Q_n to the Q_{n-1} output (see Timing Diagram B).

The MODE input is used to select the conversion mode of the device. With the MODE input LOW (or open) the device will function as a 4-bit converter. When the mode input is driven HIGH, the data on the output will change on every eighth clock cycle, thus allowing for an 8-bit conversion scheme using two E445s. When cascaded in an 8-bit conversion scheme, the devices will not operate at the 2.5Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E445.

For lower data rate applications, a V_{BB} reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz, differential input signals are recommended. For single-ended inputs, the V_{BB} pin is tied to the inverting differential input and bypassed via a 0.01µF capacitor. The V_{BB} provides the switching reference for the input differential amplifier. The V_{BB} can also be used to AC couple an input signal.

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

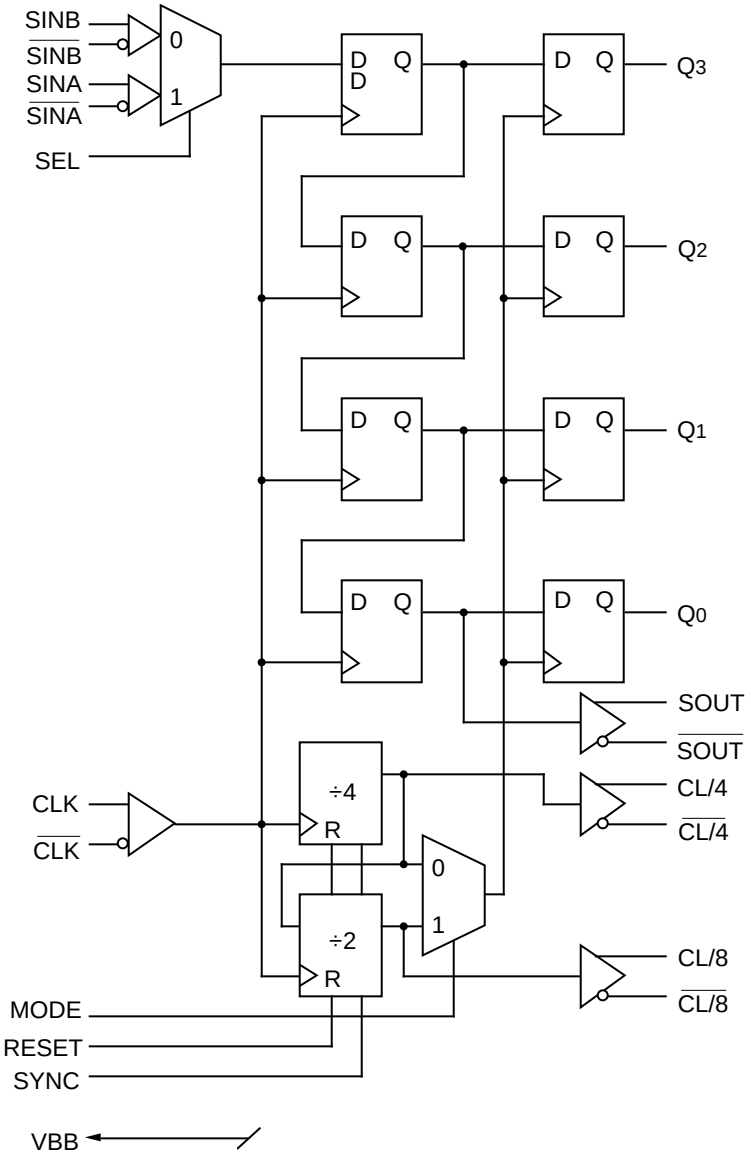
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E445JC	J28-1	Commercial	SY10E445JC	Sn-Pb
SY10E445JCTR[2]	J28-1	Commercial	SY10E445JC	Sn-Pb
SY100E445JC	J28-1	Commercial	SY100E445JC	Sn-Pb
SY100E445JCTR[2]	J28-1	Commercial	SY100E445JC	Sn-Pb
SY10E445JZ[3]	J28-1	Commercial	SY10E445JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E445JZTR[2, 3]	J28-1	Commercial	SY10E445JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E445JZ[3]	J28-1	Commercial	SY100E445JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E445JZTR[2, 3]	J28-1	Commercial	SY100E445JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



TRUTH TABLES

Mode	Conversion
L	4-Bit
H	8-Bit

SEL	Serial Input
H	A
L	B

DC CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
V_{OH}	Output HIGH Voltage										V	
	(S_{OUT} only) 10E	–1020	—	–790	–980	—	–760	–910	—	–670		1
	(S_{OUT} only) 100E	–1025	—	–830	–1025	—	–830	–1025	—	–830		1
V_{BB}	Output Reference Voltage										V	
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{EE}	Power Supply Current										mA	—
	10E	—	154	185	—	154	185	—	154	185		
	100E	—	154	185	—	154	185	—	177	212		

Note:

1. The maximum VOH limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E VOH levels.

AC CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Conversion Frequency	2.0	—	—	2.0	—	—	2.0	—	—	Gb/s	1
		2.5	—	—	2.5	—	—	2.5	—	—	NRZ	2
t_{PD}	Propagation Delay to Output										ps	—
	CLK to Q	1500	1800	2100	1500	1800	2100	1500	1800	2100		
	CLK to S_{OUT}	800	975	1150	800	975	1150	800	975	1150		
	CLK to CL/4	1100	1325	1550	1100	1325	1550	1100	1325	1550		
	CLK to CL/8	1100	1325	1550	1100	1325	1550	1100	1325	1550		
t_S	Set-up Time										ps	—
	SINA, SINB	–100	–250	—	–100	–250	—	–100	–250	—		
	SEL	0	–200	—	0	–200	—	0	–200	—		
t_H	Hold Time, SINA, SINB, SEL	450	300	—	450	300	—	450	300	—	ps	—
t_{RR}	Reset Recovery Time	500	300	—	500	300	—	500	300	—	ps	—
t_{PW}	Minimum Pulse Width	400	—	—	400	—	—	400	—	—	ps	—
	CLK, MR											
t_r	Rise/Fall Times										ps	—
t_f	20% to 80%											
	S_{OUT}	100	225	350	100	225	350	100	225	350		
	Other	200	425	650	200	425	650	200	425	550		

Notes:

1. Guaranteed for input clock amplitudes of 150mV to 800mV.
2. Guaranteed for input clock amplitudes of 150mV to 400mV.

APPLICATIONS INFORMATION

The SY10/100E are integrated 1:4 serial-to-parallel converters. The chips are designed to work with the E446 devices to provide both transmission and receiving of a high-speed serial data path. The E445, under special input conditions, can convert up to a 2.5Gb/s NRZ data stream into 4-bit parallel data. The device also provides a divide-by-four clock output to be used to synchronize the parallel data with the rest of the system.

The E445 features multiplexed dual serial inputs to provide test loop capability when used in conjunction with the E446. Figure 1 illustrates the loop test architecture. The architecture allows for the electrical testing of the link without requiring actual transmission over the serial data path medium. The SINA serial input of the E445 has an extra buffer delay and, thus, should be used as the loop back serial input.

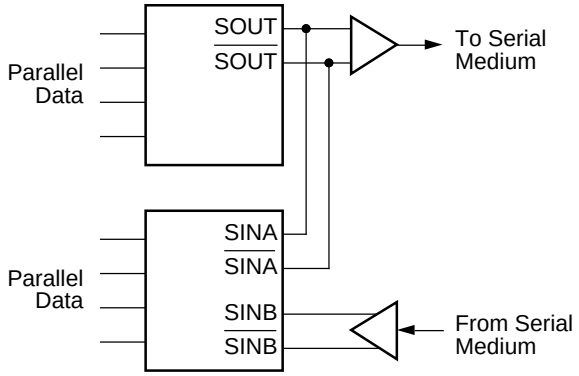


Figure 1. Loop Test Architecture

The E445 features a differential serial output and a divide-by-8 clock output to facilitate the cascading of two devices to build a 1:8 demultiplexer. Figure 2 illustrates the architecture of a 1:8 demultiplexer using two E445s. The timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the higher order device. This feedthrough of the serial inputs bounds the upper end of the frequency of operation. The clock-to-serial output propagation delay, plus the set-up time of the serial input pins, must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, t_{PD} CLK to SOUT = 1150ps or a clock frequency of 950MHz.

The clock frequency is significantly lower than that of a single converter. To increase this frequency, some games can be played with the clock input of the higher order E445. By delaying the clock feeding the second E445 relative to the clock of the first E445, the frequency of operation can be increased. The delay between the two clocks can be increased until the minimum delay of

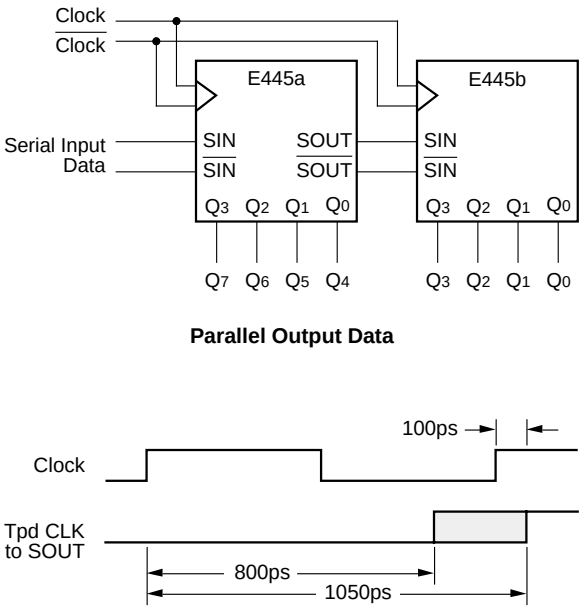


Figure 2. Cascaded 1:8 Converter Architecture

clock-to-serial-out would potentially cause a serial bit to be swallowed (Figure 3). With a minimum delay of 800ps on this output, the clock for the lower order E445 cannot be delayed more than 800ps relative to the clock of the first E445 without potentially missing a bit of information. Because the set-up time on the serial input pin is negative, coincident excursions on the data and clock inputs of the E445 will result in correct operation.

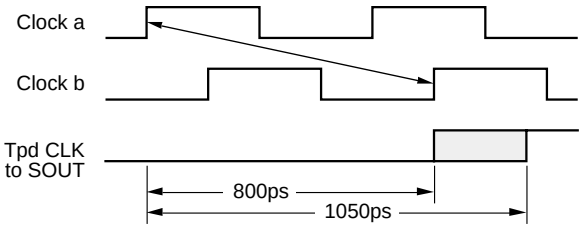
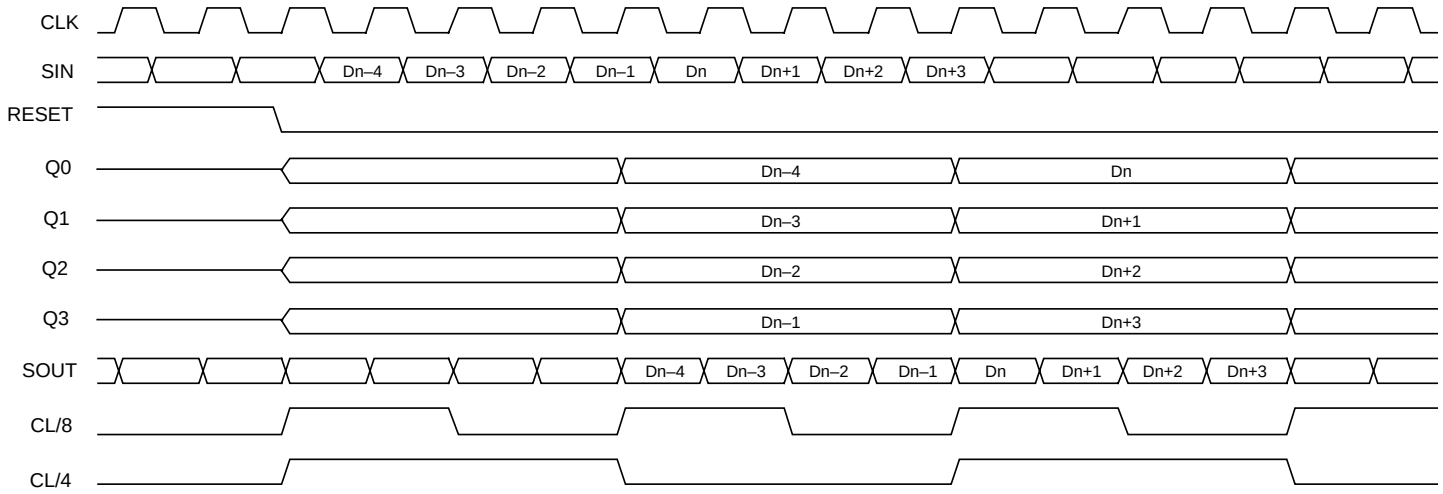


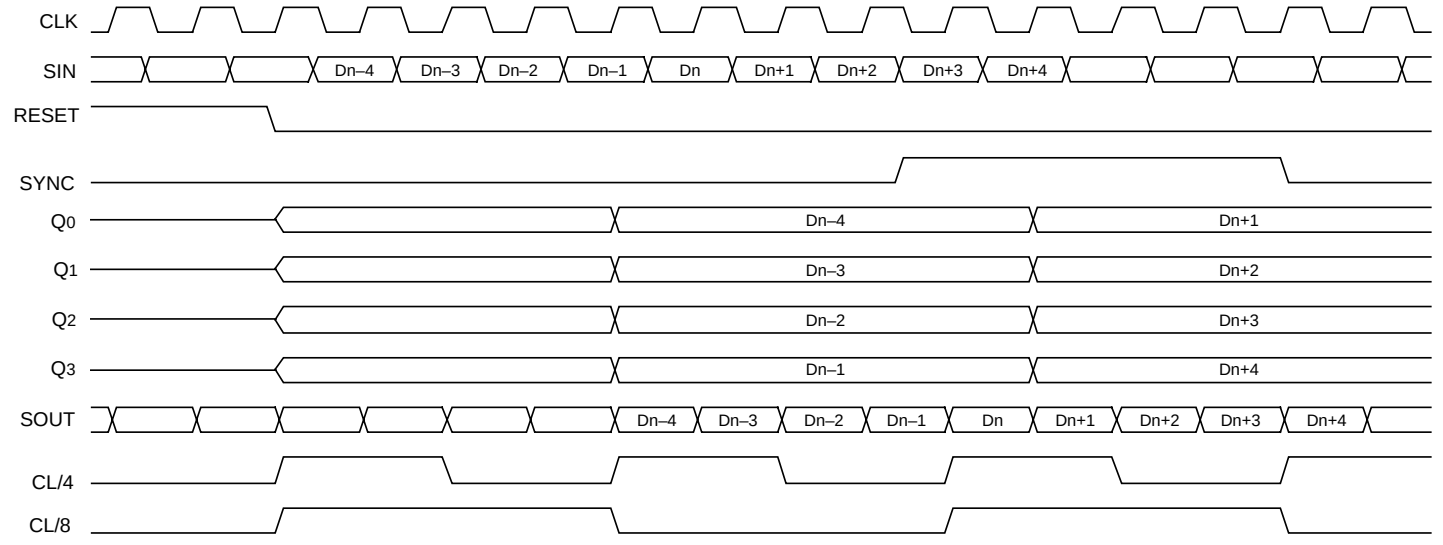
Figure 3. Cascade Frequency Limitation

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E445. By connecting the clock for the second E445 to the complimentary clock input pin, the device will clock a half a clock period after the first E445 (Figure 4). Utilizing this simple technique will raise the potential conversion frequency up to 1.5GHz. The divide-by-eight clock of the second E445 should be used to synchronize the parallel data to the rest of the system as the parallel data of the two E445s will no longer be synchronized. This skew problem between the outputs can be worked around as the parallel information will be static for eight more clock pulses.

TIMING DIAGRAMS



Timing Diagram A. 1:4 Serial to Parallel Conversion



Timing Diagram B. 1:4 Serial to Parallel Conversion with SYNC Pulse

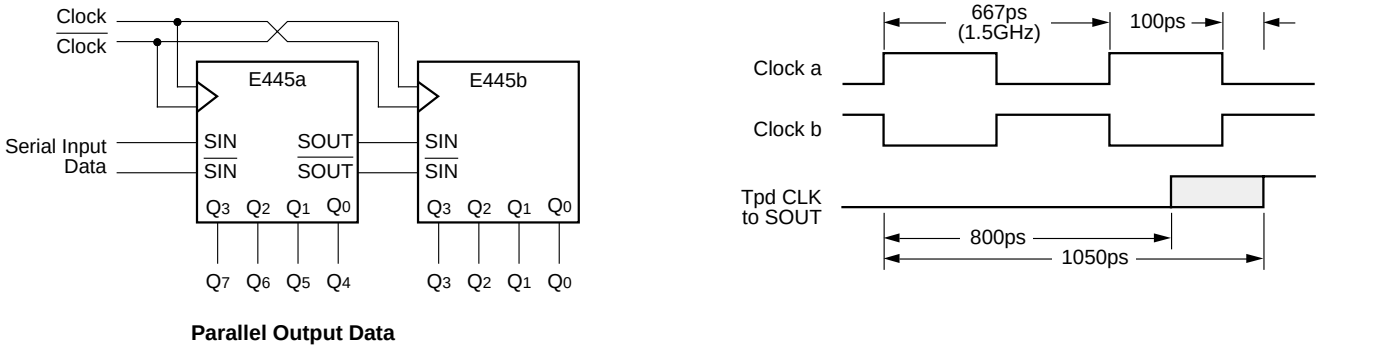
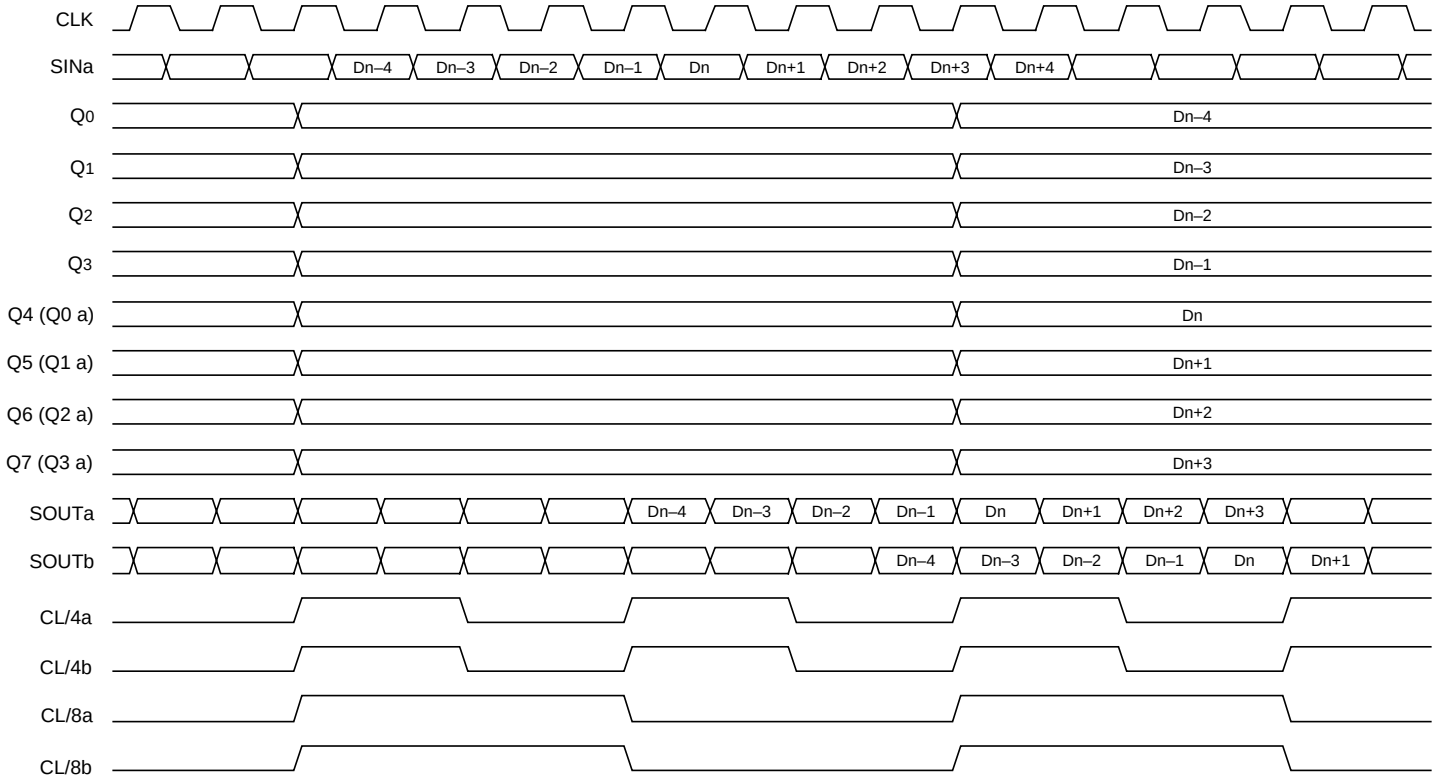
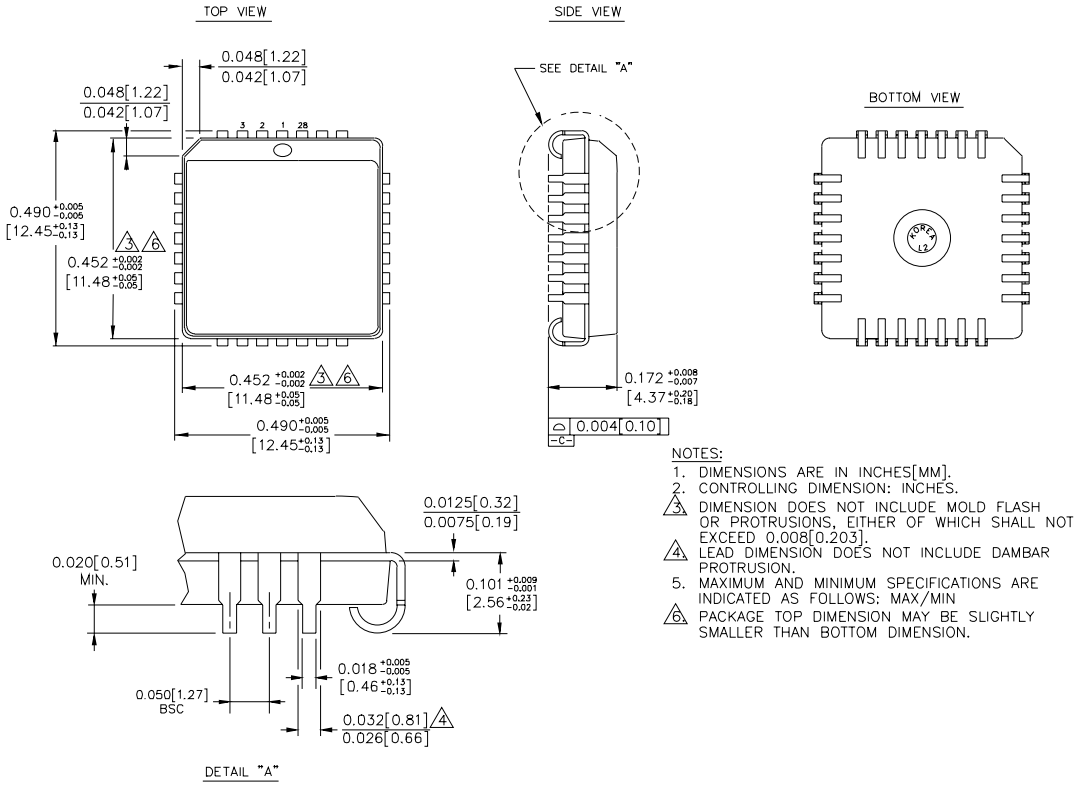


Figure 4. Extended Frequency 1:8 Demultiplexer



Timing Diagram

28-PIN PLCC (J28-1)



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