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August 20144

FSA3230 — High-Speed USB2.0 / Mobile High-Definition Link (MHL™) with Negative Swing Audio

Features

- Low On Capacitance: 6 pF / 6 pF MHL / USB (Typical)
- Low Power Consumption: 30 µA Maximum
- Supports MHL Rev. 2.0
- MHL Data Rate: 4.0 Gbps
- Audio Swing: -1.5 V to +1.5 V (Typical)
- V_{BUS} Powers Device with No V_{CC}
- Packaged in 16-Lead UMLP (1.8 x 2.6 mm)
- Over-Voltage Tolerance (OVT) on all USB Ports, Up to 5.25 V without External Components

Applications

- Cell Phones and Digital Cameras

Description

The FSA3230 is a bi-directional, low-power, high-speed, 3:1, USB2.0, MHL™ and audio switch. Configured as a double-pole, triple-throw (DP3T) switch, it is optimized for switching between high- or full-speed USB, Mobile High-Definition Link sources (per MHL Rev. 2.0 specification) and negative swing capable audio. A Single-Pole, Double-Throw (SPDT) switch is provided for ID. This ID switch provides path to support On-The-Go (OTG) communication for the USB Path OR CBUS for the MHL Path.

The FSA3230 contains special circuitry on the switch I/O pins, for applications where the V_{CC} supply is powered off (V_{CC}=0), that allows the device to withstand an over-voltage condition. This switch is designed to minimize current consumption even when the control voltage applied to the control pins is lower than the supply voltage (V_{CC}). This is especially valuable in mobile applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, digital cameras, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA3230UMX	LK	-40 to +85°C	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6 mm

Analog Symbol

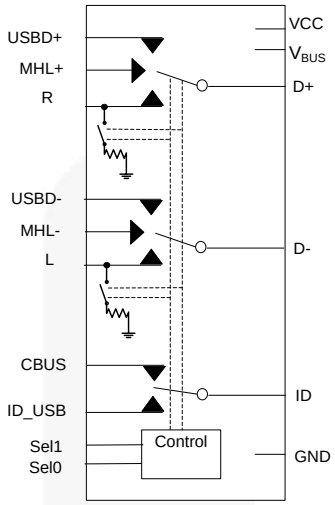


Figure 1. Analog Symbol

Table 1. Data Switch Select Truth Table

SEL1[1]	SEL0[1]	Shunt	Function
0	0	Enable	D+/D- connected to USB+/USB-; ID connected to ID_USB
0	1	Disable	D+/D- connected to R/L; ID connected to ID_USB
1	0	Enable	D+/D- connected to MHL+/MHL; ID connected to CBUS
1	1	Enable	D+/D- high impedance; ID Hi-Z

Note:

1. Control inputs should never be left floating or unconnected. To guarantee default switch closure to the USB position, the SEL[0:1] pins should be tied to GND with a weak pull-down resistor (3 MΩ) to minimize static current draw.

Pin Configuration

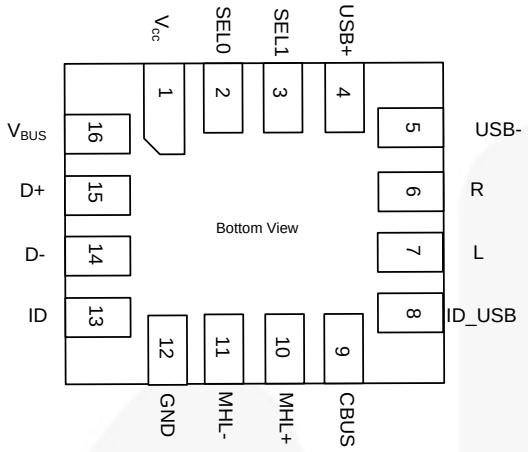


Figure 2. Pin Assignments

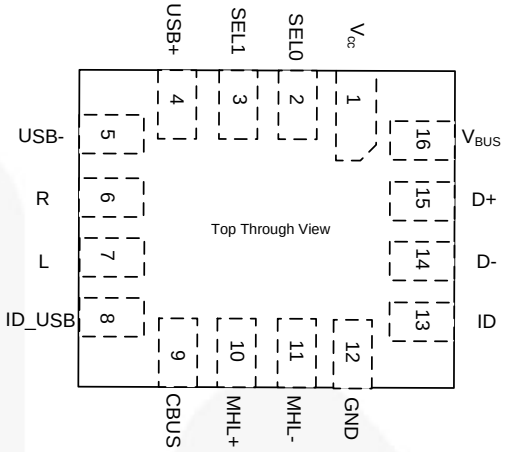


Figure 3. Top Through View

Pin Definitions

Pin	Name	Description
1	V_{CC}	V_{CC} Supply
2	SEL0	Control Pin
3	SEL1	Control Pin
4	USB+	USB Differential Data (Positive)
5	USB-	USB Differential Data (Negative)
6	R	Audio R (Negative Swing)
7	L	Audio L (Negative Swing)
8	ID_USB	ID for USB Host
9	CBUS	CBUS for MHL Host
10	MHL+	MHL Differential Data (Positive)
11	MHL-	MHL Differential Data (Negative)
12	GND	Ground
13	ID	Common Data Path for ID
14	D-	Common Data Path D-
15	D+	Common Data Path D+
16	V_{BUS}	V_{BUS} Pin from Micro-USB Connector

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}, V_{BUS}	Supply Voltage		-0.5	6.0	V
V_{CNTRL}	DC Input Voltage (SEL[1:0])[2]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[2]	USB	-0.5	6.0	V
		MHL	-0.5	6.0	
		AUDIO	-2.0	3	
		ID	-0.5	6.0	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	Switch DC Output Current (Continuous)	USB		60	mA
		MHL		60	mA
		AUDIO		60	mA
$I_{OUTPEAK}$	Switch DC Output Peak Current (Pulsed at 1ms Duration, <10% Duty Cycle)	USB		150	mA
		MHL		150	mA
		AUDIO		150	mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level: JEDEC J-STD-020A			1	
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		3.5	kV
	IEC 61000-4-2, Level 4, for D+/D- and V_{CC} Pins[3]	Contact		8	
	IEC 61000-4-2, Level 4, for D+/D- and V_{CC} Pins[3]	Air		15	
	Charged Device Model, JESD22-C101			2	

Notes:

2. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed. V_{SW} refers to analog data switch paths (USB, MHL, and audio).
3. Testing performed in a system environment using TVS diodes.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	Supply Voltage Running from V_{BUS} Voltage	4.2	5.25	V
V_{CC}	Supply Voltage Running from V_{CC}	2.5	4.5	V
$t_{RAMP(VBUS)}$	Power Supply Slew Rate from V_{BUS}	100	1000	µs/V
$t_{RAMP(VCC)}$	Power Supply Slew Rate from V_{CC}	100	1000	µs/V
Θ_{JA}	Thermal Resistance, Junction to Ambient		283	C°/W
Θ_{JC}	Thermal Resistance, Junction to Case		145	C°/W
V_{CNTRL}	Control Input Voltage (SEL[1:0])(4)	0	4.5	V
$V_{SW(USB)}$	Switch I/O Voltage (USB and ID Switch Path)	-0.5	3.6	V
$V_{SW(MHL)}$	Switch I/O Voltage (MHL Switch Path)	1.65	3.45	V
$V_{SW(AUD)}$	Switch I/O Voltage (Audio Switch Path)	-1.5	3.0	V
T_A	Operating Temperature	-40	+85	°C

Note:

4. The control inputs must be held HIGH or LOW; they must not float.

DC Electrical Characteristics

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA	2.5			-1.2	V
V_{IH}	Control Input Voltage High SEL[1:0]		2.5 to 4.50	1.0			V
V_{IL}	Control Input Voltage Low SEL[1:0]		2.5 to 4.50			0.5	V
I_{IN}	Control Input Leakage SEL[1:0]	V_{SW}(USB/MHL)=0 to 3.6 V, V_{SW}(AUD)=0 to 3.0 V, V_{CNTRL}=0 to V_{CC}	4.5	-0.5		0.5	µA
$I_{OZ(MHL)}$	Off-State Leakage for Open MHL Data Paths	V_{SW}=1.65 ≤ MHL ≤ 3.45 V SEL[1:0]=V_{CC}	4.5	-1		1	µA
$I_{OZ(USB)}$	Off-State Leakage for Open USB Data Paths	V_{SW}=0 ≤ USB ≤ 3.6 V SEL[1:0]=V_{CC}	4.5	-0.5		0.5	µA
$I_{OZ(ID)}$	Off-State Leakage for Open ID Data Paths	V_{SW}=0 ≤ ID ≤ 3.6 V, SEL[1:0]=V_{CC}	4.5	-1		1	µA
$I_{CL(MHL)}$	On-State Leakage for Closed MHL Data Paths(5)	V_{SW}=1.65 ≤ MHL ≤ 3.45 V, SEL0=GND, SEL1=V_{CC}, Other Side of Switch Float	4.5	-0.75		0.75	µA
$I_{CL(USB)}$	On-State Leakage for Closed USB Data Paths(5)	V_{SW}=0 ≤ USB ≤ 3.6 V SEL[1:0]=GND, Other Side of Switch Float	4.5	-0.75		0.75	µA

Continued on the following page…

DC Electrical Characteristics

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
$I_{CL(AUD)}$	On-State Leakage for Closed[5] AUDIO Data Path	V_{SW}=-1.5 ≤ R/L ≤ 1.5 V SEL1=GND, SEL0=V_{CC}, Other Side of Switch Float	4.5	-1.0		1.0	µA
$I_{CL(ID)}$	On-State Leakage for Closed ID Data Paths[5]	V_{SW}=0 ≤ ID ≤ 3.6 V, SEL[1:0]=00, 01 or 10	4.5	-1.0		1.0	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}(USB/MHL)=0 to 3.6 V, V_{SW}(AUD)=0 to 3.0 V, Figure 4	0	-1		1	µA
$R_{ON(USB)}$	HS Switch On Resistance (USB to D Path)	V_{SW}=0.4 V, I_{ON}=-8 mA, SEL[1:0]=GND, Figure 5	2.5		3.9	6.5	Ω
$R_{ON(MHL)}$	HS Switch On Resistance (MHL to D Path)	V_{SW}=V_{CC}-1050 mV, SEL0=GND, SEL1=V_{CC}, I_{ON}=-8 mA, Figure 5	2.5		5		Ω
$R_{ON(Audio)}$	Audio Switch On Resistance (R/L Path)	V_{SW}=-1.5 V to 1.5 V, SEL1=GND, SEL0=V_{CC}, I_{ON}=-24 mA, Figure 5	2.5		4		Ω
$R_{ON(ID)}$	ID Switch On Resistance (ID_USB or CBUS to D Path)	V_{SW}=3 V, I_{ON}=-8 mA, SEL[1:0]=00, 01 or 10, Figure 5	2.5		12		Ω
$\Delta R_{ON(MHL)}$	Difference in R_{ON} Between MHL Positive-Negative	V_{SW}=V_{CC}-1050 mV, SEL0=GND, SEL1=V_{CC}, I_{ON}=-8 mA, Figure 5	2.5		0.03		Ω
$\Delta R_{ON(USB)}$	Difference in R_{ON} Between USB Positive-Negative	V_{SW}=0.4 V, I_{ON}=-8 mA, SEL[1:0]=GND, Figure 5	2.5		0.18		Ω
$\Delta R_{ON(ID)}$	Difference in R_{ON} Between ID_USB and CBUS	V_{SW}=3 V, I_{ON}=-8 mA, SEL[1:0]=00, 01 or 10, Figure 5	2.5		0.4		Ω
$R_{ONF(MHL)}$	Flatness for R_{ON} MHL Path	V_{SW}=1.65 to 3.45 V, SEL0=GND, SEL1=V_{CC}, I_{ON}=-8 mA, Figure 5	2.5		1		Ω
$R_{ONFA(AUDIO)}$	Flatness for R_{ON} Audio Path	V_{SW}=-1.5 V to 1.5 V, SEL1=GND, SEL0=V_{CC}, I_{ON}=-24 mA, Figure 5	2.5		0.1		Ω
R_{SH}	Shunt Resistance		3.6		125	200	Ω
I_{CC}	Quiescent Current	V_{CNTRL}=0 or 4.5 V, I_{OUT}=0	4.5			30	µA
I_{CCT}	Delta Increase in Quiescent Current per Control Pin	V_{CNTRL}=1.65 V, I_{OUT}=0	4.5			18	µA
		V_{CNTRL}=2.5 V, I_{OUT}=0	4.5			10	

Note:

5. For this test, the data switch is closed with the respective switch pin floating.

AC Electrical Characteristics

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
t_{ONUSB}	USB Turn-On Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, $V_{SW(AUD)}$=1.5 V, Figure 6, Figure 7	2.5 to 3.6		445	600	ns
t_{OFFUSB}	USB Turn-Off Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, $V_{SW(AUD)}$=1.5 V, Figure 6, Figure 7	2.5 to 3.6		445	600	ns
t_{ONAUD}	AUDIO Turn-On Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, $V_{SW(AUD)}$=1.5 V, Figure 6, Figure 7	2.5 to 3.6		445	600	ns
t_{OFFAUD}	AUDIO Turn-Off Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, $V_{SW(AUD)}$=1.5 V, Figure 6, Figure 7	2.5 to 3.6		445	600	ns
t_{ONMHL}	MHL Turn-On Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3V, $V_{SW(AUD)}$=1.5 V, Figure 6, Figure 7	2.5 to 3.6		445	600	ns
t_{OFFMHL}	MHL Turn-Off Time, SEL[1:0] to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MHL)}$=3.3 V, $V_{SW(AUD)}$=1.5 V, Figure 6, Figure 7	2.5 to 3.6		445	600	ns
t_{PD}	Propagation Delay[6]	C_L=5 pF, R_L=50 Ω, Figure 6, Figure 8	2.5 to 3.6		0.25		ns
t_{BBM}	Break-Before-Make[6]	R_L=50 Ω, C_L=5 pF, V_{AUD}=1.5 V, V_{MHL}=3.3 V, V_{USB}=0.8 V, Figure 9	2.5 to 3.6		350		ns
$O_{IRR(MHL)}$	Off Isolation[6]	V_S=1 V_{pk-pk}, R_L=50 Ω, f=240 MHz, Figure 10	2.5 to 3.6		-41		dB
$O_{IRR(USB)}$		V_S=400 mV_{pk-pk}, R_L=50 Ω, f=240 MHz, Figure 10	2.5 to 3.6		-38		dB
$Xtalk_{MHL}$	Non-Adjacent Channel Crosstalk[6]	V_S=1 V_{pk-pk}, R_L=50 Ω, f=240 MHz, Figure 11	2.5 to 3.6		-37		dB
$Xtalk_{USB}$		V_S=400 mV_{pk-pk}, R_L=50 Ω, f=240 MHz, Figure 11	2.5 to 3.6		-34		dB
$Xtalk_{AUD}$		V_S=100 mV_{RMS}, R_L=32 Ω, f=20 kHz, Figure 11	2.5 to 3.6		-70		dB
THD	Total Harmonic Distortion	R_T=32 Ω, V_{SW}=2 V_{pk-pk}, f=20 Hz to 20 kHz, V_{BIAS}=0 V	2.5		0.03		%
BW	S_{DD21} Differential -3db Bandwidth[6]	V_{IN}=1 V_{pk-pk}, Common Mode Voltage=V_{CC} - 1.1 V, MHL Path, R_L=50 Ω, C_L=0 pF, Figure 12	2.5 to 3.6		2.0		GHz
		V_{IN}=400 mV_{pk-pk}, Common Mode Voltage=0.2 V, USB Path, R_L=50 Ω, C_L=0 pF, Figure 12			2.0		
		AUDIO Path, R_L=50 Ω, C_L=0p F			50		MHz

Note:

6. Guaranteed by characterization.

USB High-Speed AC Electrical Characteristics

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output[7]	C_L=5 pF, R_L=50 Ω, Figure 13	3.0 to 3.6	3	ps
t_J	Total Jitter[7]	R_L=50 Ω, C_L=5 pF, t_R=t_F=500 ps (10-90%) at 480 Mbps, PN7	3.0 to 3.6	15	ps

Note:
7. Guaranteed by characterization.

MHL AC Electrical Characteristics

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output[8]	R_{PU}=50 Ω to V_{CC}, C_L=0 pF	3.0 to 3.6	3	ps
t_J	Total Jitter[8]	f=2.25 Gbps, PN7, R_{PU}=50 Ω to V_{CC}, C_L=0 pF	3.0 to 3.6	26	ps

Note:
8. Guaranteed by characterization.

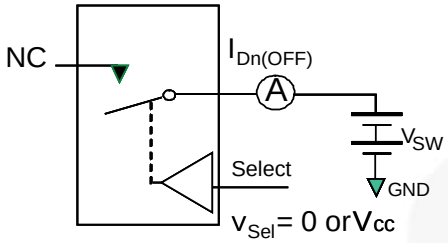
Capacitance

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Typ.	Unit
C_{IN}	Control Pin Input Capacitance[9]	V_{CC}=0 V, f=1 MHz	1.5	pF
$C_{ON(USB)}$	USB Path On Capacitance[9]	V_{CC}=3.3 V, f=240 MHz, Figure 14	6.0	
$C_{OFF(USB)}$	USB Path Off Capacitance[9]	V_{CC}=3.3 V, f=240 MHz, Figure 15	2.5	
$C_{ON(MHL)}$	MHL Path On Capacitance[9]	V_{CC}=3.3 V, f=240 MHz, Figure 14	6.0	
$C_{OFF(MHL)}$	MHL Path Off Capacitance[9]	V_{CC}=3.3 V, f=240 MHz, Figure 15	2.5	
$C_{ON(AUD)}$	Audio Path On Capacitance[9]	V_{CC}=3.3 V, f=1 MHz, Figure 14	10	
$C_{OFF(AUD)}$	Audio Path Off Capacitance[9]	V_{CC}=3.3 V, f=1 MHz, Figure 15	2.5	
$C_{ON(ID)}$	ID Path On Capacitance[9]	V_{CC}=3.3 V, f =1 MHz, Figure 14	3.5	
$C_{OFF(ID)}$	ID Path Off Capacitance[9]	V_{CC}=3.3 V, f =1 MHz, Figure 15	1.5	

Note:
9. Guaranteed by characterization.

Test Diagrams



**Each switch port is tested separately

Figure 4. Off Leakage

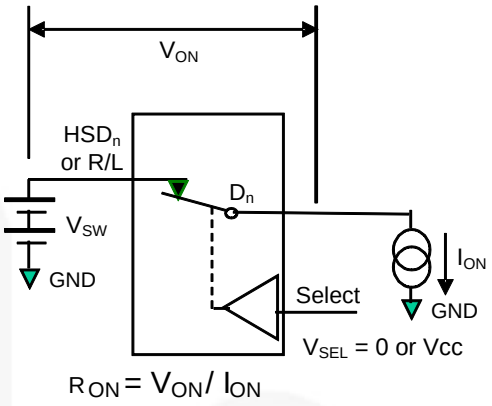
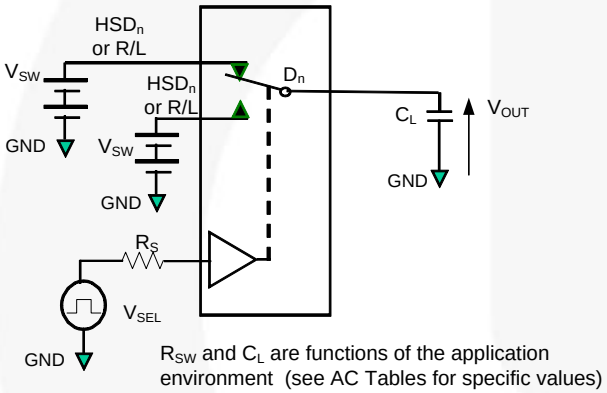


Figure 5. On Resistance



R_{SW} and C_L are functions of the application environment (see AC Tables for specific values)

Figure 6. AC Test Circuit Load

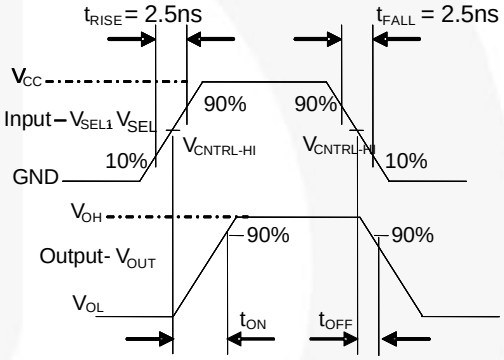


Figure 7. Turn-On / Turn-Off Waveforms

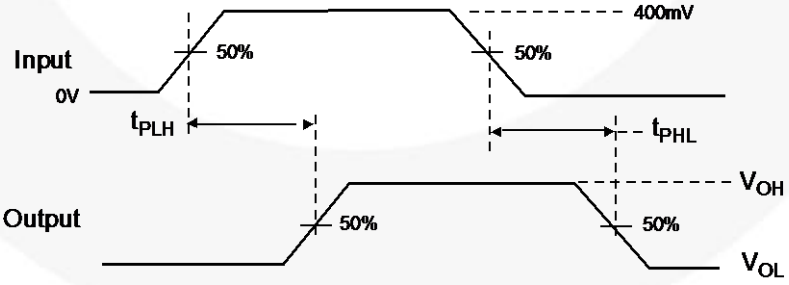
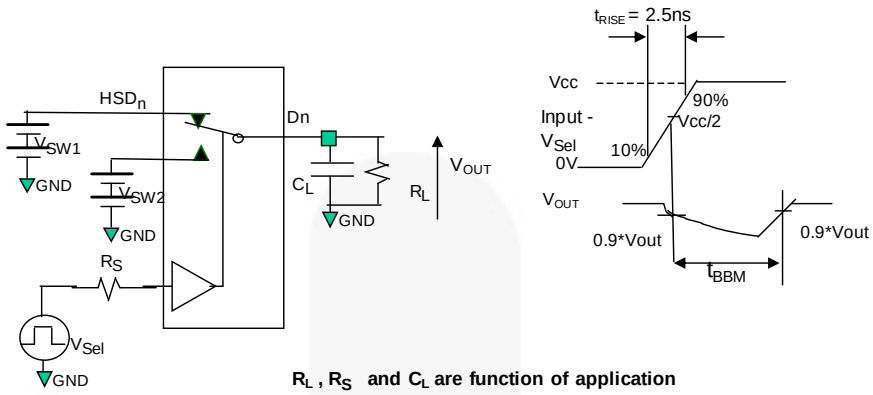


Figure 8. Propagation Delay ($t_R t_F$ – 500ps)

Note:

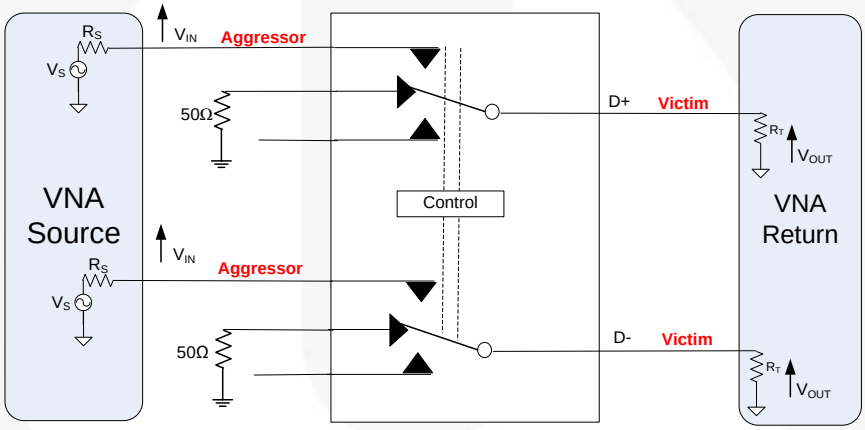
10. HSD_n refers to the high-speed data USB or MHL paths.

Test Diagrams



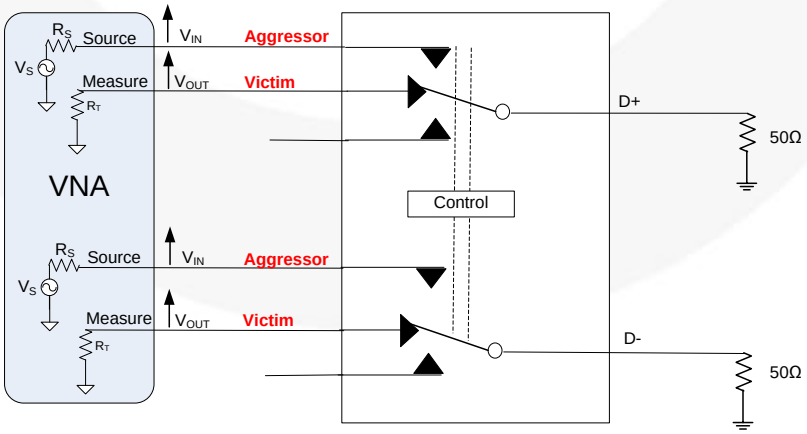
R_L , R_S and C_L are function of application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 9. Break-Before-Make Interval Timing



V_S, R_S and R_T are functions of the application environment (see AC/DC Tables for values).
Off Isolation = 20 Log (V_{OUT} - V_{IN})

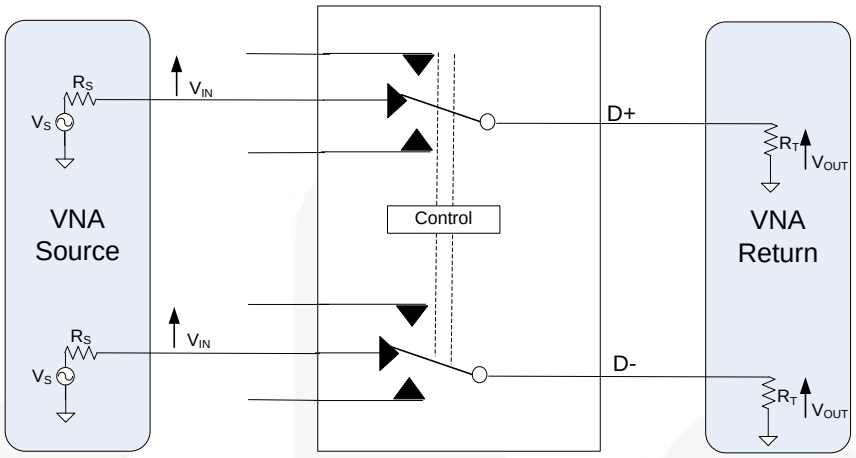
Figure 10. Channel Off Isolation (SDD21)



VS, RS and RT are functions of the application environment (see AC/DC Tables for values).
Off Isolation = 20 Log (VOUT - VIN)

Figure 11. Non-Adjacent Channel-to-Channel Crosstalk (SDD21)

Test Diagrams



V_S, R_S and R_T are functions of the application environment (see AC/DC Tables for values).

Figure 12. Insertion Loss (SDD21)

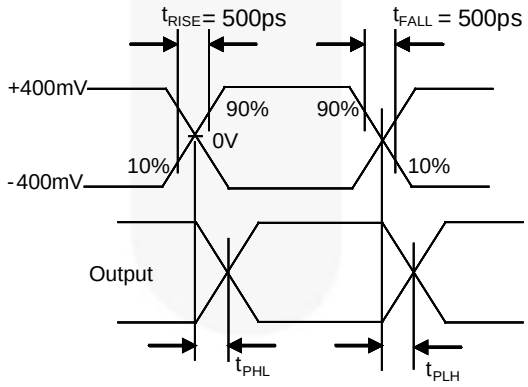


Figure 13. Intra-Pair Skew Test $t_{SK(P)}$

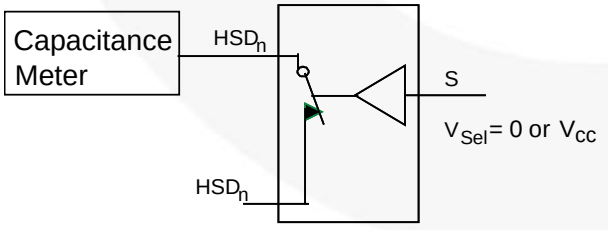


Figure 14. Channel On Capacitance

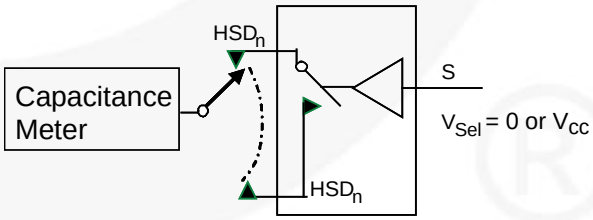


Figure 15. Channel Off Capacitance

Functional Description

Insertion Loss

One of the key factors for using the FSA3230 in mobile digital video applications is the small amount of insertion loss experienced by the received signal as it passes through the switch. This results in minimal degradation of the received eye. One of the ways to measure the quality of the high data rate channels is using balanced ports and four-port differential S-parameter analysis, particularly SDD21.

Bandwidth is measured using the S-parameter SDD21 methodology.

Figure 16. MHL Path SDD21 Insertion Loss Curve

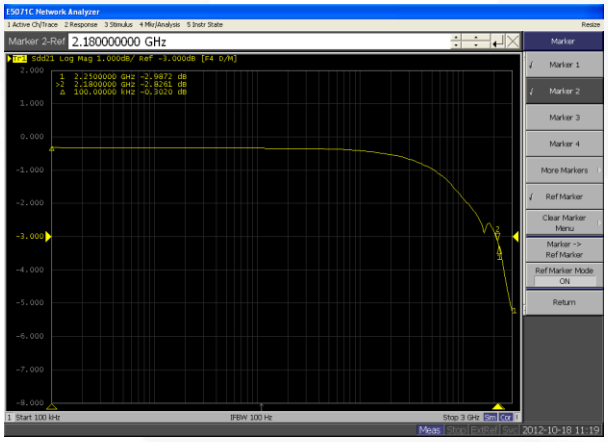


Figure 17. USB Path SDD21 Insertion Loss Curve

Typical Applications

Figure 18 shows the FSA3230 utilizing the V_{BUS} from the micro-USB connection. The 3 MΩ resistors are used to ensure, for manufacturing test via the micro-USB connector, that the FSA3230 configures for connectivity to the baseband or application processor. Figure 19 shows the configuration for the FSA3230 "self powered" by battery only.

Switch Power Operation

In normal operation, the FSA3230 is powered from the V_{CC} pin, which typically is derived from a regulated power management device. In special circumstances, such as production test or system firmware upgrade, the device can be powered from the V_{BUS} pin. If both V_{CC} and V_{BUS} pins are present, V_{CC} is selected as the power source and V_{BUS} is ignored (*see Table 2*).

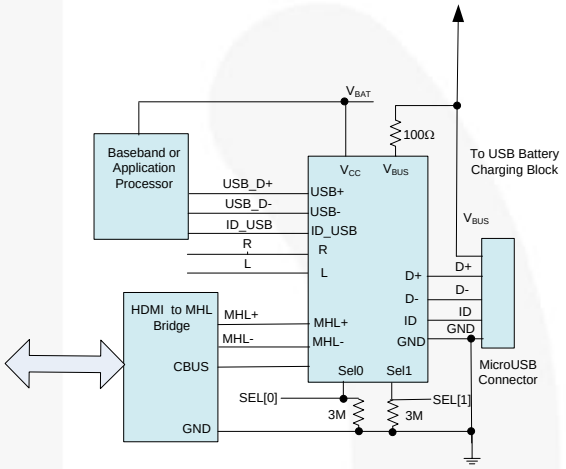


Figure 18. Application Using V_{BUS}

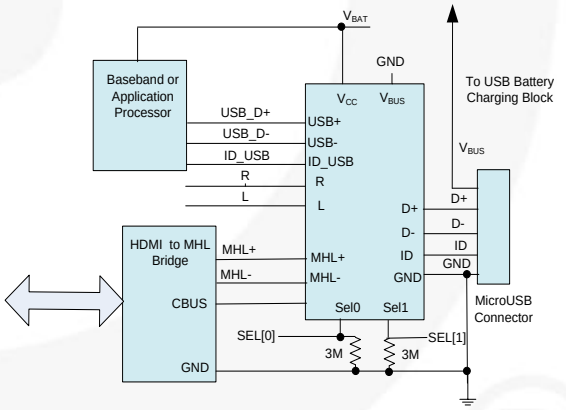
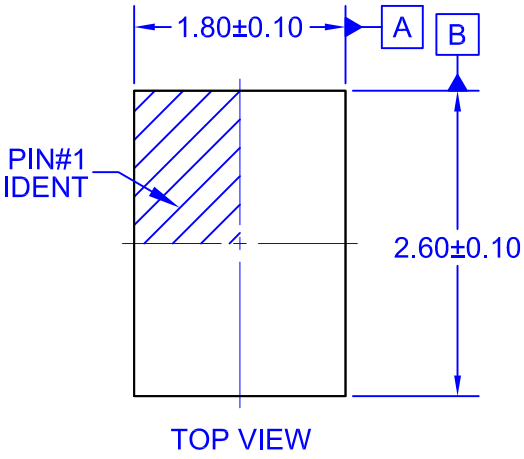


Figure 19. "Self-Powered" Application Using V_{BAT}

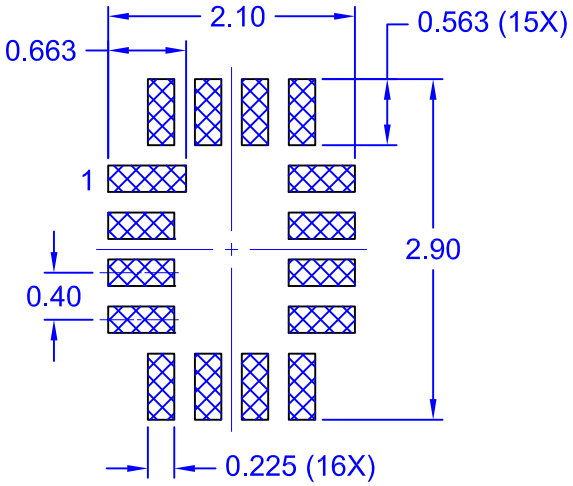
Table 2. Switch Power Selection Truth Table

V_{CC}	V_{BUS}	Switch Power Source
0	0	No Switch Power, Switch Paths High Z
0	1	V_{BUS}
1	0	V_{CC}
1	1	V_{CC}

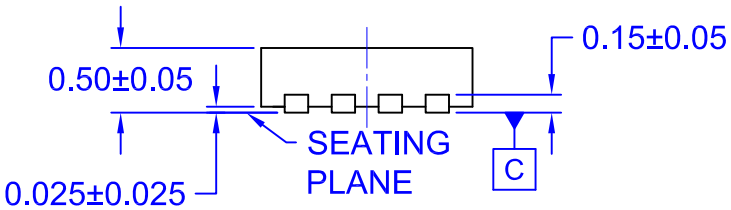
Description	Nominal Values for MKT-UMLP16A Rev5 (mm)
Overall Height	0.50
Package Standoff	0.012
Lead Thickness	0.15
Lead Width	0.20
Lead Length	0.40
Lead Pitch	0.40
Body Length (Y)	Min: 2.50, Nom: 2.60, Max: 2.70
Body Width (X)	Min: 1.70, Nom: 1.80, Max: 1.90



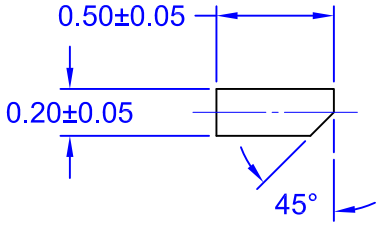
TOP VIEW



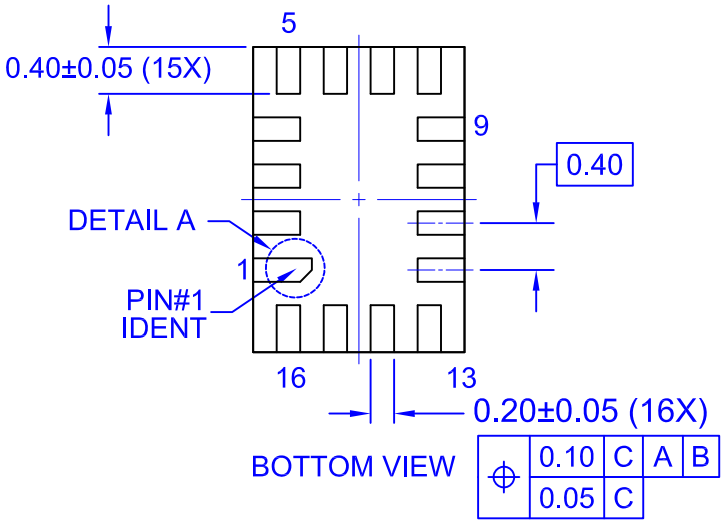
RECOMMENDED
LAND PATTERN



SIDE VIEW

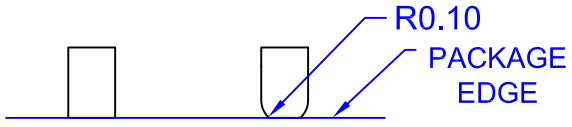


DETAIL A
SCALE 2:1



BOTTOM VIEW

LEAD SHAPE AT PACKAGE EDGE



LEAD
OPTION 1
SCALE 2:1

LEAD
OPTION 2
SCALE 2:1

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
D DRAWING FILENAME: MKT-UMLP16ArevG.
E. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

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