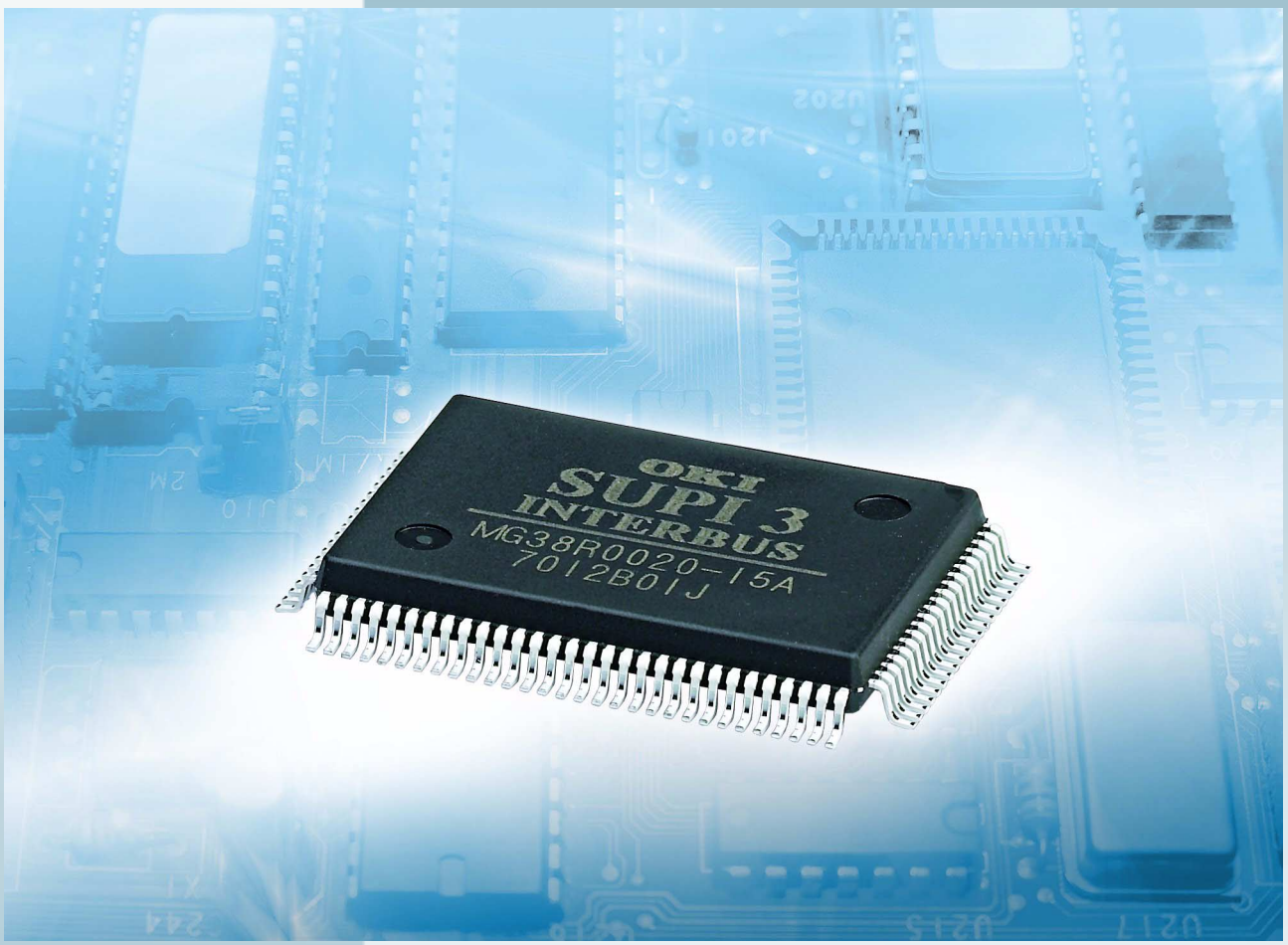
AUTOMATION



User manual

IBS SUPI 3 UM E

Order No.: —

INTERBUS protocol chip IBS SUPI 3

PHOENIX CONTACT
INSPIRING INNOVATIONS

AUTOMATION

User manual
INTERBUS protocol chip IBS SUPI 3

2010-12-09

Designation: IBS SUPI 3 UM E

Revision: 03

Order No.: —

This user manual is valid for:

Designation	Order No.
IBS SUPI 3 QFP	2746087
IBS CHIP-Muster/...	2746951

Please observe the following notes

In order to ensure the safe use of the product described, you have to read and understand this manual. The following notes provide information on how to use this manual.

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This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.

DANGER
This indicates a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING
This indicates a hazardous situation which, if not avoided, could result in death or serious injury.

CAUTION
This indicates a hazardous situation which, if not avoided, could result in minor or moderate injury.

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NOTE
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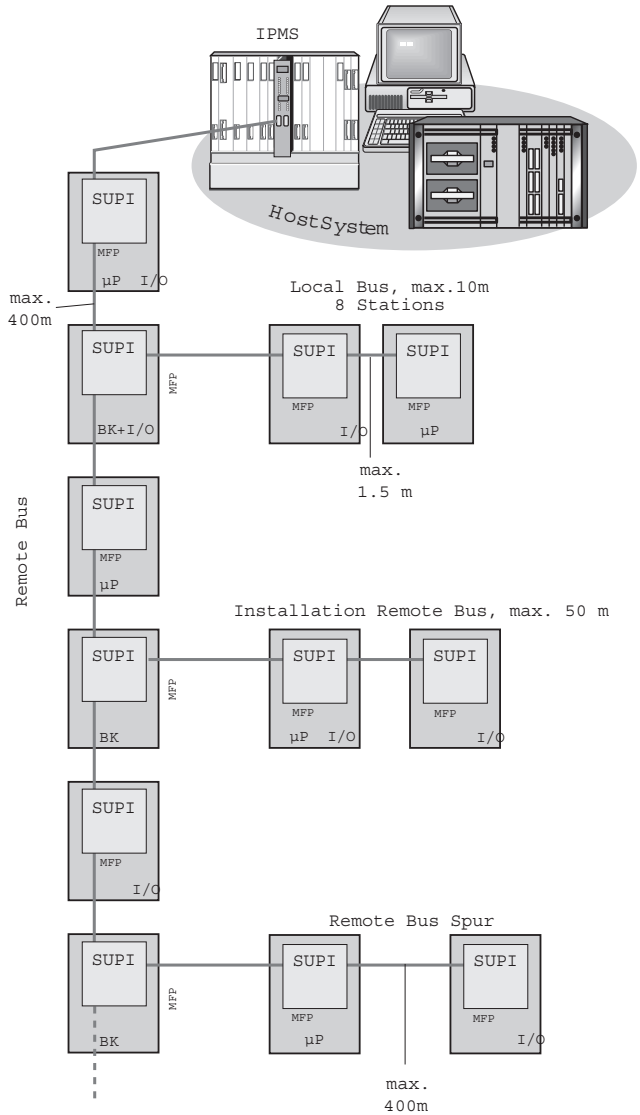
1 Structure and basic wiring

The IBS SUPI 3 (**S**erial **U**niversal **P**rotocol **I**nterface) chip represents a new generation of INTERBUS slave protocol chips and an easy interface to INTERBUS. The integrated diagnostic and error management is a novelty in the chip; it allows an exact determination of error location and cause in a system and also reduces external circuitry.

On the basis of this description you may implement your own INTERBUS devices within a very short time. With the end user in mind, subject the devices to the INTERBUS conformance test.

In addition to this document you will find the INTERBUS Club guideline "Conformity Test and Certification" as a reference work on the Internet at www.interbusclub.com.

Current hardware and software information for the device manufacturer as well as further product documents from Phoenix Contact can be found on the Internet at www.phoenixcontact.net/catalog.



Application areas of the INTERBUS slave protocol chip

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Figure 1-1 Fields of application of the INTERBUS SUPI 3 slave protocol chip

1.1 Introduction

The IBS SUPI 3 chip is an ASIC in 0.5 µm CMOS technology. It represents the third generation of INTERBUS slave protocol chips and is pin- and function-compatible to the previous SUPI 2 chip. Every INTERBUS master operates together with the SUPI 3 chip. The IBS PC AT-T PC interface board supports the SUPI 3 chip by driver version 3.1 or later.

Currently, the SUPI 3 is available in one housing type (QFP 100).

Table 1-1 Different versions

Housing	Order designation	Order No.
QFP 100	IBS SUPI 3 QFP	2746087
QFP 100	IBS CHIP-Muster/...	2746951

1.2 Basic structure

The SUPI 3 is the third generation of INTERBUS slave protocol chips. It is pin- and function-compatible with the previous SUPI 1 and 2 chip versions. Its most important new feature is its central diagnostics and report manager being part of the new INTERBUS diagnostic concept.

The INTERBUS SUPI 3 protocol chip resulted from a VHDL model and has a complexity of about 15000 gate equivalents. The following block diagram shows the structure of the circuit.

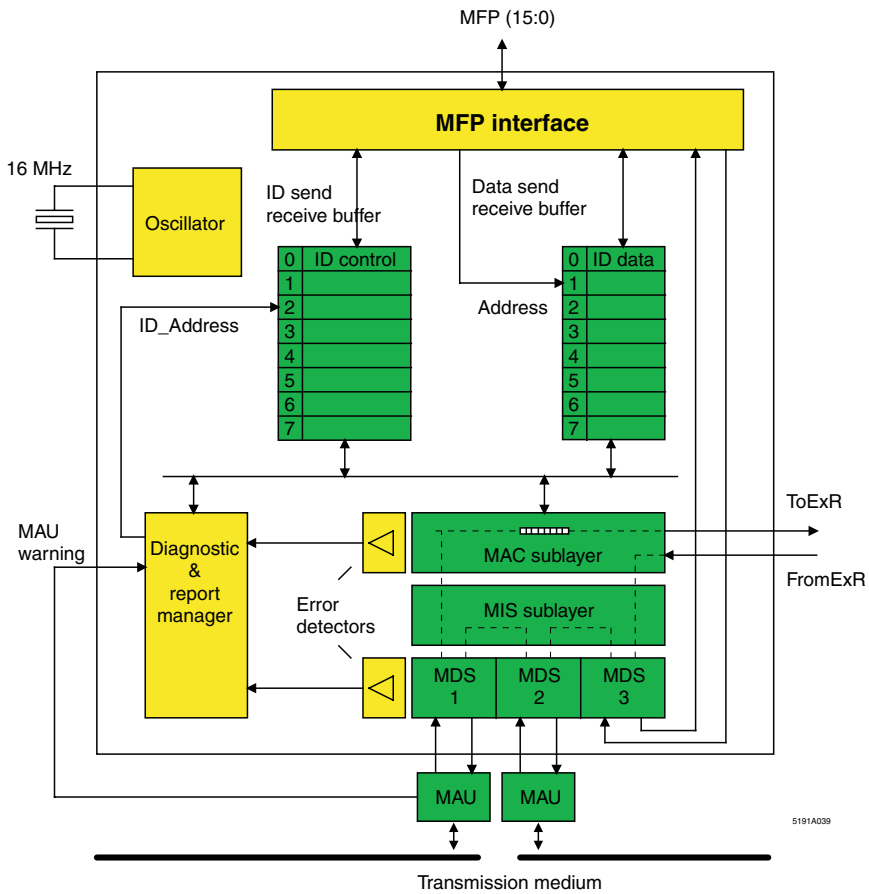


Figure 1-2 Block diagram of the chip

The protocol stack in the middle comprises layer 1 and layer 2 of the ISO/OSI reference model. Data is provided to the MDS (Medium Dependent Sublayer) from an external MAU (Medium Attachment Unit) e.g., RS-485 or fiber-optic access. In this layer, scanning, line decoding and encoding are carried out and time conditions are defined. The SUPI 3 chip has three channels in the MDS for one incoming and two outgoing interfaces.

The MIS (Medium Independent Sublayer) forms the upper edge of layer 1, i.e., the physical layer. It is intended for routing the three MDS channels and for connecting layer 2.

Its lower edge represents the medium access control (MAC). This layer performs the ring access as well as the data security. The MAC sublayer serves the 8-byte transmit and receive buffers for INTERBUS data as well as the 16-byte transmit and receive buffers for the identification transmission cycle. The application and higher protocol layers have access to these buffers via the 16-bit **M**ulti-**F**unctions **P**in interface (MFP interface). The MFP interface can be set according to the interface implementation requirements via four configuration pins as an I/O port or as a microprocessor interface of a CPU environment. The MFP interface contains an interrupt controller with the necessary write and read registers as well as parameterization and state registers for CPU applications. These registers allow to configure the chip and to visualize certain protocol events.

Data of the transmit and receive buffers is taken from the MAC sublayer, encoded correspondingly and sent to the suitable MDS channel via the MDS sublayer. After the line encoding, data is sent to the medium via the external MAU.

Compared to previous chips, the central diagnostics and report manager as well as the error detectors which are able to read certain error patterns at all MDS channels and the MAC sublayer, are important new features of the SUPI 3 chip. This block distinguishes between events with high or low priority. Events of low priority, also called report events are, for example, the MAU warnings in the block diagram. These warnings are provided by the MAU and indicate an impairment of the transmission quality. This means that not only faults, but also creeping impairment in quality is detected and signaled at a very early stage.

Diagnostic events with high priority are error sources which cause interference in the transmission cycle. The diagnostics and report manager ensures both generation and non-time-critical transmission of error patterns. The error patterns are stored in the ID send buffer and transmitted from the MAC sublayer to the bus master.

If an error exceeds the permissible data update time of the bus system but is too short for a central check of all devices by the master, the on-chip diagnostics shows its performance. The diagnostics manager stores all detected errors on the transmission medium as well as breakdowns of the voltage supply as error patterns in the chip until it has been read and acknowledged by the bus master. This procedure allows a unique assignment of sporadic errors, which in general are difficult to identify, to the error location.

1.2.1 New features of the IBS SUPI 3 chip

Although the diagnostics described above is an important feature, it is less important to developers of INTERBUS devices when designing the circuit. The efforts are reduced because functions are implemented in the SUPI 2 chip by additional hardware.

For example, the voltage monitoring of all electrically isolated areas is no longer necessary because the MDS sublayers offer a better evaluation. This reduces hardware expense considerably. The power-up reset circuitry of the SUPI 3 chip has also been optimized.

For a better detection of errors caused by the transmission medium (e.g. loose contacts or failure of a differential signal line of the RS-485 interface), this state must be mapped to a high level at the data input. This means for the RS-485 interface to force a logic "1" on the receive data line in the event of an error. The line decoders in the MDS sublayer interpret this as an idle message. Since idle messages defined in the protocol have a logic "0" encoding, a distinction is possible using MAU fail timers. If the MAU fail timer recognizes this "1" state for a set time, this is indicated as a MAU error to the diagnostics manager. The "MAU warning" function can detect, for example, the impairment of optical components caused by aging or an increasing pollution of lenses in the data light barriers before it comes to a complete failure. For this, the output of a trigger must be led to the new "MAU warning" inputs of the SUPI 3 chip.

For a better support of software flexibility on the slaves, the module identification code (ID code) can now be loaded to the SUPI 3 chip. Like the length code in the SET-I register, this code is protected from accidental writing by an automatic latching mechanism.

This mechanism and applying the "µP_not_Ready" ID code to the physical pins of the SUPI 3 allows reconfiguration of the protocol chip by intelligent modules even after the bus master has initialized the INTERBUS system. This means when the INTERBUS master has detected a device with the "µP_not_Ready" ID code in the INTERBUS system, it waits for the final configuration. Therefore, the same hardware can be used for very different applications.

Two message registers which realize a management channel to the INTERBUS master, are another new feature. The user has no direct access to the channel. It is an option for future applications. A new function has been implemented in the SET-II register. By setting bit 5, a µP watchdog input is activated. Register 14, which was previously not available is used to enable additional interrupts. In this way an interrupt can be generated when the master writes a processor alarm register or when the layer 2 watchdog has elapsed. The new register 15 stores test functions for an engineering test during the development of the chip. These functions are not important for the user.

Summary of the new IBS SUPI 3 chip features:

- With its diagnostic features, the diagnostic and report manager is the heart of the SUPI extensions. It stores error localization information for the bus master.
- The new SUPI 3 functions are supported by controller boards as of Generation 4 only (firmware 4.0 or later).
- The SUPI 3 is manufactured in a 0.5 µm technology. This requires a more careful design and offers the use of additional quartz types for the oscillator with new external circuitry.
- The pad dimensions of the QFP 100 housing were modified so that chip requires less space.

Improvements compared to SUPI 2

– Filtering of the quasi-static inputs:

RBST, LBST	: 270 ms
CONF	: 35 ms
/StatErr	: 270 ms (standard) / 2.5 µs (µP watchdog)
/ResIN	: 520 µs

These signals also had Schmitt trigger input circuits.

– Increase of driver capability of the outputs /ResReg, ClkExR, BA, RD, LD/TR, Error from 2 mA to 12 mA.
– Watchdog for "bus active" is now reset for every valid ID or data cycle.
– Start bit recognition: A spike (pulse <100 ns) in the critical range is recognized as a start bit error.

Additional functions

– Manufacturer/mask identification. Hardware version can be detected by the master. Information is mapped to the INFO register of the ID send buffer.
– Layer 2 timeout monitoring: If LaOuD is not sent within a preset time, process OUT data is reset and /ResReg activated, provided that the master has enabled the function.
– µP, ID code register: Now, the entire ID code (ID0-ID12) can be set by a microprocessor.
– "µP_not_Ready" ID code: If ID0 to ID7 = 38_{hex} (remote bus device) or ID0 to ID7 = 78_{hex} (local bus device) is set, new functions are active internally.
– /StatErr can additionally be used to indicate activation of an external processor watchdog.
– Processor command and alarm registers on address 9 form a management channel to the master (currently still reserved).
– On-chip diagnostics: The master activates on-chip diagnostics on the devices during the bus system detection. All devices capable of diagnostics exchange their operation ID registers and diagnostic ID registers. The master thus recognizes all devices able for diagnostics. If errors should occur, they are stored in the diagnostic register. The following diagnostic elements are implemented in the line decoder (forward, return, branch):
  – Power-up reset detection
  – MAU fail (wire interrupt, wire short-circuit).
  – CRC (Cyclic Redundancy Check)
  – Stop bit error detection
  – Validity check of the check sequence
  – RBST, LBST change detection
  – MAU warnings (impairment of the transmission quality).
  – Eight alternative ID registers are addressed by a control word of the controller board and transmitted in the next ID cycle.

– The following registers can be selected:

  0 Standard register
  1 First diagnostic bit register
  2 Second diagnostic Register
  3 Alarm bit register
  4 Processor alarm register
  5 Reserved
  6 Reserved
  7 Manufacturer/mask identification

The standard ID register is the default setting.

1.2.2 Field of application

The SUPI 3 has been designed for industrial applications.

Table 1-2 General data

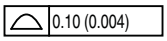
	Quantity			
Value	**Min.**	**Type**	**Max.**	**Unit**
Supply voltage	4.5	5.0	5.5	V
Temperature	-40	+25	+85	°C

1.3 Housing type

The following list explains general symbols and text that will be used in the drawing of the housing.

Position

Maximum material condition MMC



Feature control frame

Basic or exact dimension

BSC Basic - untoleranced dimension locating true position

REF A dimension which is obtained from other dimensions and their tolerances

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1.3.1 QFP 100 pin table

Table 1-3 QFP 100 pin table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	RBST	36	MFP10	70	ID0
2	KM0	37	MFP9	71	SLI1
3	n.c.	38	MFP8	72	RGNDA
4	KM1	39	n.c.	73	/StatErr
5	n.c.	40	V_{DD}	74	n.c.
6	CKO2	41	V_{SS}	75	CRI1
7	n.c.	42	MFP7	76	n.c.
8	FromExR	43	V_{SS}	77	CONF
9	DO2	44	MFP6	78	n.c.
10	LBST	45	MFP5	79	BA
11	C0	46	MFP4	80	LBDA/TR
12	C1	47	MFP3	81	Error
13	C2	48	MFP2	82	DI1
14	CKO1	49	MFP1	83	C3
15	DO1	50	n.c.	84	/LBRes
16	CRO1 / MAUWR	51	MFP0	85	/ModAck
17	SLO1 / MAUWH	52	/ResIn / MAUWS	86	RBDA
18	V_{SS}	53	ID12	87	V_{SS}
19	V_{DD}	54	n.c.	88	CKI1
20	OSC1	55	ID11	89	V_{DD}
21	OSC2	56	n.c.	90	n.c.
22	/ResU	57	ID10	91	V_{SS}
23	DI2	58	ID9	92	SLO2
24	n.c.	59	ID8	93	LaOuC
25	CRI2	60	ID7	94	/LaInD
26	n.c.	61	n.c.	95	LaOuD
27	SLI2	62	ID6	96	/ClkExR
28	CKI2	63	ID5	97	CRO2
29	MFP15	64	V_{DD}	98	/ResReg
30	n.c.	65	ID4	99	ToExR2

Table 1-3 QFP 100 pin table (continued)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
31	MFP14	66	V_{SS}	100	ToExR1
32	MFP13	67	ID3		
33	n.c.	68	ID2		
34	MFP12	69	ID1		
35	MFP11				

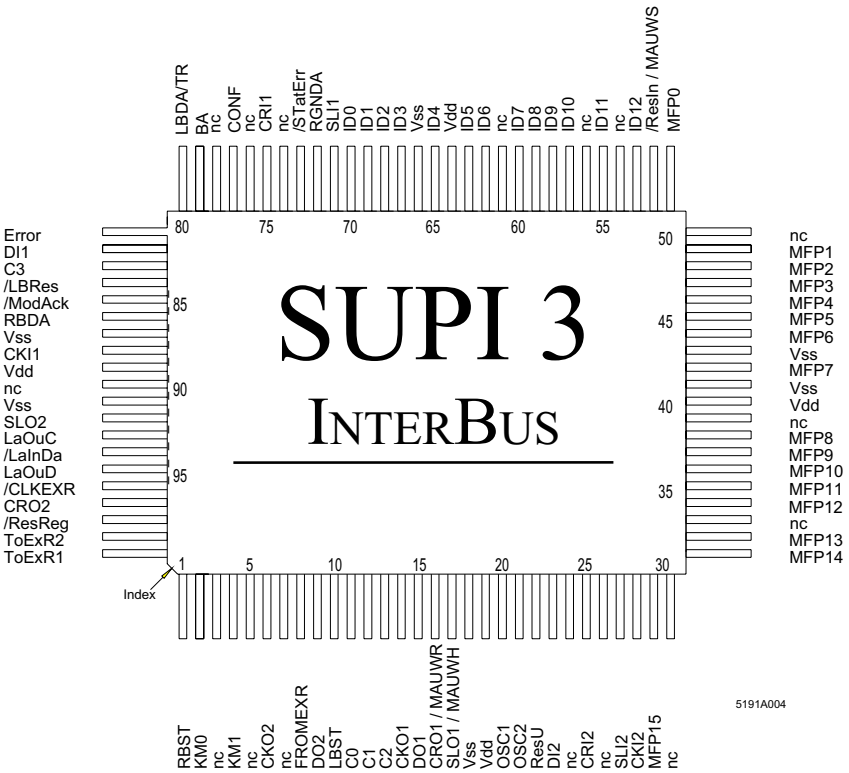


Figure 1-3 Pin layout of the QFP 100 housing

1.3.2 QFP 100 (Quad Flat Pack)

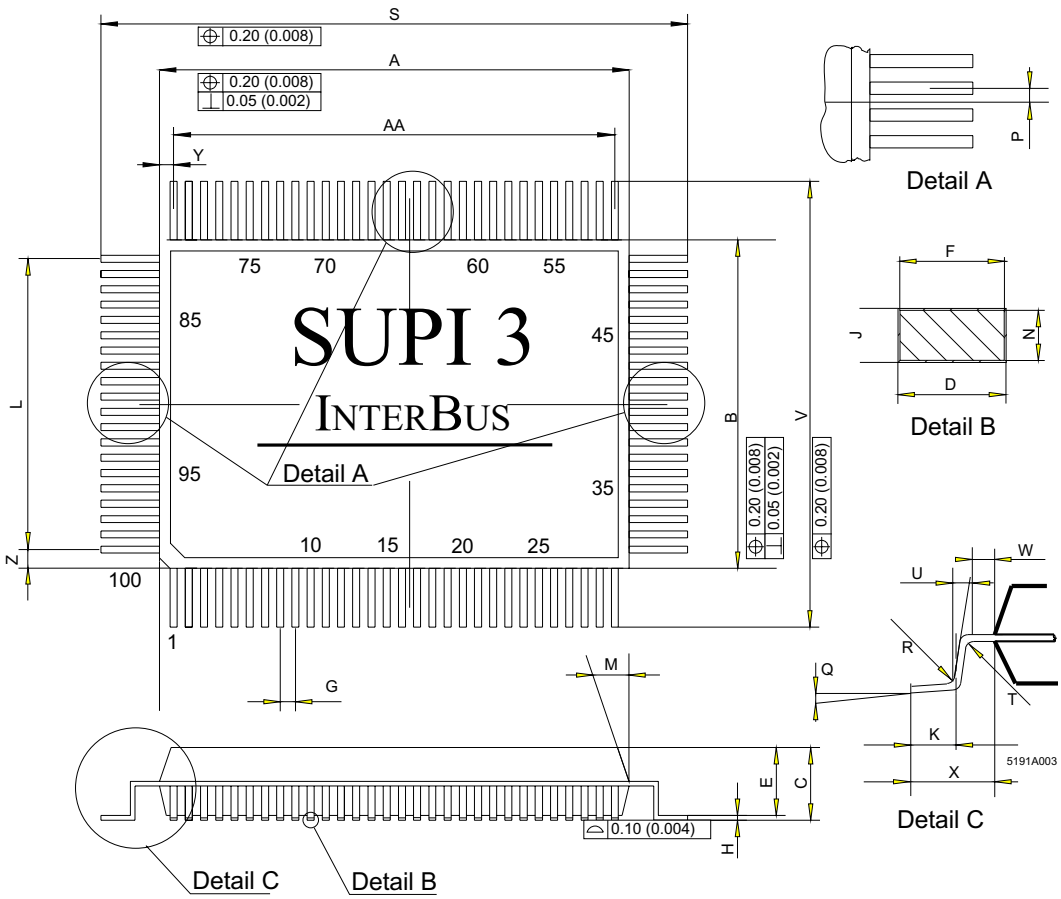


Figure 1-4 Mechanical dimensions of the QFP 100 housing (original dimension: millimeters)

Table 1-4 Mechanical dimensions of the QFP 100 housing

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	19.90	20.10	0.783	0.791	P	0.325 BSC		0.013 BSC	
B	13.90	14.10	0.547	0.555	Q	0°	7°	0°	7°
C	2.80	3.40	0.110	0.134	R	0.25	0.35	0.010	0.014
D	0.22	0.38	0.009	0.015	S	22.95	23.45	0.904	0.923
E	2.55	3.05	0.100	0.120	T	0.13	–	0.005	–
F	0.22	0.33	0.009	0.013	U	0°	–	0°	–
G	0.65 BSC		0.026 BSC		V	16.95	17.45	0.667	0.687
H	0.25	–	0.010	–	W	0.40	–	0.016	–
J	0,11	0,23	0.004	0.009	X	1.60 REF		0.063 REF	
K	0.73	1.03	0.028	0.040	Y	0.58 REF		0.023 REF	
L	12.35 REF		0.486 REF		Z	0.83 REF		0.033 REF	
M	5°	16°	5°	16°	AA	18.85 REF		0.742 REF	
N	0.11	0.17	0.004	0.007					

1.3.3 Signal description

Table 1-5 Signal description

Designation	Meaning	Type
OSC1 OSC2	Oscillator input Oscillator output	OSC OSC
C3 C2 C1 C0	Configuration inputs for the MFP interface**	CIp CI CI CI
KM1 KM0 RGNDA	Configuration inputs for the INTERBUS interface**	CI
ID12-ID0	Identification code setting data length entry**	CI
MFP15-MFP0	Multi-function pins	BDp
SLxx	**Control line ID/data cycle**	
SLO1/MAUWH SLO2 SLI1 SLI2	Select line IN forward path/MAU warning forward path* Select line OUT forward path Select line OUT return path Select line IN return path	ST B12 B12 ST
Dxx	**Data line of the INTERBUS ring**	
DO1 DO2 DI1 DI2	Data line IN forward path Data line OUT forward path Data line OUT return path Data line IN return path	ST B12 B12 ST
CKxx	**Clock line for the INTERBUS devices**	
CKO1 CKO2 CKI1 CKI2	Clock line IN forward path Clock line OUT forward path Clock line OUT return path Clock line IN return path	ST B12 B12 ST
CRxx	**Control line check sequence**	
CRO1/MAUWR CRO2 CRI1 CRI2	Control line IN forward path/MAU warning return path* Control line OUT forward path Control line OUT return path Control line IN return path	ST B12 B12 ST
/ResIn/MAUWS	INTERBUS reset input/MAU warning branch*. Input filtered with t_{f2} = 520 µs***, directly passed on to pin /LBRes.	STp
/LBRes	INTERBUS reset output	B2
RBST	Alarm input whether outgoing INTERBUS interface is used. Input filtered with t_{f1} = 270 ms***	ST

Table 1-5 Signal description (continued)

Designation	Meaning	Type
LBST	Alarm input whether local bus interface is used in BK module applications. In all other modes of operation this pin is to be connected to V_{SS}. Input filtered with t_{f1} = 270 ms***	ST
	Diagnostic signals	
/StatErr	"Module error" alarm input or µP watchdog, input filtered with t_{f1} = 270 ms***. When using the pin as a µP watchdog pin the scan time is set to t_{f3} = 2.5 µs***. See also Section "SET-II register" on page 3-19.	STp
/ModAck	Acknowledge output for a recognized module error. This output is not used in standard applications.	B2
CONF	"Reconfiguration request" alarm input. The input is filtered with t_{f4} = 35 ms***. This input is connected to GND in standard applications.	STp
RBDA	"Outgoing interface is disabled" alarm output	B12
LBDA/TR	"Local bus disabled" alarm output for BK "PCP active" with µP with PCP protocol software	B12
BA	"INTERBUS active" alarm output	B12
Error	"Error in the connected local bus" alarm output for BK modules	B12
	Signals for external register expansion	
ClkExR	Clock for external shift registers	B12
ToExR1	Data output for external shift registers without using the SUPI 3 internal registers	B2
ToExR2	Data output for external shift registers after use of the SUPI 3 internal registers	B2
FromExR	Data input for external shift registers	ST
LaOuD	Latch signal of output data shift registers -> latch registers	B2
LaOuC	Latch signal of control data shift registers -> latch registers	B2
/LaInD	Latch signal of input data peripherals -> shift registers	B2
/ResReg	Reset signal for external latch registers. Can also be used as the "INTERBUS reset inactive" alarm output	B12
/ResU	Initialization reset	ST
V_{DD}	+5 V supply voltage	
V_{SS}	Ground	

* The MAU warning bits (**M**edium **A**ttachment **U**nit) indicate a critical, but still functioning transmission path. MAU warnings can only be used in dedicated 2-wire operation (as MAU warning input filtered with t_{f3}=520 µs). See also "Diagnostic inputs and outputs" on page 3-32

** These inputs require a hardware connection and the levels applied must not be modified during bus operation. (See Section "Overview" on page 2-1 and Section "Overview" on page 3-1)

*** The filtering causes the signals to have the same state for at least t_{fi} before a modified signal state becomes effective internally.

Explanation of cell types

BDp	Bidirectional, with Schmitt trigger inputs with internal pull-up resistor (50 kΩ typical) and 4 mA driver outputs
CI	CMOS input
CIp	CMOS input with internal pull-up resistor (50 kΩ typical)
ST	Schmitt trigger input
STp	Schmitt trigger input with internal pull-up resistor (50 kΩ typical)
B2	2 mA output
B12	12 mA driver output
OSC	Oscillator cell

1.4 Basic wiring

1.4.1 Clock, initialization

Clock supply

The SUPI 3 has an on-chip oscillator. Therefore, for applications in which the 15 MHz clock required by the SUPI 3 is of no further use, it is sufficient to use a 16 MHz quartz. The quartz is connected to the OSC1 and OSC2 pins. With the two capacitors that are connected from OSC1 and OSC2 to ground, the quartz forms a three-point oscillator. To set the working point of the on-chip oscillator, a 1 MΩ resistor is inserted, from OSC1 to OSC2, in parallel to the quartz. The capacitor values given in Figure "Clock lines of the SUPI 3" on page 1-16 are only a typical case. Please observe that due to the board layout the interfering capacitances have a considerable effect on the response time of the quartz oscillating circuit. Therefore, it is required to check, as for any other design, the correct behavior in the specified range and to modify the proposed values, if necessary. Tests of typical layouts with the quartz elements recommended in the component reference list of the INTERBUS Club have shown a safe response with the circuit and case capacitances of 22 pF each described in the SUPI 2 manual. The circuit of Figure 1-5 should be used for new designs or redesigns.

With this clock no other components must be operated additionally when a quartz crystal is used. The oscillator can also be operated by an external 16 MHz clock with a CMOS level. In this case, the oscillator operates as a buffer. The external clock signal is to be connected to the OSC1 oscillator input.

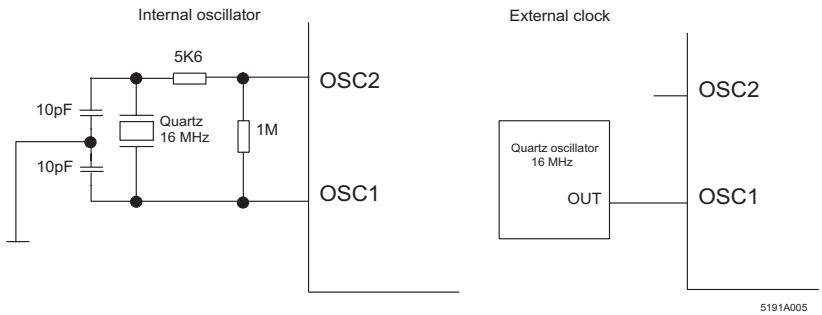


Figure 1-5 Clock lines of the SUPI 3

For the clock applies:

f = 16 MHz ± 100 ppm

Clock ratio: 50% ± 10% duty cycle

The permissible deviation applies to both short-time as well as long-time stability.

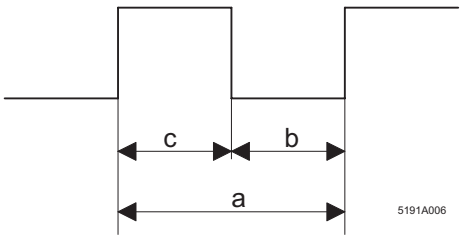


Figure 1-6 Clock ratio for the clock of INTERBUS protocol chips

Table 1-6 Clock timing

Designation	Name	Symbol	Min.	Typical	Max.	Unit
a	Clock period	t_C	62.5 -6.25	62.5	62.5 +6.25	ns ps
b	Pulse width high	t_{pH}	25	31.25	37.5	ns
c	Pulse width low	t_{pL}	25	31.25	37.5	ns

Initialization

To put the SUPI 3 to a defined state after power up, the initialization input /ResU should be set to low during power up. During operation, /ResU should be set to high. The reset time must be at least 2 clock cycles (125 ns) when the oscillator has settled and the voltage has been applied. During the reset phase all outputs have a low level. If in microprocessor applications the "µP_not_Ready" ID code is not used (see Section "ID code register" on page 3-20), the SUPI 3 must be initialized before the INTERBUS master is started up.

Reset conditions

The following conditions must be met for the INTERBUS reset at protocol chips of the 3rd generation (SUPI 3 kernel):

– The voltage must be monitored in the specified range (5 V ± 10%).
– The reset time must be at least 2 clock cycles (125 ns) when the oscillator has settled and the voltage is reached.
– The reset must not be influenced by software, LCAs, or similar.

In particular, the reset must not be controlled by a microprocessor.

NOTE: For indirect and direct connection of the reset input, the components used in the entire voltage range of the voltage monitor must be operated in accordance with regulations. Standard logic gates are not suitable for this purpose.

1.4.2 Configuration options

INTERBUS interfaces

The SUPI 3 has two separate INTERBUS interfaces, and one interface to the application. The SUPI 3 chip can be interfaced to the INTERBUS remote bus or local bus. The RGNDA pin of the SUPI 3 determines whether the chip will be used for a remote or local bus device.

In addition, pins KM0, KM1 and CKO1 have to be configured according to the following table.

Table 1-7 Configuration of the INTERBUS interface

KM0	KM1	CKO1	RGNDA	INTERBUS interface mode
0	0	-	1	8-wire local bus
1	1	0	1	2-wire local bus
1	1	0	0	2-wire remote bus 500 kbit
0	1	0	0	2-wire remote bus 2 Mbit*

* For copper interfaces only

– Pin CKO1 is the incoming INTERBUS clock line for 8-wire applications. For 2-wire applications, the pin must have a low level.

Multifunction interface

The 16-bit multifunction pin interface (MFP) is the interface to the application. Configuration pins C3, C2, C1, C0 allow the following interface connections to the INTERBUS network

Table 1-8 Configuration of the MFP interface

C3	C2	C1	C0	MFP mode
1	0	0	0	BK 8-wire local bus
0	0	1	1	BK I/O module with 8-wire local bus
0	0	0	0	BK module 2-wire branch line
0	1	0	0	BK I/O module with 2-wire branch line
1	0	0	1	16-bit output
1	0	1	0	16-bit input
1	1	0	1	8-bit input and 8-bit output
0	0	0	1	µP interface 1 byte
1	0	1	1	µP interface 2 bytes
1	1	1	1	µP interface 4 bytes
1	1	0	0	µP interface 6 bytes
0	0	1	0	µP interface 8 bytes

Identification code

Each INTERBUS device has an identification code (ID code), which can be read by the INTERBUS master (controller) in an identification cycle (ID cycle). The INTERBUS master obtains information from the identification code about the type of the device and its data register length in a data cycle. The identification code consists of three groups.

– An 8-bit code is applied to pins ID0-ID7. The INTERBUS Club has determined this code in the ID code specification, depending on the functionality of the device. An extract of these codes can be obtained from the Appendix.
– Signals ID13-ID15 are not available as pins. They are reserved for the system management (e.g. diagnostics) and cannot be changed directly by the user.
– Pins ID8-ID12 specify the physical data length of the entire bus device. It is to be set for each device according to the following table.

Table 1-9 ID code data length

ID12	ID11	ID10	ID9	ID8	Data length	Firmware version*
0	0	0	0	0	0 words	
0	0	0	0	1	1 word	
0	0	0	1	0	2 words	
0	0	0	1	1	3 words	
0	0	1	0	0	4 words	
0	0	1	0	1	5 words	
0	0	1	1	0	8 words	

Table 1-9 ID code data length (continued)

ID12	ID11	ID10	ID9	ID8	Data length	Firmware version*
0	0	1	1	1	9 words	
0	1	0	0	0	1 nibble	4.0
0	1	0	0	1	1 byte	4.0**
0	1	0	1	1	3 bytes	4.0**
0	1	1	0	0	Reserved	
0	1	1	0	1	2 bits	4.0
0	1	1	1	0	6 words	3.2
0	1	1	1	1	7 words	3.2
1	0	0	0	0	Reserved	
1	0	0	0	1	26 words	3.7
1	0	0	1	0	16 words	3.2
1	0	0	1	1	24 words	3.2
1	0	1	0	0	32 words	3.2
1	0	1	0	1	10 words	3.2
1	0	1	1	0	12 words	3.2
1	0	1	1	1	14 words	3.2
1	1	x	x	x	Reserved	

* The data length is supported by the controller board (bus master) with the specified firmware version or later.

** The data lengths 1 byte and 3 bytes are supported by the PC AT-T board, version 3.1 or later. The data lengths supported by firmware version 3.2 or later are recognized by the PC AT-T board by driver version 2.0 or later.

The length entry determines the data register length of the entire INTERBUS device - that means the total of registers configurable in the SUPI chip and additional external registers, if any. By default this length entry is wired via the SUPI 3 pins ID12-ID8 by hardware. The physical data length of the IBS SUPI 3 to be set by C0-C3 and possibly used external register must match the logic data length to be set by ID8-ID12, even if the chip was reconfigured with software afterwards (see Section "SET-I register" on page 3-16 and Section "SET-II register" on page 3-19).

Example: **SUPI 3 chip with register expansion SRE 1:**

Data length SUPI 3:	4 words	C3 to C0	0010
Data length SRE 1:	3 words		
Length entry at the ID pins	7 words	ID12 to 8	01111
(Total of SUPI 3 and register expansion)			

2 INTERBUS interfaces

2.1 Overview

When the chip is interfaced to INTERBUS it can be connected to the remote bus, installation remote bus, or local bus.

Remote bus connection is always chosen when long distances (up to 800 m via fiber-optic HCS fiber or up to 400 m via wires) have to be covered. An asynchronous 2-wire protocol and a fiber-optic or differential voltage interface according to RS-485 are used in the remote bus. Therefore the bus cable requires two fibers or five signal lines. Five signal lines for electrical transmission are necessary since there is always one wire pair for the forward and return path as well as a ground cable. A remote bus device always has its own voltage supply. In the event of a remote bus failure, the entire network can only be operated up to the last functioning remote bus device. Post-connected devices can no longer be addressed.

The installation remote bus is a special type of remote bus. In a hybrid cable it carries additional 24 V for the power supply of the I/O. This limits expansion of the installation remote bus to a maximum of 50 m.

A local bus device is used where the physical distance to the next device is limited to less than 10 m (e.g., switch cabinet level). The synchronous 8-wire protocol with CMOS levels or the 2-wire protocol with CMOS levels is used for the local bus. The entire logic required for the INTERBUS interface of a local bus device is supplied by the pre-connected bus terminal module through a supply line in the bus cable. This allows to operate the INTERBUS interface even if the voltage of the application breaks down.

When a local bus branch device fails the bus terminal module can disconnect the defective local bus branch from the network. The rest of the network can continue operation.

2.2 Local bus interface 8-wire protocol

Table 2-1 8-wire local bus configuration

KM0	KM1	CKO1	RGNDA	INTERBUS interface mode
0	0	-	1	8-wire local bus

The RGNDA pin is to be set to high and the KM0 and KM1 pins to low for local bus applications. The bus signal pins of the SUPI 3 fulfill the INTERBUS specification of the local bus. The 9 V supply of the local bus can be lowered to 5 V and monitored. The active low output signal of a monitoring module is connected to the /ResU initialization pin. The RBST pin is connected to pin 4 of the local bus output connector. The output connector of the INTERBUS cable contains a jumper. Without an output connector and thus without a jumper (RBST = 0), the outgoing interface is switched off and diverted to the return path by circuitries inside the chip.

15-pos D-SUB connectors are used for the local bus. The following table lists the assignments of the input and output interfaces.

Table 2-2 Pin assignment of the 15-pos. D-SUB INTERBUS local bus connector

Pin	Signal name of the incoming interface (male connector)	Signal name of the outgoing interface (female connector)
1	+9 V	+9 V
2	+9 V	+9 V
3	Not used	+5 V
4	Not used	RBST
5	SLI1	SLI2
6	CKI1	CKI2
7	CRI1	CRI2
8	DI1	DI2
9	GND	GND
10	GND	GND
11	/ResIn	/LBRes
12	SLO1	SLO2
13	CKO1	CKO2
14	CRO1	CRO2
15	DO1	DO2

Please refer to the Appendix for application examples.

Local bus interface 2-wire protocol

Table 2-3 2-wire local bus configuration

KM0	KM1	CKO1	RGNDA	INTERBUS interface mode
1	1	0	1	2-wire local bus

The two INTERBUS interfaces only consist of the data lines DO1, DI1, DO2, DI2 and RBST. All other input signals of the two interfaces are to be connected to a low potential. The **incoming** bus interface can be equipped with optocouplers for electrical isolation. The /RBST signal is jumpered in the output connector to V_{SS}. Without output connector (/RBST = 1), the outgoing interface is thus switched off and diverted to the return path by circuitries inside the chip.

2.3 Remote bus connection

Table 2-4 Remote bus configuration

KM0	KM1	CKO1	RGNDA	INTERBUS interface mode
1	1	0	0	2-wire remote bus, 500 kbits

Fiber-optic transmitters and receivers or RS-485 drivers are pre-connected to the INTERBUS interface. The two INTERBUS interfaces consist only of data lines DO1, DI1, DO2, and DI2. All other input signals of the two interfaces are to be connected to a low potential. The incoming bus interface is equipped with optocouplers for electrical isolation.

The RBST pin is connected to pin 9 of the remote bus output connector. Pin RBST recognizes the physical position of the device in the ring. A low potential is connected externally to this pin via a resistor. Pin 9 is jumpered to V_{DD} in the remote bus cable connector. The RBST input is thus connected to high and SUPI 3 recognizes that it is not the last device in the ring. Therefore, it forwards its data to the following device in the ring. Without output connector (RBST = 0), the outgoing interface is switched off and diverted to the return path by circuitries inside the chip.

By default, 9-pos D-SUB connectors are used for the remote bus. When using other connectors, make sure that RBST is high when the connector is connected and low when the connector is disconnected. The following table lists the assignments of the input and output interfaces.

Table 2-5 Pin assignment of the 9-pos. D-SUB INTERBUS remote bus connector

Pin	Signal name of the incoming interface (male connector)	Signal name of the outgoing interface (female connector)
1	DO1	DO2
2	DI1	DI2
3	GNDI	GND
4	Reserved	Reserved
5	Reserved	+5 V
6	/DO1	/DO2
7	/DI1	/DI2
8	Reserved	Reserved
9	Reserved	RBST

Please refer to the Appendix for application examples.

3 Application interface

3.1 Overview

The configuration of the MFP interface determines how the application accesses the INTERBUS network via the SUPI 3 chip.

Three classes are distinguished:

– Bus terminal module (BK)
– Direct input/output
– Access using a microprocessor (µP interface).

The following table lists the three classes and the configuration via pins C3, C2, C1 and C0.

Table 3-1 Operating modes of the MFP interface

C3	C2	C1	C0	MFP mode
1	0	0	0	BK module 8-wire local bus
0	0	1	1	BK I/O module with 8-wire local bus
0	0	0	0	BK module 2-wire branch line
0	1	0	0	BK I/O module with 2-wire branch line
1	0	0	1	16-bit output
1	0	1	0	16-bit input
1	1	0	1	8-bit input and 8-bit output
0	0	0	1	µP interface 1 byte
1	0	1	1	µP interface 2 bytes
1	1	1	1	µP interface 4 bytes
1	1	0	0	µP interface 6 bytes
0	0	1	0	µP interface 8 bytes

3.2 Bus terminal module mode

A bus terminal (BK) module always starts a new level in the INTERBUS system. A new level can be a remote bus or a local bus. A maximum of 16 levels (FW 4.0 or later) is permitted. BK modules are always remote bus devices.

A BK module connects the INTERBUS local bus devices in the field with the INTERBUS remote bus. The BK module makes voltage supply (9 V/1 A) available for the INTERBUS logic of the local bus devices. The BK module can also connect or disconnect the connected remote bus or local bus branch to or from the rest of the network when requested by the INTERBUS master.

A distinction is made between a standard BK module and a BK module (BK) with I/O points (BK I/O).

The standard BK module fulfills the functions described above. However, it has no I/O points so that a data length of "0" must be set. Since no external I/O points are implemented, the FromExR input pin is to be connected to the ToExR1 output.

In addition to the BK functions described above, the BK modules with I/O points can loop external in I/O points between pins ToExR1 and FromExR (see also Section 3.5). The LBST message input is used in these operating modes to recognize a connected local bus or remote bus branch cable.

BK module with 8-wire local bus branch

Table 3-2 Configuration BK module with local bus branch

C3	C2	C1	C0	MFP mode
1	0	0	0	BK module 8-wire local bus
0	0	1	1	BK I/O module with 8-wire local bus

Both operating modes provide as local bus an 8-wire interface which is available at the MFP interface according to the following table:

MFP(n)	Assignment	
0	CKI	Clock line input
1	SLI	Control line data/ID cycle input
2	DI	Data line input
3	CRI	Control line check sequence input
4	CKO	Clock line output
5	SLO	Control line data/ID cycle output
6	DO	Data line output
7	CRO	Control line check sequence output
8	ALARM	Alarm output[1]
9	X	
10	X	
11	X	
12	X	
13	X	
14	X	
15	X	

[1] The INTERBUS master can set the alarm output via a corresponding service.

X: Not to be used

In this case, the /LBRes signal belongs to the complete 8-wire local bus interface.

BK module with 2-wire branch

A second group within the "bus terminal module" class are BKs with 2-wire branch as an additional INTERBUS interface. The 2-wire branch can be used, for example, for setting up an (installation) remote bus segment or a 2-wire local bus segment. In this group a distinction is also made between a BK and a BK I/O.

Table 3-3 Configuration BK module with 2-wire branch

C3	C2	C1	C0	MFP mode
0	0	0	0	BK module 2-wire branch line
0	1	0	0	BK I/O module with 2-wire branch line

In this group the MFP interface has the following assignment:

MFP(n)	Assignment	
0	X	
1	X	
2	DI	Incoming data line
3	X	
4	X	
5	X	
6	DO	Outgoing data line
7	X	
8	ALARM	Alarm output *
9	X	
10	X	
11	X	
12	X	
13	X	
14	X	
15	X	

X: Not to be used

* The INTERBUS master can set the alarm output via a corresponding service.

3.3 Input/output mode

16-bit output

In the 16-bit output mode the INTERBUS OUT data of the first two internal OUT registers is available in parallel at the multifunction pins and can be connected directly to the application. Data is updated synchronously with the INTERBUS cycle. The outputs are 4 mA CMOS drivers. If no additional I/O points are to be used, the 'ToExR2' and 'FromExR' pins are to be connected. Should additional IN data be used, external shift registers are to be connected between pins 'ToExR1' and 'FromExR'. OUT data can be expanded by the connection of external shift registers to the 'ToExR2' pin (see also Section "Register expansion" on page 3-25).

Table 3-4 Configuration 16-bit output

C3	C2	C1	C0	MFP mode
1	0	0	1	16-bit output

Table 3-5 Assignment of the MFP interface for the 16-bit output mode

MFP(n)	Assignment	Significance
0	Byte0A(0)	2^8
1	Byte0A(1)	2^9
2	Byte0A(2)	2^{10}
3	Byte0A(3)	2^{11}
4	Byte0A(4)	2^{12}
5	Byte0A(5)	2^{13}
6	Byte0A(6)	2^{14}
7	Byte0A(7)	2^{15} MSB
8	Byte1A(0)	2^0 LSB
9	Byte1A(1)	2^1
10	Byte1A(2)	2^2
11	Byte1A(3)	2^3
12	Byte1A(4)	2^4
13	Byte1A(5)	2^5
14	Byte1A(6)	2^6
15	Byte1A(7)	2^7

Please note that the lower byte of the data word is on the MFP pins 8 to 15 and the higher byte is on the MFP pins 0 to 7.

16-bit input

In the 16-bit input mode, the application can connect 16 parallel signals directly to the multi-function pins. The inputs are designed as CMOS Schmitt triggers. Data is taken over synchronously to the INTERBUS cycle and transmitted to the INTERBUS master. The data length can be expanded by external shift registers which are connected between 'ToExR2' and 'FromExR'. Should additional OUT data be used, these external shift registers are to be connected to pin 'ToExR1'. If no external extension is necessary, pins 'ToExR2' and 'FROMEXR' are to be connected (see Section "Register expansion" on page 3-25).

Table 3-6 Configuration 16-bit input

C3	C2	C1	C0	MFP mode
1	0	1	0	16-bit input

Table 3-7 Assignment of the MFP interface for the 16-bit input mode

MFP(n)	Assignment	Significance
0	Byte0E(0)	2^8
1	Byte0E(1)	2^9
2	Byte0E(2)	2^{10}
3	Byte0E(3)	2^{11}
4	Byte0E(4)	2^{12}
5	Byte0E(5)	2^{13}
6	Byte0E(6)	2^{14}
7	Byte0E(7)	2^{15} MSB
8	Byte1E(0)	2^0 LSB
9	Byte1E(1)	2^1
10	Byte1E(2)	2^2
11	Byte1E(3)	2^3
12	Byte1E(4)	2^4
13	Byte1E(5)	2^5
14	Byte1E(6)	2^6
15	Byte1E(7)	2^7

Please note that the lower byte of the data word is on the MFP pins 8 to 15 and the higher byte is on the MFP pins 0 to 7.

8-bit input and 8-bit output

Unlike the two I/O modes described above, this mode does not represent a 16-bit, but an 8-bit device. The MFP interface is configured in such a way, that both 8-bit input, as well as 8-bit output is possible simultaneously without register expansion. The outputs are 4 mA CMOS drivers. Please observe (see also Section "Identification code") that the INTERBUS controller boards support the data length of 1 byte (8 bits) only as of firmware version 4.0. If no external expansion is necessary, the 'ToExR2' and 'FROMEXR' pins are to be connected (see Section "Register expansion" on page 3-25).

Table 3-8 Configuration 8-bit input and 8-bit output

C3	C2	C1	C0	MFP mode
1	1	0	1	8-bit input and 8-bit output

Table 3-9 Assignment of the MFP interface for the 8-bit input and 8-bit output mode

MFP(n)	Assignment	Significance	
0	Byte0A(0)	2^0 LSB	
1	Byte0A(1)	2^1	
2	Byte0A(2)	2^2	
3	Byte0A(3)	2^3	OUTPUT
4	Byte0A(4)	2^4	Byte
5	Byte0A(5)	2^5	
6	Byte0A(6)	2^6	
7	Byte0A(7)	2^7 MSB	
8	Byte0E(0)	2^0 LSB	
9	Byte0E(1)	2^1	
10	Byte0E(2)	2^2	
11	Byte0E(3)	2^3	INPUT
12	Byte0E(4)	2^4	Byte
13	Byte0E(5)	2^5	
14	Byte0E(6)	2^6	
15	Byte0E(7)	2^7 MSB	

Byte0A = Output byte

Byte0E = Input byte

Please refer to the Appendix for application examples.

3.4 µP (microprocessor) access mode

In the µP access mode it is possible to address the SUPI 3 chip from a microprocessor, like an I/O component (e.g., RAM). For this purpose, the SUPI 3 has an 3-bit bidirectional data bus D7 to D0, a 4-bit address bus A3 to A0), the active-low control signals Chip Select /CS (/ENCR, /ENDRR, /ENDRW), Read (/RD), and Write (/WR) and an active-low interrupt request line /IRQ.

Table 3-10 Assignment of the MFP interface for the µP access mode

MFP(n)	Assignment
0	A0
1	A1
2	A2
3	A3
4	/RD
5	/WR
6	/CS
7	/IRQ
8	D0
9	D1
10	D2
11	D3
12	D4
13	D5
14	D6
15	D7

Please refer to the Appendix for application examples.

MFP interface timing

The MFP interface timing is suitable for both Intel- and Motorola-based bus access. The signal /CS and /WR or /CS and /RD are connected internally such that even an inactive signal is sufficient to stop the access.

Write access

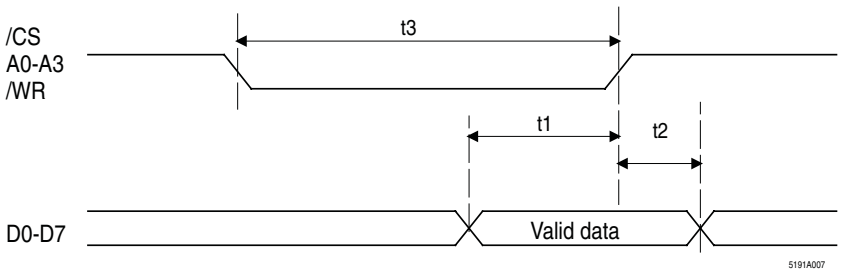


Figure 3-1 MFP interface timing, write access

Table 3-11 MFP interface timing, write access

Symbol	Explanation	Time / ns minimum
t1	Valid data before positive edge of /WR	15
t2	Valid data after positive edge of /WR	10
t3	/WR pulse width	30

Read access

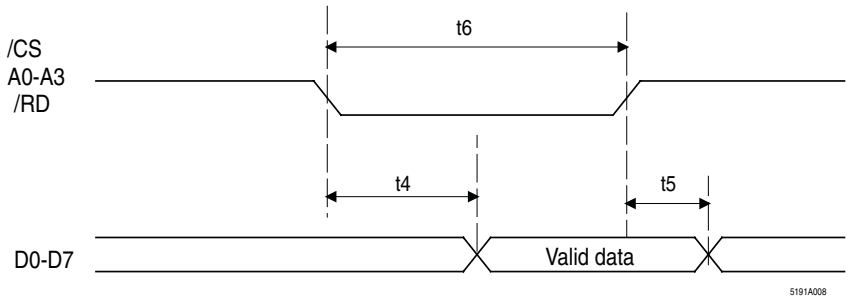


Figure 3-2 MFP interface timing, read access

Table 3-12 MFP interface timing, read access

Symbol	Explanation	Time / ns	
		Min.	Max.
t4	Valid data after negative edge of /RD		25
t5	Data bus high resistance after positive edge of /RD		25
t6	/RD pulse width	80	

µP modes of operation

Table 3-13 µP modes of operation

SUPI pin				MFP interface mode
C3	C2	C1	C0	
0	0	0	1	µP interface 1 byte
1	0	1	1	µP interface 2 bytes
1	1	1	1	µP interface 4 bytes
1	1	0	0	µP interface 6 bytes
0	0	1	0	µP interface 8 bytes

In the µP modes of operation, the data width may be varied between one and eight bytes with the configuration pins C0 to C3. The five µP modes of operation, therefore, differ only with respect to the active data length. This data length can also be changed with the software (see Section "SET-II register" on page 3-19).

Address area assignment

The following register descriptions are independent of the selected µP mode of operation. The SUPI 3 chip provides four address lines A3 to A0. The address area assignment is backward-compatible with the SUPI 2 chip.

Table 3-14 Address area assignment of the SUPI 3

Rel. address	Write register	Read register
0	IB-IN byte 0 (MSB)	IB-OUT byte 0 (MSB)
1	IB-IN byte 1	IB-OUT byte 1
2	IB-IN byte 2	IB-OUT byte 2
3	IB-IN byte 3	IB-OUT byte 3
4	Interrupt enable I	Interrupt event I
5	Set I	Interrupt event II
6	Set II	Reserved
7	ID code (low byte)	IB state
8	Cycle write	Cycle read
9	Processor message register	Processor command register
10	IB-IN byte 4	IB-OUT byte 4
11	IB-IN byte 5	IB-OUT byte 5
12	IB-IN byte 6	IB-OUT byte 6
13	IB-IN byte 7 (LSB)	IB-OUT byte 7 (LSB)
14	Interrupt enable II	Reserved
15	Test mode	Test state

All registers of the SUPI 3 chip have the default value 0. The INTERBUS IN/OUT data registers are set to their initial value 0 by /ResU and INTERBUS reset. All other registers are set to 0 only during power-up reset (/ResU). The contents of the cycle read register is mapped to the reserved read registers (relative addresses 6 and 14). To maintain compatibility with future protocol chips, these two registers should not be used.

NOTE: The test mode and test state registers (relative address 15) are used for a production test of the chip and should not be used for applications.

By writing 40_{hex} to the test mode register it is possible to mirror the WRITE registers to the READ registers so they can be read back. The READ registers are then no longer available. This can be used, for instance, to check whether writing to the registers worked correctly. Writing 00_{hex} restores the original function.

INTERBUS data registers

The INTERBUS data registers with the relative addresses 0 to 3 and 10 to 13 are provided for the I/O exchange between application and INTERBUS master. The data registers designated INTERBUS IN byte are to be written by the application, while the INTERBUS OUT byte data registers are to be read by the application. Please note that the IN bytes 0 and 1 are cleared automatically after data is transmitted over INTERBUS (default setting). If this data register is not cyclically written to, the written data item will be transmitted only once. Afterwards, the value 0 is transmitted in those bytes.

For applications in which **no** PCP communication is used, the value 04_{hex} (disable clear) is to be written once to the SET-I register with the relative address 5 after initialization has been completed. In doing so, automatic clearing of the INTERBUS IN bytes 0 and 1 is deactivated (see Section "SET-I register" on page 3-16).

The value of the data registers falls as the address rises, i.e., for a device with a data width of 8 bytes, the byte with address 0 is the high byte and the byte with address 13 is the low byte. The data registers are set to their initial value after every INTERBUS reset.

Interrupt mode

Since the connected microprocessor reads and writes the data registers asynchronously to the INTERBUS cycle, inconsistent data may occur when the reading and writing coincides with the latch update phase[1] of an INTERBUS cycle. In this phase, secured OUT data is stored in the IB OUT data registers and data is transmitted from the IB IN data registers to red to INTERBUS.

To synchronize access to the data registers, the SUPI 3 chip as an interrupt logic, which makes available several INTERBUS-cycle-synchronous events as interrupts. It is also possible to use certain events as polling bits. The different interrupt sources are enabled via two common interrupt enable registers by setting the corresponding bit to 1. After an interrupt event (/IRQ becomes 0) occurs, the source can either be read in the Interrupt Event I register and/or in the Interrupt Event II register. The bit which corresponds to the event is set to 1 by the SUPI 3 chip. The read access causes an automatic reset of the registers and the /IRQ request line after an interrupt.

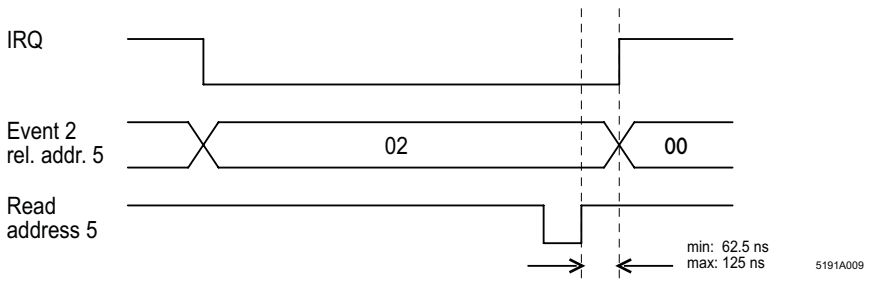


Figure 3-3 Timing of the interrupt signals using the example of the DATA cycle interrupt

[1] The latch phase completes the check sequence of every INTERBUS cycle

Interrupt enable register

The interrupt enable registers enable the interrupt sources of the interrupt event register separately. An interrupt is enabled when the corresponding bit is set to 1. The RESET value of the interrupt enable register is 0.

Interrupt enable I register, **Relative write address: 4**

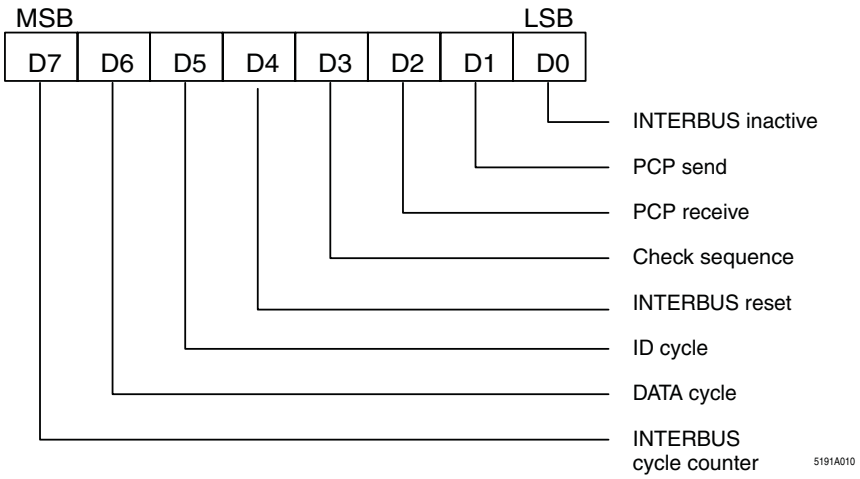


Figure 3-4 Assignment of the interrupt enable I register

Interrupt enable II register, **Relative write address: 14**

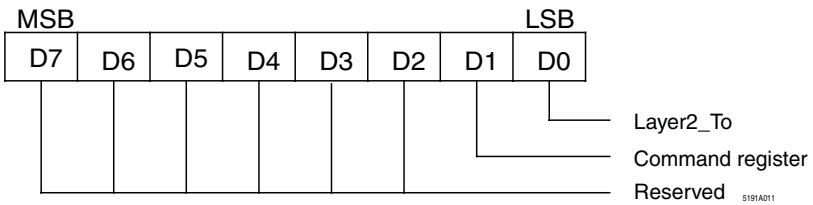


Figure 3-5 Assignment of the interrupt enable II register

Interrupt event register

The interrupt event registers store events which have caused an interrupt. Access to this register is only permitted after an interrupt request. Polling these registers is not permitted.

Interrupt event I register, **Relative read address: 4**

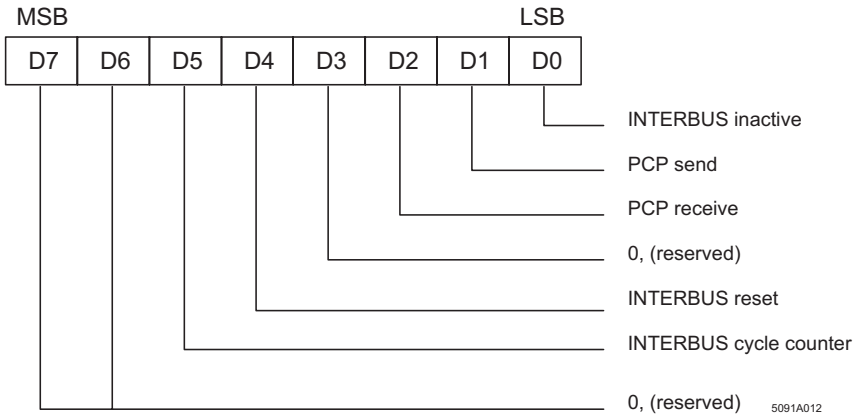


Figure 3-6 Assignment of the interrupt event I register

Interrupt event II register, **Relative read address: 5**

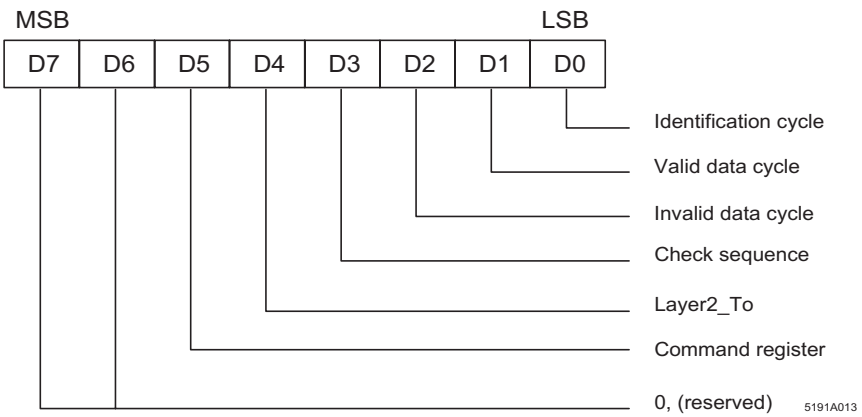


Figure 3-7 Assignment of the interrupt event II register

Explanation of the interrupt sources

INTERBUS inactive	A watchdog which monitors INTERBUS activity and which can be parameterized via the SET-I register elapsed. This means that user data was not updated during this time. This event also resets the Bus Active (BA) diagnostic signal. INTERBUS data registers are not reset (see Section 3.4.2).
PCP send	Interrupt source for PCP communication. If this interrupt is present, the CPU can write a new communication word to the SUPI 3 chip. The SEND interrupt identifies the end of a data or ID cycle.
PCP receive	Interrupt source for PCP communication. If this interrupt is present, the CPU can read a new communication word from the SUPI 3 chip. Interrupt receive identifies the end of a valid data cycle with IDLE bit = 1.
INTERBUS reset	This INTERBUS device has been set to the reset state, due to a fatal error or by the master using the INTERBUS reset ("Alarm Stop Request" command at the master). **This event should always be evaluated.** The INTERBUS data registers are reset.
INTERBUS cycle counter	An 8-bit counter loaded via the register, with the relative address 8 and value n, counted n valid data cycles. Before the interrupt occurs, the current counter value can be read via relative address 8 (see Section "Cycle read and cycle write registers" on page 3-24).
Identification cycle	This interrupt indicates the end of an identification cycle.
Valid data cycle	This interrupt indicates the end of a data cycle. Current OUT data is present. This interrupt can also be used to synchronize CPU access to the SUPI 3 chip. Data can be read and/or written again.
Invalid data cycle	After his IR event, data of the OUT bytes originates from the last valid data cycle, since the just finished data cycle has been detected invalid. Although the CPU may write to IN bytes and read the OUT bytes.
Check sequence	The check sequence* has been initiated by the INTERBUS master. IN and OUT bytes can only be written or read for 60 µs.
Layer2_To	A time basis on the chip which is independent of the bus monitors cyclic operation. Layer 2 monitoring can only be set by the INTERBUS master (FW 4.0 or later). If no valid INTERBUS cycle is detected within the time preset by the master (50 ms, 200 ms, 1000 ms, off) process data is reset. The /ResReg signal is activated for connected external registers, if any. A single pulse of 375 ns is generated. The event is communicated to the microprocessor of the device with an interrupt. (G4 error message: $0C6B_{hex}$)

Command register	In an ID cycle, the master can write to the contents of the command register. A connected microprocessor receives an interrupt with every new command, if it was switched on (see also Section "Processor alarm register and processor command register" on page 3-24).

* The check sequence completes an INTERBUS cycle and ensures the validity of the data transmitted.

3.4.1 Synchronization options

To ensure data consistency, CPU access to the SUPI 3 chip must be synchronized with the INTERBUS cycle. In principle, there are two options for synchronizing the CPU access with the INTERBUS cycle:

– Using interrupts
– Using a polling bit

Using interrupts

When interrupt-controlled synchronization is used, the "Data Cycle" interrupt is suitable.

How to proceed

The interrupt is enabled by writing 40_{hex} to the interrupt-enable-I register with the relative address 4 (only once during initialization). After each interrupt request (/IRQ becomes low), the interrupt-event-II register with the relative address 5 has to be read. If the contents of this register is 02_{hex}, current data can now be read out of the OUT data registers. If the contents of the register is 04_{hex}, OUT data originates from the last valid data cycle. Independent of the contents of the interrupt-event-II register, the CPU can write to and read from the INTERBUS IN and OUT data registers after the interrupt request. After reading the interrupt-event-II register, the contents are cleared automatically and the IRQ line becomes inactive.

Time requirements

After an interrupt request (/IRQ low), the CPU in and ideal system has the following time periods available for reading the interrupt-event-II register and the INTERBUS OUT data registers as well as for writing the INTERBUS IN data registers:

$$\mathbf{T = 13 * (5 + n) * t_{Bit}}$$

t_{Bit} : Length of an INTERBUS bit (2 µs, typical)

n : Number of bytes in the entire network

T : Permissible access time of the CPU

The minimum time T occurs when the INTERBUS NETWORK comprises one device only.

Example:

Implemented device: 2 words (32 bits). The input and output direction is to be used.

The worst case time amounts to

-> T = 234 µs

After an interrupt request, the CPU has a maximum of 234 µs to read the interrupt-event-II register and the INTERBUS OUT data registers 0 to 3 and to write the IN data registers 0 to 3.

Using a polling bit

If it is not possible in the application to achieve synchronization with interrupts, the "I/O access" bit can be polled. For this purpose, the IB-state register with relative address 7 must be read.

If the "I/O access" polling bit has the value 1, INTERBUS data registers must no longer be accessed. If the I/O access bit is 0, access to the data registers may take place during the next 34 bit times. This time is independent of the device data length and the INTERBUS configuration. Therefore, synchronization via the polling bit places higher time demands on the CPU (see Section "IB state register" on page 3-23).

3.4.2 SET-I register

Relative write address: 5

The SET-I register allows to parameterize the INTERBUS watchdog and the length entry of the identification word can be preset.

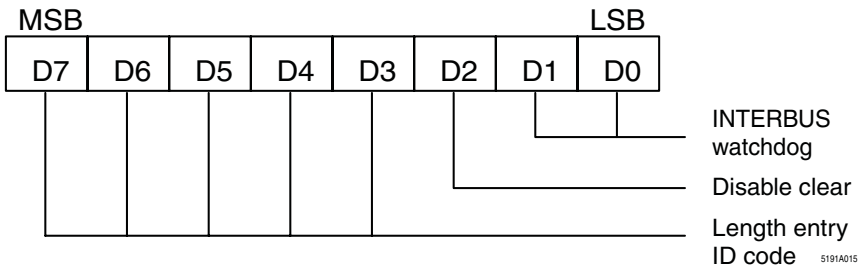


Figure 3-8 Assignment of the SET-I register

Description of the INTERBUS watchdog

The INTERBUS watchdog monitors Layer 2 transmission on INTERBUS. The watchdog is reset with every valid cycle. It has no effect on the data registers of the SUPI 3 chip.

The watchdog has two outputs:

– BA output (Bus Active)
  This output which is available as physical pin on the SUPI 3 chip is used as the diagnostic output BA. The off-delay of BA is as long as the INTERBUS watchdog.
– Interrupt source "INTERBUS inactive".
  This interrupt is generated if the SUPI 3 chip has not detected any valid data cycle until after the watchdog time elapsed.

The following table shows the parameterization options.

Table 3-15 INTERBUS watchdog in the SUPI 3 chip

D1	D0	Watchdog time in ms
0	0	630 - 635 (default)
0	1	315 - 320
1	0	143 - 148
1	1	73 - 78

Disable clear

In order to support PCP communication, INTERBUS IN bytes 0 and 1 which form the communication channel for PCP devices, are automatically cleared after they have been taken over by INTERBUS. The clearing mechanism is enabled by default. To use IN bytes 0 and 1 for dedicated I/O applications, the clearing mechanism can be disabled with the 'Disable Clear' bit. After this bit has been set the data item written in IN bytes 0 and 1 is transmitted in each data cycle. Thus, IN bytes 0 and 1 act in the same way as IN bytes 2 to 3 and 10 to 13.

Table 3-16 PCP bit

	'Disable Clear' bit
PCP device	0
I/O device	1

Length entry of the identification code

The length entry determines the data register length of the entire INTERBUS device, i.e. all external registers are included. By default, this length entry is wired via the SUPI 3 pins ID12-ID8 by hardware. The SUPI 3 chip offers the possibility of setting the length entry of the identification code in the SET-I register by means of software. This allows to adapt the data length to the application without changing the hardware.

Set the 'ID Length' bit in the SET-II register to 1 so that the length entry can take effect. The external setting is always the default setting.

Table 3-17 Mapping of the SET-I register to the length entry in the ID code

SET-I register	D7	D6	D5	D4	D3
ID code	D12	ID11	ID10	ID9	ID8

A flexible setting of the data register length is also possible with the hardware setting of the "µP_Not_Ready" ID codes (see Section "ID code register" on page 3-20).

The meaning of the ID lengths bits ID12-ID8 can be obtained from the following table.

Table 3-18 Encoding of the data length in the SET-I register

ID12	ID11	ID10	ID9	ID8	Data length	Firmware version*
0	0	0	0	0	0 words	
0	0	0	0	1	1 word	
0	0	0	1	0	2 words	
0	0	0	1	1	3 words	
0	0	1	0	0	4 words	
0	0	1	0	1	5 words	
0	0	1	1	0	8 words	
0	0	1	1	1	9 words	
0	1	0	0	0	1 nibble	4.0
0	1	0	0	1	1 byte	4.0**
0	1	0	1	1	3 bytes	4.0**
0	1	1	0	0	Reserved	
0	1	1	0	1	2 bits	4.0
0	1	1	1	0	6 words	3.2
0	1	1	1	1	7 words	3.2
1	0	0	0	0	Reserved	
1	0	0	0	1	26 words	3.7
1	0	0	1	0	16 words	3.2
1	0	0	1	1	24 words	3.2
1	0	1	0	0	32 words	3.2
1	0	1	0	1	10 words	3.2
1	0	1	1	0	12 words	3.2
1	0	1	1	1	14 words	
1	1	x	x	x	Reserved	3.2

* The data length is supported by the controller board (bus master) with the specified firmware version or later.

** The data lengths 1 byte and 3 bytes are supported by the PC AT-T board, version 3.1 or later. The data lengths supported by firmware version 3.2 or later are recognized by the PC AT-T board by driver version 2.0 or later.

The length entry determines the data register length of the entire INTERBUS device - that means the total of registers configurable in the SUPI chip and additional external registers, if any.

3.4.3 SET-II register

Relative write address: 6

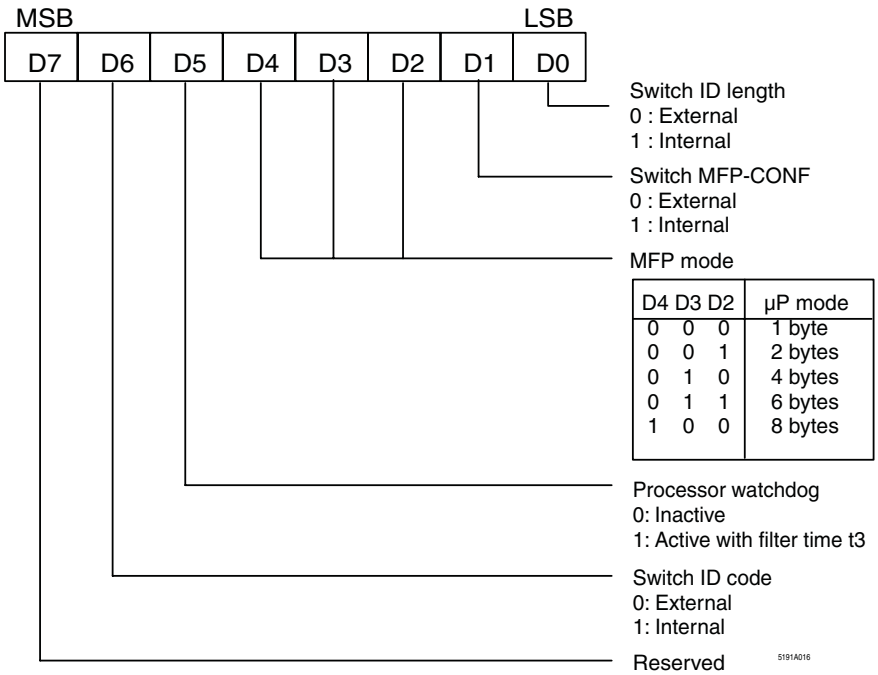


Figure 3-9 Assignment of the SET-II register

For the internal ID code setting, bits D0 and D1 must be set to "internal".

Switch ID length

This bit allows to separate the hardware connections of pins ID12 to ID8 and to reroute them to bits D7 to D3 of the SET-I register. The bit must always be considered together with Switch ID code (bit 6), see below.

Switch MFP CONF

MFP CONF allows to separate the hardware connections of pins C3 to C0 and to map them to the table with bits D4 to D2 of the SET-II register.

MFP CONF mode

In the µP modes of operation the internal SUPI 3 register length can be set using this table.

Processor watchdog

The /StatErr pin can be used, for example, to indicate a breakdown of the I/O voltage in the slave or the release of an external processor watchdog. The microprocessor can select whether this pin is active as "I/O error" with a filter time of t_{f1} (270 ms) or as input for a µP watchdog with a filter time of t_{f3} (2.5 µs) by bit 5 in the SET-II register. Setting the bit results in selecting the µP watchdog function. Bit D5 of the SET-II register is mapped to the message bit register. The master recognizes which of the functions is active and corresponding messages are generated.

Switch ID code

If "Switch ID code" is set together with "Switch ID length", the lower byte of the ID code is set according to the contents of the register with the relative write address 7. Hardware settings at ID pins ID0 to ID7 are then ignored. The "Switch ID code" bit can only be activated when the "Switch ID length" bit is set.

3.4.4 ID code register

The ID code is defined in the INTERBUS Club ID Code Specification depending on the functions of the device. An extract from this code can be found in Appendix. By default, this ID code is specified by the hardware of SUPI 3 pins ID0 to ID7. The SUPI 3 offers the option of setting the ID code in the ID code register (relative address 7) with software. This makes it possible to adapt the ID code to the application type without modifying the hardware.

In order to make the ID code in the ID code register (relative address 7) valid, the "Switch ID code" bit in the SET-II register must be set to 1. The external setting is always the default setting.

Table 3-19 Mapping of the ID code register to the ID code

ID code register	D7	D6	D5	D4	D3	D2	D1	D0
ID code	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

A flexible setting of the ID code is also possible by setting the "µP_Not_Ready" ID code (see""µP_not_Ready" ID code" on page 3-21).

Application example

The following example is to show how to proceed when you are using the ID length and MFP mode bits:

Example:

Depending on the degree of extension, an application requires data lengths of 16 to 32 bits as input, output, or I/O module. The changeover is to be done without changing the hardware, i.e. by the CPU with software.

Solution:

The SUPI 3 is set to the "µP-Interface 2 byte" mode using hardware pins C3-C0=1011b and to a data length of one word using pins ID12-ID8 = 00001b. ID code 03_{hex} is set to ID pins (ID0-ID7). If the application requires a data length of 32 bits as an output module, the following write commands have to be executed:

– Writing 14_{hex} in the SET-I register (write address 5)

– Writing 01_{hex} in the ID code register (write address 7)
– Writing $4B_{hex}$ in the SET-II register (write address 6)

Please note, that these changeover commands can only be executed during the initialization phase of the SUPI 3 chip, that means before the master started the first ID cycle and not during operation.

Alternatively, the SUPI 3 chip offers the possibility of using the "µP_Not_Ready" ID code for operation with microprocessor. This variant should be preferred to the direct changeover explained above.

"µP_not_Ready" ID code

With the "µP_Not_Ready" ID codes, subsequent initialization of the SUPI 3 chip is easily possible for a µP application. **It is irrelevant when the SUPI 3 is initialized.** The bus master can operate the bus in any case and expects the new configuration of devices not yet initialized. This function is supported by firmware version 4.0.x or later.

For microprocessor applications, two "µP_Not_Ready" ID codes are defined.

"µP_not_Ready" ID code
– Remote bus device ID: 38_{hex}
– Local bus device ID: 78_{hex}

If one of the two codes is applied to pins ID7-ID0, new functions are internally active:
1. The created ID code is valid after power up.
2. The data length is set to zero inside the chip.
3. The data length zero is entered in the ID register, independently of the code at pins ID12-ID8.
4. After the microprocessor has written the Set-II register (address 6), further access to all initialization registers (write address 5, 6 and 7) is disabled.

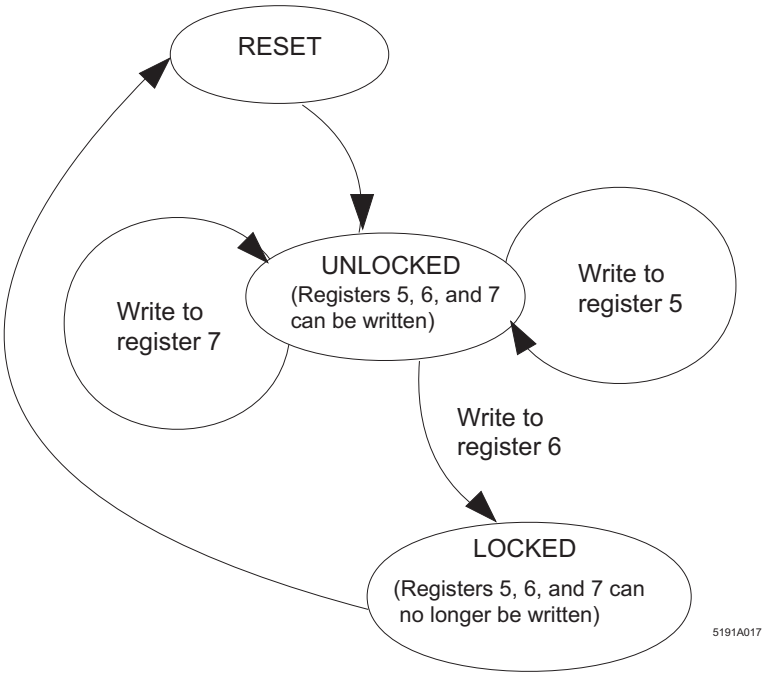


Figure 3-10 Flow chart for the initialization with created "µP_Not_Ready" ID code

The SET-II register can only be written once after RESET (UNLOCKED state). The registers with write addresses 5 and 7 must therefore be written before. In this way initialization data is changed only once during operation. In addition, the bus master recognizes microprocessor devices that have not been initialized via the "µP_Not_Ready" ID code and expects a re-initialization with the correct values. However, bus operation is still possible since there a devices with the data length zero on the bus that have not yet been initialized. After writing to register 6. the "locked" state is achieved.

Application example

The following example shows you how to proceed when using the "µP_Not_Ready" ID code.

Example:

Depending on the degree of extension, an application requires data lengths of 16 to 32 bits as input, output, or I/O module. The changeover is to be done without changing the hardware, i.e. by the CPU. The module is connected to the remote bus.

Solution:

The SUPI 3 is set to the " µP interface 2 byte" mode using hardware pins C3-C0 = 1011b, to a data length of one word via pins ID12-ID8 = 0 0001b, and to the "µP_Not_Ready" ID code 0011 1000b via pins ID7-ID0. When pins ID7-ID0 are set in this way, the SUPI 3 has a length of "zero" in the INTERBUS system.

If the application requires a data length of 16 bits as an I/O module, the following write commands have to be executed:

– Writing $0C_{hex}$ in the SET-I register (relative address 5)
– Writing ID code 03_{hex} in the ID code register (write address 7), and then
– Writing 41_{hex} in the SET-II register (write address 6).

If the application requires a data length of 32 bits as an output module, the following write commands have to be executed:

– Writing 14_{hex} in the SET-I register (write address 5)
– Writing ID code 01_{hex} in the ID code register (write address 7), and then
– Writing $4B_{hex}$ in the SET-II register (write address 6)

3.4.5 IB state register

Relative read address: 7

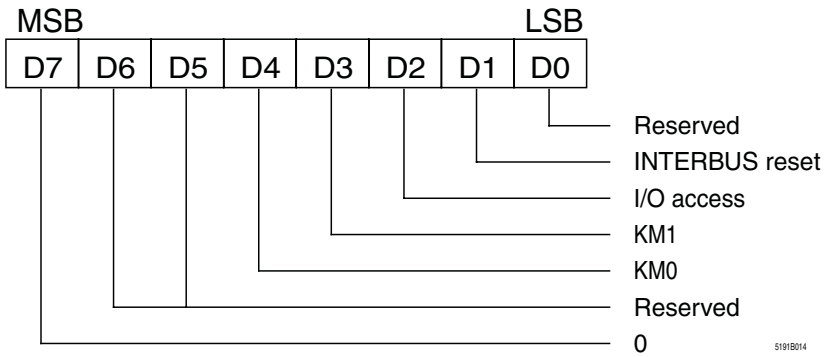


Figure 3-11 Assignment of the IB state register

Different internal operating states are mapped in the IB state register. The physical assignment of configuration pins KM1 and KM0 can be read in bits D4 and D3, immediately after the operating voltage U_L has been applied.

The active bit D2 maps the check sequence phase. The check sequence completes an INTERBUS cycle and ensures validity of the data transmitted. The I/O access bit is therefore suitable for synchronization of µP access by polling (see Section "Synchronization options" on page 3-15).

Like the "INTERBUS reset" interrupt, an active bit D1 indicates an INTERBUS reset i.e., this INTERBUS device was set to the reset state due to a fatal error or by the master using an INTERBUS reset ("Alarm Stop Request" command at the master). **This event should always be evaluated.** The INTERBUS data registers are reset.

Bits marked "reserved" have no meaning and must be masked out for evaluation.

3.4.6 Cycle read and cycle write registers

The cycle read and cycle write registers can be used for cycle-synchronous processing together with the enabled "INTERBUS cycle counter" interupt, e.g., to check the number of INTERBUS cycles from the slave application and the react on a certain (n-th) cycle. Any desired 8-bit value can be written in the cycle write register. The cycle read register is incremented with every valid data cycle. If the value of the cycle write register is reached, an interrupt is activated, bit 5 in the interrupt-event-I register is set, and the value in the cycle read register is reset to zero. Then the described procedure is repeated.

3.4.7 Processor alarm register and processor command register

The SUPI 3 offers a management channel to the bus master. This function must be enabled by the bus master and is supported by firmware 4.0 or later. Management messages from the master to the slave are received in the processor command register and can trigger an interrupt. Management messages from the master to the slave are written to the processor message register. The management channel is reserved for future applications.

3.5 Register expansion

If the data length of the SUPI 3 is to be extended, this can be done independently of the selected mode of operation, using external shift registers or the serial register expansion chip IBS SRE 1 (Order No. 2752851). The SUPI 3 chip has two data outputs which offer a simple serial interface. The ToExR1 output lies before and the ToExR2 output after the SUPI 3 internal buffers. The FromExR input can be used to return the shift register data. The ClkExR signal is to be used as a clock for the external registers. The active low /LaInD signal is used as a transfer signal from the application to the shift registers. The active high LaOutD signal is used as latch signal from the shift registers to the memory registers. The active low /ResReg reset signal is available for resetting the memory registers after an INTERBUS reset.

The possibility of expanding internal registers with external registers or the SRE 1 should be used as such. For EMC reasons it is not useful to implement an internal serial interface with remote shift registers using these signals. Extension ICs should be located as close as possible to the IBS SUPI.

3.5.1 Examples

There are various combination options for expanding the registers:

No register expansion:

Pins ToExR2 and FromExR are to be connected with each other. The internal SUPI 3 registers are used only.

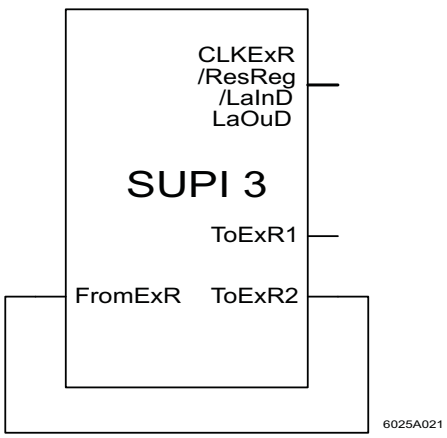


Figure 3-12 No register expansion

Expansion of the SUPI 3-internal data registers with the IBS SRE 1.

Its register length can be configured from one to six word(s).

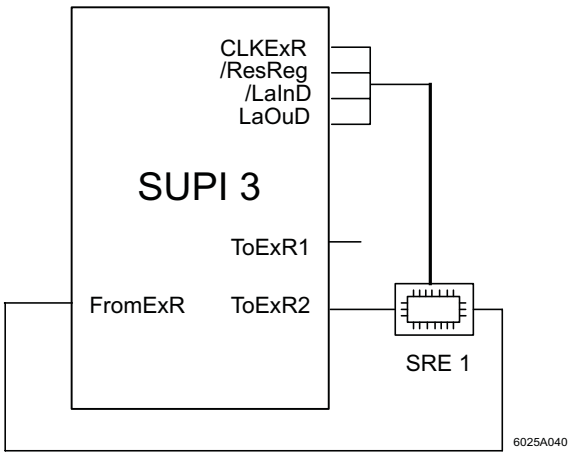


Figure 3-13 Register expansion with SRE 1

Expansion of the SUPI 3-internal INTERBUS data registers:

In this case, the external shift registers are to be connected to the ToExR2 output and to be fed back to the FromExR input. IN and OUT registers are possible.

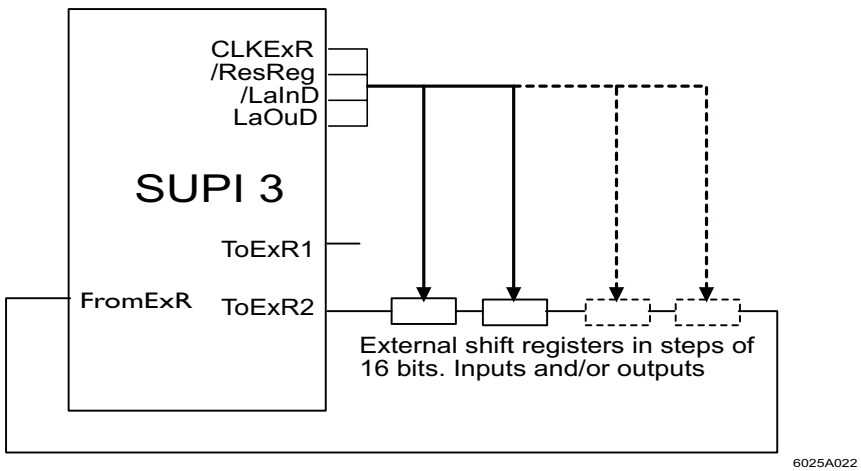


Figure 3-14 Expansion of the internal SUPI 3 registers by means of register expansion

Implementing a 16-bit device with 16 inputs and 16 outputs

Using the SUPI 3 as a 16-bit output:

In this case, a 16-bit shift register (asynchronous and parallel loading) is to be connected between pins ToExR1 and FromExR.

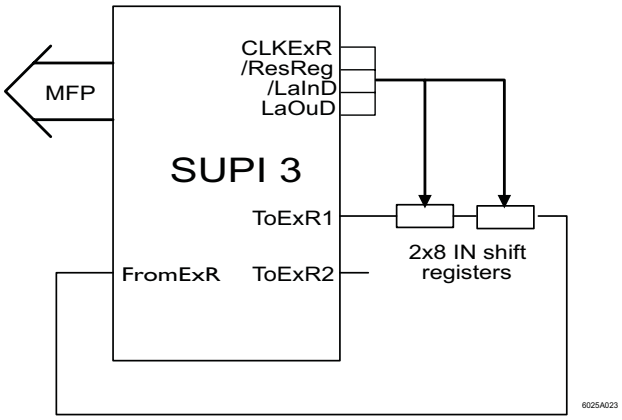


Figure 3-15 16 bit I/O device with 2x8-bit IN register expansion

Using the SUPI 3 as a 16-bit input:

In this case, a 16-bit shift register is to be connected to pin ToExR1.

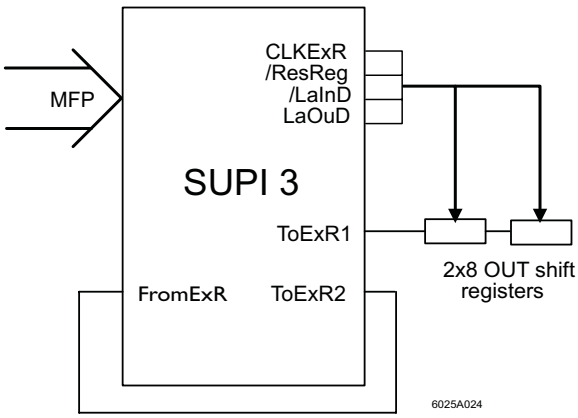


Figure 3-16 16 bit I/O device with 2x8-bit OUT register expansion

Implementing an I/O device with 32-bit input and 16-bit output:

There are different ways of assigning an address. The internal registers of the SUPI 3 can be used as inputs, outputs, or not at all. In addition it is also possible to assign different data lengths to such a device. The following figures show the different ways.

48-bit device with 16 OUT and 32 IN addresses:

The internal SUPI 3 registers have been used as outputs and expanded by 4x8 bit shift registers with inputs.

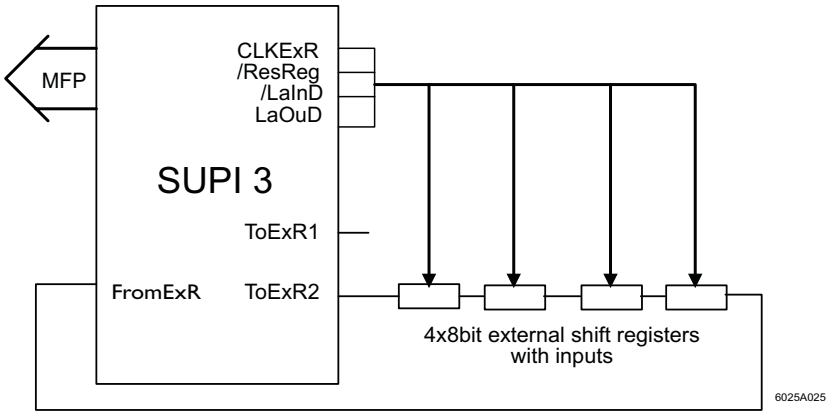


Figure 3-17 48 bit I/O device with 4x8-bit IN register expansion

48-bit device with 16 OUT and 32 IN addresses:

The internal SUPI 3 registers have been used as inputs and expanded by 4x8 bit shift registers with inputs and outputs.

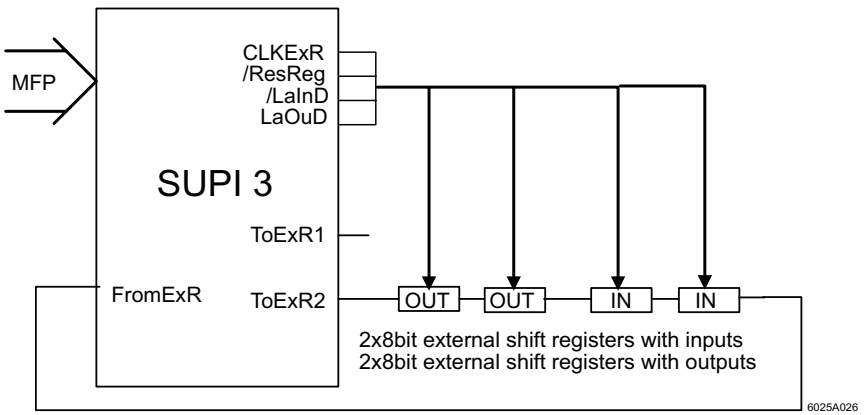


Figure 3-18 48 bit I/O device with 2x8-bit IN and 2x8-bit OUT register expansion

32-bit device with 16 OUT and 32 IN addresses:

The internal SUPI 3 registers have been used as outputs. Parallel to this, 4x8-bit shift registers with inputs have been looped in between pins ToExR1 and FromExR.

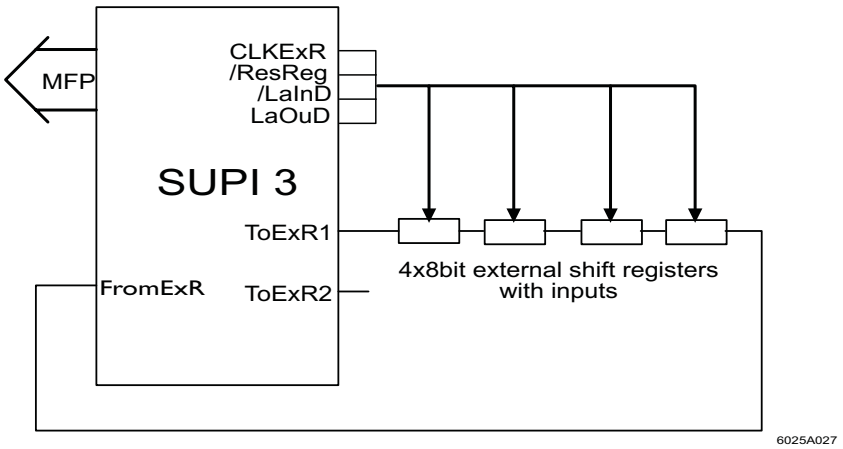


Figure 3-19 32 bit I/O device with 4x8-bit IN register expansion

32-bit device with 16 OUT and 32 IN addresses:

The internal SUPI 3 registers have been used as inputs and expanded by 2x8-bit IN registers. Parallel to this, 2x8-bit shift registers with outputs are connected with ToExR1.

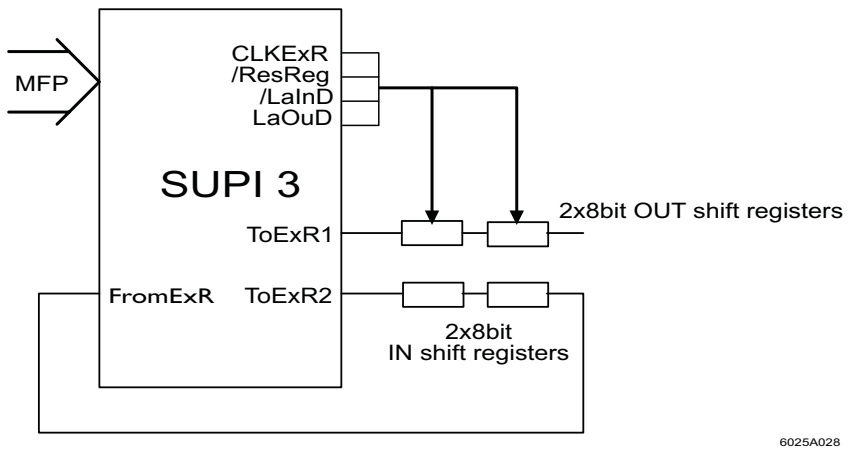


Figure 3-20 32 bit I/O device with 2x8-bit IN and 2x8-bit OUT register expansion

3.5.2 Register expansion interface timing

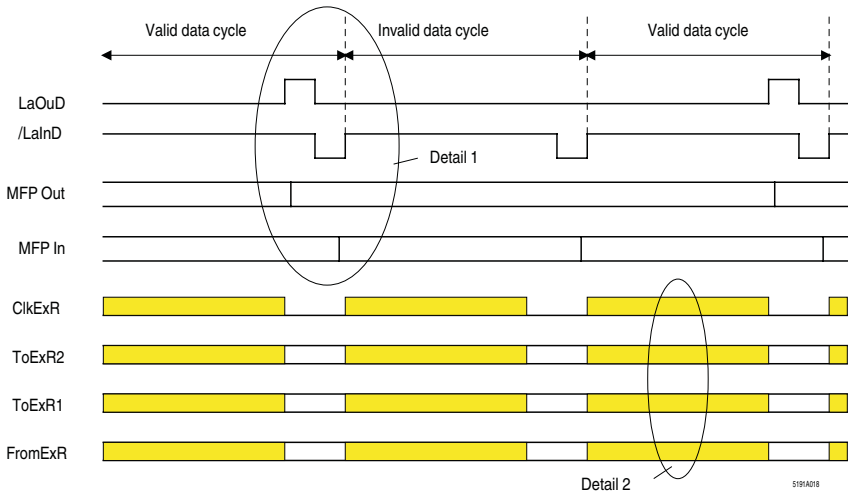


Figure 3-21 Timing diagram for register expansion

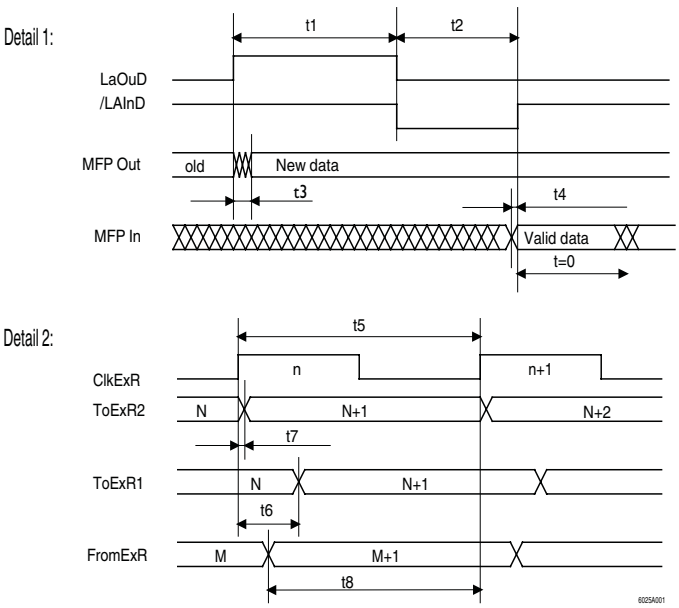


Figure 3-22 Timing diagram, in detail

Table 3-20 Timing for register expansion

Symbol	Explanation	Time / ns	
		Minimum	Maximum
t1	LaOuD length	18000	
t2	LaInD length	8000	
t3	OUT data valid after rising LaOuD edge		66
t4	IN data valid before rising /LaInD edge	19	
t5	CLKExR length	2000	
t6	ToExR1 valid after rising ClkExR edge	1000	
t7	ToExR2 valid after rising ClkExR edge	62.5	
t8	Serial data valid before rising ClkExR edge	1125	

(All outputs loaded with 30 pF)

The data at the FromExR input is always taken over with the falling edge of ClkExR. The /ResReg signal has no time reference to the other signals of the register expansion.

For a register expansion it must be ensured that the ClkExR signal is not deformed by loading with external capacitances and thus shifted excessively behind. If ClkExR is buffered, ToExR2 must also be buffered because of the signal shift. In this case, the runtimes to ToExR2 are less critical than in the cycle line itself. The times specified for the components in the shift registers used must also be considered.

Please refer to the Appendix for application examples.

3.6 Diagnostic inputs and outputs

The SUPI 3 protocol chip has different diagnostic inputs and outputs which simplify the location of error sources within the INTERBUS network. The diagnostic inputs and outputs to be used depend on the physical location of the device within the INTERBUS network and its functions.

Certification of a module by the club requires that the status of diagnostic pins and power supply is indicated with LEDs.

Remote bus device

Table 3-21 Diagnostic inputs/outputs of a remote bus device

Operating mode	CC	BA	RD	TR	/StatErr	/ModAck	LD	Conf	Error
	/ResReg		RBDA				LBDA		
Bus terminal module	M	M	M	-	O	O	M	M	O
Input/output	M	M	M	-	O	O	-	-	-
PCP device	M	M	M	M	O	O	-	-	-

M: Mandatory

O: Optional

Local bus device

Table 3-22 Diagnostic inputs/outputs of a local bus device

Operating mode	TR	CC /ResReg	BA	/StatErr	/ModAck
Input/output		O	O	O	O
PCP device	M	O	O	O	O

M: Mandatory

O: Optional

Explanation of diagnostic inputs and outputs

CC

The green CC (Cable Check) diagnostic LED is connected to the CMOS output /ResReg of the SUPI 3. CC monitors the bus activity on Layer 1 of the incoming bus. CC is active when the cable connection is good and the INTERBUS controller board is not in a reset state. The CC LED becomes inactive after an INTERBUS reset or power up reset.

BA

The green BA (Bus Active) LED at the SUPI 3 output is a Layer 2 activity display. The output has an off delay of the duration of the preset INTERBUS watchdog (default: 630 ms). See Section "SET-I register" on page 3-16.

TR The green TR (Transmit/Receive) diagnostic LED becomes active when PCP communication is being carried out via INTERBUS. It is connected to the active high SUPI 3 LBDA/TR pin in the µP modes. An external off delay is provided for this output to guarantee a visible indication on the LED. The output pulse has a minimum length of 8 µs.

RD The yellow RD LED at the RBDA output indicates statically that the outgoing remote bus (Remote Bus Disabled) is switched off. This diagnostic feature is only relevant for remote bus devices and is active in the "INTERBUS RESET" state.

LD Only for bus terminal modules shows the active high LBDA/TR pin with a yellow LED that the branch has been disconnected (Local Bus Disabled). This output is active in the "INTERBUS RESET" state.

Input/output module error

Input (/StatErr)

The active low input /StatErr is used, for example, to report a module error (e.g., I/O voltage not applied) to the INTERBUS controller board. Applying a low-level to this input causes a module error. If /StatErr is not used, it has to be statically connected to V_{DD}. The input is filtered (see Section "Signal description" on page 1-13). The default filter value is 270 ms. Setting this input causes a message (Peripheral error indication, $0BB1_{hex}$ for G4).

Acknowledge output (/ModAck)

The /ModAck output can be used to acknowledge a set module error. In the bus master, the error is acknowledged with the following command:

"Quit Peripheral Error"

This output will then be active once for 4-bit times (8 µs).

Reconfiguration request (CONF)

The active high CONF message input is used to request a reconfiguration for the INTERBUS network. If this input is not used, it has to be statically connected to V_{SS}. The input is filtered. The filter value is 35 ms. Setting this input causes a message (Reconfiguration request, $0BB1_{hex}$ for G4).

E (Error)

Only for bus terminal module applications indicates the red LED an error in the connected branch. The INTERBUS controller board activates this output with a corresponding command (0714_{hex} for G4).

MAU warning

The active high MAU inputs (MAUWH - incoming INTERBUS interface, MAUWR - outgoing INTERBUS interface, MAUWS - branch interface (only for BK modules)) indicates the impairment of the transmission quality for e.g. optical or HF paths to a critical value, however, still performing a proper function. The MAU of the corresponding interface (incoming, outgoing or branch) must be able to evaluate the receive quality and to provide this as a digital signal to the corresponding input. Setting this input causes a corresponding message (5340_{hex} for G4). This function is supported as of firmware version 4.0.x by the bus master. The inputs are filtered in the "MAU warning" function. The filter value is 520 µs.

A Technical data

Table A-1 Absolute limit values

Symbol	Parameters	Value	Unit
V_{DD}	DC supply voltage	-0.5 to +7.0	V
V_{in}	DC input voltage	-1.5 to V_{DD} + 1.5	V
V_{out}	DC output voltage	-0.5 to V_{DD} + 0.5	V
I	DC current per pin, inputs and outputs	50	mA
I	DC current per pin, V_{DD} and V_{SS} pins	75	mA

Table A-2 Recommended operating conditions

Symbol	Parameters	Min.	Max.	Unit
V_{DD}	DC supply voltage	4.5	5.5	V
V_{in}, V_{out}	DC input, output voltage	0.0	V_{DD}	V
T_A	Industrial temperature range	-40	+85	°C

Table A-3 DC data

Symbol	Parameters	Condition	-40°C to 85°C	
			Min.	Max.
V_{IH}	Input voltage high, CMOS inputs	V_{out} = 0.1 V, or	0.7 V_{DD}	-
V_{IL}	Input voltage low, CMOS inputs	V_{DD} - 0.1 V $\lvert I_{out} \rvert$ = 20 µA	-	0.3 V_{DD}
	Schmitt trigger inputs			
V_{T+}	Positive switching threshold		–	0.7 V_{DD}
V_{T-}	Negative switching threshold		0.25 V_{DD}	–
V_{Hy}	Hysteresis	V_{T+} to V_{T-}	0.12 V_{DD}	–
V_{OH}	Output voltage high			
	Outputs B2	I_{OH} = 2 mA	3.7 V	V_{DD}
	Outputs BDp	I_{OH} = 4 mA	3.7 V	V_{DD}
	Outputs B12	I_{OH} = 12 mA	3.7 V	V_{DD}

Table A-3 DC data (continued)

Symbol	Parameters	Condition	-40°C to 85°C	
			Min.	Max.
V_{OL}	Output voltage low			
	Outputs B2	I_{OH} = -2 mA	V_{SS}	0.4 V
	Outputs BDp	I_{OH} = -4 mA	V_{SS}	0.4 V
	Outputs B12	I_{OH} = -12 mA	V_{SS}	0.4 V
I_{OH}	Output current high			
	Outputs B2	V_{OH}= 3.7 V	–	2 mA
	Outputs BDp		–	4 mA
	Outputs B12		–	12 mA
I_{OL}	Output current low			
	Outputs B2	V_{OL}= 0.4 V	–	-2 mA
	Outputs BDp		–	-4 mA
	Outputs B12		–	-12 mA
I_{in}	Input leakage current, no internal pull-up resistor	$V_{in} = V_{DD}$ or V_{SS}	-5 µA	+5 µA
	Input leakage current with	PUH; $V_{in} = V_{SS}$	-30 µA	-165 µA
	internal pull-up resistor (50 kohms, typical)	PUL; $V_{in} = V_{SS}$	-15 µA	-120 µA
I_{oz}	Output leakage current	High resistance	-10 µA	+10 µA
I_{DD}	Current consumption*	–	Approx. 20 mA	–

* All input static, all outputs unused, oscillator operates with 16 MHz.

A 1 General notes about processing

These guidelines do not necessarily specify extreme conditions which must be observed for safety reasons for the named surface-mounted components (IBS SUPI 3 QFP and IBS CHIP-Muster/...). In many cases, the housings withstand much higher temperatures than standard PCBs. These guidelines are intended to create soldering conditions permitting high-quality design and minimum improvement work.

A 1.1 Storage

Table A-4 Storage

Symbol	Parameters	Value	Unit
T_{stg}	Storage temperature	5 to 30	°C
RH_{stg}	Relative humidity for storage	30 to 60	%

A 1.2 Processing time

We recommend using the ASICs within two years of delivery. Proper storage of the components in an unopened package is required for good processing.

If the ASICs are packaged in dry packs and the moisture content is OK, according to HIC, the ASICs do not have to be dried before use. If this is not the case, the ASICs can be treated according to IPC/JEDEC J-STD-20A.

A 1.3 Soldering

For information on soldering the surface-mounted components described in this manual (IBS SUPI 3 QFP and IBS CHIP-Muster/...), please refer to the "**IPC/JEDEC J-STD-020...JOINT INDUSTRY STANDARD)**" document.

This document is available upon request. Please contact Phoenix Contact.

A 2 ID code specification (extract)

Table A-5 Extract from the ID code specification

Description of module function		ID code (dec)	ID code (hex)
Bus terminal modules (BK)			
BK with 8-wire local bus branch	BK-8L-LB	52	34
BK with 2-wire local bus branch	BK-2L-LB	8	08
BK with INTERBUS-Loop branch	BK-SL	4	04
BK with 2-wire remote bus branch	BK-2L-RB	12	0C
Remote bus device (digital)			
Digital output modules	DO	1	01
Digital input modules	DI	2	02
Digital input/output modules	DIO	3	03
Profile-compliant digital output modules	PROFILE DO	13	0D
Profile-compliant digital input modules	PROFILE DI	14	0E
Profile-compliant digital input/output modules	PROFILE DIO	47	2F
ISO valve manifolds	ISO valve manifolds	5	05
Remote bus device (analog)			
Analog output modules	AO	49	31
Analog input modules	AI	50	32
Analog input/output modules	AIO	51	33
Profile-compliant analog output modules	PROFILE AO	53	35
Profile-compliant analog input modules	PROFILE AI	58	3A
Profile-compliant analog input/output modules	PROFILE AIO	59	3B
ENCOM with input data	ENCOM	54	36
ENCOM with input and output data	ENCOM	55	37
Remote bus devices with parameter channel			
Modules with parameter channel (2 PCP words) *)	PA channel	240	F0
Modules with parameter channel (4 PCP words) *)	PA channel	241	F1
Modules with parameter channel (1 PCP word)	PA channel	243	F3
DRIVECOM (2 PCP words) *)	DRIVECOM	224	E0
DRIVECOM (4 PCP words) *)	DRIVECOM	225	E1

Table A-5 Extract from the ID code specification (continued)

Description of module function		ID code (dec)	ID code (hex)
DRIVECOM (1 PCP word)	DRIVECOM	227	E3
ENCOM (2 PCP words) *)	ENCOM	244	F4
ENCOM (4 PCP words) *)	ENCOM	245	F5
ENCOM (1 PCP word)	ENCOM	247	F7
Profile-compliant modules (2 PCP words) *)	Profile PA channel	228	E4
Profile-compliant modules (4 PCP words) *)	Profile PA channel	229	E5
Profile-compliant module (1 PCP word)	Profile PA channel	231	E7
"µP_Not_Ready" (with register latching) remote bus *)	Special	56	38
"µP_Not_Ready" (for re-initialization) remote bus *)	Special	60	3C
Local bus device (digital)			
Digital output modules	DO	189	BD
Digital input modules	DI	190	BE
Digital input/output modules	DIO	191	BF
Digital INTERBUS Loop output modules	IBS Loop DO	177	B1
Digital INTERBUS Loop input modules	IBS Loop DI	178	B2
Digital INTERBUS Loop input/output modules	IBS Loop DIO	179	B3
Profile-compliant digital output modules	PROFILE DO	181	B5
Profile-compliant digital input modules	PROFILE DI	182	B6
Profile-compliant digital input/output modules	PROFILE DIO	183	B7
Wrenching controllers	Wrench. contr.	187	BB
Local bus device (analog)			
Analog output modules	AO	125	7D
Analog output modules with alarm inputs **)	AIO^2	91	5B
Analog input modules	AI	126	7E
Analog input modules with configuration outputs	AI^2O	95	5F
Analog input/output modules	AIO	127	7F
Analog input and output modules with alarm inputs and configuration outputs	AI^2O^2	83	53
Analog INTERBUS Loop output modules	AO Loop	113	71
Analog INTERBUS Loop output modules with alarm inputs	AIO^2 Loop	107	6B**
Analog INTERBUS Loop input modules	AI Loop	114	72

Table A-5 Extract from the ID code specification (continued)

Description of module function		ID code (dec)	ID code (hex)
Analog INTERBUS Loop input modules with configuration outputs	AI^2O Loop	111	6F**
Analog INTERBUS Loop input and output modules	AIO Loop	115	73
Analog INTERBUS Loop input and Loop output modules with alarm inputs and configuration outputs	AI^2O^2 Loop	99	63**
Profile-compliant analog output modules	PROFILE AO	121	79
Profile-compliant analog input modules	PROFILE AI	122	7A
Profile-compliant analog input/output modules	PROFILE AIO	123	7B
ENCOM with input data	ENCOM	102	66
ENCOM with input and output data	ENCOM	103	67
Local bus devices with parameter channel			
Modules with parameter channel (2 PCP words) *)	PA channel	220	DC
Modules with parameter channel (4 PCP words) *)	PA channel	221	DD
Modules with parameter channel (1 PCP word)	PA channel	223	DF
DRIVECOM (2 PCP words) *)	DRIVECOM	192	C0
DRIVECOM (4 PCP words) *)	DRIVECOM	193	C1
DRIVECOM (1 PCP word)	DRIVECOM	195	C3
ENCOM (2 PCP words) *)	ENCOM	212	D4
ENCOM (4 PCP words) *)	ENCOM	213	D5
ENCOM (1 PCP word)	ENCOM	215	D7
Profile-compliant modules (2 PCP words) *)	Profile PA channel	216	D8
Profile-compliant modules (4 PCP words) *)	Profile PA channel	217	D9
Profile-compliant module (1 PCP word)	Profile PA channel	219	DB
"µP_Not_Ready" (with register latching), local bus *)	Special	120	78
"µP_Not_Ready" (for re-initialization) local bus *)	Special	108	6C
"µP_Not_Ready" (for re-initialization), Loop *)	Special	104	68

* This ID code is only supported by INTERBUS masters of Generation 4 or later.

** This ID code is only supported by INTERBUS masters with firmware 4.50 or later.

A 3 Length code specification

Table A-6 ID code data length

ID12	ID11	ID10	ID9	ID8	Data length	Firmware version*
0	0	0	0	0	0 words	
0	0	0	0	1	1 word	
0	0	0	1	0	2 words	
0	0	0	1	1	3 words	
0	0	1	0	0	4 words	
0	0	1	0	1	5 words	
0	0	1	1	0	8 words	
0	0	1	1	1	9 words	
0	1	0	0	0	1 nibble	4.0
0	1	0	0	1	1 byte	4.0**
0	1	0	1	1	3 bytes	4.0**
0	1	1	0	0	Reserved	
0	1	1	0	1	2 bits	4.0
0	1	1	1	0	6 words	3.2
0	1	1	1	1	7 words	3.2
1	0	0	0	0	Reserved	
1	0	0	0	1	26 words	3.7
1	0	0	1	0	16 words	3.2
1	0	0	1	1	24 words	3.2
1	0	1	0	0	32 words	3.2
1	0	1	0	1	10 words	3.2
1	0	1	1	0	12 words	3.2
1	0	1	1	1	14 words	3.2
1	1	x	x	x	Reserved	

* The data length is supported by the controller board (bus master) with the specified firmware version or later.

** The data lengths 1 byte and 3 bytes are supported by the PC AT-T board, version 3.1 or later. The data lengths supported by firmware version 3.2 or later are recognized by the PC AT-T board by driver version 2.0 or later.

The length entry determines the data register length of the entire INTERBUS device - that means the total of register configurable in the SUPI chip and additional external registers, if any. By default this length entry is wired via SUPI 3 pins ID12-ID8 by hardware. The physical data length of the IBS SUPI 3 to be set using C0-C3 and possibly used external register must match the logic data length to be set using ID8-ID12, even if the chip was reconfigured with software afterwards (see Section "SET-I register" on page 3-16 and Section "SET-II register" on page 3-19).

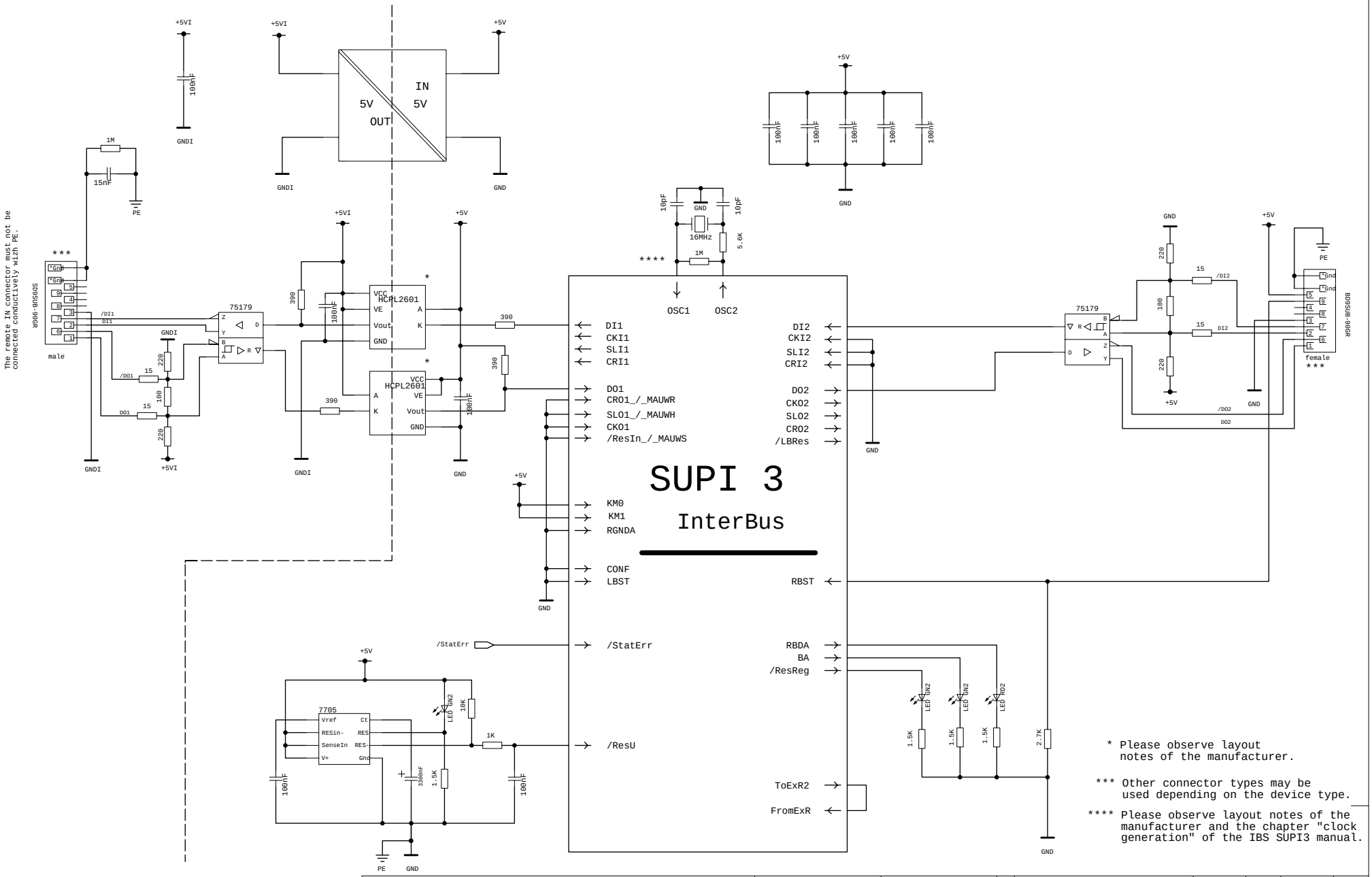
B Wiring examples

The following applies for all wiring examples:

- All resistors have a tolerance of ±1%, maximum.
- All capacitors have a tolerance of ±20%, maximum.
- Electrical isolation has to be at least 500 VAC
- Only components from the component reference list of the INTERBUS Club will be used.

The circuit diagrams were prepared with the greatest possible care. Phoenix Contact does not guarantee the correctness of the circuit diagrams.

application remote bus with optical isolation type 1



				Masstab:								
Remotebus with optical isolation typ 1		Anzahl Blaetter:	Blatt Nr.:	gepr								
PHOENIX CONTACT	1-1	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei			version 2.0	01.08.96	Lutz		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

application optical fibre remote bus

REMOTE IN

REMOTE OUT

SUPI 3
InterBus

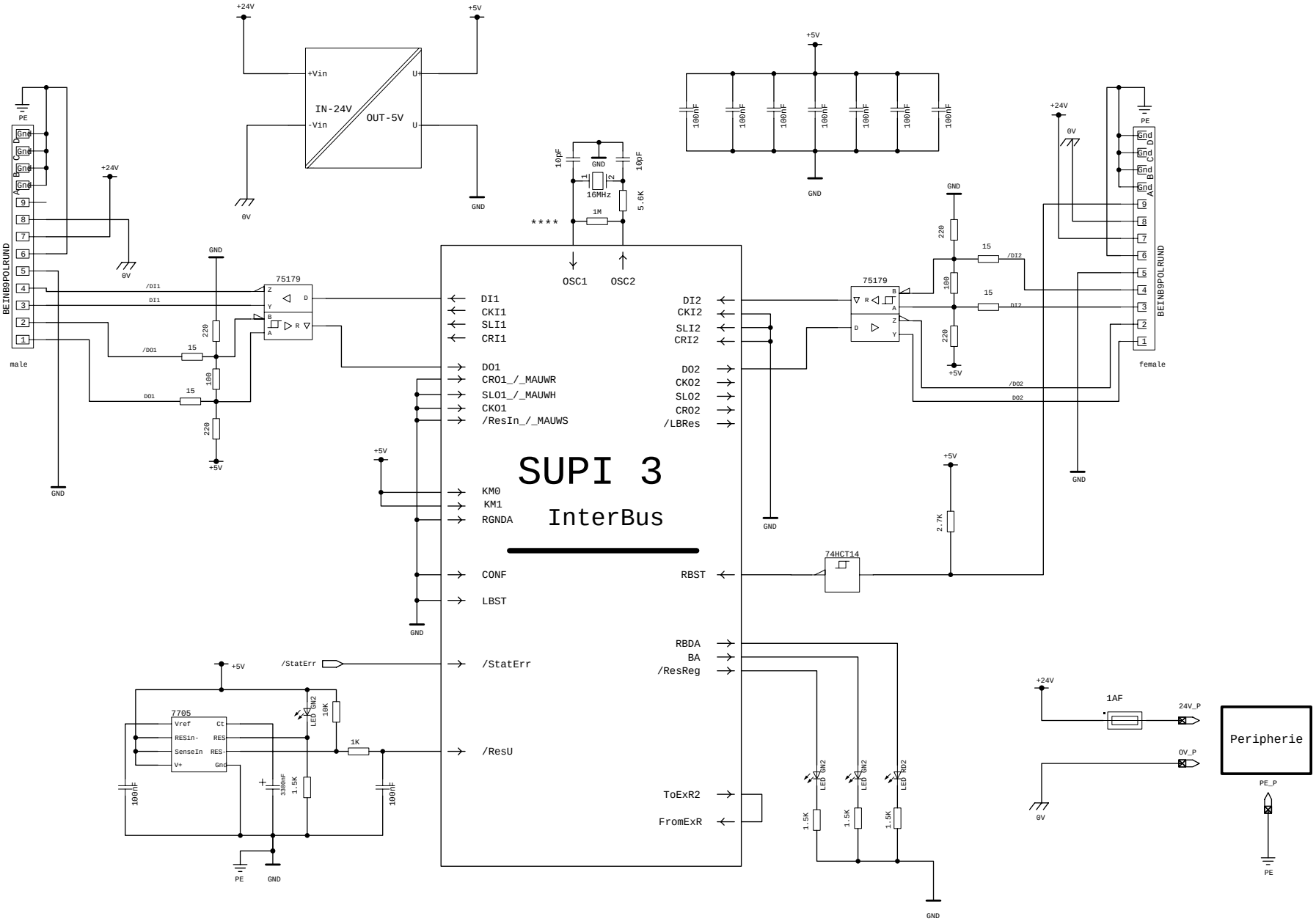
DI1
CKI1
SLI1
CRI1
DO1
CRO1_/_MAUWR
SLO1_/_MAUWS
CKO1
/ResIn_/_MAUWH
KM0
KM1
RGNDA
CONF
LBST
/StatErr
/ResU
ToExR2
FromExR
OSC2
OSC1
DI2
CKI2
SLI2
CRI2
DO2
CKO2
SLO2
CRO2
/LBRes
RBST
RBDA
BA
/ResReg

QFBR 1607
BST74A
TORX 104
74HCT04
7705
LED GN2
LED RD2
16MHz
S2xU
NEXT
END

** Leckstrom beachten.

optical fibre remote bus			Anzahl Blaetter:	Blatt Nr.:	Masstab:								
PHOENIX CONTACT	1-1	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gepr								
					gezei				version 2.01	28.04.97	Lutz		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

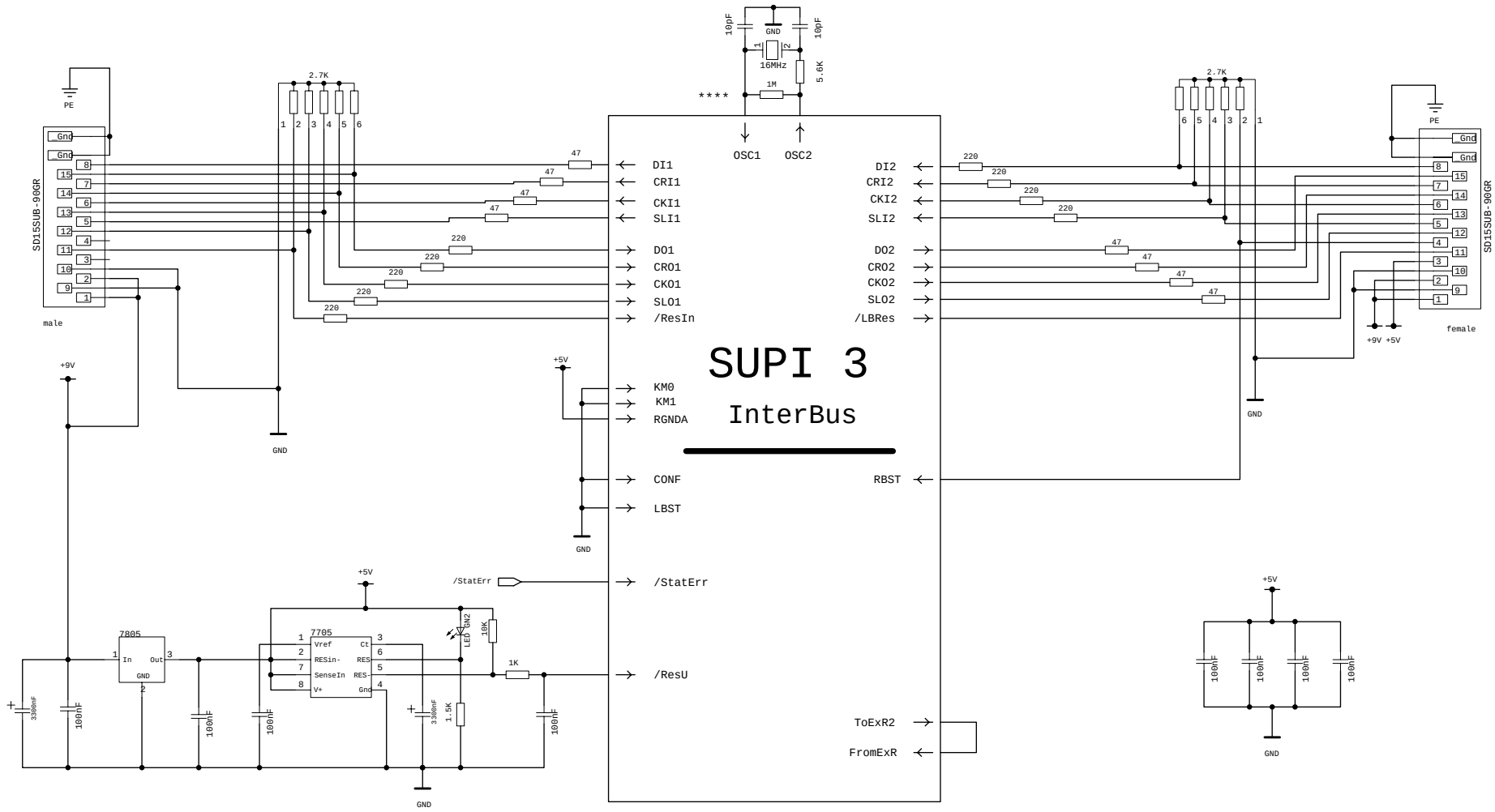
application installation remote bus



**** Please observe layout notes of the manufacturer and the chapter "clock generation" of the IBS SUPI3 manual.

				Masstab:									
appliction instalation remote bus			Anzahl Blaetter:	Blatt Nr.:	gepr								
PHOENIX CONTACT	1-4	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei				version 2.0	01.08.96	Lutz		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

application local bus

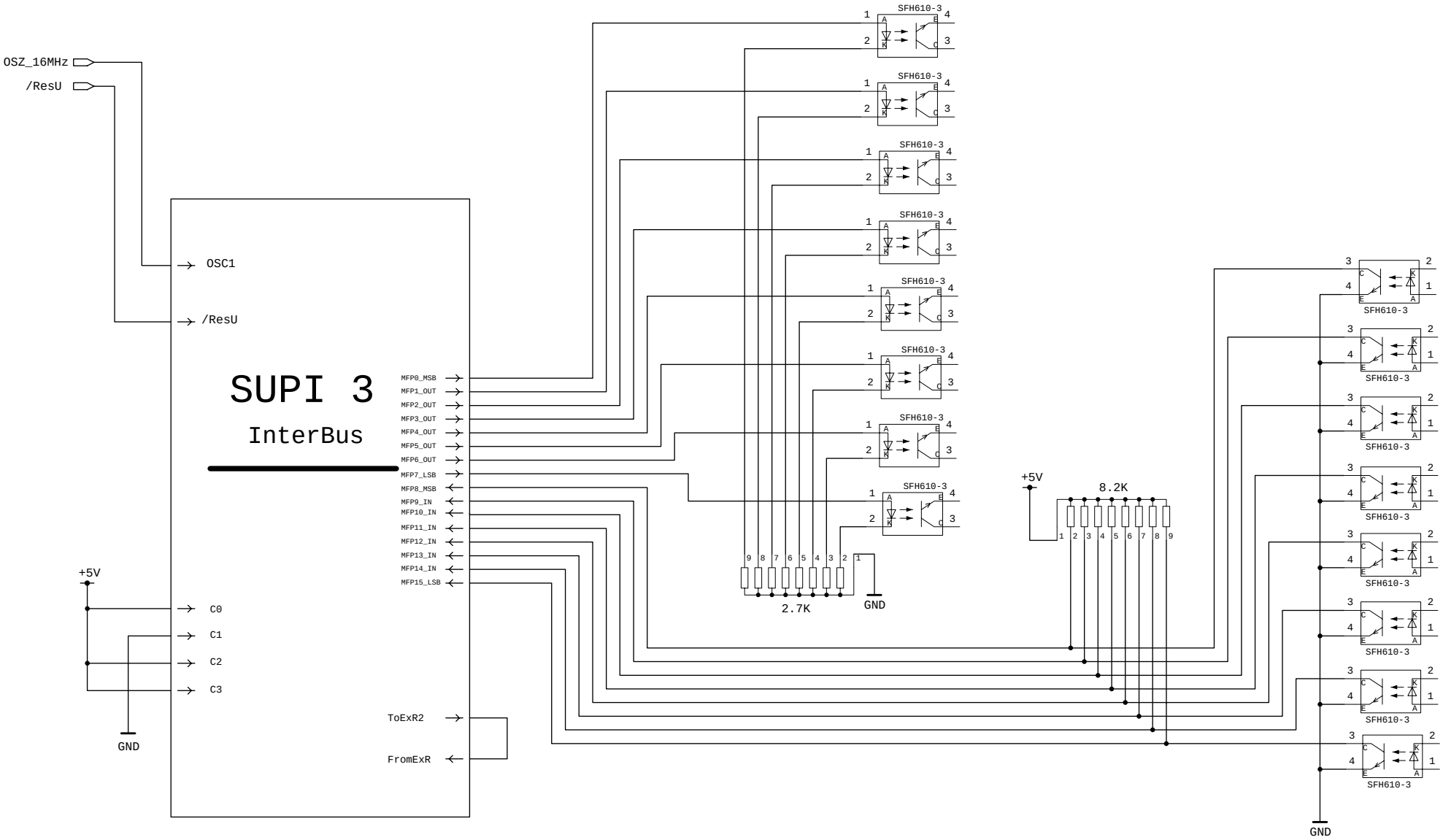


**** Please observe layout notes of the manufacturer and the chapter "clock generation" of the IBS SUPI3 manual.

The LEDs RC and BA could be connected by option.

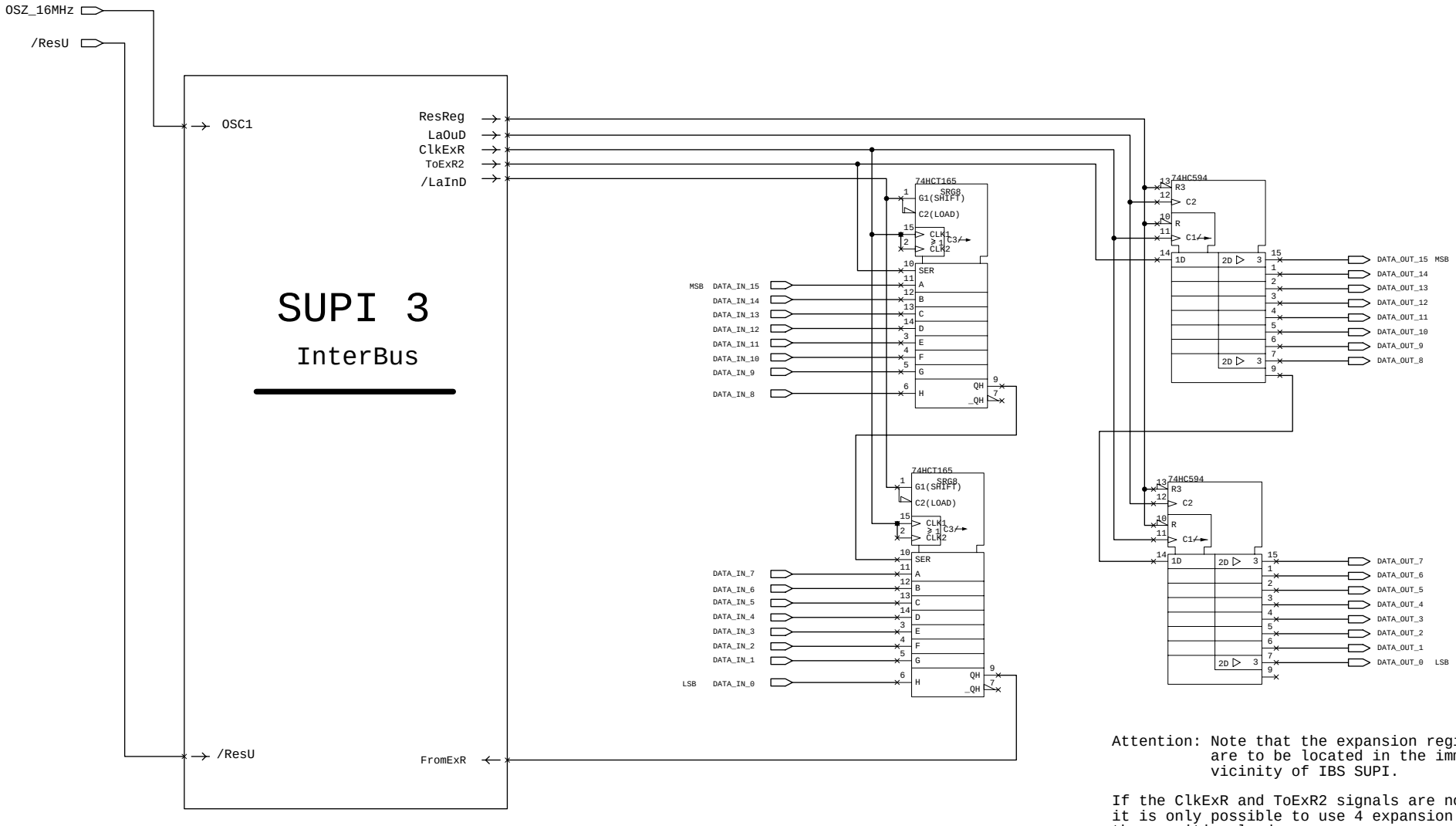
				Masstab:										
application local bus			Anzahl Blaetter:	Blatt Nr.:	gepr									
PHOENIX CONTACT	2-1	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei				version 2.0	01.08.96	Lutz			
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.	

application 8 Bit Input und 8 Bit Output



					Masstab:									
8 IN / 8 Out			Anzahl Blaetter:	Blatt Nr.:	gepr	———	———							
PHOENIX CONTACT	4-3	Z.Nr.: ———	Anzahl Kopien:	Kopie Nr.:	gezei	———	———			version 1.1	01.08.96	Lutz		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.	

application register expansion for digital I/O

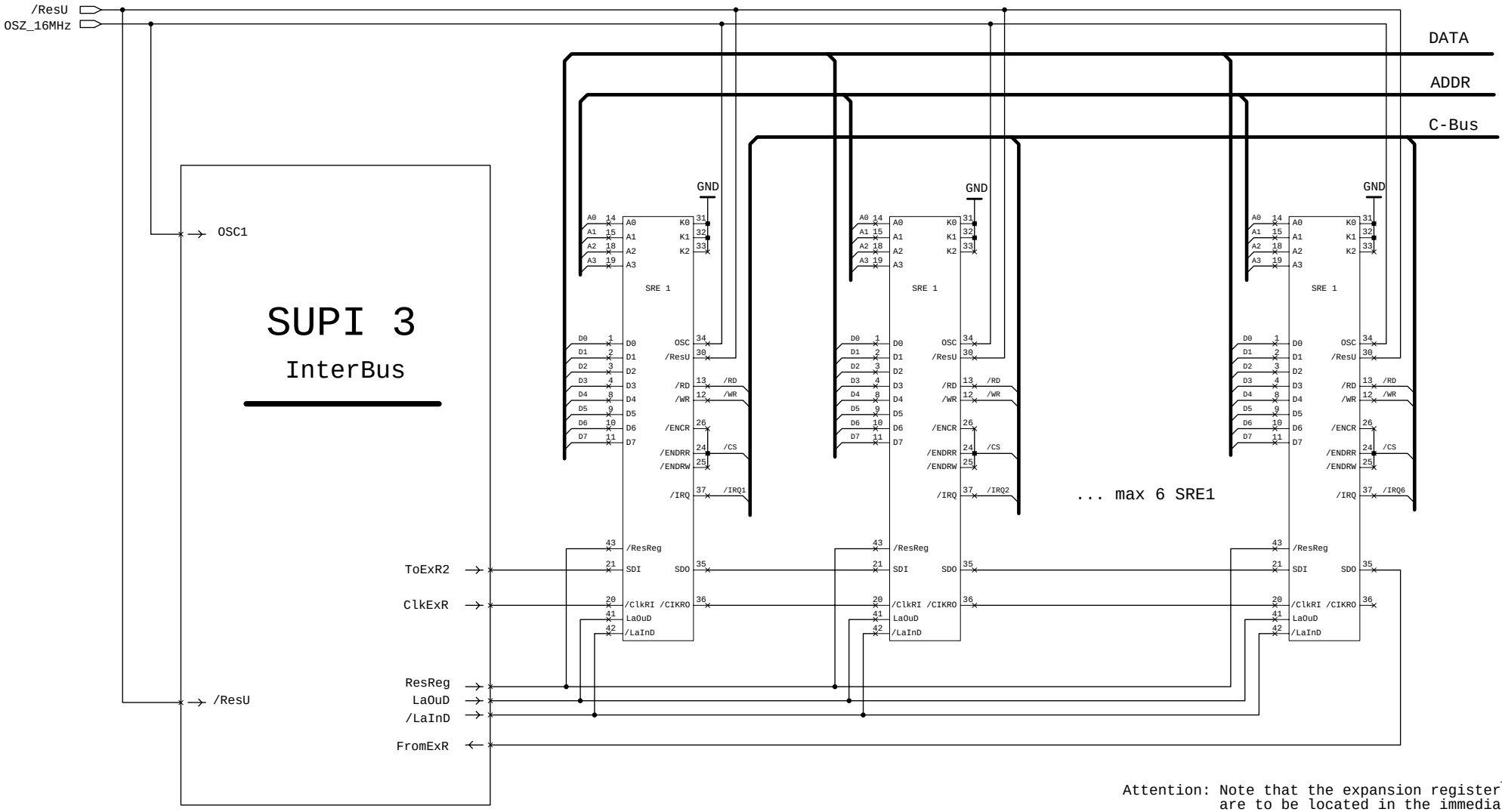


Attention: Note that the expansion register are to be located in the immediate vicinity of IBS SUPI.

If the ClkExR and ToExR2 signals are not buffered, it is only possible to use 4 expansion ICs due to the capcitive load.

				Masstab:									
register expansion for digit. I/O		Anzahl Blaetter:	Blatt Nr.:	gepr									
PHOENIX CONTACT	3-1	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei				version 1.1	01.08.96	Lutz		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

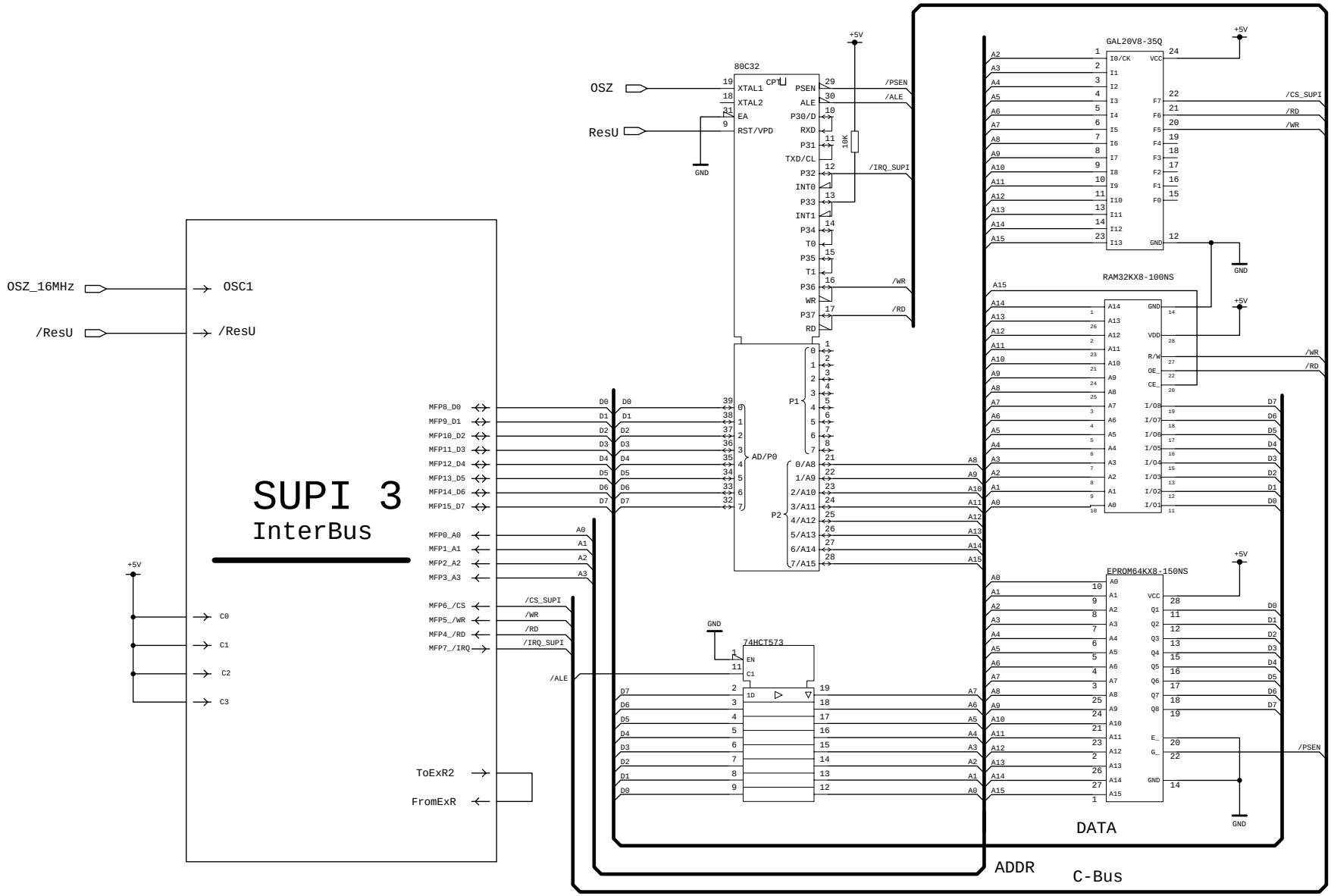
application register expansion with IBS SRE 1



Attention: Note that the expansion register are to be located in the immediate vicinity of IBS SUPI.

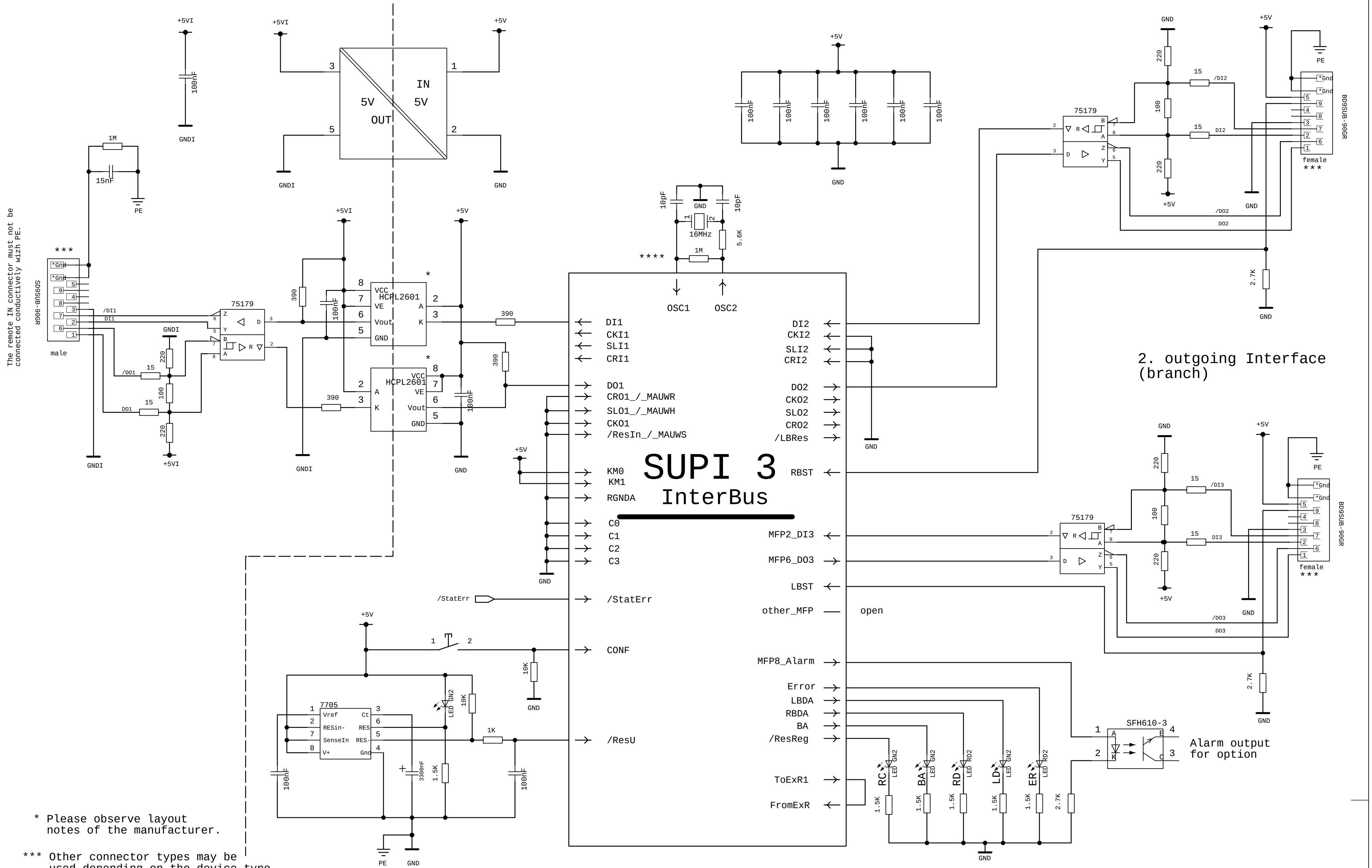
				Masstab:									
register expansion with IBS SRE 1		Anzahl Blaetter:	Blatt Nr.:	gepr									
PHOENIX CONTACT	3-3	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei				version 1.1	01.08.96	Lutz		
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.

application microcontroller interface



				Masstab:										
uP-Interface		Anzahl Blaetter:	Blatt Nr.:	gepr										
PHOENIX CONTACT	4-4	Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	gezei				version 1.1	01.08.96	Lutz			
						Datum	Name	Rev	Aenderung	Datum	Name	Pruefdatum	gepr.	

application remotebus terminal module



* Please observe layout notes of the manufacturer.

*** Other connector types may be used depending on the device type.

**** Please observe layout notes of the manufacturer and the chapter "clock generation" of the IBS SUPI3 manual.

remotebus terminal module	Anzahl Blaetter:	Blatt Nr.:	Masstab:					
			gepr					
			gezei			version 0.0	01.02.97	Lutz
PHOENIX CONTACT 1-5 Z.Nr.:	Anzahl Kopien:	Kopie Nr.:	Datum	Name	Rev	Aenderung	Datum	Name · Pruefdatum · gepr.

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