

DATA SHEET

TDA8571J

4 × 40 W BTL quad car radio power amplifier

Product specification
Supersedes data of 1998 Mar 13

2002 Mar 05

4 × 40 W BTL quad car radio power amplifier

TDA8571J

FEATURES

- Requires very few external components
- High output power
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit safe to ground and to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Pin compatible with the TDA8568Q, except for the gain.

GENERAL DESCRIPTION

The TDA8571J is a integrated class-B output amplifier contained in a 23-lead Single-In-Line (SIL) plastic power package. It contains four amplifiers in a BTL configuration, each with a gain of 34 dB. The output power is 4 × 40 W (EIAJ) into a 4 Ω load.

APPLICATIONS

- Primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	200	–	mA
I_{stb}	standby current		–	0.2	100	μ A
I_{sw}	switch-on current		–	–	80	μ A
$ Z_i $	input impedance		25	30	–	k Ω
$P_{O(EIAJ)}$	EIAJ output power	THD = maximum	–	40	–	W
SVRR	supply voltage ripple rejection	$R_s = 0 \Omega$	–	50	–	dB
α_{CS}	channel separation	$R_s = 10 k\Omega$	–	50	–	dB
$G_{V(cl)}$	closed-loop voltage gain		33	34	35	dB
$V_{n(o)}$	noise output voltage	$R_s = 0 \Omega$	–	–	170	μ V
$ V_{OS} $	DC output offset voltage	MUTE	–	–	80	mV
$ \Delta V_{OS} $	delta DC output offset voltage	ON $\leftrightarrow$ MUTE	–	–	80	mV

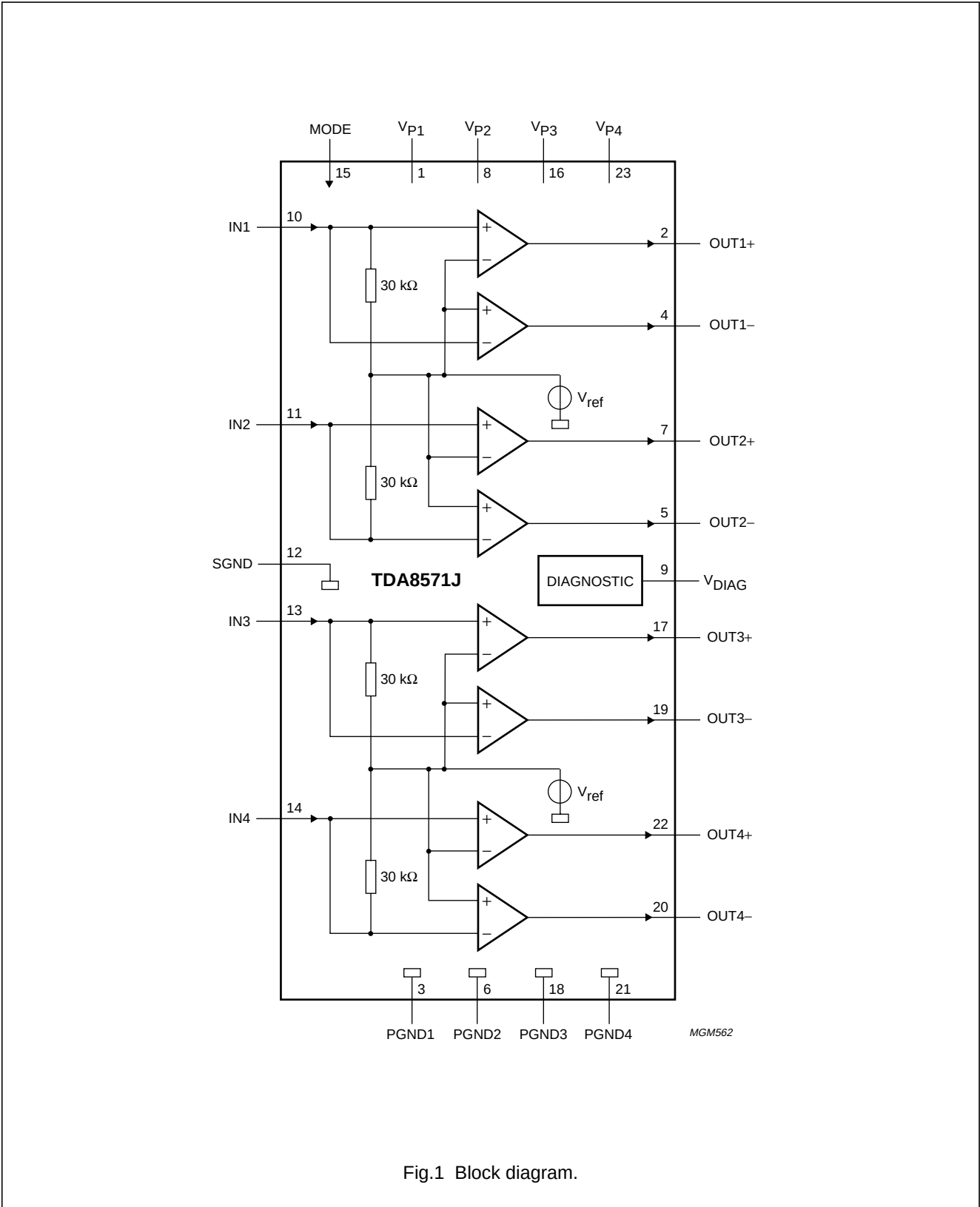
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8571J	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1

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BLOCK DIAGRAM

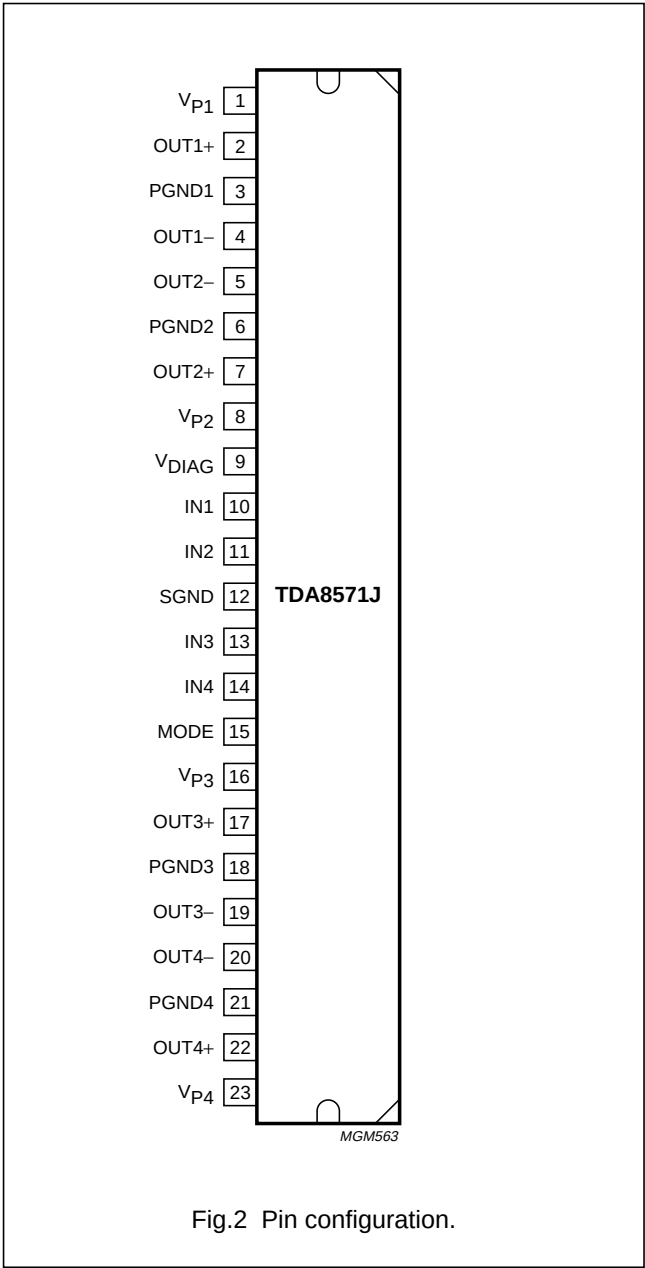


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PINNING

SYMBOL	PIN	DESCRIPTION
V _{P1}	1	supply voltage 1
OUT1+	2	output 1+
PGND1	3	power ground 1
OUT1–	4	output 1–
OUT2–	5	output 2–
PGND2	6	power ground 2
OUT2+	7	output 2+
V _{P2}	8	supply voltage 2
V _{DIAG}	9	diagnostic output
IN1	10	input 1
IN2	11	input 2
SGND	12	signal ground
IN3	13	input 3
IN4	14	input 4
MODE	15	mode select switch input
V _{P3}	16	supply voltage 3
OUT3+	17	output 3+
PGND3	18	power ground 3
OUT3–	19	output 3–
OUT4–	20	output 4–
PGND4	21	power ground 4
OUT4+	22	output 4+
V _{P4}	23	supply voltage 4



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FUNCTIONAL DESCRIPTION

The TDA8571J contains four identical amplifiers which can be used for bridge applications. The gain of each amplifier is fixed at 34 dB.

Mode select switch (pin MODE)

- Standby: low supply current (<100 μ A)
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a low input current (<80 μ A), a low cost supply switch can be applied.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥ 150 ms (charging of the input capacitors at pins IN1, IN2, IN3 and IN4). When switching from standby to mute, the slope should be at least 18 V/s. This can be realized by:

- Microprocessor control
- External timing circuit (see Fig.3).

Diagnostic output (pin V_{DIAG})

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin V_{DIAG} goes LOW. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and so limit the distortion. The output level of pin V_{DIAG} is independent of the number of channels that are clipping (see Fig.4).

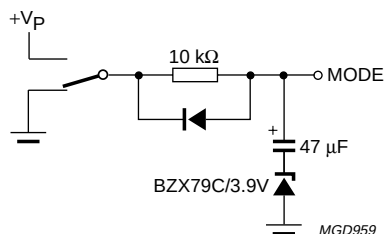


Fig.3 Mode select switch circuitry.

SHORT-CIRCUIT DIAGNOSTIC

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 10 ms after removal of the short-circuit. During this short-circuit condition, pin V_{DIAG} is continuously LOW.

When a short-circuit occurs across the load of one or more channels, the output stages are switched off during approximately 10 ms. After that time it is checked during approximately 50 μ s to determine whether the short-circuit is still present. Due to this duty cycle of 50 μ s/10 ms the average current consumption during this short-circuit condition is very low.

During this short-circuit condition, pin V_{DIAG} is LOW for 10 ms and HIGH for 50 μ s (see Fig.5). The protection circuits of all channels are coupled. This means that if a short-circuit condition occurs in **one** of the channels, **all** channels are switched off. Consequently, the power dissipation in any short-circuit condition is very low.

TEMPERATURE PRE-WARNING

When the virtual junction temperature T_{vj} reaches 145 °C, pin V_{DIAG} goes LOW.

OPEN-COLLECTOR OUTPUTS

The diagnostic pin has an open-collector output, so more devices can be tied together. An external pull-up resistor is needed.

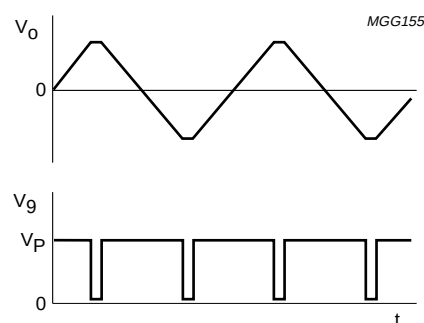


Fig.4 Distortion detector waveform.

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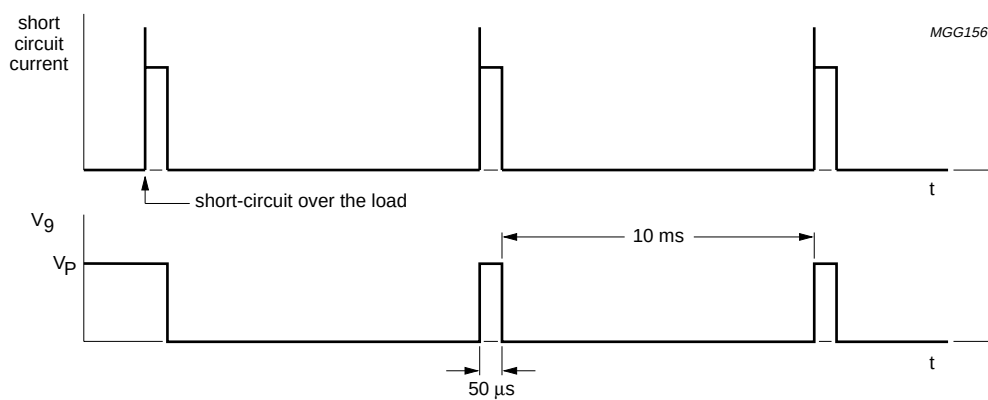


Fig.5 Short-circuit waveform.

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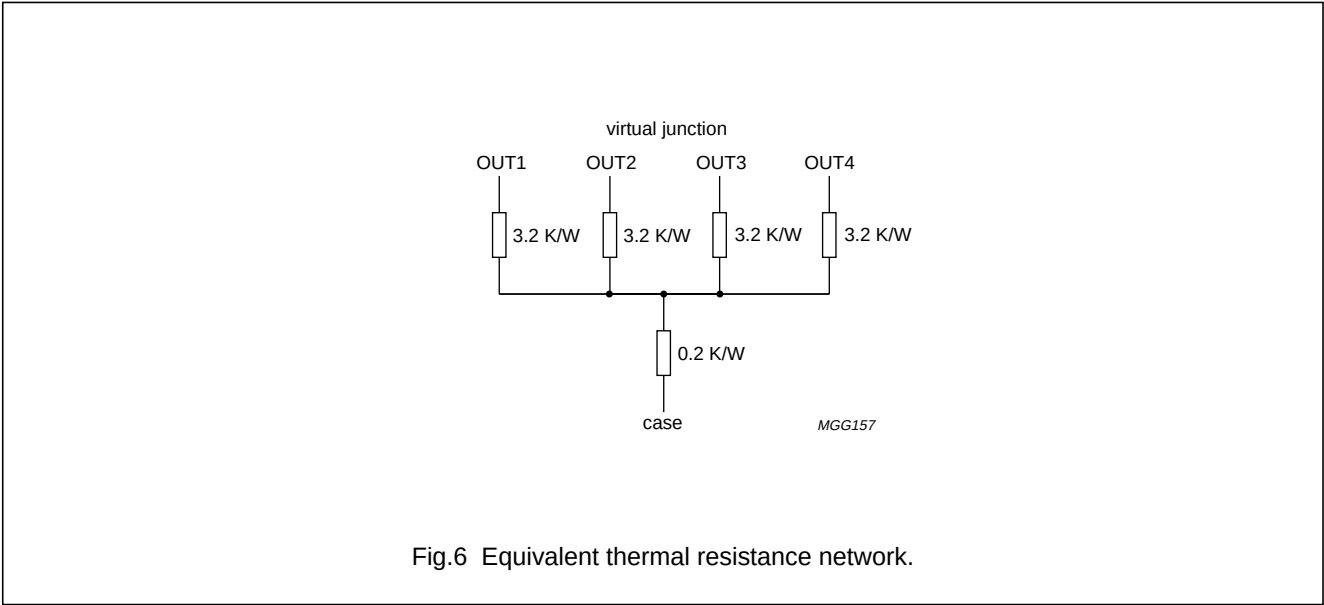
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump protection; during 50 ms; t _r ≥ 2.5 ms	–	45	V
V _{sc(safe)}	short-circuit safe voltage		–	18	V
V _{rp}	reverse polarity voltage		–	6	V
I _{OSM}	non-repetitive peak output current		–	10	A
I _{ORM}	repetitive peak output current		–	7.5	A
P _{tot}	total power dissipation		–	60	W
T _{stg}	storage temperature		–55	+150	°C
T _{amb}	ambient temperature		–40	+85	°C
T _{vj}	virtual junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient in free air	40	K/W
R _{th j-c}	thermal resistance from junction to case (see Fig.6)	1	K/W



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QUALITY SPECIFICATION

In accordance with "General Quality Specification For Integrated Circuits (SNW-FQ-611D)".

DC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6	14.4	18	V
$I_{q(\text{tot})}$	quiescent current	$R_L = \infty$	–	200	360	mA
Operating condition						
V_{MODE}	mode select switch level		8.5	–	V_P	V
I_{MODE}	mode select switch current	$V_{\text{MODE}} = 14.4\text{ V}$	–	30	80	μA
V_O	output voltage	note 2	–	7.0	–	V
Mute condition						
V_{MODE}	mode select switch level		3.3	–	6.4	V
V_O	output voltage	note 2	–	7.0	–	V
$ V_{\text{OS}} $	DC output offset voltage	MUTE	–	–	80	mV
$ \Delta V_{\text{OS}} $	delta DC output offset voltage	ON ↔ MUTE	–	–	80	mV
Standby condition						
V_{MODE}	mode select switch level		0	–	2	V
I_{stb}	standby current		–	0.2	100	μA
Diagnostic						
V_{DIAG}	diagnostic output voltage	during any fault condition	–	–	0.6	V
T_{vj}	temperature pre-warning	$V_{\text{DIAG}} = 0.6\text{ V}$	–	145	–	°C

Notes

1. The circuit is DC adjusted at $V_P = 6$ to 18 V and AC operating at $V_P = 8.5$ to 18 V .
2. At $18\text{ V} < V_P < 30\text{ V}$ the DC output voltage $\leq \frac{1}{2}V_P$.

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AC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $R_L = 4\ \Omega$; $f = 1\text{ kHz}$; $T_{\text{amb}} = 25\text{ °C}$; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	THD = 0.5%	16	19	–	W
		THD = 10%	21	26	–	W
		$V_P = 13.7\text{ V}$; THD = 0.5%	–	17.5	–	W
		$V_P = 13.7\text{ V}$; THD = 10%	–	23	–	W
$P_{O(\text{EIAJ})}$	EIAJ output power	THD = maximum; $V_i = 2\text{ V (p-p)}$ square wave	35	40	–	W
$P_{O(\text{max})}$	maximum output power	THD = maximum; $V_P = 15.2\text{ V}$; $V_i = 2\text{ V (p-p)}$ square wave	40	45	–	W
THD	total harmonic distortion	$P_O = 1\text{ W}$	–	0.1	–	%
		$V_{\text{MODE}} = 0.6\text{ V}$; note 1	–	10	–	%
B_p	power bandwidth	THD = 0.5%; $P_O = -1\text{ dB}$ with respect to 16 W	–	20 to 20000	–	Hz
$f_{ro(l)}$	low frequency roll-off	at -1 dB ; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	at -1 dB	20	–	–	kHz
$G_{V(\text{cl})}$	closed-loop voltage gain		33	34	35	dB
SVRR	supply voltage ripple rejection	$R_S = 0\ \Omega$; maximum ripple $V_{\text{ripple}} = 2\text{ V (p-p)}$				
		on	40	–	–	dB
		mute	50	–	–	dB
		standby	80	–	–	dB
$ Z_i $	input impedance		25	30	38	k Ω
$V_{n(o)}$	noise output voltage	$B = 20\text{ Hz to }20\text{ kHz}$				
		on; $R_S = 0\ \Omega$	–	125	170	μV
		on; $R_S = 10\text{ k}\Omega$	–	150	–	μV
		mute; independent of R_S	–	100	–	μV
α_{CS}	channel separation	$P_O = 16\text{ W}$; $R_S = 10\text{ k}\Omega$	45	–	–	dB
$ \Delta G_V $	channel unbalance		–	–	1	dB
V_o	output signal in mute	maximum input voltage $V_i = 1\text{ V (RMS)}$	–	–	2	mV

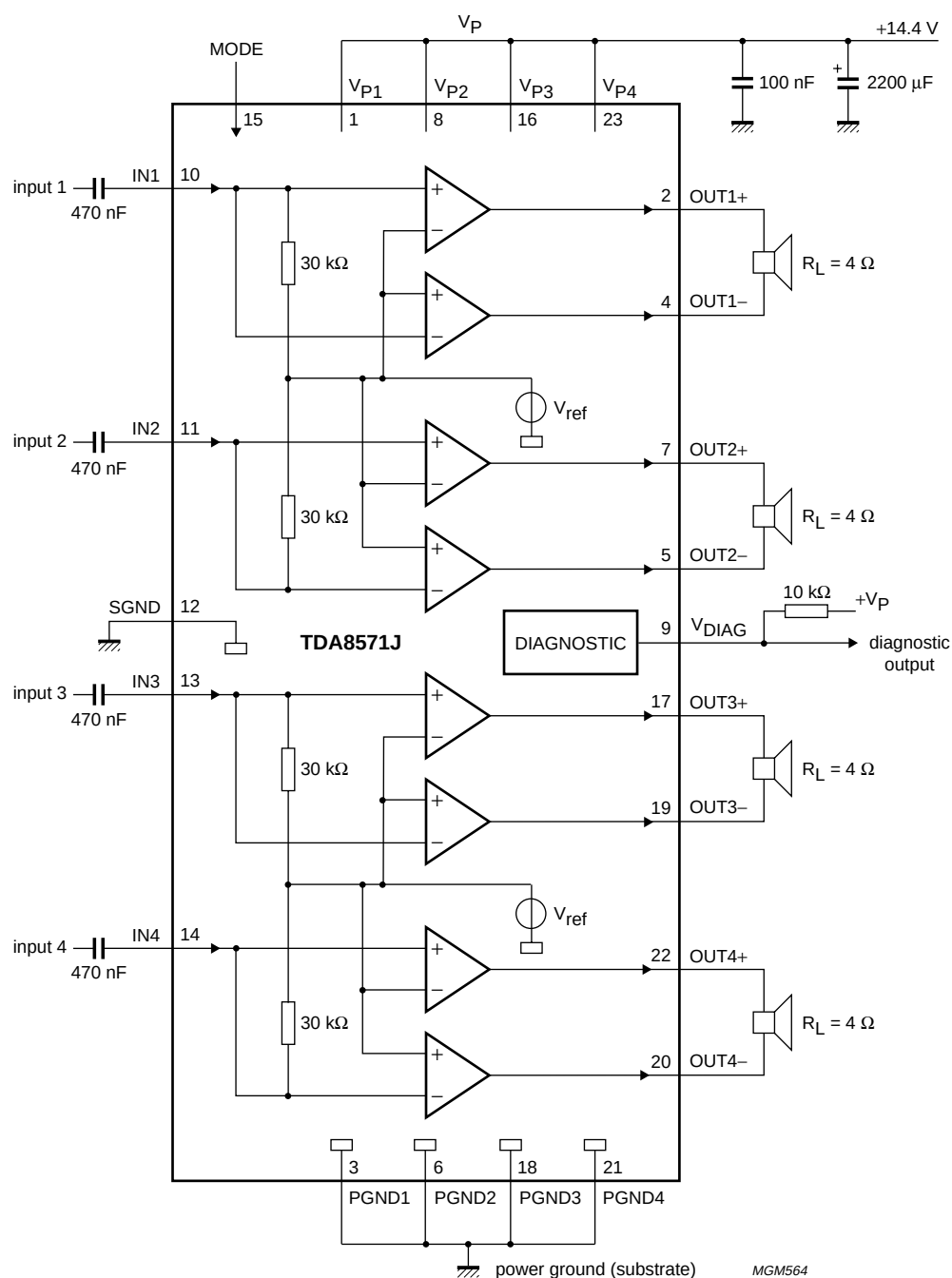
Notes

- Dynamic Distortion Detector (DDD) active, pin V_{DIAG} is set to LOW level.
- Frequency response externally fixed.

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TEST AND APPLICATION INFORMATION



Special care must be taken in the PCB-layout to separate pin V_{DIAG} from the pins IN1, IN2, IN3 and IN4 to minimize the crosstalk between the clip output and the inputs.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during a period of $\geq 150\text{ ms}$ (charging the input capacitors at pins IN1, IN2, IN3 and IN4).

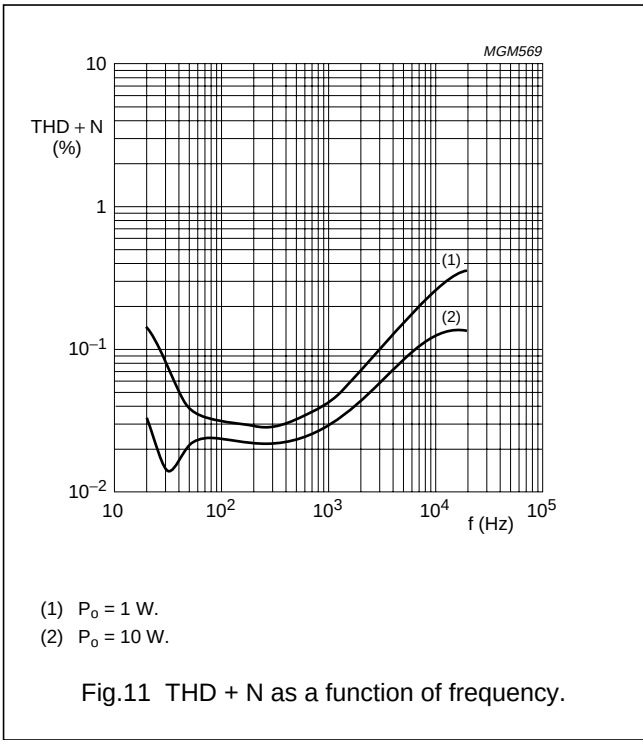
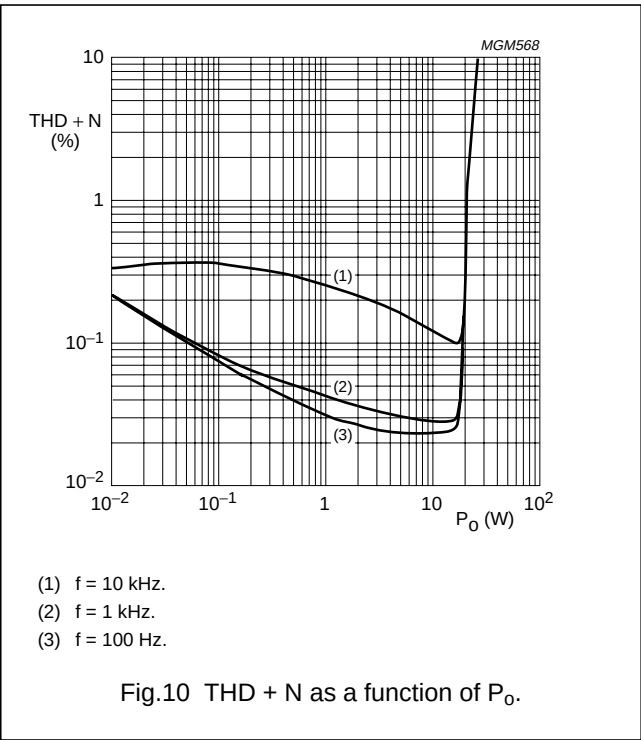
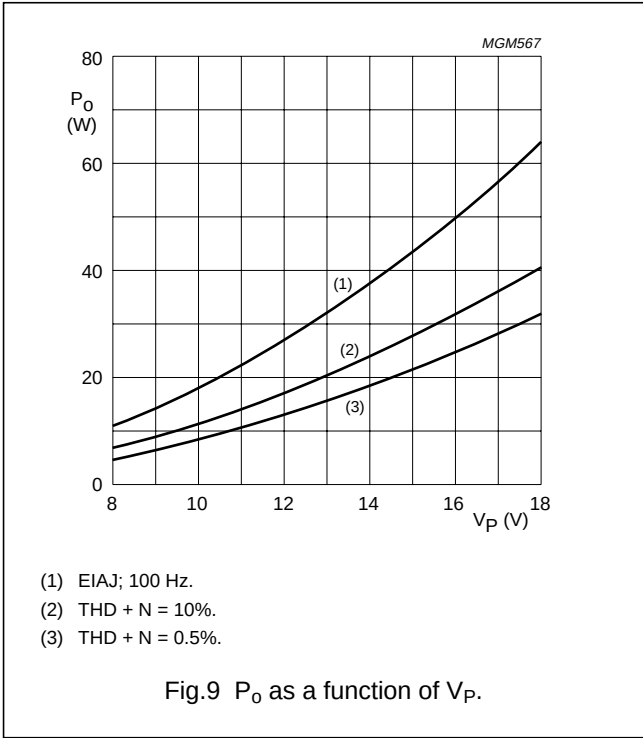
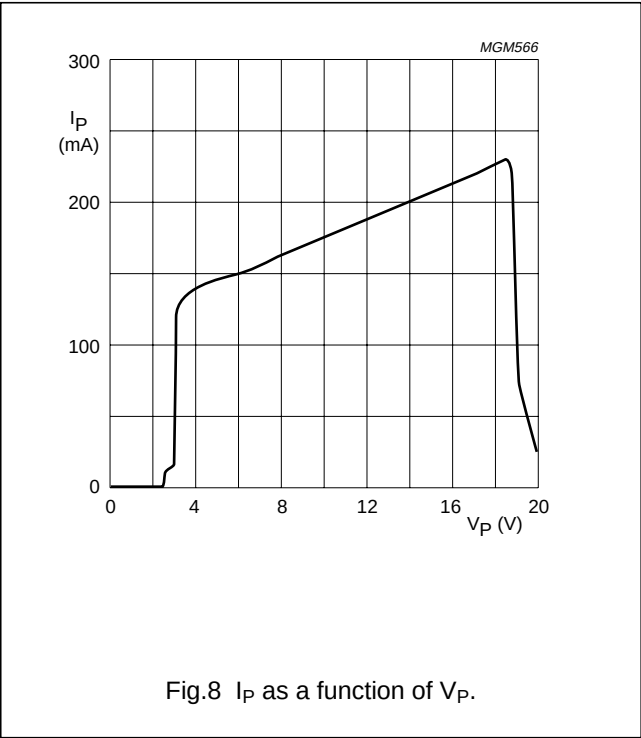
Fig.7 Application circuit diagram.

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Test information

Figures 8 to 13 have the following conditions: $V_P = 14.4\text{ V}$; $R_L = 4\ \Omega$; $f = 1\text{ kHz}$; 80 kHz filter used; unless otherwise specified.



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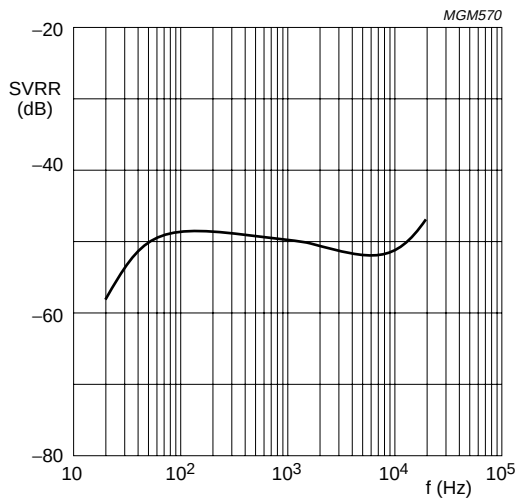
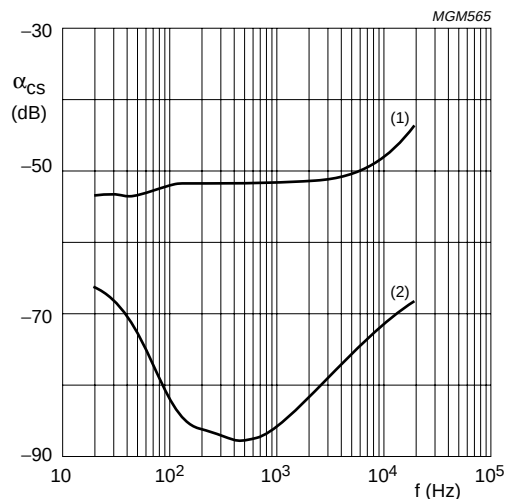


Fig.12 SVRR as a function of frequency.



- (1) Between channels 1 and 2 or between channels 3 and 4.
- (2) Between channels 1 or 2 and channels 3 or 4.

Fig.13 Channel separation as a function of frequency.

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PCB layout

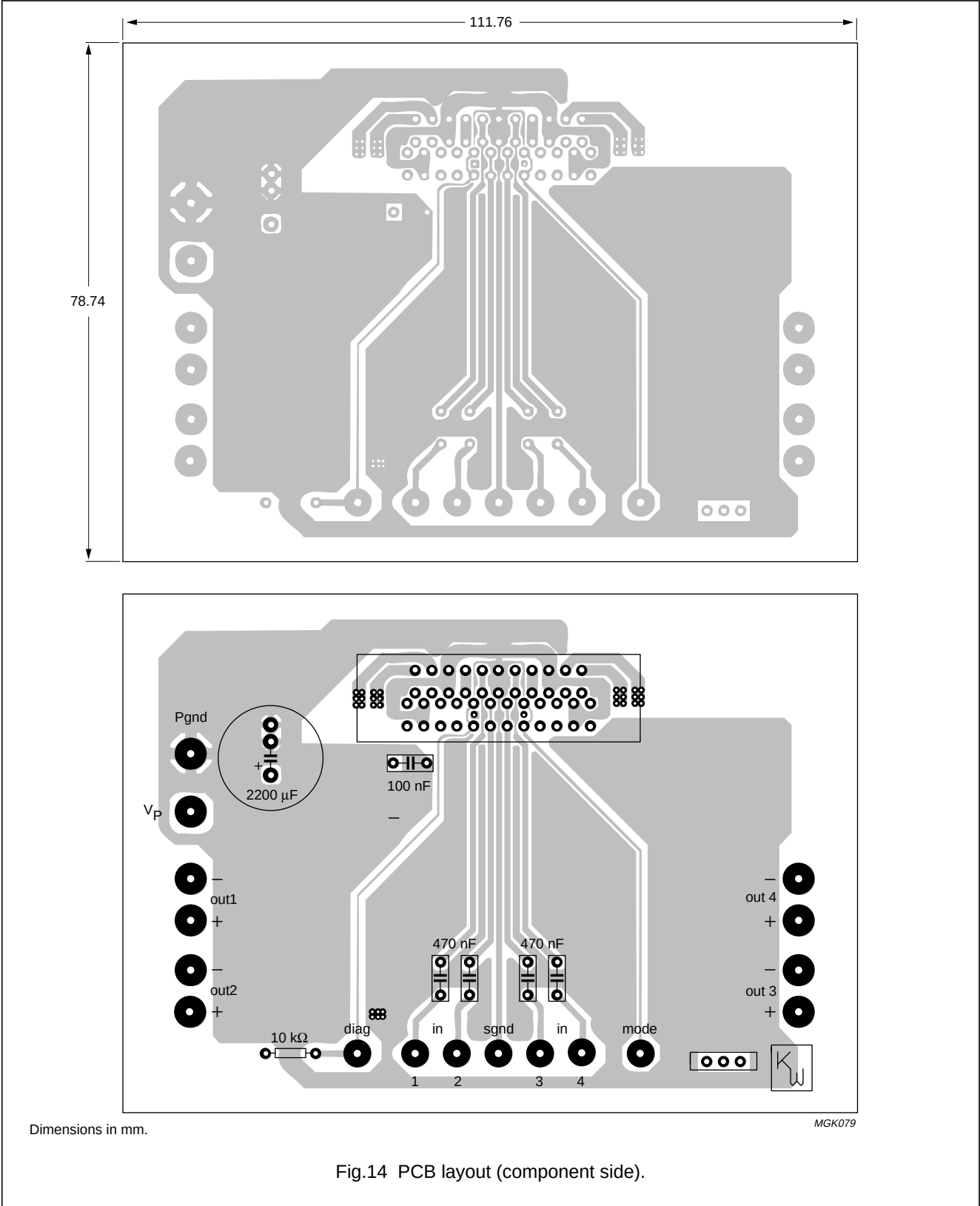
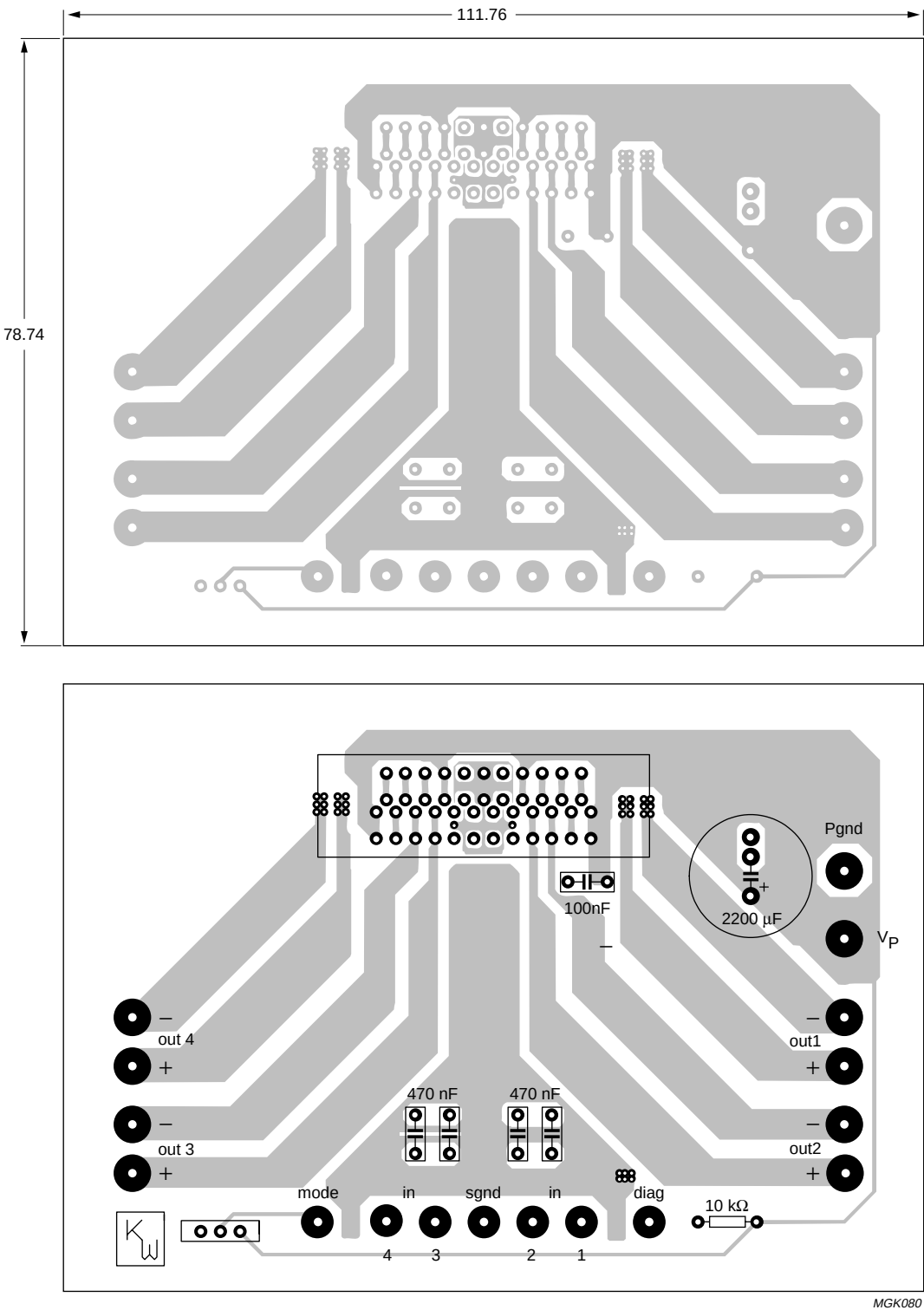


Fig.14 PCB layout (component side).

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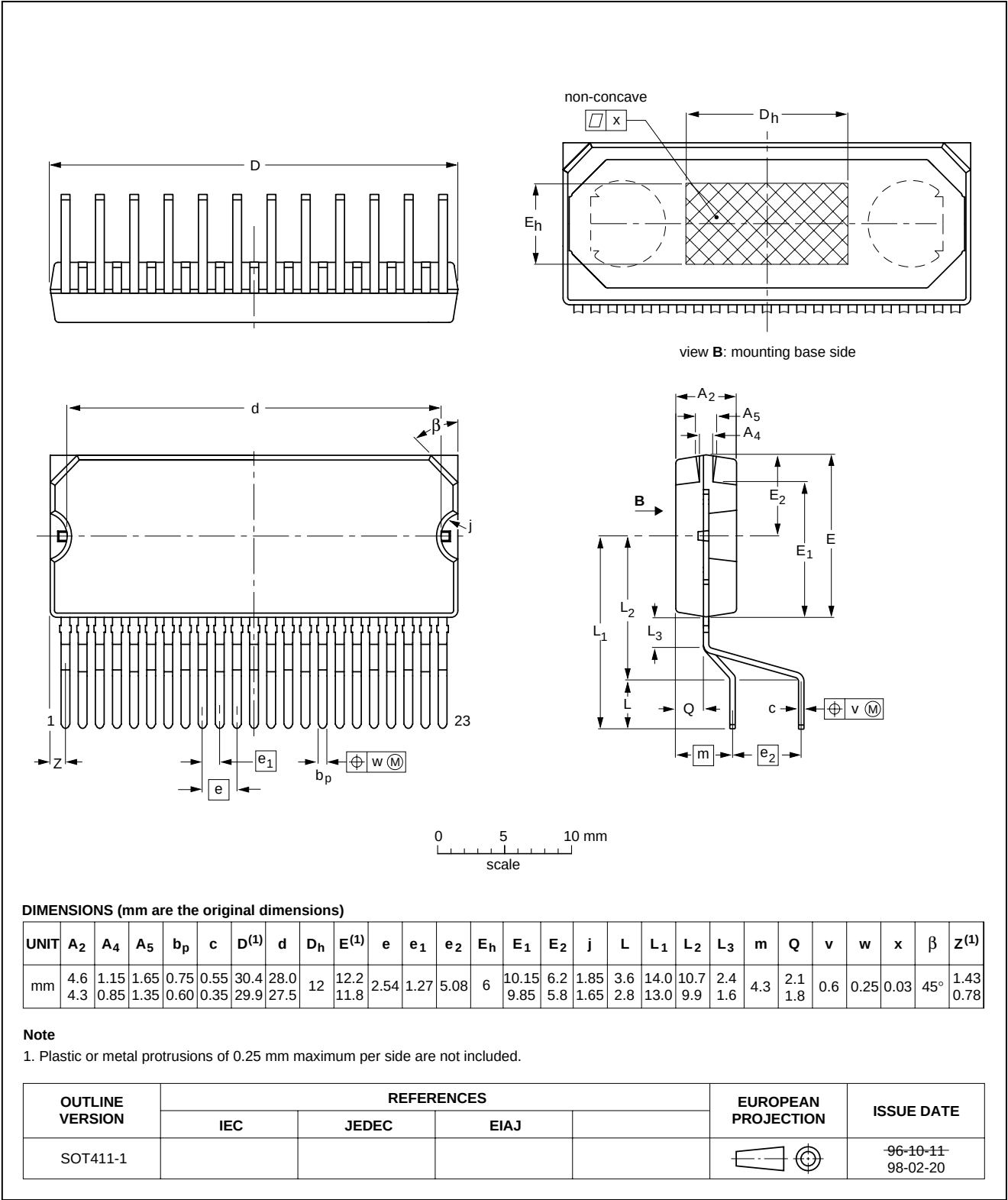
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PACKAGE OUTLINE

DBS23P: plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)

SOT411-1



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SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature (T_{stg(max)}). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable ⁽¹⁾

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

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DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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Notes

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NOTES

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NOTES

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