ECHELON

Neuron® 6050

IP Processor for IzoT™ Enabled Devices

Neuron 6050 Key Features

- Upto 80MHz system clock, 64KB RAM and 16KB ROM on-chip memories
- Support for larger external flash memories, up to 256KB applications
- Support for up to 254 Network Variables (NVs), 127 aliases
- 16-fold increase in address table entries, up to 254 entries
- User programmable interrupts, hardware UART, 12 I/O pins with 35 programmable standard I/O models
- 5-pin network communications port with 3.3V drive and 5V-tolerant pins.
- Unique 48-bit IEEE MAC ID in every device for network installation and management
- 7mm x 7mm 48-pin QFN package, -40°C to +85°C

The Neuron 6050 is optimized for modernizing and consolidating smart control devices and networks. It is a key product in Echelon's IzoT™ Platform — the most comprehensive and open control networking platform for the Industrial Internet of Things (IIoT). It offers options for backward compatibility with LONWORKS® while adding native IP addressing at the device level and consolidating multiple control protocols on the same device.

The Neuron 6050 Processor incorporates communication and control functions on a single chip, in both hardware and firmware, to facilitate the design of LonTalk®, LonTalk/IP or BACnet/IP devices. Its flexible 5-pin communications port can be configured to interface with a wide variety of transceivers — including twisted-pair, RF, IR, fiber-optics, and coaxial — at a wide range of data rates.

The Neuron 6050 Processor includes 3 independent 8-bit logical processors to manage the physical MAC layer, the network, and the user application. These are called the Media-Access Control (MAC) processor, the network (NET) processor, and the application (APP) processor, respectively (see Figure 1). At higher system clock rates, a fourth processor called the IRQ CPU can be used to handle interrupts.

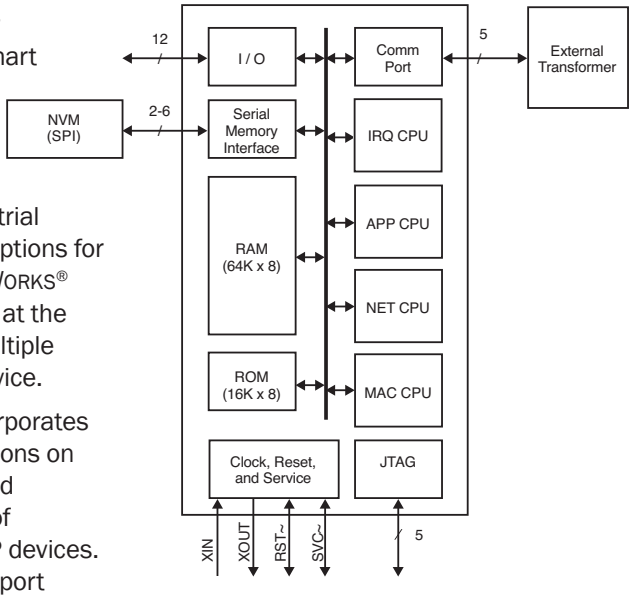

Figure 1: Neuron 6050 Processor

Multi-protocol Operation, Future Proofing and Backward Compatibility

The Neuron 6050 Processor supports up to four different modes of operation, as shown in Figure 2, allowing device makers unprecedented flexibility in creating control devices for a wide variety of applications using one common development effort. Backward compatibility and future proofing can both be met using a common platform based on the Neuron 6050 Processor family.

The pins for the Neuron 6050 Processor's communications port drive a 3.3V signal and are 5V input-tolerant. Thus, the Neuron 6050 Processor is compatible with 3.3V transceivers and with 5V transceivers that have TTL-compatible input.

The Neuron 6050 Processor is compatible with transceivers for TP/XF-1250 and EIA-485 channels, and can be used with the LONWORKS LPT-11 Link Power Transceiver. It also supports a variety of other channels used with previous-generation Neuron Chips, such as RF, IR, fiber-optic, and coax. It does not, however, support a TP/XF-78 channel. To support a TP/FT-10 channel, use an Echelon Free Topology Smart Transceiver (FT 6050 or FT 5000 Smart Transceiver); to support a PL-20 power line channel, use an Echelon Power Line Smart Transceiver (PL 3120/3150/3170 Smart Transceiver). Echelon's Smart Transceivers integrate the transceiver for the channel type and the Neuron core into a single chip, which enables smaller designs and provides cost savings.

The Neuron core in the Neuron 6050 Processor uses the same instruction set and architecture as the previous-generation Neuron core, including instructions for hardware multiplication and division. The Series 6050 Neuron core is source code compatible with applications written for the Series 5000 and 3100 Neuron core. Applications written for the Series 5000 and 3100 Neuron core must be recompiled with the IzoT NodeBuilder Software before they can be used with the Neuron 6050 Processor.

The Neuron 6050 Processor uses Neuron firmware version 21 or later. Firmware versions prior to version 21 are not compatible with the Neuron 6050 Processor. The Neuron firmware is loaded into RAM from off chip flash. The Neuron 6050 Processor firmware can be upgraded over the network.

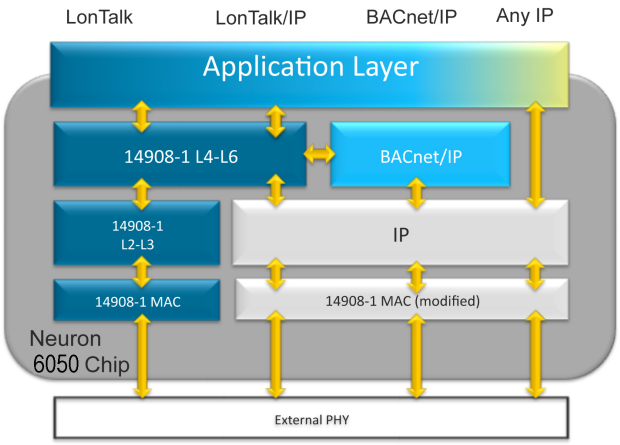

Figure 2: Neuron 6050 Modes of Operation

In the "LonTalk mode", the Neuron 6050 Processor runs the LonTalk stack down to the MAC layer and is fully backward compatible with devices running the LonTalk stack, including devices based on the Neuron 3120, Neuron 3150 or FT 3120/3150/5000 Smart Transceiver.

In the "LonTalk/IP mode", the Neuron 6050 Processor preserves the services offered by LonTalk layers 4-6, replacing layers 2-3 with UDP/IP. This allows the creation of devices that are fully compatible with LonTalk applications while supporting native IP addressing at the device level. In this mode, the network layer has been enhanced to support translation between LonTalk addresses and IP addresses in a manner that is transparent to both the LonTalk application above and the network below. This allows LonTalk compatible applications to run unmodified over a variety of media types while gaining IP addressing at the device level.

In the "BACnet/IP mode", LonTalk layers 4-6 services are used to create BACnet/IP devices borrowing from a rich set of LONMARK services and profiles. LONMARK® compatible applications can now run unmodified over a variety of channel types, and present their LONMARK interfaces as native BACnet Objects, thus pushing BACnet/IP all the way down to the simplest of devices. Provisioning and commissioning of BACnet/IP devices is now possible with available and powerful LONWORKS commissioning tools. Devices thus provisioned are fully compatible and discoverable using industry standard, BTL-certified BACnet management clients.

And finally, in the "Any IP mode", the Neuron 6050 Processor allows any control protocol to be modernized with IP addressing transported over a variety of channel types.

Enhanced Performance

Fast system clock. The internal system clock for the Neuron 6050 Processor can be user configured to run from 5MHz to 80MHz. The required external crystal provides a 10MHz clock frequency, and an internal PLL boosts the frequency to a maximum of 80MHz as the internal system clock speed. The fast clock is the same as what is available with the Neuron Processor; however, the Neuron 3120/3150 core divided the external oscillator frequency by two to create the internal system clock. Hence, a Neuron 3120/3150 core running with a 10MHz external crystal had a 5MHz internal system clock. A Neuron 6050 Processor running with an 80MHz internal clock is thus 16 times faster than a 10MHz Neuron 3120/3150 core running with a 5MHz internal system clock.

The 5MHz system clock mode in the Neuron 6050 Processor provides backward compatibility to support time-critical applications designed for the 10MHz Neuron 3150 or Neuron 3120 processor.

The Neuron core inside the Neuron 6050 Processor includes a built-in hardware multiplier and divider to increase the performance of arithmetic operations.

Support for large number of network variables.

Interrupts. The Neuron 6050 Processor lets developers define application interrupts to handle asynchronous events triggered by selected state changes on any of the 12 I/O pins, by on-chip hardware timer-counter units, or by an on-chip high-performance hardware system timer. An application uses the Neuron C interrupt() clause to define the interrupt condition and the interrupt task that handles the condition. The Neuron C program runs the interrupt task whenever the interrupt condition is met. See the Neuron C Programmer's Guide for more information about writing interrupt tasks and handling interrupts.

Enhancements for processing IP packets:

The Neuron 6050 Processor has an enhanced MAC layer that allows frame sizes up to 1280 bytes that allows large IP frames to be carried over a variety of channel types without fragmenting the packet which provides better bandwidth utilization of the channel. Having dedicated processor contexts for the MAC and network protocol support allows the application to have the same performance independent of the network traffic. Traditional uni-processor designs must be interrupted repeatedly to receive every packet on the network, even when the packet turns out to not be addressed to the node. This increases the demands on the application processor and makes the amount of processing available to the application difficult to predict as it becomes a function of the network load.

JTAG. The Neuron 6050 Processor provides an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG) to allow a Series 6050 chip to be included in the boundary-scan chain for device production tests.

Communications Port

The Neuron 6050 Processor includes a versatile 5-pin communications port that can be configured in two ways: 3.3 V Single-Ended Mode and 3.3 V Special-Purpose Mode. In Single-Ended Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, and pin CP2 for enabling an external transmitter. Data is communicated using Differential Manchester encoding.

In Special-Purpose Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, pin CP2 transmits a bit clock, and pin CP4 transmits a frame clock for use by an external intelligent transceiver. In this mode, the external transceiver is responsible for encoding and decoding the data stream.

Unlike the Neuron 3120/3150 Chips, the Neuron 6050 Processor does not support the Differential Mode configuration for the communications port. Thus, devices that require Differential Mode transceiver types must be redesigned for a Neuron 6050 Processor to use Single-Ended Mode with external circuitry to provide Single-Ended to Differential Mode conversions. See the Series 6050 Chip Data Book and the Connecting a Neuron 6050 Processor to an External Transceiver Engineering Bulletin for more information.

Any 3.3V transceiver or a 5V transceiver with TTL-compatible inputs can be used with the Neuron 6050 Processor because the communications port has pins that are 5V tolerant and drive a 3.3V signal. Common transceiver types that can be used with a Neuron 6050 Processor include twisted-pair, RF, IR, fiber-optic, and coax.

I/O Pins and Counters

The Neuron 6050 Processor provides 12 bidirectional I/O pins that are 5V tolerant and can be configured to operate in one or more of 35 predefined standard input/output models. The chip also has two 16-bit timer/counters that reduce the need for external logic and software development.

Memory Architecture

The Neuron 6050 Processor eliminates the need for external serial EEPROM that the previous generation Neuron 5000 required and instead relies on inexpensive external flash memories for non-volatile application and data storage, and for Neuron firmware upgrades. It has 16KB of ROM and 64KB (44 KB user-accessible) of RAM on the chip. It has no on-chip non-volatile memory for application use. Each chip, however, contains its unique identifier (IEEE MAC ID) in an on-chip, non-volatile, read-only memory. Typical external flash memory configuration is 512KB of which 128KB is available for application code. This is a three-fold increase in application size that can be hosted on the Neuron 6050 compared to previous generations. Larger application sizes are possible with larger flashes. For example, a 256KB application is possible on a 1 MB flash part.

The application code and configuration data are stored in the external non-volatile memory (NVM) and copied into the internal RAM during device reset; the instructions then execute from internal RAM. Writes to NVM are shadowed in the internal RAM and pushed out to external NVM by the Neuron 6050 firmware. The application does not manage NVM directly.

External memories supported. The Neuron 6050 Processor supports serial peripheral interface (SPI) for accessing off-chip non-volatile memories.

The Neuron 6050 Processor supports a variety of flash devices from different manufacturers. Echelon has qualified the following SPI flash memory devices for use with the Neuron 6050 Processor:

Winbond W25X40CL 4-Mbit SPI Serial Flash Memory.

Memory map. The Neuron 6050 Processor maps the Neuron firmware, application code, application data, and system data to an on-chip 64 KB RAM. The Neuron firmware, application code, persistent data are loaded from an external serial flash memory. The application code and persistent data can be up to 256 KB, and is automatically swapped into and out of the on-chip RAM by the Neuron firmware.

Programming memory devices. Because the Neuron 6050 Processor does not have any on-chip user-accessible NVM, only the external flash devices need to be programmed with the application and configuration data. The memory devices can be programmed in any of the following ways:

- In-circuit programming on the board.
- Over the network.
- Pre-programming before soldering on the board.

Migration Considerations

Most device designs that use the previous-generation Neuron 5000, Neuron 3120 or Neuron 3150 Chip can transition to using the Neuron 6050 Processor. Because the supply voltage and memory architecture of Neuron 3120/3150 Chips and Neuron 6050 Processors are different, the transition requires a hardware re-design of the boards. The supply voltage of the Neuron 5000 and the Neuron 6050 are the same but they have different memory architectures. Neuron 5000 designs using external flash could transition

to the Neuron 6050 Processor with minimal changes to the hardware. The recommended migration path for devices based on a Neuron Chip depends on the transceiver type used with the Neuron Chip, as shown in Table 1.

Current Transceiver Type Used	Equivalent Series 6050 Design	Comments
FTT-10A Transceiver	FT 6050 Smart Transceiver plus FT-X3 Communications Transformer	Use an FT 6050 Smart Transceiver for TP/FT-10 channels.
EIA-485 Transceiver	Neuron 6050 Processor plus EIA-485 Transceiver or (if possible) FT 6050 Smart Transceiver plus FT-X3 Communications Transformer	If your design is flexible enough to allow either an EIA-485 channel or a TP/FT-10 channel, use the FT 6050 Smart Transceiver with the TP/FT-10 channel.
TPT Twisted Pair Transceiver Module (for a TP/XF-1250 channel type)	Neuron 6050 Processor plus TPT/XF-1250 Twisted Pair Transceiver Module (for a TP/XF-1250 channel type)	The Neuron 6050 Processor must be configured to operate in 3.3V Single-Ended Mode with the TPT Twisted Pair Transceiver Module and external circuitry must be added for Single-Ended to Differential Mode conversion.
LonWorks LPT-11 Link Power Transceiver	Neuron 6050 Processor plus LPT-11 Link Power Transceiver	The Neuron 6050 Processor must be configured to operate in 3.3V Single-Ended Mode with the LPT-11 Link Power Transceiver.
Other transceiver type	Neuron 6050 Processor plus other transceiver type	The Neuron 6050 Processor can connect to other transceiver types for the supported channel types, but more hardware design work may be required.

Table 1: Migration for Devices with Neuron Chips

Contact your local Echelon representative for an in-depth discussion about migration considerations.

End-to-End Solutions

A typical Neuron 6050 Processor-based device requires a power source, crystal, external memory, and an I/O interface to the device being controlled (see Figure 3 for a typical Neuron 6050 Processor-based device).

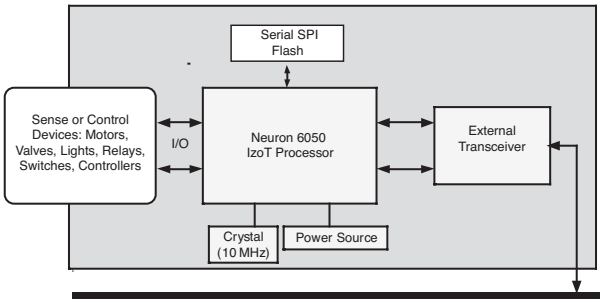

Figure 3: Typical LONWORKS based device

Echelon provides all of the building blocks required to successfully design and field cost-effective, robust products based on the Neuron 6050 Processor. Our end-to-end solutions include a comprehensive set of development tools, network interfaces, routers, and network tools. Pre-production design review services, training, and worldwide technical support — including on-site support — are available through Echelon's Support technical assistance program.

Please contact your local Echelon representative for further details.

Ordering Information

14550R-500 Neuron 6050 Processor: Supports all four operating modes LonTalk, LonTalk/IP, BACnet/IP and Any IP.

Preliminary

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