ISL26132, ISL26134

Low-Noise 24-bit Delta Sigma ADC

FN6954
Rev 3.00
November 20, 2014

The ISL26132 and ISL26134 are complete analog front ends for high resolution measurement applications. These 24-bit Delta-Sigma Analog-to-Digital Converters include a very low-noise amplifier and are available as either two or four differential multiplexer inputs. The devices offer the same pinout as the ADS1232 and ADS1234 devices and are functionally compatible with these devices. The ISL26132 and ISL26134 offer improved noise performance at 10Sps and 80Sps conversion rates.

The on-chip low-noise programmable-gain amplifier provides gains of 1x/2x/64x/128x. The 128x gain setting provides an input range of ±9.766mVFS when using a 2.5V reference. The high input impedance allows direct connection of sensors, such as load cell bridges to ensure the specified measurement accuracy without additional circuitry. The inputs accept signals 100mV outside the supply rails when the device is set for unity gain.

The Delta-Sigma ADC features a third order modulator providing up to 21.6-bit noise-free performance. The device can be operated from an external clock source, crystal (4.9152MHz typical), or the on-chip oscillator.

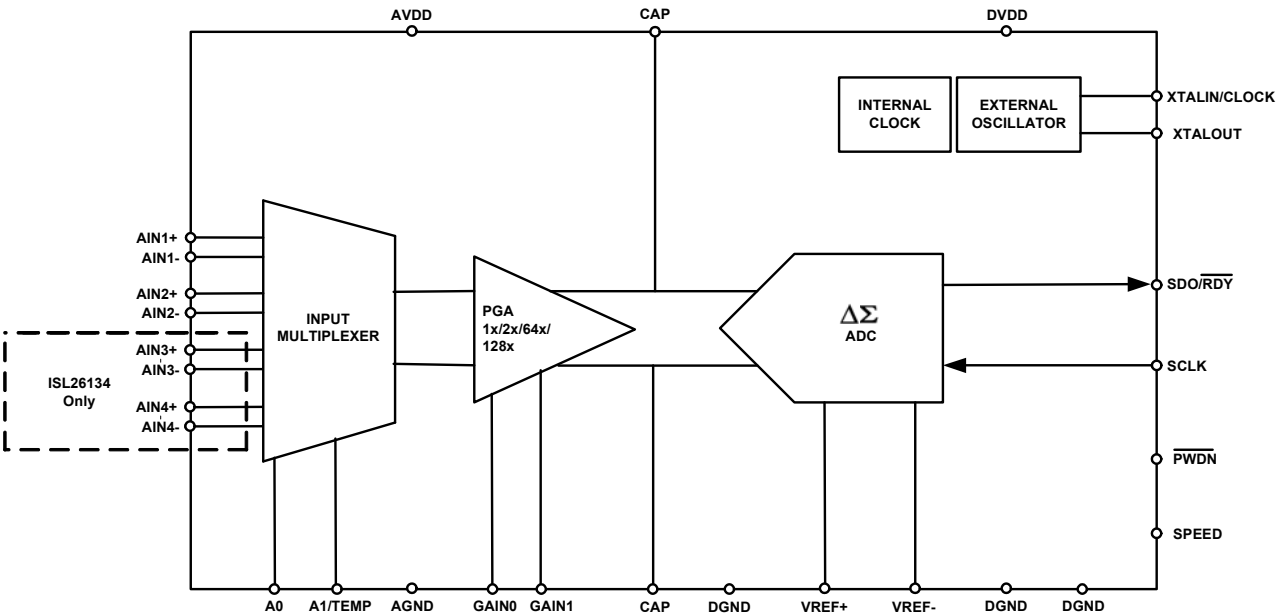
The two channel ISL26132 is available in a 24 Ld TSSOP package and the four channel ISL26134 is available in a 28 Ld TSSOP package. Both are specified for operation over the automotive temperature range (-40°C to +105°C).

Features

- Up to 21.6 Noise-free bits
- Low noise amplifier with gains of 1x/2x/64x/128x
- RMS noise: 10.6nV @ 10Sps (PGA = 128x)
- Linearity error: 0.0002% FS
- Simultaneous rejection of 50Hz and 60Hz (@ 10Sps)
- Two (ISL26132) or four (ISL26134) channel differential input multiplexer
- On-chip temperature sensor (ISL26132)
- Automatic clock source detection
- Simple interface to read conversions
- +5V Analog, +5 to +2.7V digital supplies
- Pb-Free (RoHS compliant)
- TSSOP packages: ISL26132, 24 pin; ISL26134, 28 pin

Applications

- Weigh scales
- Temperature monitors and controls
- Industrial process control
- Pressure sensors



NOTE for A1/TEMP pin: Functions as A1 on ISL26134; Functions as TEMP on ISL26132

FIGURE 1. BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMPERATURE RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL26132AVZ	26132 AVZ	-40 to +105	24 Ld TSSOP	M24.173
ISL26132AVZ-T (Note 1)	26132 AVZ	-40 to +105	24 Ld TSSOP (Tape & Reel)	M24.173
ISL26132AVZ-T7A (Note 1)	26132 AVZ	-40 to +105	24 Ld TSSOP (Tape & Reel)	M24.173
ISL26134AVZ	26134 AVZ	-40 to +105	28 Ld TSSOP	M28.173
ISL26134AVZ-T (Note 1)	26134 AVZ	-40 to +105	28 Ld TSSOP (Tape & Reel)	M28.173
ISL26134AVZ-T7A (Note 1)	26134 AVZ	-40 to +105	28 Ld TSSOP (Tape & Reel)	M28.173
ISL26134AV28EV1Z	Evaluation Board			

NOTES:

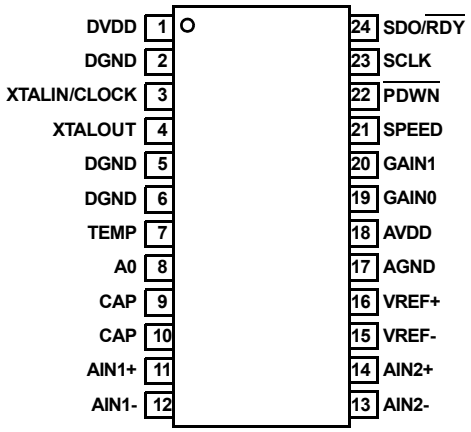
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL26132, ISL26134. For more information on MSL please see techbrief TB363.

TABLE 1. KEY DIFFERENCES OF PARTS

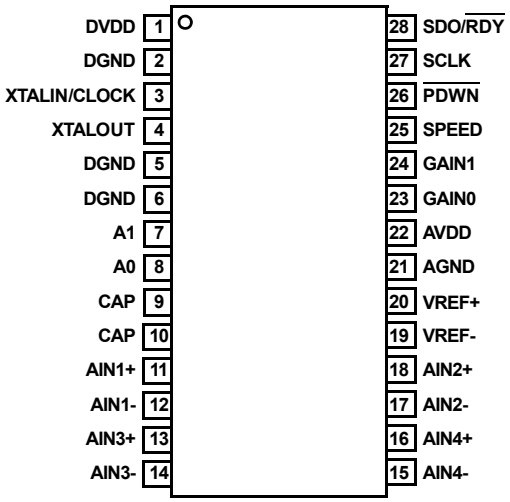
PART NUMBER	NUMBER OF CHANNELS	ON-CHIP TEMPERATURE SENSOR	NUMBER OF PINS
ISL26132	2	YES	24
ISL26134	4	NO	28

Pin Configurations

ISL26132
(24 LD TSSOP)
TOP VIEW



ISL26134
(28 LD TSSOP)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER ISL26132	PIN NUMBER ISL26134	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
DVDD	1	1	Digital	Digital Power Supply (2.7V to 5.25V)
DGND	2, 5, 6	2, 5, 6	Digital	Digital Ground
XTALIN/CLOCK	3	3	Digital/Digital Input	External Clock Input: typically 4.9152MHz. Tie low to activate internal oscillator. Can also use external crystal across XTALIN/CLOCK and XTALOUT pins.
XTALOUT	4	4	Digital	External Crystal connection
TEMP	7	-	Digital Input	On-chip Temperature Diode Enable
A1 A0	- 8	7 8	Digital Input	TABLE 2. INPUT MULTIPLEXER SELECT ISL26134 / ISL26132 A1 / A0 / CHANNEL 0 / 0 / AIN1 0 / 1 / AIN2 1 / 0 / AIN3 1 / 1 / AIN4
CAP	9, 10	9, 10	Analog	PGA Filter Capacitor
AIN1+	11	11	Analog Input	Positive Analog Input Channel 1
AIN1-	12	12	Analog Input	Negative Analog Input Channel 1
AIN3+	-	13	Analog Input	Positive Analog Input Channel 3
AIN3-	-	14	Analog Input	Negative Analog Input Channel 3
AIN4-	-	15	Analog Input	Negative Analog Input Channel 4
AIN4+	-	16	Analog Input	Positive Analog Input Channel 4
AIN2-	13	17	Analog Input	Negative Analog Input Channel 2
AIN2+	14	18	Analog Input	Positive Analog Input Channel 2
VREF-	15	19	Analog Input	Negative Reference Input
VREF+	16	20	Analog Input	Positive Reference Input
AGND	17	21	Analog	Analog Ground
AVDD	18	22	Analog	Analog Power Supply 4.75V to 5.25V
GAIN0 GAIN1	19 20	23 24	Digital Input	TABLE 3. GAIN SELECT GAIN1 / GAIN0 / GAIN 0 / 0 / 1 0 / 1 / 2 1 / 0 / 64 1 / 1 / 128

Pin Descriptions (Continued)

NAME	PIN NUMBER		ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
	ISL26132	ISL26134		
SPEED	21	25	Digital Input	TABLE 4. DATA RATE SELECT SPEED: 0 — DATA RATE: 10Sps SPEED: 1 — DATA RATE: 80Sps
$\overline{\text{PDWN}}$	22	26	Digital Input	Power-Down: Holding this pin low powers down the entire converter and resets the ADC.
SCLK	23	27	Digital Input	Serial Clock: Clock out data on the rising edge. Also used to initiate Offset Calibration and Sleep modes. See “Serial Clock Input (SCLK)” on page 14 for more details.
SDO/$\overline{\text{RDY}}$	24	28	Digital Output	Dual-Purpose Output: Data Ready: Indicate valid data by going low. Data Output: Outputs data, MSB first, on the first rising edge of SCLK.

Circuit Description

The ISL26132 (2-channel) and ISL26134 (4-channel) devices are very low noise 24-bit delta-sigma ADCs that include a programmable gain amplifier and an input multiplexer. The ISL26132 offers an on-chip temperature measurement capability.

The ISL26132, ISL26134 provide pin compatibility and output data compatibility with the ADS1232/ADS1234, and offer the same conversion rates of 10Sps and 80Sps.

All the features of the ISL26132, ISL26134 are pin-controllable, while offset calibration, standby mode, and output conversion data are accessible through a simple 2-wire interface.

The clock can be selected to come from an internal oscillator, an external clock signal, or crystal (4.9152MHz typical).

Absolute Maximum Ratings

A_{GND} to D_{GND} . . . . . -0.3V to +0.3V
Analog In to A_{GND} . . . . . -0.3 to A_{VDD}+0.3V
Digital In to D_{GND} . . . . . -0.3 to D_{VDD}+0.3V
Input Current
Momentary 100mA
Continuous 10mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 7.5kV
Machine Model (Per JESD22-A115) 450V
Charged Device Model (Per JESD22-C101) 2kV
Latch-up (Per JEDEC JESD-78C; Class 2, Level A)
. . . . . 100mA @ Room and Hot (+105°C)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld TSSOP (Notes 4, 5)	65	18
28 Ld TSSOP (Notes 4, 5)	63	18

Maximum Power Dissipation 80mW
Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +105°C
A_{VDD} to A_{GND} . . . . . 4.75V to 5.25V
D_{VDD} to D_{GND} . . . . . 2.7V to 5.25V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{REF}+ = 5V, V_{REF}- = 0V, A_{VDD} = 5V, D_{VDD} = 5V, A_{GND} = D_{GND} = 0V, MCLK = 4.9152MHz, and T_A = -40°C to +105°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C**

SYMBOL	PARAMETER	TEST LEVEL or NOTES	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
ANALOG INPUTS						
	Differential Input Voltage Range			±0.5V_{REF}/ Gain		V
	Common Mode Input Voltage Range	Gain = 1, 2	**A_{GND} - 0.1**		**A_{VDD} + 0.1**	V
		Gain = 64, 128	**A_{GND}+1.5**		**A_{VDD} - 1.5**	V
	Differential Input Current	Gain = 1		±20		nA
		Gain = 2		±40		nA
		Gain = 64, 128		±1		nA
SYSTEM PERFORMANCE						
	Resolution	No Missing Codes	**24**			Bits
	Data Rate	Internal Osc. SPEED = High		80		SPS
		Internal Osc. SPEED = Low		10		SPS
		External Osc. SPEED = High		f_{CLK}/61440		SPS
		External Osc. SPEED = Low		f_{CLK}/491520		SPS
	Digital Filter Settling Time	Full Setting		4		Conversions
INL	Integral Nonlinearity	Differential Input Gain = 1, 2		±0.0002	±0.001	% of FSR (Note 7)
		Differential Input Gain = 64, 128		±0.0004		% of FSR (Note 7)
	Input Offset Error	Gain = 1		±0.4		ppm of FS
		Gain = 128		±1.5		ppm of FS
	Input Offset Drift	Gain = 1		0.3		µV/°C
		Gain = 128		10		nV/°C
	Gain Error (Note 8)	Gain = 1		±0.007	±0.02	%
		Gain = 128		±0.02		%
	Gain Drift	Gain = 1		0.5		ppm/°C
		Gain = 64		3.5		ppm/°C
		Gain = 128		3.5		ppm/°C

Electrical Specifications

$V_{REF}+$ = 5V, V_{REF-} = 0V, A_{VDD} = 5V, D_{VDD} = 5V, A_{GND} = D_{GND} = 0V, MCLK = 4.9152MHz, and T_A = -40°C to +105°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C (Continued)**

SYMBOL	PARAMETER	TEST LEVEL or NOTES	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CMRR	Common Mode Rejection	At DC, Gain = 1, ΔV = 1V	**85**	100		dB
		At DC, Gain = 128, ΔV = 0.1V		100		dB
	50Hz/60Hz Rejection (Note 9)	External 4.9152MHz Clock		130		dB
PSRR	Power Supply Rejection	At DC, Gain = 1, ΔV = 1V	**82**	100		dB
		At DC, Gain = 128, ΔV = 0.1V	**100**	105		dB
	Input Referred Noise	See “Typical Characteristics” beginning on page 8				
	Noise Free Bits	See “Typical Characteristics” beginning on page 8				
VOLTAGE REFERENCE INPUT						
VREF	Voltage Reference Input	VREF = VREF+ - VREF-	**1.5**	AVDD	**A_{VDD} + 0.1**	V
VREF-	Negative Reference Input		**A_{GND} - 0.1**		**V_{REF+} - 1.5**	V
VREF+	Positive Reference Input		**V_{REF-} + 1.5**		**A_{VDD} + 0.1**	V
IREF	Voltage Reference Input Current			±350		nA
POWER SUPPLY REQUIREMENTS						
A_{VDD}	Analog Supply Voltage		**4.75**	5.0	**5.25**	V
D_{VDD}	Digital Supply Voltage		**2.7**	3.3	**5.25**	V
A_{IDD}	Analog Supply Current	Normal Mode, A_{VDD} = 5, Gain = 1, 2		7	**8.5**	mA
		Normal Mode, A_{VDD} = 5, Gain = 64, 128		9	**12**	mA
		Standby Mode		0.2	**3**	µA
		Power-Down		0.2	**2.5**	µA
D_{IDD}	Digital Supply Current	Normal Mode, A_{VDD} = 5, Gain = 1, 2		750	**950**	µA
		Normal Mode, A_{VDD} = 5, Gain = 64, 128		750	**950**	µA
		Standby Mode		1.5	**26**	µA
		Power-Down		1	**26**	µA
P_D	Power Dissipation, Total	Normal Mode, A_{VDD} = 5, Gain = 1, 2			**49.6**	mW
		Normal Mode, A_{VDD} = 5, Gain = 64, 128			**68**	mW
		Standby Mode			**0.14**	mW
		Power-Down			**0.14**	mW
DIGITAL INPUTS						
V_{IH}			**0.7 D_{VDD}**			V
V_{IL}					**0.2 D_{VDD}**	V
V_{OH}		I_{OH} = -1mA	**D_{VDD} - 0.4**			V
V_{OL}		I_{OL} = 1mA			**0.2 D_{VDD}**	V
	Input Leakage Current				**±10**	µA
	External Clock Input Frequency		**0.3**	4.9152		MHz
	Serial Clock Input Frequency			1		MHz

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. FSR = Full Scale Range = VREF/Gain
8. Gain accuracy is calibrated at the factory (AVDD = +5V).
9. Specified for word rate equal to 10Sps.

Noise Performance

The ISL26132 and ISL26134 provide excellent noise performance. The noise performance on each of the gain settings of the PGA at the selected word rates is shown in Tables 5 and 6.

Resolution in bits decreases by 1-bit if the ADC is operated as a single-ended input device. Noise measurements are input-referred, taken with bipolar inputs under the specified operating conditions, with f_{CLK} = 4.9152MHz.

TABLE 5. A_{VDD} = 5V, V_{REF} = 5V, DATA RATE = 10Sps

GAIN	RMS NOISE (nV)	PEAK-TO-PEAK NOISE (nV) (Note 10)	NOISE-FREE BITS (Note 11)
1	243	1604	21.6
2	148	977	21.3
64	11.3	75	20
128	10.6	70	19

TABLE 6. A_{VDD} = 5V, V_{REF} = 5V, DATA RATE = 80Sps

GAIN	RMS NOISE (nV)	PEAK-TO-PEAK NOISE (nV) (Note 10)	NOISE-FREE BITS (Note 11)
1	565	3730	20.4
2	285	1880	20.3
64	29.5	194.8	18.6
128	28.2	186.1	17.6

NOTES:

10. The peak-to-peak noise number is 6.6 times the rms value. This encompasses 99.99% of the noise excursions that may occur. This value best represents the worst case noise that could occur in the output conversion words from the converter.
11. Noise-Free Bits is defined as: Noise-Free Bits = ln(FSR/peak-to-peak noise)/ln(2) where FSR is the full scale range of the converter, VREF/Gain.

Typical Characteristics

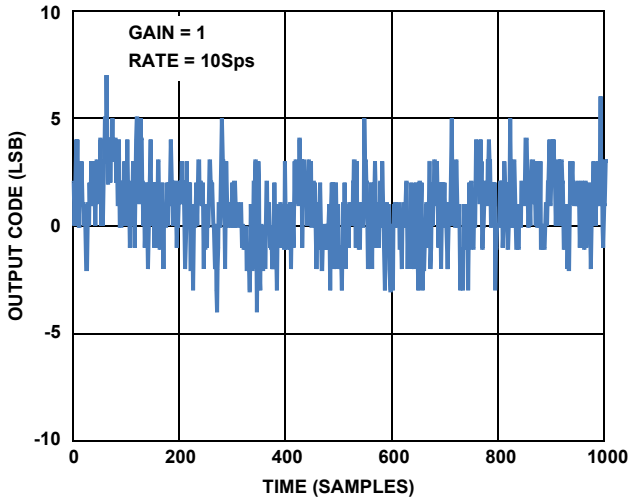


FIGURE 2. NOISE AT GAIN = 1, 10Sps

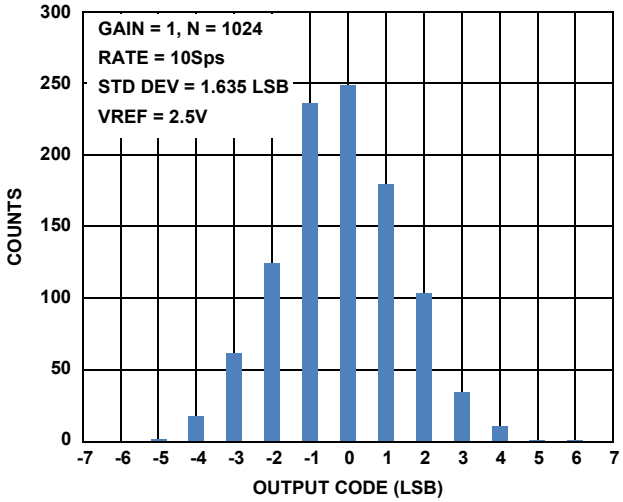


FIGURE 3. NOISE HISTOGRAM AT GAIN = 1, 10Sps

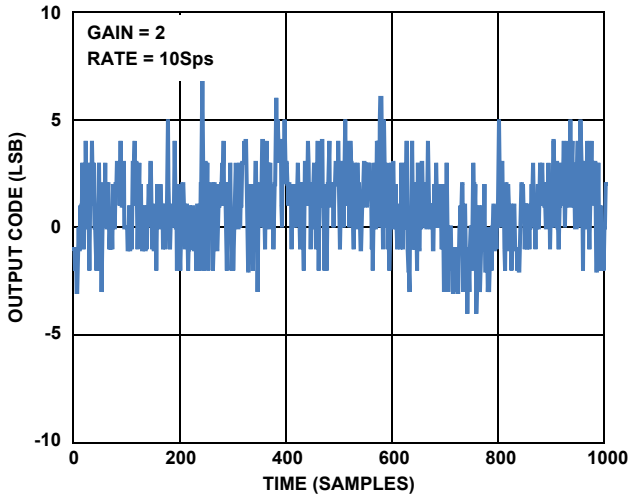


FIGURE 4. NOISE AT GAIN = 2, 10Sps

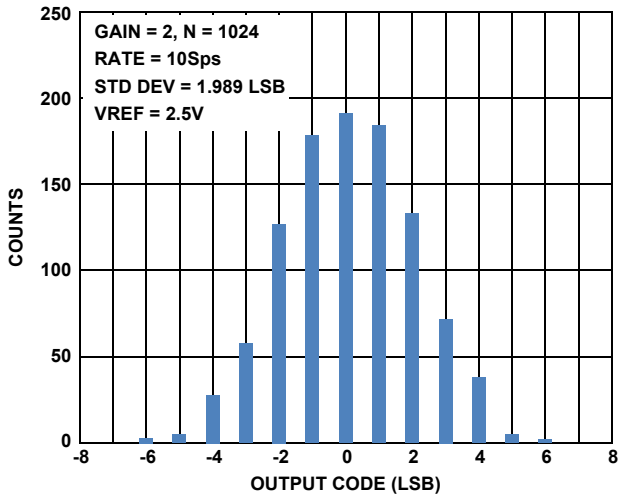


FIGURE 5. NOISE HISTOGRAM AT GAIN = 2, 10Sps

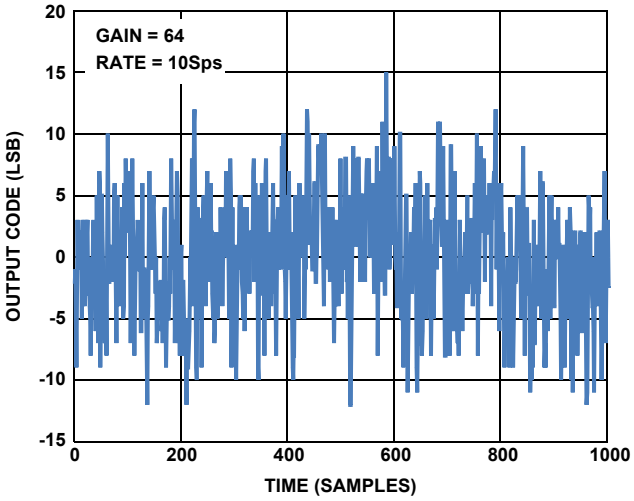


FIGURE 6. NOISE AT GAIN = 64, 10Sps

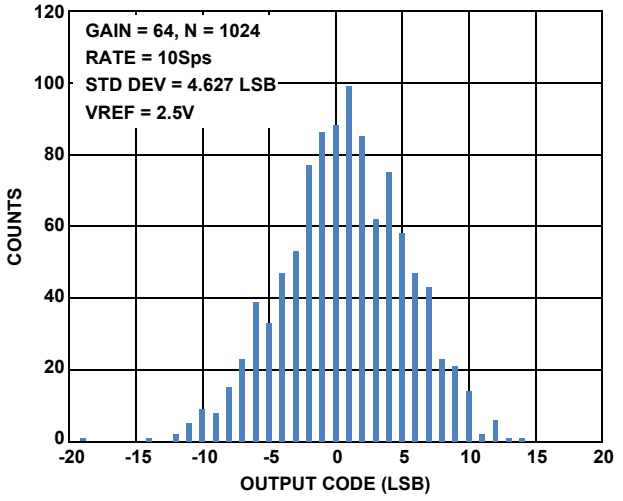


FIGURE 7. NOISE HISTOGRAM AT GAIN = 64, 10Sps

Typical Characteristics (Continued)

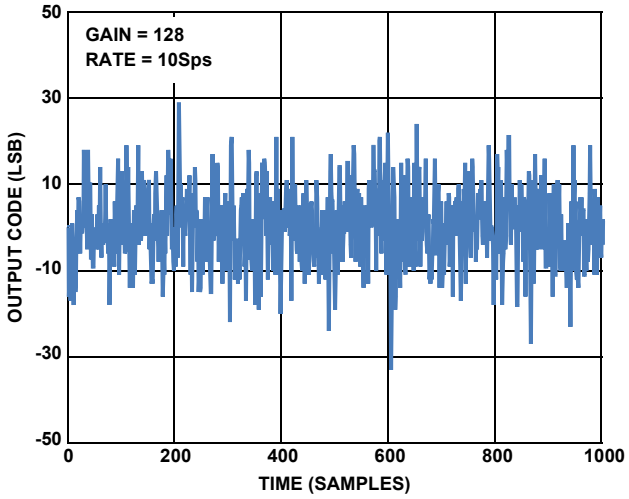


FIGURE 8. NOISE AT GAIN = 128, 10Sps

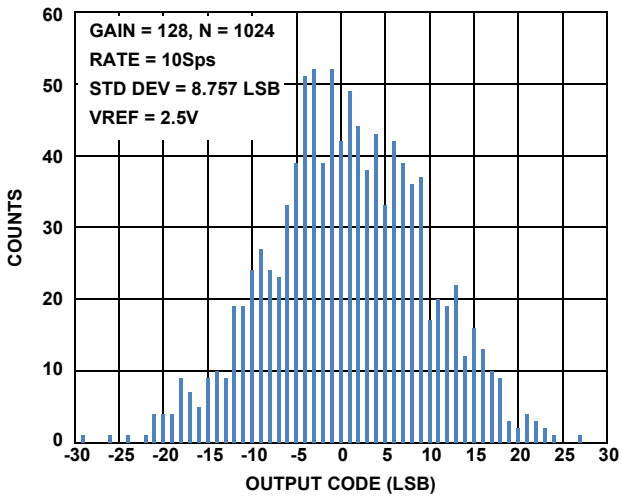


FIGURE 9. NOISE HISTOGRAM AT GAIN = 128, 10Sps

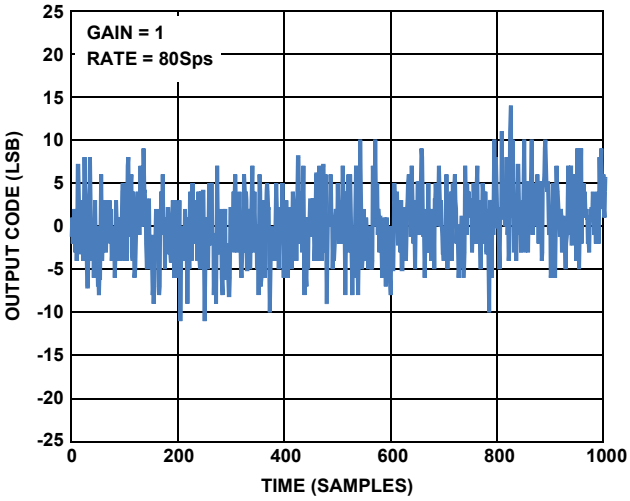


FIGURE 10. NOISE AT GAIN = 1, 80Sps

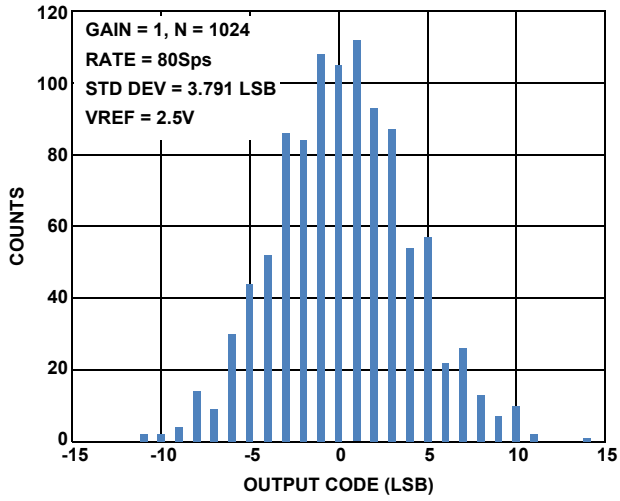


FIGURE 11. NOISE HISTOGRAM AT GAIN = 1, 80Sps

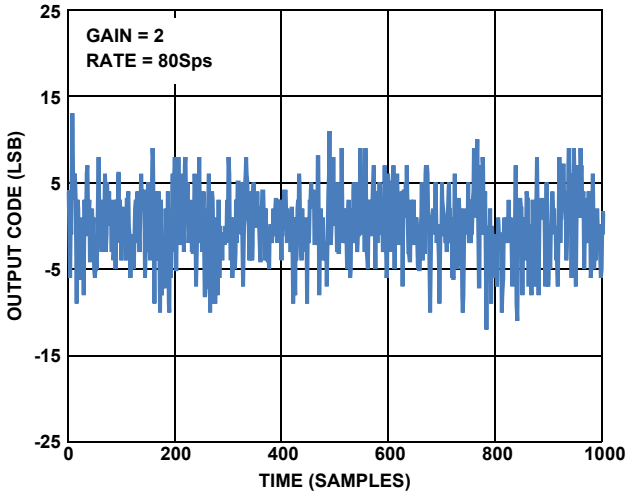


FIGURE 12. NOISE AT GAIN = 2, 80Sps

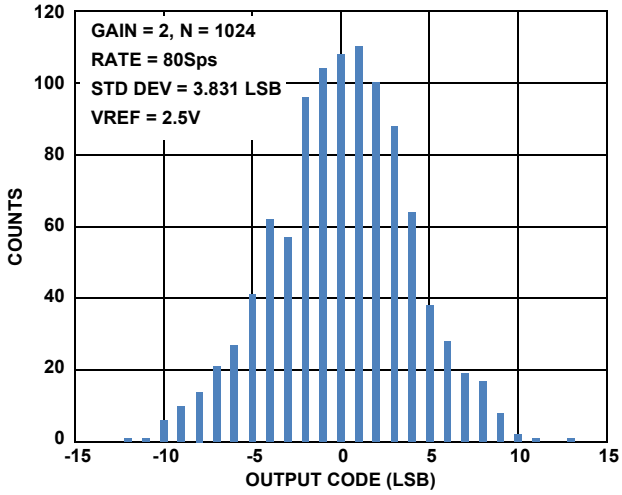


FIGURE 13. NOISE HISTOGRAM AT GAIN = 2, 80Sps

Typical Characteristics (Continued)

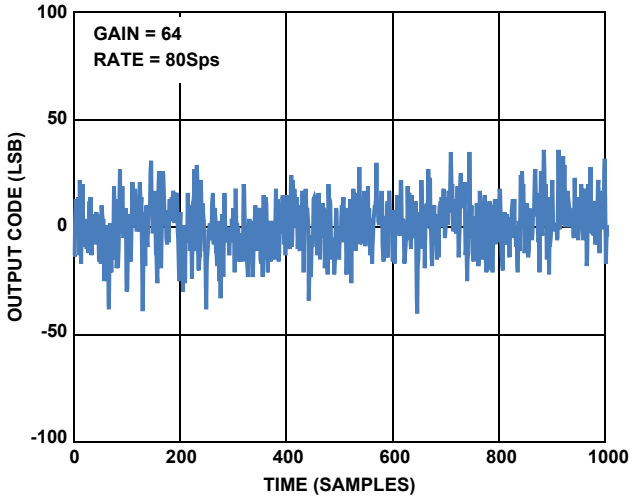


FIGURE 14. NOISE AT GAIN = 64, 80Sps

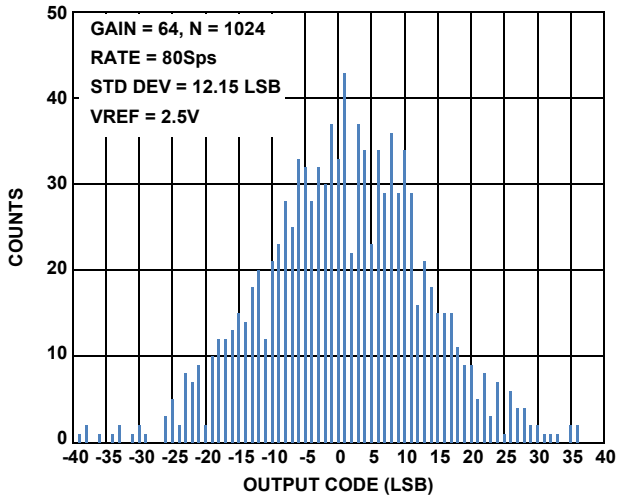


FIGURE 15. NOISE HISTOGRAM AT GAIN = 64, 80Sps

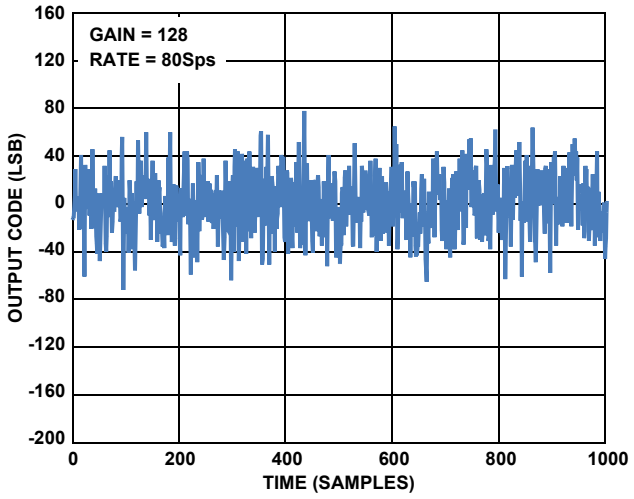


FIGURE 16. NOISE AT GAIN = 128, 80Sps

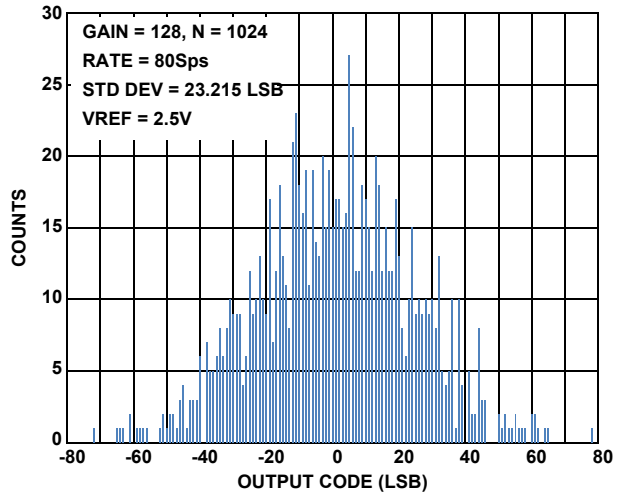


FIGURE 17. NOISE HISTOGRAM AT GAIN = 128, 80Sps

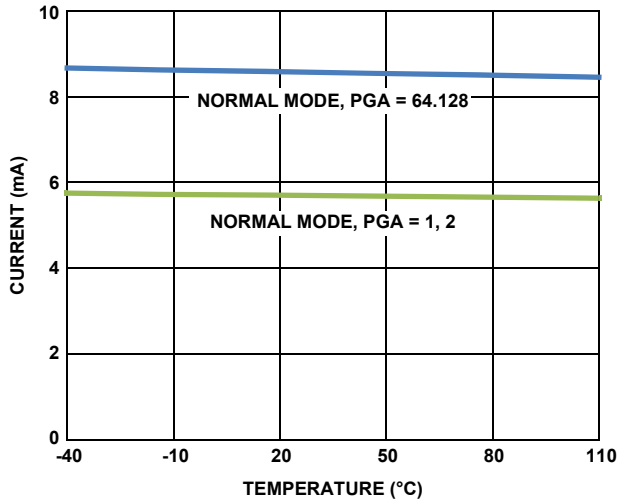


FIGURE 18. ANALOG CURRENT vs TEMPERATURE

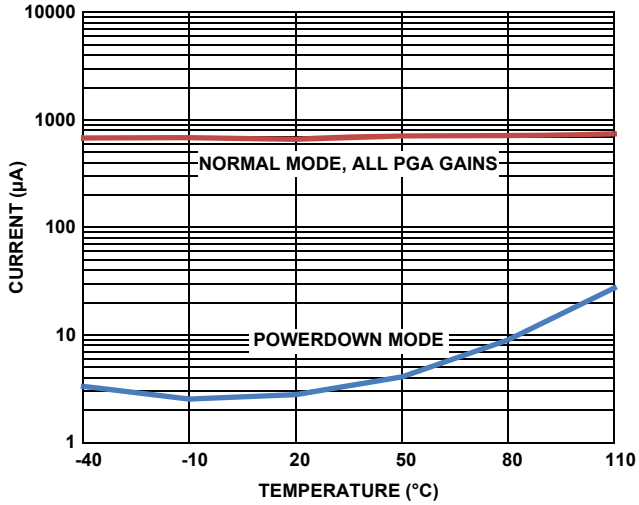


FIGURE 19. DIGITAL CURRENT vs TEMPERATURE

Typical Characteristics (Continued)

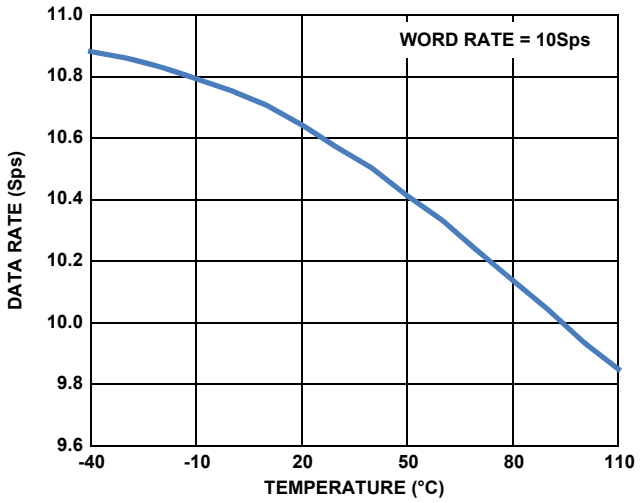


FIGURE 20. TYPICAL WORD RATE vs TEMPERATURE USING INTERNAL OSCILLATOR

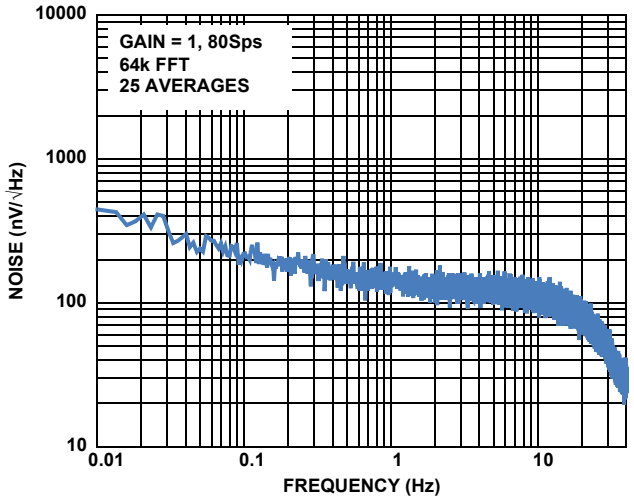


FIGURE 21. NOISE DENSITY vs FREQUENCY AT GAIN = 1, 80Sps

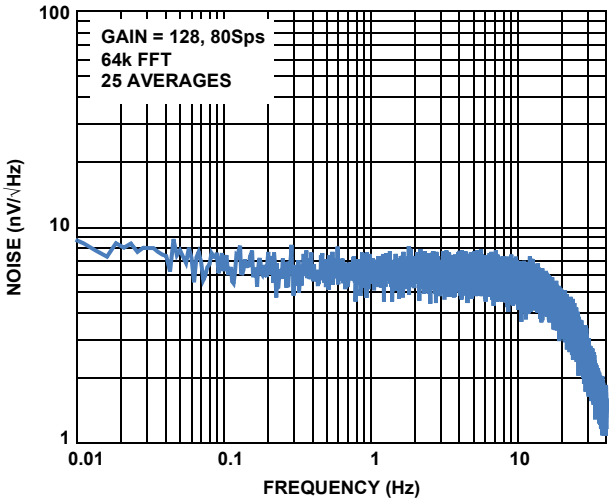


FIGURE 22. NOISE DENSITY vs FREQUENCY AT GAIN = 128, 80Sps

Functional Description

Analog Inputs

The analog signal inputs to the ISL26132 connect to a 2-Channel differential multiplexer and the ISL26134 connect to a 4-Channel differential multiplexer (Mux). The multiplexer connects a pair of inputs to the positive and negative inputs (AINx+, AINx-), selected by the Channel Select Pins A0 and A1 (ISL26134 only). Input channel selection is shown in Table 7. On the ISL26132, the TEMP pin is used to select the Temperature Sensor function.

TABLE 7. INPUT CHANNEL SELECTION

CHANNEL SELECT PINS		ANALOG INPUT PINS SELECTED	
A1	A0	AIN+	AIN-
0	0	AIN1+	AIN1-
0	1	AIN2+	AIN2-
1	0	AIN3+	AIN3-
1	1	AIN4+	AIN4-

Whenever the MUX channel is changed (i.e. if any one of the following inputs - A0/A1, Gain1/0, SPEED is changed), the digital logic will automatically restart the digital filter and will cause SDO/$\overline{RDY}$ to go low only when the output is fully settled. But if the input itself is suddenly changed, then the user needs to ignore the first four $\overline{RDY}$ pulses (going low) to get an accurate measurement of the input signal.

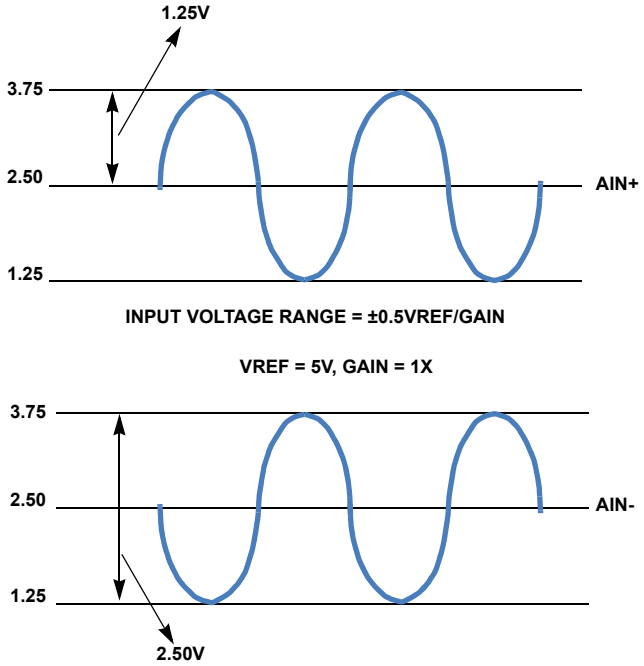


FIGURE 23. DIFFERENTIAL INPUT FOR VREF = 5V, GAIN = 1X

The input span of the ADC is ±0.5 VREF/GAIN. For a 5V VREF and a gain of 1x, the input span will be $5V_{P-P}$ fully differential as shown in Figure 23. Note that input voltages that exceed the supply rails by more than 100mV will turn on the ESD protection diodes and degrade measurement accuracy.

If the differential input exceeds well above the +VE or the -VE FS (by ~1.5x times) the output code will clip to the corresponding FS value. Under such conditions, the output data rate will become 1/4th of the original value as the Digital State Machine will RESET the Delta-Sigma Modulator and the Decimation Filter.

Temperature Sensor (ISL26132 only)

When the TEMP pin of the ISL26132 is set High, the input multiplexer is connected to a pair of diodes, which are scaled in both size and current. The voltage difference measured between them corresponds to the temperature of the die according to Equation 1:

$$V = 102.2mV + (379\mu V*T(°C))*Gain \quad \text{(EQ. 1)}$$

Note: Valid only for GAIN = 1x or 2x

Where T is the temperature of the die, and Gain = the PGA Gain Setting.

At a temperature of +25°C, the measured voltage will be approximately 111.7mV. Note that this measurement indicates only the temperature of the die itself. Applying the result to correct for the temperature drift of a device external to the package requires that thermal coupling between the sensor and the die be taken into account.

Low-Noise Programmable Gain Amplifier (PGA)

The chopper-stabilized programmable gain amplifier features a variety of gain settings to achieve maximum dynamic range and measurement accuracy from popular sensor types with excellent low noise performance, input offset error, and low drift, and with minimal external parts count. The GAIN0 and GAIN1 pins allow the user to select gain settings of 1x, 2x, 64x, or 128x. A block diagram is shown in Figure 24. The differential input stage provides a gain of 64, which is bypassed when the lower gain settings are selected. The lower gain settings (1 and 2) will accept inputs with common mode voltages up to 100mV outside the rails, allowing the device to accept ground-referred signals. At gain settings of 64 or 128 the common mode voltage at the inputs is limited to 1.5V inside the supply rails while maintaining specified measurement accuracy.

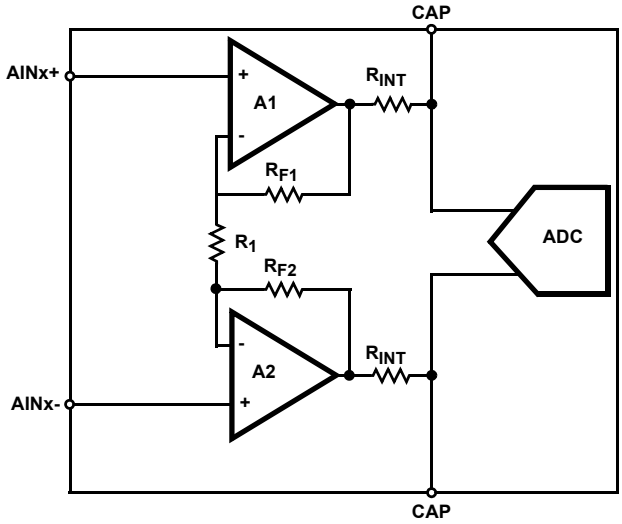


FIGURE 24. SIMPLIFIED PROGRAMMABLE GAIN AMPLIFIER BLOCK DIAGRAM

Filtering PGA Output Noise

The programmable gain amplifier, as shown in Figure 24, includes a passive RC filter on its output. The resistors are located inside the chip on the outputs of the differential amplifier stages. The capacitor (nominally a 100nF C0G ceramic or a PPS film (Polyphenylene sulfide)) for the filter is connected to the two CAP pins of the chip. The outputs of the differential amplifier stages of the PGA are filtered before their signals are presented to the delta-sigma modulator. This filter reduces the amount of noise by limiting the signal bandwidth and filters the chopping artifacts of the chopped PGA stage.

Voltage Reference Inputs (VREF+, VREF-)

The voltage reference for the ADC is derived from the difference in the voltages presented to the VREF+ and VREF- pins; VREF = (VREF+ - VREF-). The ADCs are specified with a voltage reference value of 5V, but a voltage reference as low as 1.5V can be used. For proper operation, the voltage on the VREF+ pin should not be greater than AVDD + 0.1V and the voltage on the VREF- pin should not be more negative than AGND - 0.1V.

Clock Sources

The ISL26132, ISL26134 can operate from an internal oscillator, an external clock source, or from a crystal connected between the XTALIN/CLOCK and XTALOUT pins. See the block diagram of the clock system in Figure 25. When the ADC is powered up, the CLOCK DETECT block determines if an external clock source is present. If a clock greater than 300kHz is present on the XTALIN/CLOCK pin, the circuitry will disable the internal oscillator on the chip and use the external clock as the clock to drive the chip circuitry. If the ADC is to be operated from the internal oscillator, the XTALIN/CLOCK pin should be grounded.

If the ADC is to be operated from a crystal, it should be located close to the package pins of the ADC. Note that external loading capacitors for the crystal are not required as there are loading capacitors built into the silicon, although the capacitor values are optimized for operation with a 4.9152MHz crystal.

The XTALOUT pin is not intended to drive external circuits.

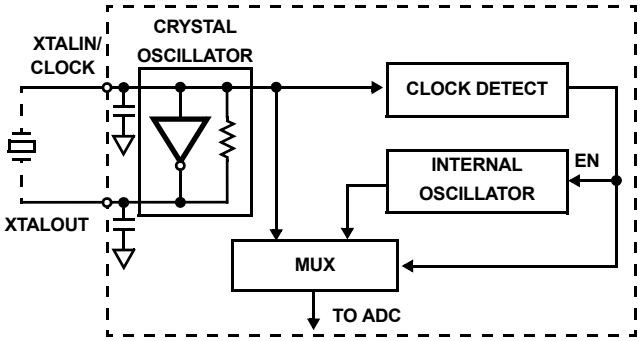


FIGURE 25. CLOCK BLOCK DIAGRAM

Digital Filter Characteristics

The digital filter inside the ADC is a fourth-order Sinc filter. Figures 26 and 27 on page 14 on illustrate the filter response for the ADC when it is operated from a 4.9152MHz crystal. The internal oscillator is factory trimmed so the frequency response for the filter will be much the same when using the internal oscillator. The figures illustrate that when the converter is operated at 10Sps the digital filter provides excellent rejection of 50Hz and 60Hz line interference.

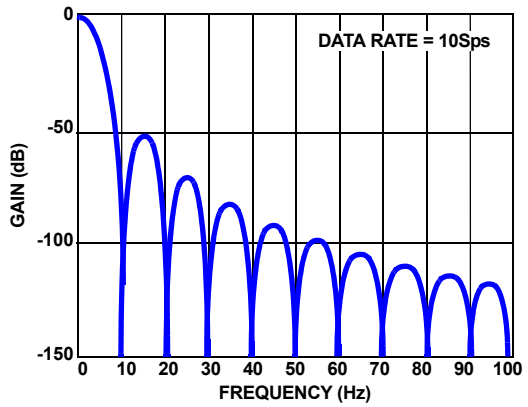


FIGURE 26. 10Sps: FREQUENCY RESPONSE OUT TO 100Hz

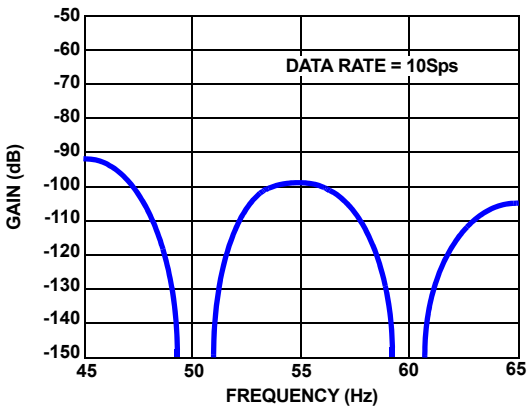


FIGURE 27. 10Sps: 50/60Hz NOISE REJECTION, 45Hz TO 65Hz

Serial Clock Input (SCLK)

The serial clock input is provided with hysteresis to minimize false triggering. Nevertheless, care should be taken to ensure reliable clocking.

Filter Settling Time and ADC Latency

Whenever the analog signal into the ISL26132, ISL26134 converters is changed, the effects of the digital filter must be taken into account. The filter takes four data ready periods for the output code to fully reflect a new value at the analog input. If the multiplexer control input is changed, the modulator and the digital filter are reset, and the device uses four data ready periods to fully settle to yield a digital code that accurately represents the analog input. Therefore, from the time the control inputs for the multiplexer are changed until the SDO/$\overline{\text{RDY}}$ goes low, four data ready periods will elapse. The settling time delay after a multiplexer channel change is listed in Table 8 for the converter operating in continuous conversion mode. This is also shown pictorially in Figure 28 for a change in the MUX setting and Figure 29 for an abrupt change in the analog input V_{IN}.

TABLE 8. SETTLING TIME

PARAMETER	DESCRIPTION (f_{CLK} = 4.9152MHz)		MIN	MAX	UNITS
t_S	A0, A1, SPEED, Gain1, Gain0 change set-up time		40	50	µs
t1	Settling time	SPEED = 1	54	55	ms
		SPEED = 0	404	405	ms

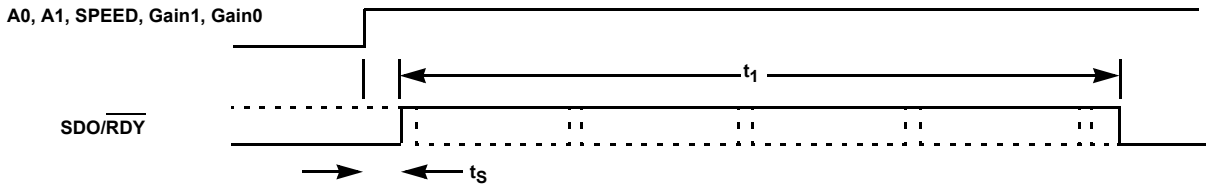


FIGURE 28. SDO/$\overline{\text{RDY}}$ DELAY AFTER MULTIPLEXER CHANGE

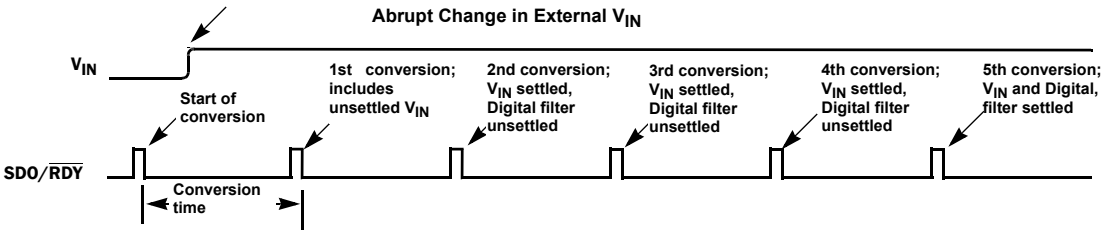


FIGURE 29. SDO/$\overline{RDY}$ DELAY AFTER MULTIPLEXER CHANGE

Conversion Data Rate

The SPEED pin is used to select between the 10Sps and 80Sps conversion rates. The 10Sps rate (SPEED = Low) is preferred in applications requiring 50/60Hz noise rejection. Note that the sample rate is directly related to the oscillator frequency, as 491,520 clocks are required to perform a conversion at the 10Sps rate, and 61,440 clocks at the 80Sps rate.

Output Data Format

The 24-bit converter output word is delivered in two's complement format. Input exceeding full scale results in a clipped output which will not return to in-range values until after the input signal has returned to the specified allowable voltage range and the digital filter has settled as discussed previously.

TABLE 9. OUTPUT CODES CORRESPONDING TO INPUT

INPUT SIGNAL	OUTPUT CODE (HEX)
$\geq +0.5V_{REF}/GAIN$	7FFFFF
$(+0.5V_{REF}/GAIN)/(2^{23} - 1)$	000001
0	000000
$(-0.5V_{REF}/GAIN)/(2^{23} - 1)$	FFFFFF
$\leq -0.5V_{REF}/GAIN$	800000

Reading Conversion Data from the Serial Data Output/Ready SDO/$\overline{RDY}$ Pin

When the ADC is powered, it will automatically begin doing conversions. The SDO/$\overline{RDY}$ signal will go low to indicate the completion of a conversion. After the SDO/$\overline{RDY}$ signal goes low, the MSB data bit of the conversion word will be output from the SDO/$\overline{RDY}$ pin after SCLK is transitioned from a low to a high. Each subsequent new data bit is also output on the rising edge of SCLK (see Figure 30). The receiving device should use the falling edge of SCLK to latch the data bits. After the 24th SCLK, the SDO/$\overline{RDY}$ output will remain in the state of the LSB data bit until a new conversion is completed. At this time, the SDO/$\overline{RDY}$ will go high if low and then go low to indicate that a new conversion word is available. If not all data bits are read from the SDO/$\overline{RDY}$ pin prior to the completion of a new conversion, they will be overwritten. SCLK should be low during time t_6, as shown in Figure 30, when SDO/$\overline{RDY}$ is high.

If the user wants the SDO/$\overline{RDY}$ signal to go high after reading the 24 bits of the conversion data word, a 25th SCLK can be issued. The 25th SCLK will force the SDO/$\overline{RDY}$ signal to go high and remain high until it falls to signal that a new conversion word is available. Figure 31 illustrates the behavior of the SDO/$\overline{RDY}$ signal when a 25th SCLK is used.

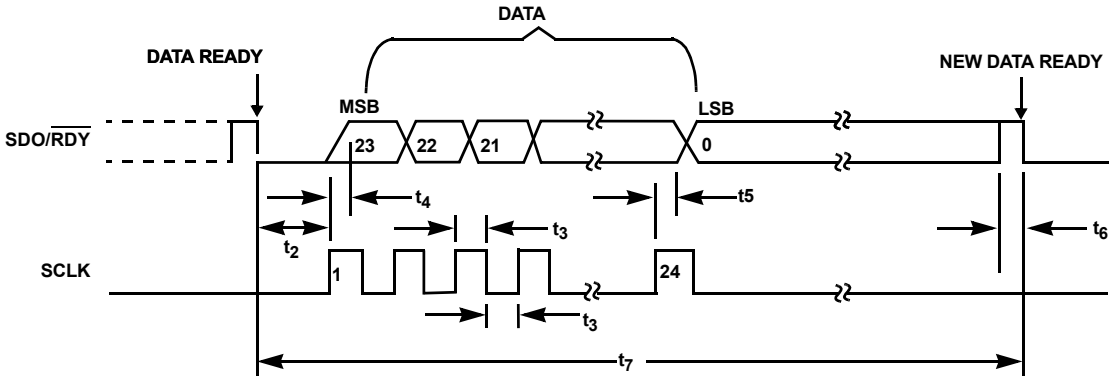


FIGURE 30. OUTPUT DATA WAVEFORMS USING 24 SCLKS TO READ CONVERSION DATA

TABLE 10. INTERFACE TIMING CHARACTERISTICS

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
t_2	SDO/$\overline{RDY}$ Low to first SLK		0			ns
t_3	SCLK pulsewidth, Low or High		100			ns
t_4	SCLK High to Data Valid				50	ns
t_5	Data Hold after SCLK High		0			ns
t_6	Register Update Time		39			µs
t_7	Conversion Period	SPEED = 1		12.5		ms
		SPEED = 0		100		ms

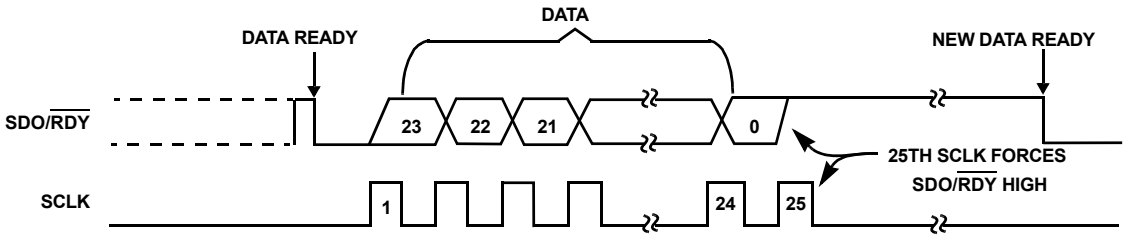


FIGURE 31. OUTPUT DATA WAVEFORMS FOR SDO/$\overline{RDY}$ POLLING

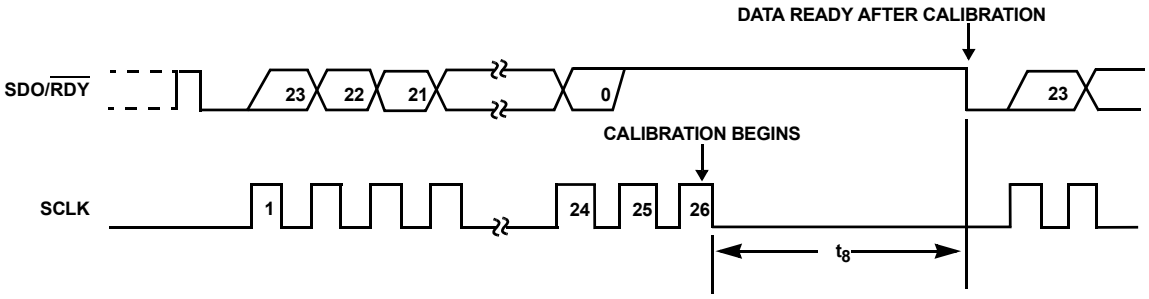


FIGURE 32. OFFSET CALIBRATION WAVEFORMS

Offset Calibration Control

The offset internal to the ADC can be removed by performing an offset calibration operation. Offset calibration can be initiated immediately after reading a conversion word with 24 SCLKs by issuing two additional SCLKs. The offset calibration operation will begin immediately after the 26th SCLK occurs. Figure 32 illustrates the timing details for the offset calibration operation.

During offset calibration, the analog inputs are shorted internally and a regular conversion is performed. This conversion generates a conversion word that represents the offset error. This value is stored and used to digitally remove the offset error from future conversion words. The SDO/$\overline{RDY}$ output will fall to indicate the completion of the offset calibration operation.

TABLE 11. SDO/$\overline{RDY}$ DELAY AFTER CALIBRATION

PARAMETER		MIN	MAX	UNITS
t_8	SPEED = 1	108	109	ms
	SPEED = 0	808	809	ms

Standby Mode Operation

The ADC can be put into standby mode to save power. Standby mode reduces the power to all circuits in the device except the crystal oscillator amplifier. To enter the standby mode, take the SCLK signal high and hold it high after SDO/$\overline{RDY}$ falls. The converter will remain in standby mode as long as SCLK is held high. To return to normal operation, take SCLK back low and wait for the SDO/$\overline{RDY}$ to fall to indicate that a new conversion has completed. Figure 33 and Table 12 illustrate the details of standby mode.

Supply currents are equal in Standby and Power-down modes unless a Crystal is used. If the Crystal is used, the Crystal amplifier is turned ON, even in the standby mode.

Performing Offset Calibration After Standby Mode

To perform an offset calibration automatically upon returning from standby, deliver two or more additional SCLKs following a data read cycle, and then set and hold SCLK high. The device will remain in Standby as long as SCLK remains high. A calibration cycle will begin once SCLK is brought low again to resume normal operation. Additional time will be required to perform the calibration after returning from Standby. Figure 34 and Table 13 illustrate the details of performing offset calibration after standby mode.

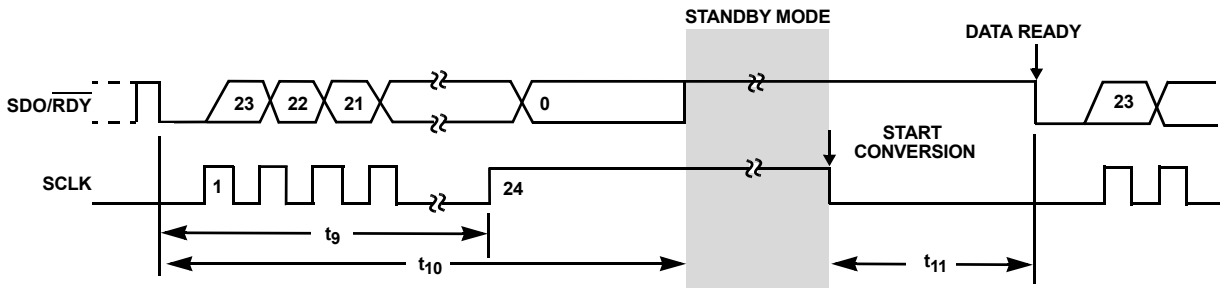


FIGURE 33. STANDBY MODE WAVEFORMS

TABLE 12. STANDBY MODE TIMING

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
t_9	SCLK High after SDO/$\overline{RDY}$ Low	SPEED = 1	0	12.44	ms
		SPEED = 0	0	99.94	ms
t_{10}	Standby Mode Delay	SPEED = 1	12.5		ms
		SPEED = 0	100		ms
t_{11}	SDO/$\overline{RDY}$ falling edge after SCLK Low	SPEED = 1	50	60	ms
		SPEED = 0	400	410	ms

TABLE 13. OFFSET CALIBRATION TIMING AFTER STANDY

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
t_{12}	SDO/$\overline{RDY}$ Low after SCLK Low	SPEED = 1	108	113	ms
		SPEED = 0	808	813	ms

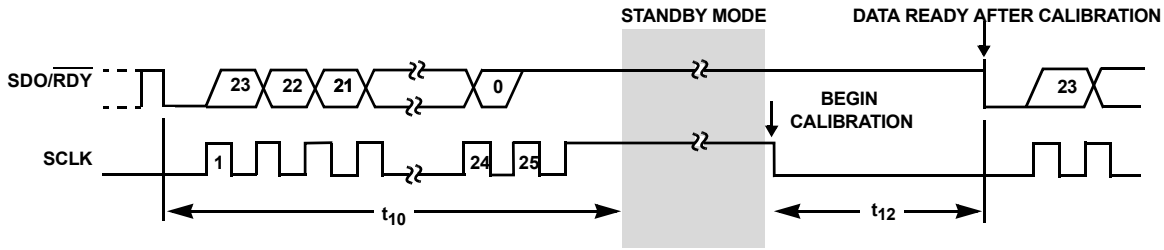


FIGURE 34. OFFSET CALIBRATION WAVEFORMS AFTER STANDBY

Operation of $\overline{\text{PDWN}}$

$\overline{\text{PDWN}}$ must transition from low to high after both power supplies have settled to specified levels in order to initiate a correct power-up reset (Figure 35). This can be implemented by an external controller or a simple RC delay circuit, as shown in Figure 36.

In order to reduce power consumption, the user can assert the Power-down mode by bringing $\overline{\text{PDWN}}$ Low as shown in Figure 37. All circuitry is shut down in this mode, including the Crystal Oscillator. After $\overline{\text{PDWN}}$ is brought High to resume operation, the reset delay varies depending on the clock source used. While an external clock source will resume operation immediately, a circuit utilizing a crystal will incur about a 20ms delay due to the inherent start-up time of this type of oscillator.

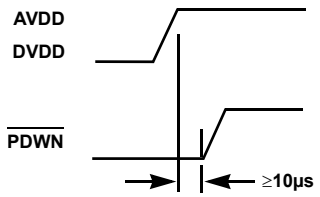


FIGURE 35. POWER-DOWN TIMING RELATIVE TO SUPPLIES

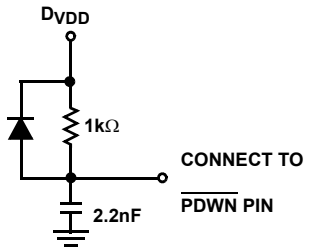


FIGURE 36. $\overline{\text{PDWN}}$DELAY CIRCUIT

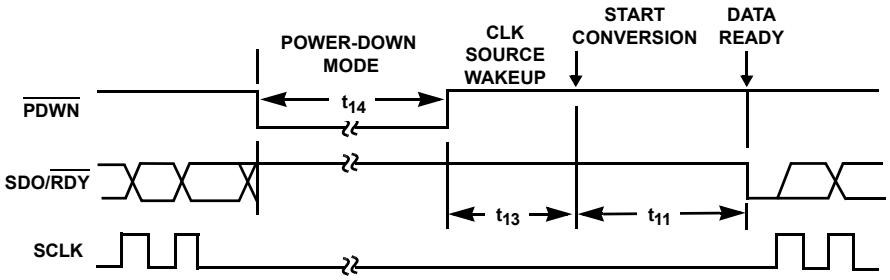


FIGURE 37. POWER-DOWN MODE WAVEFORMS

TABLE 14. POWER-DOWN RECOVERY TIMING

PARAMETER	DESCRIPTION		TYP	UNITS
t_{13}	Clock Recovery after $\overline{\text{PDWN}}$ High	Internal Oscillator	7.95	µs
		External Clock Source	0.16	µs
		4.9152MHz Crystal Oscillator	5.6	ms
t_{14}	$\overline{\text{PDWN}}$ Pulse Duration		26	µs (min)

Application Information

Power-up Sequence – Initialization and Configuration

The sequence to properly power-up and initialize the device are as follows. For details on individual functions, refer to their descriptions.

1. A_{VDD}, D_{VDD} ramp to specified levels
2. Apply External Clock
3. Pull $\overline{PDWN}$ High to initiate Reset
4. Device begins conversion
5. SDO/$\overline{RDY}$ goes low at end of first conversion

OPTIONAL ACTIONS

- Perform Offset Calibration
- Place device in Standby
- Return device from Standby
- Read on-chip Temperature (applicable to ISL26132 only)

Application Examples

WEIGH SCALE SYSTEM

Figure 38 illustrates the ISL26132 connected to a load cell. The A/D converter is configured for a gain of 128x and a sample rate of 10Sps. If a load cell with 2mV/V sensitivity is used, the full scale output from the load cell will be 10mV. On a gain of 128x and sample rate of 10Sps, the converter noise is $67nV_{P-P}$. The converter will achieve $10mV/67nV_{P-P}$ = 149,250 noise free counts across its 10mV input signal. This equates to 14,925 counts per millivolt of input signal. If five output words are averaged together this can be improved by √5 to yield √5*14925 counts = 33,370 counts per millivolt of input signal with an effective update rate of 2 readings per second.

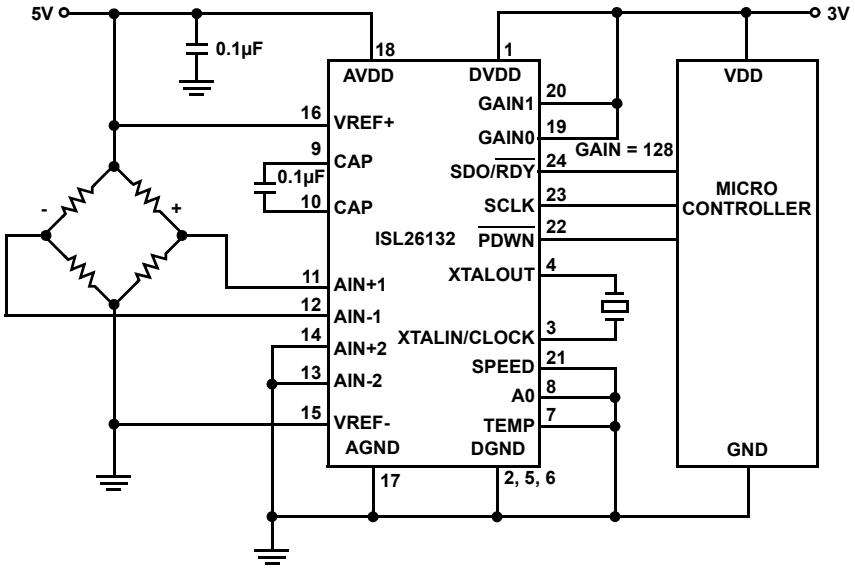


FIGURE 38. WEIGH SCALE APPLICATION

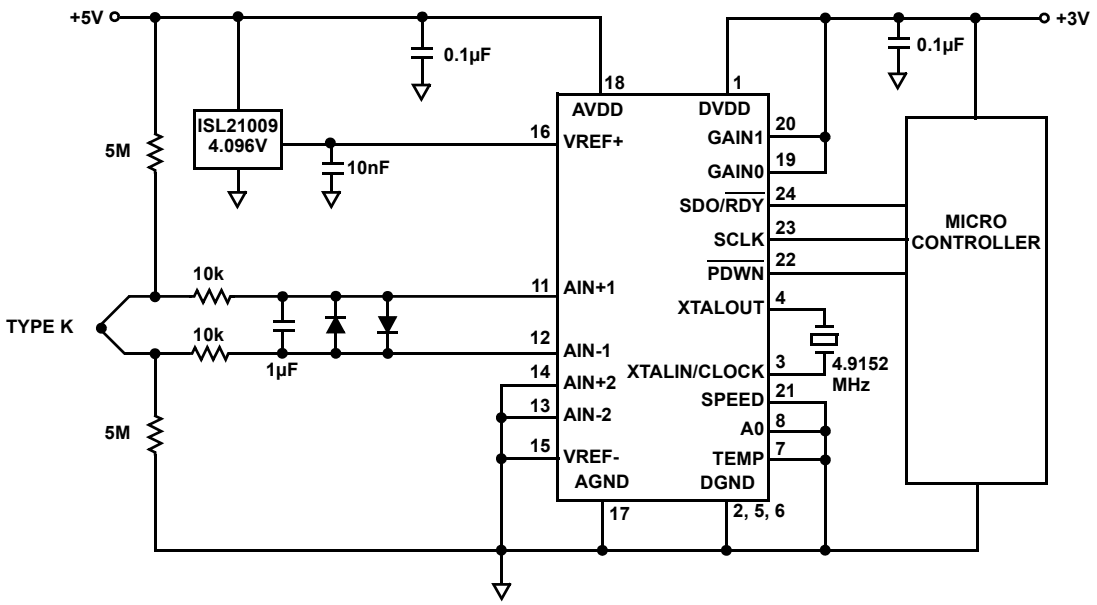


FIGURE 39. THERMOCOUPLE MEASUREMENT APPLICATION

THERMOCOUPLE MEASUREMENT

Figure 39 illustrates the ISL26132 in a thermocouple application. The 4.096V reference combined with the PGA gain set to 128x sets the input span of the converter to ±16mV. This supports the K type thermocouple measurement for temperatures from -270°C at -6.485mV to +380°C at about 16mV.

If a higher temperature is preferred, the PGA can be set to 64x to provide a converter span of ±32mV. This will allow the converter to support temperature measurement with the K type thermocouple up to about +765°C.

Figure 39 shows that the thermocouple is referenced to a voltage dictated by the resistor divider from the +5V supply to ground. These set the common mode voltage at about 2.5V. The 5M resistors provide a means for detection of an open thermocouple. If the thermocouple fails to open or is not connected, the bias through the 5M resistors will cause the input to the PGA to go to full scale.

PCB Board Layout and System Configuration

The ISL26132, ISL26134 ADC is a very low noise converter. To achieve the full performance available from the device will require attention to the printed circuit layout of the circuit board. Care should be taken to have a full ground plane without impairments (traces running through it) directly under the chip on the back side of the circuit board. The analog input signals should be laid down adjacent (AIN+ and AIN- for each channel) to achieve good differential signal practice and routed away from any traces carrying active digital signals. The connections from the CAP pins to the off-chip filter capacitor should be short, and without any digital signals nearby. The crystal, if used, should be connected with relatively short leads. No active digital signals should be routed near or under the crystal case or near the traces, which connect it to the ADC. The AGND and DGND pins of the ADC should be connected to a common solid ground plane. All digital signals to the chip should be powered from the same supply, as that used for DVDD (do not allow digital signals to be active high unless the DVDD supply to the chip is alive). Route all active digital signals in a way to keep distance from any analog pin on the device (AIN, VREF, CAP, AVDD). Power on the AVDD supply should be active before the VREF voltage is present.

PCB layout patterns for the chips (ISL26132 and ISL26134) are found on the respective package outline drawings on pages 22 and 23.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
November 20, 2014	FN6954.3	Datasheet updated with minor text and graphic changes.
November 12, 2012	FN6954.2	Changed in Abs Max Rating on page 5 Latchup JESD from 78B to 78C Electrical Spec Table Gain Drift on page 5 changed the following: Added Gain = 64 and Typical value of 3.5 Changed Gain = 128 Typical value from 7 to 3.5 Table 5 on page 7 changed the following: Gain 64 RMS changed from 10.8 to 11.3 Peak to Peak from 71 to 75 NFB from 20.1 to 20 Gain 128 RMS changed from 10.2 to 10.6 Peak to Peak from 67 to 70 NFB from 19.1 to 19 Table 6 on page 7 changed the following: Gain 64 RMS changed from 28.3 to 29.5 Peak to Peak from 187 to 194.8 NFB from 18.7 to 18.6 Gain 128 RMS changed from 27 to 28.2 Peak to Peak from 178 to 186.1 NFB from 17.7 to 17.6
September 08, 2011	FN6954.1	Power Supply Requirements on page 6 - AIDD - Analog Supply Current - Normal Mode, AVDD = 5, Gain = 1,2 changed TYP and MAX from “6, 7.3” to “7, 8.5” Power Dissipation, Total Normal Mode, AVDD = 5, Gain = 1, 2 changed from “43.3” to “49.6” mW (Max)
August 22, 2011	FN6954.0	Initial Release.

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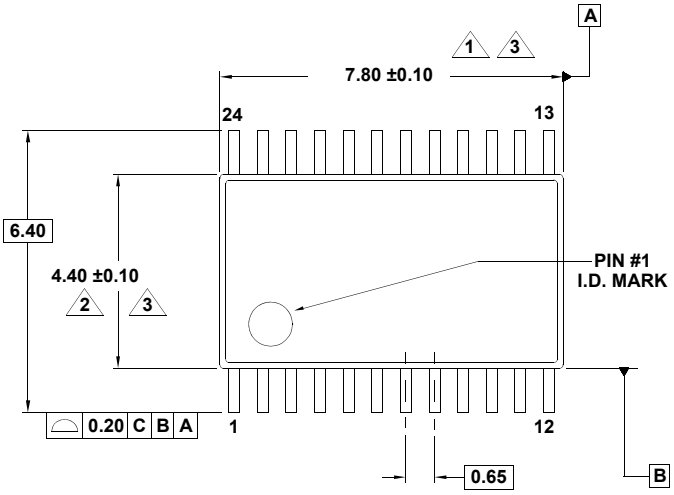
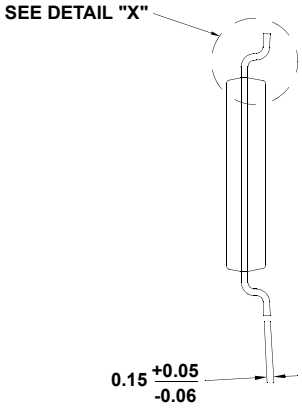
Package Outline Drawing

M24.173

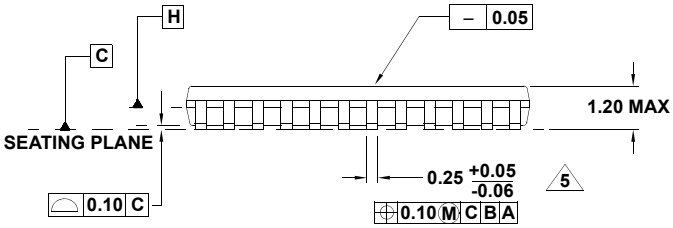
24 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10



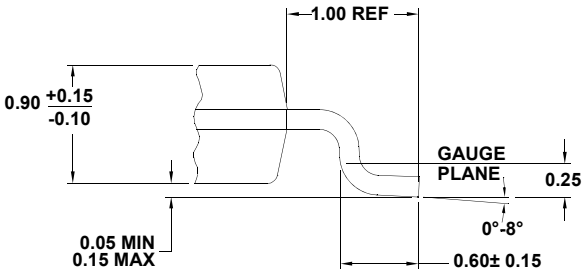
TOP VIEW



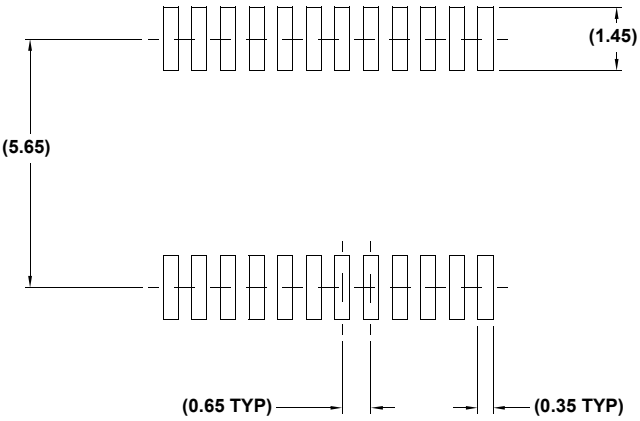
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

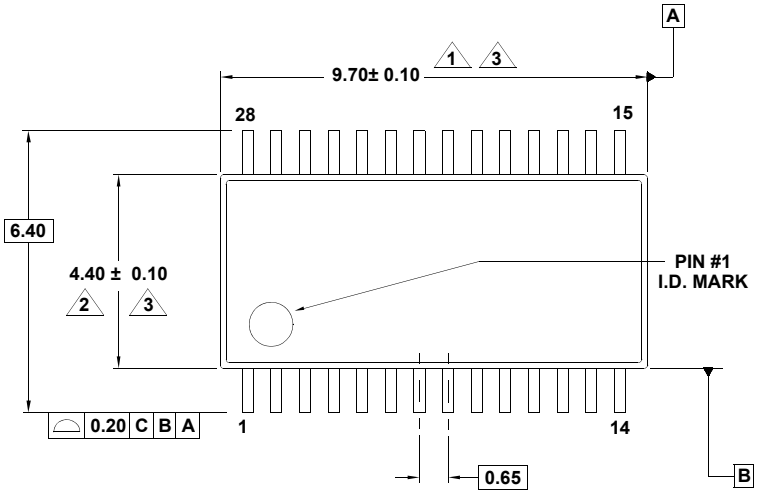
NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

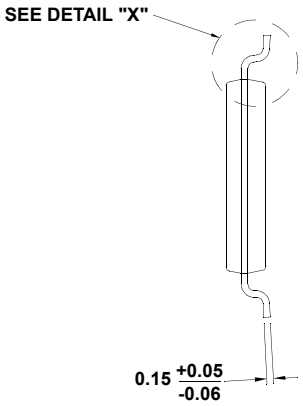
Package Outline Drawing

M28.173

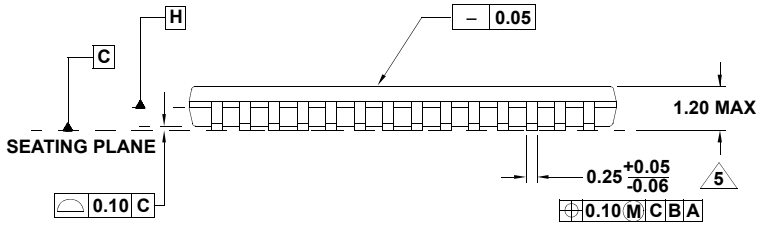
28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10



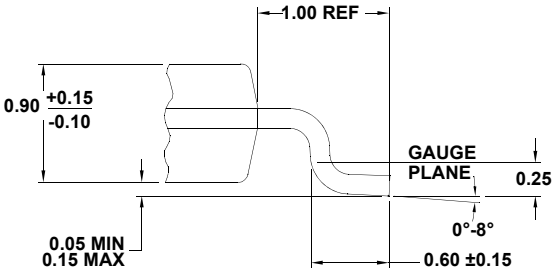
TOP VIEW



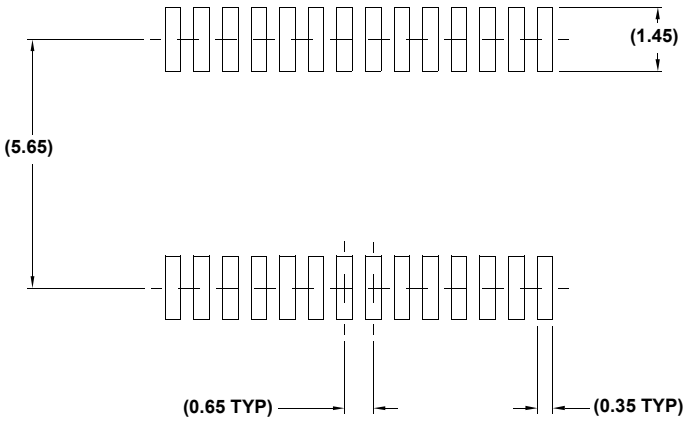
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

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7. Conforms to JEDEC MO-153.