19-3440; Rev 0; 10/04

EVALUATION KIT AVAILABLE

14-Bit, 80Msps, 3.3V ADC

MAX12554

General Description

The MAX12554 is a 3.3V, 14-bit, 80Msps analog-to-digital converter (ADC) featuring a fully differential wideband track-and-hold (T/H) input amplifier, driving a low-noise internal quantizer. The analog input stage accepts single-ended or differential signals. The MAX12554 is optimized for high dynamic performance, low power, and small size. Excellent dynamic performance is maintained from baseband to input frequencies of 175MHz and beyond, making the MAX12554 ideal for intermediate-frequency (IF) sampling applications.

Powered from a single 3.3V supply, the MAX12554 consumes only 429mW while delivering a typical 70.9dB signal-to-noise ratio (SNR) performance at a 175MHz input frequency. In addition to low operating power, the MAX12554 features a 300µW power-down mode to conserve power during idle periods.

A flexible reference structure allows the MAX12554 to use the internal 2.048V bandgap reference or accept an externally applied reference. The reference structure allows the full-scale analog input range to be adjusted from ±0.35V to ±1.10V. The MAX12554 provides a common-mode reference to simplify design and reduce external component count in differential analog input circuits.

The MAX12554 supports either a single-ended or differential input clock. Wide variations in the clock duty cycle are compensated with the ADC's internal duty-cycle equalizer (DCE).

ADC conversion results are available through a 14-bit, parallel, CMOS-compatible output bus. The digital output format is pin selectable to be either two's complement or Gray code. A data-valid indicator eliminates external components that are normally required for reliable digital interfacing. A separate digital power input accepts a wide 1.7V to 3.6V supply, allowing the MAX12554 to interface with various logic levels.

The MAX12554 is available in a 6mm x 6mm x 0.8mm, 40-pin thin QFN package with exposed paddle (EP), and is specified for the extended industrial (-40°C to +85°C) temperature range.

See the *Pin-Compatible Versions* table for a complete family of 14-bit and 12-bit high-speed ADCs.

Applications

IF and Baseband Communication Receivers
Cellular, Point-to-Point Microwave, HFC, WLAN

Medical Imaging Including Positron Emission Tomography (PET)

Video Imaging

Portable Instrumentation

Low-Power Data Acquisition

Features

- **Direct IF Sampling Up to 400MHz**
- **Excellent Dynamic Performance**
  72.4dB/70.9dB SNR at f_{IN} = 3MHz/175MHz
  86.2dBc/82.5dBc SFDR at f_{IN} = 3MHz/175MHz
- **Low Noise Floor: -74.8dBFS**
- **3.3V Low-Power Operation**
  396mW (Single-Ended Clock Mode)
  429mW (Differential Clock Mode)
  300µW (Power-Down Mode)
- **Fully Differential or Single-Ended Analog Input**
- **Adjustable Full-Scale Analog Input Range**
  ±0.35V to ±1.10V
- **Common-Mode Reference**
- **CMOS-Compatible Outputs in Two's Complement or Gray Code**
- **Data-Valid Indicator Simplifies Digital Interface**
- **Data Out-of-Range Indicator**
- **Miniature, 6mm x 6mm x 0.8mm 40-Pin Thin QFN Package with Exposed Paddle**
- **Evaluation Kit Available (Order MAX12555EVKIT)**

Ordering Information

PART*	PIN-PACKAGE	PKG CODE
MAX12554ETL	40 Thin QFN	T4066-3
MAX12554ETL+	40 Thin QFN	T4066-3

+Denotes lead-free package.
**All devices specified over the -40°C to +85°C operating range.*

Pin-Compatible Versions

PART	SAMPLING RATE (Msps)	RESOLUTION (BITS)	TARGET APPLICATION
MAX12555	95	14	IF/Baseband
MAX12554	**80**	**14**	**IF/Baseband**
MAX12553	65	14	IF/Baseband
MAX19538	95	12	IF/Baseband
MAX1209	80	12	IF
MAX1211	65	12	IF
MAX1208	80	12	Baseband
MAX1207	65	12	Baseband
MAX1206	40	12	Baseband

Pin Configuration appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

14-Bit, 80Msps, 3.3V ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +3.6V
OV_{DD} to GND.....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
INP, INN to GND ...-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
REFIN, REFOUT, REFP, REFN, COM
to GND.....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
CLKP, CLKN, CLKTYP, G/$\overline{T}$, DCE,
PD to GND .....-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
D13–D0, DAV, DOR to GND.....-0.3V to (OV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN 6mm x 6mm x 0.8mm
(derated 26.3mW/°C above +70°C).....2105.3mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 2)						
Resolution			14			Bits
Integral Nonlinearity	INL	f_{IN} = 3MHz (Note 3)		±2.4	±4.9	LSB
Differential Nonlinearity	DNL	f_{IN} = 3MHz, no missing codes over temperature (Note 4)	-1	±0.5	+1.3	LSB
Offset Error		V_{REFIN} = 2.048V		±0.1	±0.72	%FS
Gain Error		V_{REFIN} = 2.048V		±0.5	±4.9	%FS
ANALOG INPUT (INP, INN)						
Differential Input Voltage Range	V_{DIFF}	Differential or single-ended inputs		±1.024		V
Common-Mode Input Voltage				V_{DD} / 2		V
Input Capacitance (Figure 3)	C_{PAR}	Fixed capacitance to ground		2		pF
	C_{SAMPLE}	Switched capacitance		4.5		
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		80			MHz
Minimum Clock Frequency					5	MHz
Data Latency		Figure 6		8.0		Clock cycles
DYNAMIC CHARACTERISTICS (Differential Inputs) (Note 2)						
Small-Signal Noise Floor	SSNF	Input at less than -35dBFS		-74.8		dBFS
Signal-to-Noise Ratio	SNR	f_{IN} = 3MHz at -0.5dBFS (Note 5)	69.0	72.4		dB
		f_{IN} = 40MHz at -0.5dBFS		72.0		
		f_{IN} = 70MHz at -0.5dBFS		71.9		
		f_{IN} = 175MHz at -0.5dBFS (Note 5)	68.0	70.9		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 3MHz at -0.5dBFS (Note 5)	68.9	72.1		dB
		f_{IN} = 40MHz at -0.5dBFS		71.7		
		f_{IN} = 70MHz at -0.5dBFS		71.6		
		f_{IN} = 175MHz at -0.5dBFS (Note 5)	66.2	70.3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, $G/\overline{T}$ = low, f_{CLK} = 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range	SFDR	f_{IN} = 3MHz at -0.5dBFS (Note 5)	76.5	86.2		dBc
		f_{IN} = 40MHz at -0.5dBFS		84.6		
		f_{IN} = 70MHz at -0.5dBFS		85.4		
		f_{IN} = 175MHz at -0.5dBFS (Note 5)	69.0	82.5		
Total Harmonic Distortion	THD	f_{IN} = 3MHz at -0.5dBFS		-84.8	-75.9	dBc
		f_{IN} = 40MHz at -0.5dBFS		-84.0		
		f_{IN} = 70MHz at -0.5dBFS		-82.6		
		f_{IN} = 175MHz at -0.5dBFS		-79.4	-69.0	
Second Harmonic	HD2	f_{IN} = 3MHz at -0.5dBFS		-91		dBc
		f_{IN} = 40MHz at -0.5dBFS		-91		
		f_{IN} = 70MHz at -0.5dBFS		-86		
		f_{IN} = 175MHz at -0.5dBFS		-85		
Third Harmonic	HD3	f_{IN} = 3MHz at -0.5dBFS		-89		dBc
		f_{IN} = 40MHz at -0.5dBFS		-85		
		f_{IN} = 70MHz at -0.5dBFS		-88		
		f_{IN} = 175MHz at -0.5dBFS		-85		
Intermodulation Distortion	IMD	f_{IN1} = 68.5MHz at -7dBFS f_{IN2} = 71.5MHz at -7dBFS		-83		dBc
		f_{IN1} = 172.5MHz at -7dBFS f_{IN2} = 177.5MHz at -7dBFS		-80		
Third-Order Intermodulation	IM3	f_{IN1} = 68.5MHz at -7dBFS f_{IN2} = 71.5MHz at -7dBFS		-87		dBc
		f_{IN1} = 172.5MHz at -7dBFS f_{IN2} = 177.5MHz at -7dBFS		-84		
Two-Tone Spurious-Free Dynamic Range	$SFDR_{TT}$	f_{IN1} = 68.5MHz at -7dBFS f_{IN2} = 71.5MHz at -7dBFS		84		dBc
		f_{IN1} = 172.5MHz at -7dBFS f_{IN2} = 177.5MHz at -7dBFS		80		
Aperture Delay	t_{AD}	Figure 4		1.2		ns
Aperture Jitter	t_{AJ}	Figure 4		<0.2		ps_{RMS}
Output Noise	n_{OUT}	INP = INN = COM		1.05		LSB_{RMS}
Overdrive Recovery Time		±10% beyond full scale		1		Clock cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, $G/\overline{T}$ = low, f_{CLK} = 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REFERENCE (REFIN = REFOUT; V_{REFP}, V_{REFN}, and V_{COM} are generated internally)						
REFOUT Output Voltage	V_{REFOUT}		1.979	2.048	2.068	V
COM Output Voltage	V_{COM}	V_{DD} / 2		1.65		V
Differential-Reference Output Voltage	V_{REF}	V_{REF} = V_{REFP} - V_{REFN} = V_{REFIN} x 3/4		1.536		V
REFOUT Load Regulation		-1.0mA < I_{REFOUT} < +0.1mA		35		mV/mA
REFOUT Temperature Coefficient	TC_{REF}			+50		ppm/°C
REFOUT Short-Circuit Current		Short to V_{DD}—sinking		0.24		mA
		Short to GND—sourcing		2.1		
BUFFERED EXTERNAL REFERENCE (REFIN driven externally; V_{REFIN} = 2.048V, V_{REFP}, V_{REFN}, and V_{COM} are generated internally)						
REFIN Input Voltage	V_{REFIN}			2.048		V
REFP Output Voltage	V_{REFP}	(V_{DD} / 2) + (V_{REFIN} x 3/8)		2.418		V
REFN Output Voltage	V_{REFN}	(V_{DD} / 2) - (V_{REFIN} x 3/8)		0.882		V
COM Output Voltage	V_{COM}	V_{DD} / 2	1.60	1.65	1.70	V
Differential-Reference Output Voltage	V_{REF}	V_{REF} = V_{REFP} - V_{REFN} = V_{REFIN} x 3/4	1.462		1.595	V
Differential-Reference Temperature Coefficient				±25		ppm/°C
REFIN Input Resistance				>50		MΩ
UNBUFFERED EXTERNAL REFERENCE (REFIN = GND; V_{REFP}, V_{REFN}, and V_{COM} are applied externally)						
COM Input Voltage	V_{COM}	V_{DD}/2		1.65		V
REFP Input Voltage		V_{REFP} - V_{COM}		0.768		V
REFN Input Voltage		V_{REFN} - V_{COM}		-0.768		V
Differential-Reference Input Voltage	V_{REF}	V_{REF} = V_{REFP} - V_{REFN} = V_{REFIN} x 3/4		1.536		V
REFP Sink Current	I_{REFP}	V_{REFP} = 2.418V		1.2		mA
REFN Source Current	I_{REFN}	V_{REFN} = 0.882V		0.85		mA
COM Sink Current	I_{COM}	V_{COM} = 1.650V		0.85		mA
REFP, REFN Capacitance				13		pF
COM Capacitance				6		pF
CLOCK INPUTS (CLKP, CLKN)						
Single-Ended Input High Threshold	V_{IH}	CLKTYP = GND, CLKN = GND	0.8 x V_{DD}			V
Single-Ended Input Low Threshold	V_{IL}	CLKTYP = GND, CLKN = GND			0.2 x V_{DD}	V
Minimum Differential Input Voltage Swing		CLKTYP = high		0.2		V_{P-P}

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Common-Mode Voltage		CLKTYP = high		V_{DD} / 2		V
Input Resistance	R_{CLK}	Figure 5		5		kΩ
Input Capacitance	C_{CLK}			2		pF
DIGITAL INPUTS (CLKTYP, G/$\overline{T}$, PD)						
Input High Threshold	V_{IH}		0.8 x OV_{DD}			V
Input Low Threshold	V_{IL}				0.2 x OV_{DD}	V
Input Leakage Current		V_{IH} = OV_{DD}			±5	µA
		V_{IL} = 0			±5	
Input Capacitance	C_{DIN}			5		pF
DIGITAL OUTPUTS (D13–D0, DAV, DOR)						
Output-Voltage Low	V_{OL}	D13–D0, DOR, I_{SINK} = 200µA			0.2	V
		DAV, I_{SINK} = 600µA			0.2	
Output-Voltage High	V_{OH}	D13–D0, DOR, I_{SOURCE} = 200µA	OV_{DD} - 0.2			V
		DAV, I_{SOURCE} = 600µA	OV_{DD} - 0.2			
Tri-State Leakage Current	I_{LEAK}	(Note 6)			±5	µA
D13–D0, DOR Tri-State Output Capacitance	C_{OUT}	(Note 6)		3		pF
DAV Tri-State Output Capacitance	C_{DAV}	(Note 6)		6		pF
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		3.15	3.3	3.60	V
Digital Output Supply Voltage	OV_{DD}		1.7	1.8	V_{DD} + 0.3V	V
Analog Supply Current	I_{VDD}	Normal operating mode, f_{IN} = 175MHz at -0.5dBFS, CLKTYP = GND, single-ended clock		120		mA
		Normal operating mode, f_{IN} = 175MHz at -0.5dBFS, CLKTYP = OV_{DD}, differential clock		130	145	
		Power-down mode clock idle, PD = OV_{DD}		0.1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} = 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

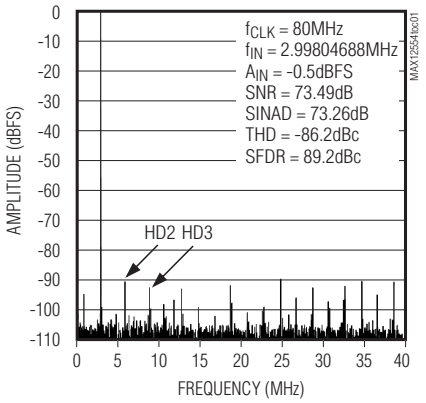
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Power Dissipation	P_{DISS}	Normal operating mode, f_{IN} = 175MHz at -0.5dBFS, CLKTYP = GND, single-ended clock		396		mW
		Normal operating mode, f_{IN} = 175MHz at -0.5dBFS, CLKTYP = OV_{DD}, differential clock		429	479	
		Power-down mode clock idle, PD = OV_{DD}		0.3		
Digital Output Supply Current	I_{OVDD}	Normal operating mode, f_{IN} = 175MHz at -0.5dBFS, OV_{DD} = 1.8V, $C_L \approx$ 5pF		8.6		mA
		Power-down mode clock idle, PD = OV_{DD}		8		µA
TIMING CHARACTERISTICS (Figure 6)						
Clock Pulse-Width High	t_{CH}			6.2		ns
Clock Pulse-Width Low	t_{CL}			6.2		ns
Data-Valid Delay	t_{DAV}	C_L = 5pF (Note 7)		5.2		ns
Data Setup Time Before Rising Edge of DAV	t_{SETUP}	C_L = 5pF (Note 3, Note 7)	5.5			ns
Data Hold Time After Rising Edge of DAV	t_{HOLD}	C_L = 5pF (Note 3, Note 7)	5.5			ns
Wake-Up Time from Power-Down	t_{WAKE}	V_{REFIN} = 2.048V		10		ms

Note 1: Specifications ≥+25°C guaranteed by production test; <+25°C guaranteed by design and characterization.
Note 2: See definitions in the *Parameter Definitions* section at the end of this data sheet.
Note 3: Guaranteed by design and characterization.
Note 4: Specifications guaranteed by design and characterization. Devices tested to ensure no missing codes during production test.
Note 5: Due to test-equipment-jitter limitations at 175MHz, 0.15% of the spectrum on each side of the fundamental is excluded from the spectral analysis.
Note 6: During power-down, D13–D0, DOR, and DAV are high impedance.
Note 7: Digital outputs settle to V_{IH} or V_{IL}.

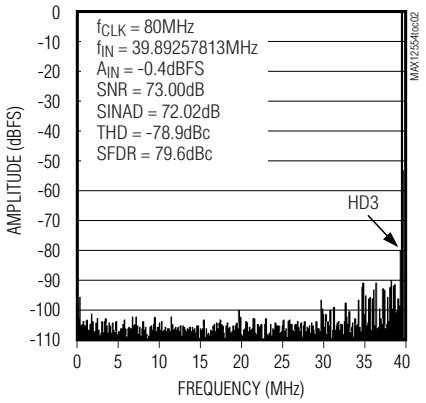
Typical Operating Characteristics

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} ≈ 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = +25°C, unless otherwise noted.)

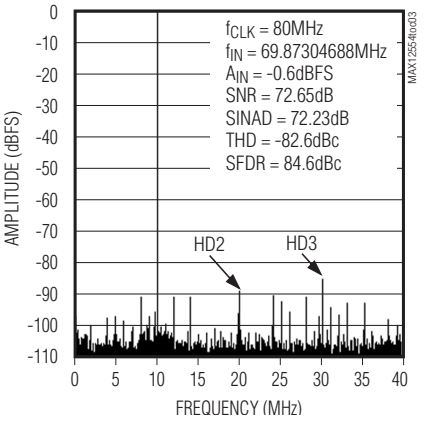
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



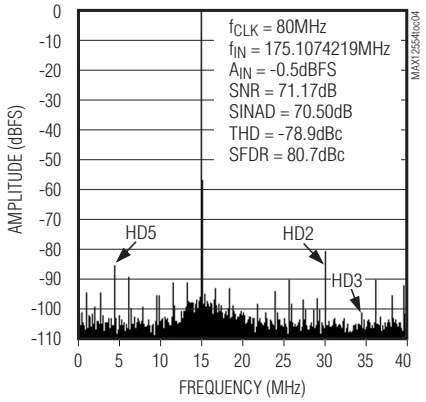
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



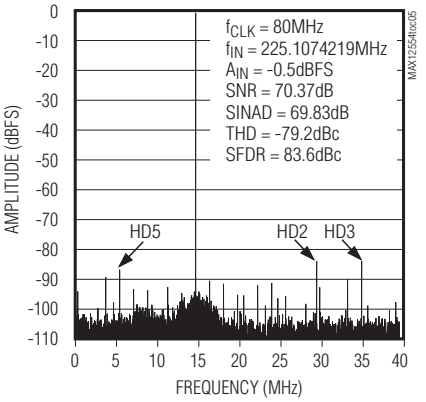
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



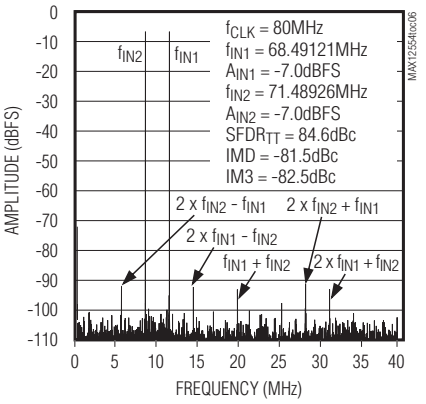
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



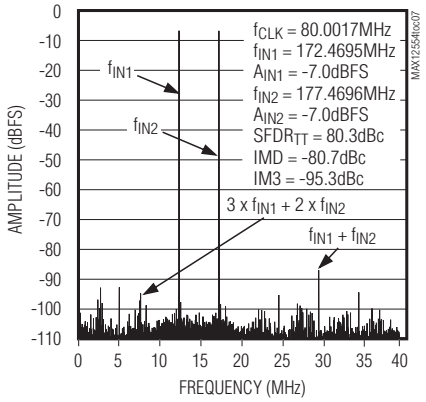
SINGLE-TONE FFT PLOT (8192-POINT DATA RECORD)



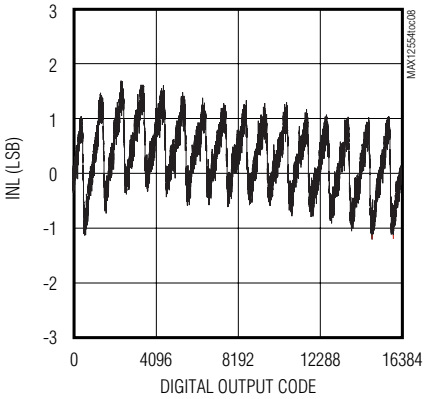
TWO-TONE FFT PLOT (16,384-POINT DATA RECORD)



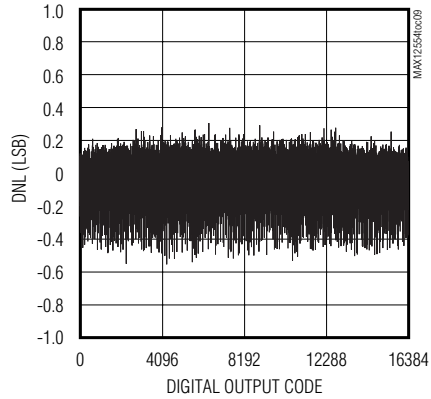
TWO-TONE FFT PLOT (16,384-POINT DATA RECORD)



INTEGRAL NONLINEARITY



DIFFERENTIAL NONLINEARITY

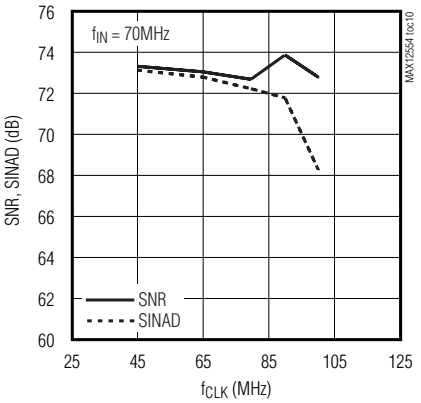


14-Bit, 80Msps, 3.3V ADC

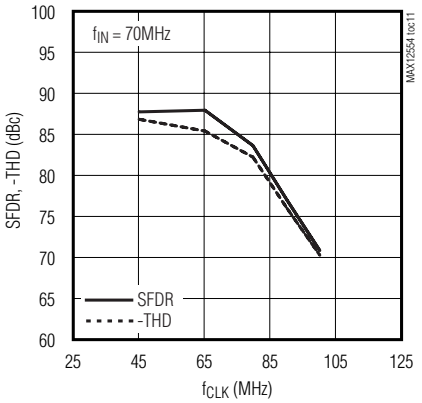
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} ≈ 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = +25°C, unless otherwise noted.)

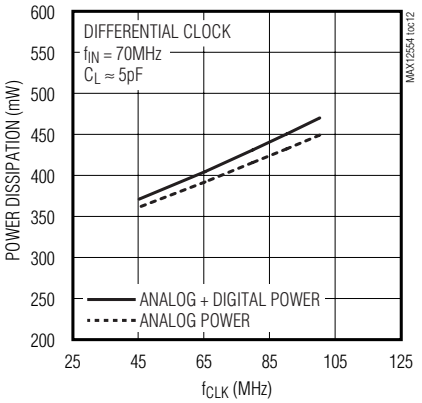
SNR, SINAD vs. SAMPLING RATE



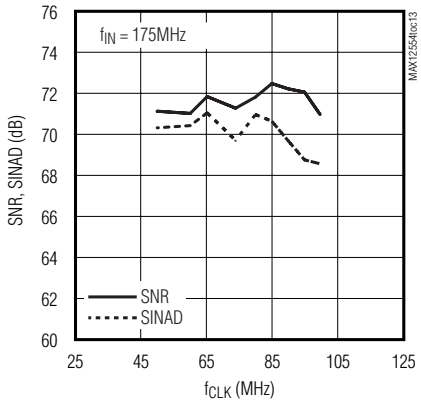
SFDR, -THD vs. SAMPLING RATE



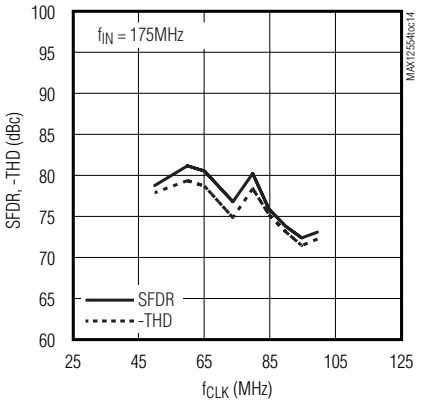
POWER DISSIPATION vs. SAMPLING RATE



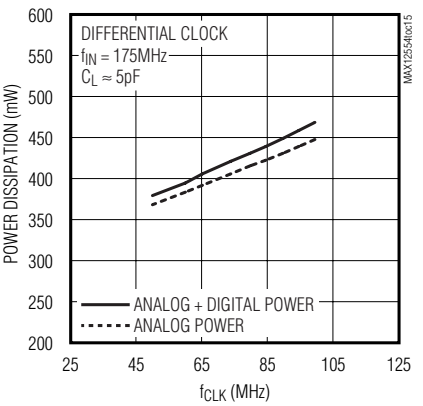
SNR, SINAD vs. SAMPLING RATE



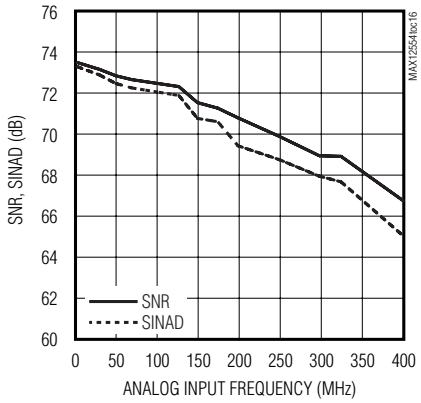
SFDR, -THD vs. SAMPLING RATE



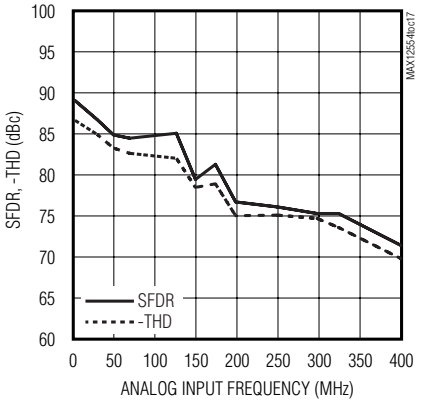
POWER DISSIPATION vs. SAMPLING RATE



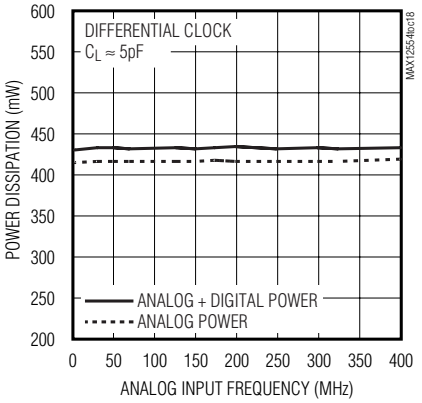
SNR, SINAD vs. ANALOG INPUT FREQUENCY



SFDR, -THD vs. ANALOG INPUT FREQUENCY



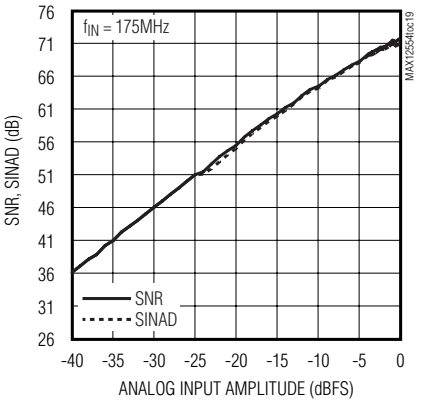
POWER DISSIPATION vs. ANALOG INPUT FREQUENCY



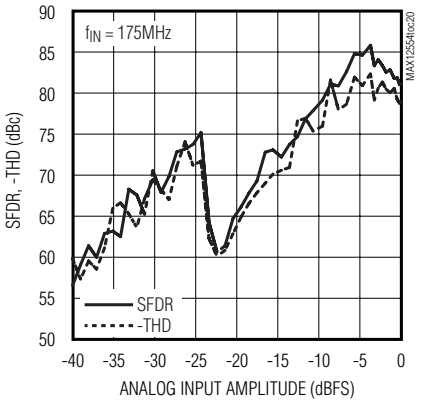
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} ≈ 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = +25°C, unless otherwise noted.)

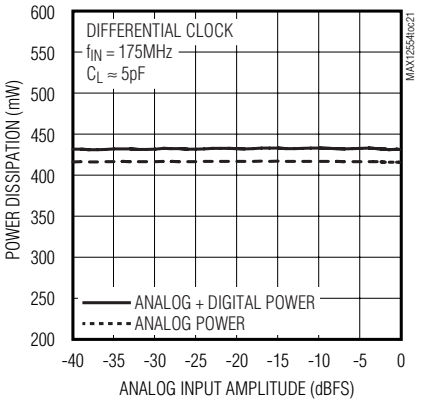
SNR, SINAD vs. ANALOG INPUT AMPLITUDE



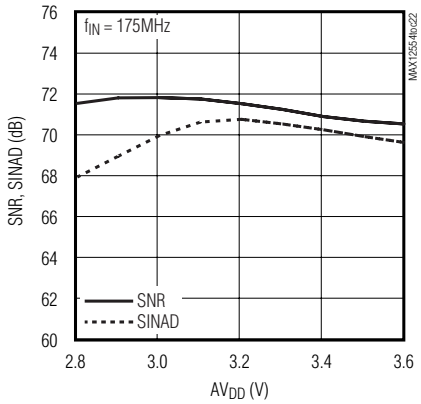
SFDR, -THD vs. ANALOG INPUT AMPLITUDE



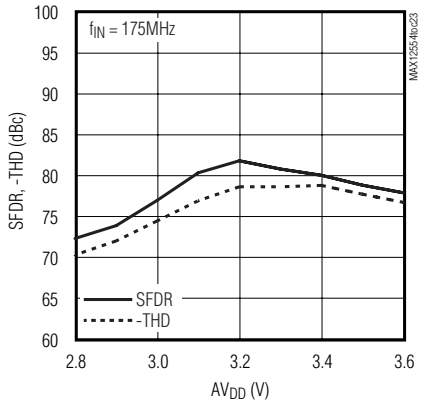
POWER DISSIPATION vs. ANALOG INPUT AMPLITUDE



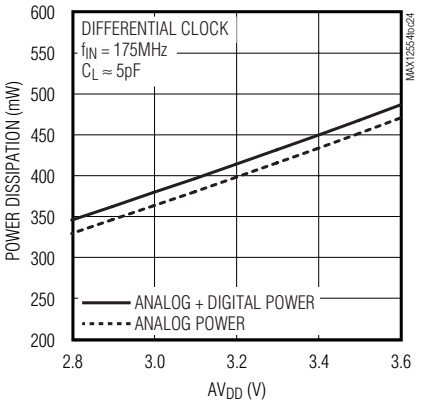
SNR, SINAD vs. ANALOG SUPPLY VOLTAGE



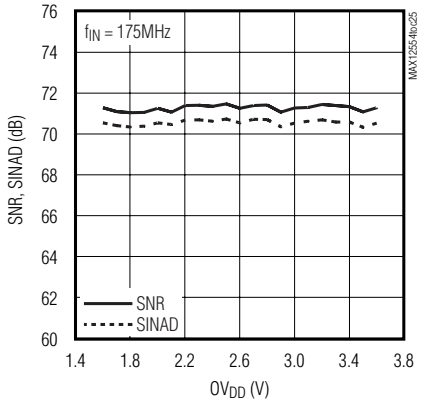
SFDR, -THD vs. ANALOG SUPPLY VOLTAGE



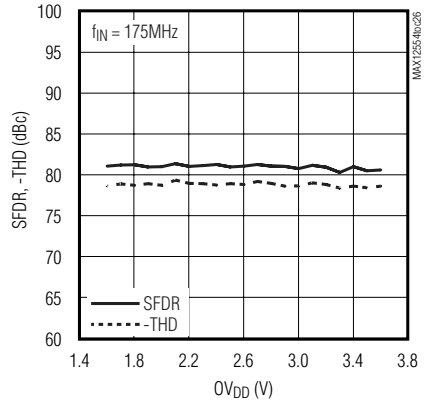
POWER DISSIPATION vs. ANALOG SUPPLY VOLTAGE



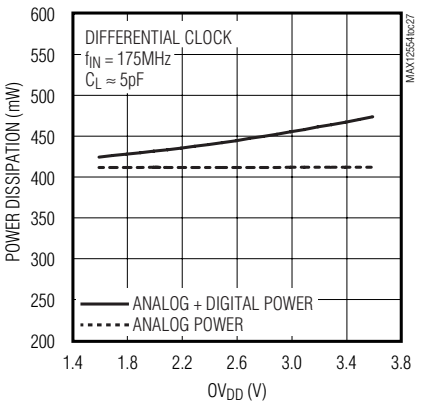
SNR, SINAD vs. DIGITAL SUPPLY VOLTAGE



SFDR, -THD vs. DIGITAL SUPPLY VOLTAGE



POWER DISSIPATION vs. DIGITAL SUPPLY VOLTAGE

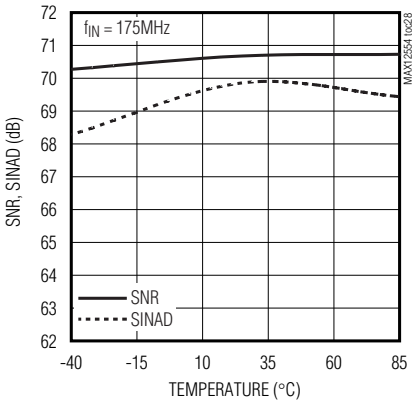


14-Bit, 80Msps, 3.3V ADC

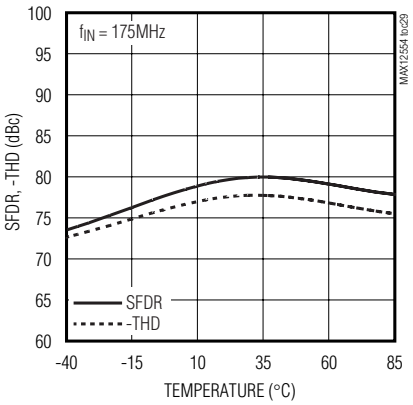
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} ≈ 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = +25°C, unless otherwise noted.)

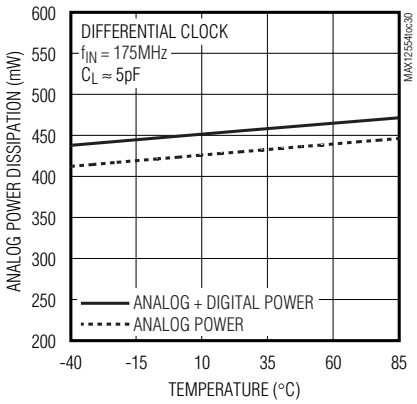
SNR, SINAD vs. TEMPERATURE



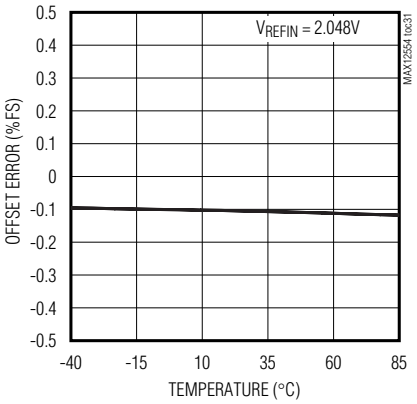
SFDR, -THD vs. TEMPERATURE



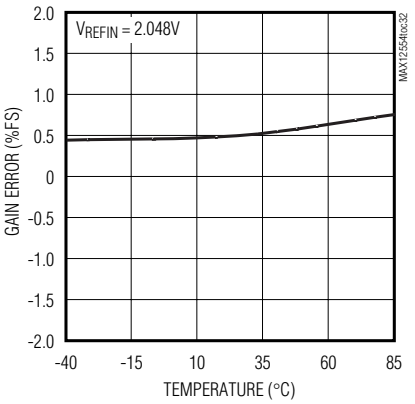
POWER DISSIPATION vs. TEMPERATURE



OFFSET ERROR vs. TEMPERATURE



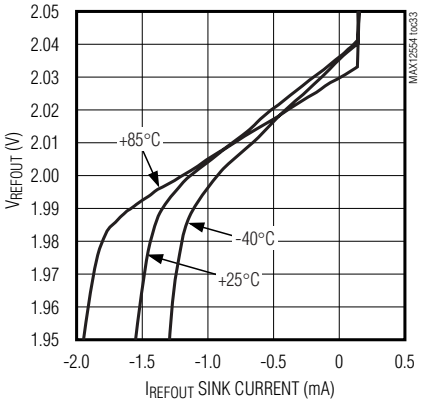
GAIN ERROR vs. TEMPERATURE



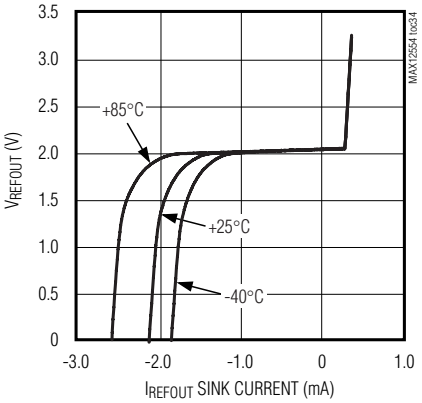
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, OV_{DD} = 1.8V, GND = 0, REFIN = REFOUT (internal reference), V_{IN} = -0.5dBFS, CLKTYP = high, DCE = high, PD = low, G/$\overline{T}$ = low, f_{CLK} ≈ 80MHz (50% duty cycle, 1.4V_{P-P} square wave), T_A = +25°C, unless otherwise noted.)

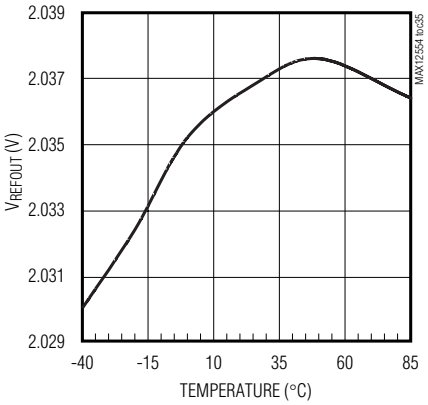
REFERENCE OUTPUT VOLTAGE LOAD REGULATION



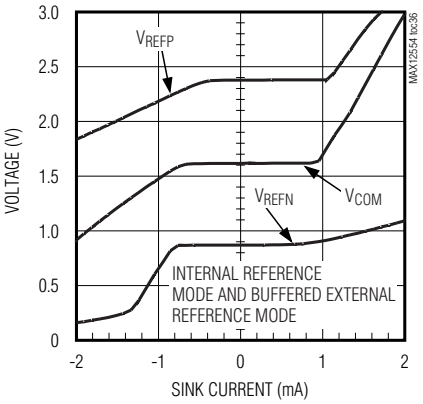
REFERENCE OUTPUT VOLTAGE SHORT-CIRCUIT PERFORMANCE



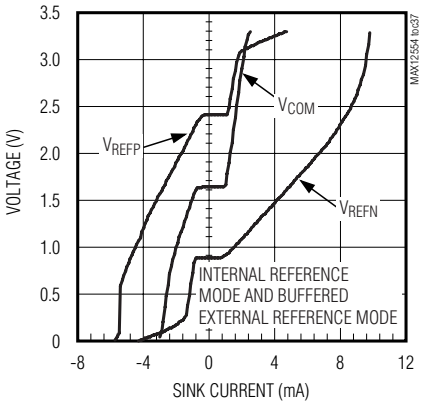
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



REFP, COM, REFN LOAD REGULATION



REFP, COM, REFN SHORT-CIRCUIT PERFORMACE



Pin Description

PIN	NAME	FUNCTION
1	REFP	Positive Reference I/O. The full-scale analog input range is ±(V_{REFP} - V_{REFN}) x 2/3. Bypass REFP to GND with a 0.1µF capacitor. Connect a 1µF capacitor in parallel with a 10µF capacitor between REFP and REFN. **Place the 1µF REFP to REFN capacitor as close to the device as possible on the same side of the PC board.**
2	REFN	Negative Reference I/O. The full-scale analog input range is ±(V_{REFP} - V_{REFN}) x 2/3. Bypass REFN to GND with a 0.1µF capacitor. Connect a 1µF capacitor in parallel with a 10µF capacitor between REFP and REFN. **Place the 1µF REFP to REFN capacitor as close to the device as possible on the same side of the PC board.**
3	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 2.2µF capacitor. **Place the 2.2µF COM to GND capacitor as close to the device as possible**. This 2.2µF capacitor can be placed on the opposite side of the PC board and connected to the MAX12554 through a via.
4, 7, 16, 35	GND	Ground. Connect all ground pins and EP together.
5	INP	Positive Analog Input
6	INN	Negative Analog Input
8	DCE	Duty-Cycle Equalizer Input. Connect DCE low (GND) to disable the internal duty-cycle equalizer. Connect DCE high (OV_{DD} or V_{DD}) to enable the internal duty-cycle equalizer.
9	CLKN	Negative Clock Input. In differential clock input mode (CLKTYP = OV_{DD} or V_{DD}), connect the differential clock signal between CLKP and CLKN. In single-ended clock mode (CLKTYP = GND), apply the single-ended clock signal to CLKP and connect CLKN to GND.
10	CLKP	Positive Clock Input. In differential clock input mode (CLKTYP = OV_{DD} or V_{DD}), connect the differential clock signal between CLKP and CLKN. In single-ended clock mode (CLKTYP = GND), apply the single-ended clock signal to CLKP and connect CLKN to GND.
11	CLKTYP	Clock-Type Definition Input. Connect CLKTYP to GND to define the single-ended clock input. Connect CLKTYP to OV_{DD} or V_{DD} to define the differential clock input.
12–15, 36	V_{DD}	Analog Power Input. Connect V_{DD} to a 3.15V to 3.60V power supply. Bypass V_{DD} to GND with a parallel capacitor combination of ≥2.2µF and 0.1µF. Connect all V_{DD} pins to the same potential.
17, 34	OV_{DD}	Output-Driver Power Input. Connect OV_{DD} to a 1.7V to V_{DD} power supply. Bypass OV_{DD} to GND with a parallel capacitor combination of ≥2.2µF and 0.1µF.
18	DOR	Data Out-of-Range Indicator. The DOR digital output indicates when the analog input voltage is out of range. When DOR is high, the analog input is beyond its full-scale range. When DOR is low, the analog input is within its full-scale range (Figure 6).
19	D13	CMOS Digital Output Bit 13 (MSB)
20	D12	CMOS Digital Output Bit 12
21	D11	CMOS Digital Output Bit 11
22	D10	CMOS Digital Output Bit 10
23	D9	CMOS Digital Output Bit 9
24	D8	CMOS Digital Output Bit 8
25	D7	CMOS Digital Output Bit 7
26	D6	CMOS Digital Output Bit 6
27	D5	CMOS Digital Output Bit 5

Pin Description (continued)

PIN	NAME	FUNCTION
28	D4	CMOS Digital Output Bit 4
29	D3	CMOS Digital Output Bit 3
30	D2	CMOS Digital Output Bit 2
31	D1	CMOS Digital Output Bit 1
32	D0	CMOS Digital Output Bit 0 (LSB)
33	DAV	Data-Valid Output. DAV is a single-ended version of the input clock that is compensated to correct for any input clock duty-cycle variations. DAV is typically used to latch the MAX12554 output data into an external back-end digital circuit.
37	PD	Power-Down Input. Force PD high for power-down mode. Force PD low for normal operation.
38	REFOUT	Internal Reference Voltage Output. For internal reference operation, connect REFOUT directly to REFIN or use a resistive divider from REFOUT to set the voltage at REFIN. Bypass REFOUT to GND with a ≥0.1µF capacitor.
39	REFIN	Reference Input. In internal reference mode and buffered external reference mode, bypass REFIN to GND with a ≥0.1µF capacitor. In these modes, V_{REFP} - V_{REFN} = V_{REFIN} x 3/4. For unbuffered external reference mode operation, connect REFIN to GND.
40	$G/\overline{T}$	Output-Format-Select Input. Connect $G/\overline{T}$ to GND for the two's-complement digital output format. Connect $G/\overline{T}$ to OV_{DD} or V_{DD} for the Gray code digital output format.
—	EP	Exposed Paddle. The MAX12554 relies on the exposed paddle connection for a low-inductance ground connection. Connect EP to GND to achieve specified performance. Use multiple vias to connect the top-side PC board ground plane to the bottom-side PC board ground plane.

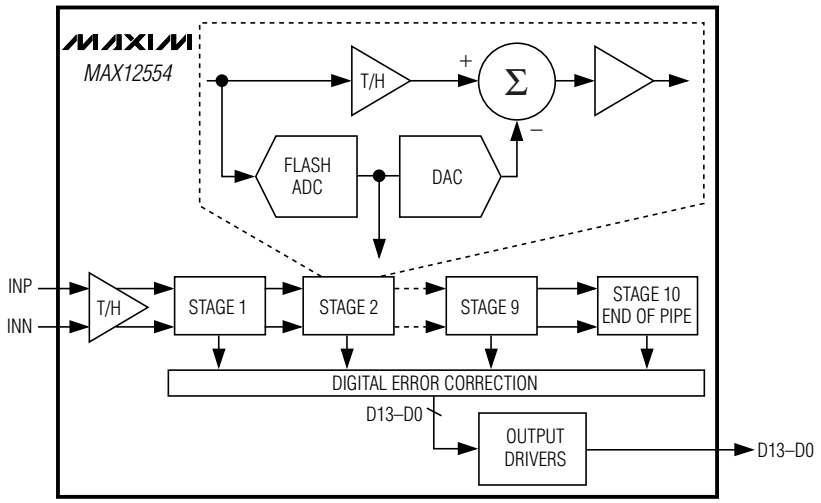


Figure 1. Pipeline Architecture—Stage Blocks

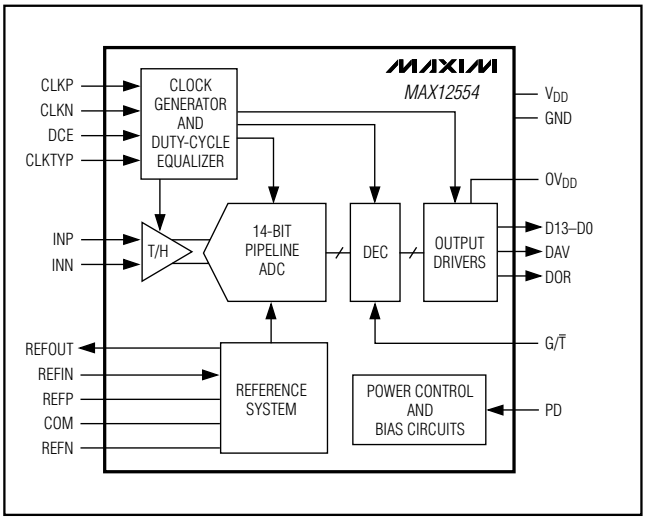


Figure 2. Simplified Functional Diagram

Detailed Description

The MAX12554 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. From input to output, the total clock-cycle latency is 8.0 clock cycles.

Each pipeline converter stage converts its input voltage into a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed along to the next pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. Figure 2 shows the MAX12554 functional diagram.

Input Track-and-Hold (T/H) Circuit

Figure 3 displays a simplified functional diagram of the input T/H circuit. This input T/H circuit allows for high analog input frequencies of 175MHz and beyond and supports a common-mode input voltage of V_{DD} / 2 ±0.5V.

The MAX12554 sampling clock controls the ADC's switched-capacitor T/H architecture (Figure 3) allowing the analog input signal to be stored as a charge on the sampling capacitors. These switches are closed (track) when the sampling clock is high and open (hold) when the sampling clock is low (Figure 4). The analog input signal source must be capable of providing the dynamic current necessary to charge and discharge the sampling capacitors. To avoid signal degradation, these

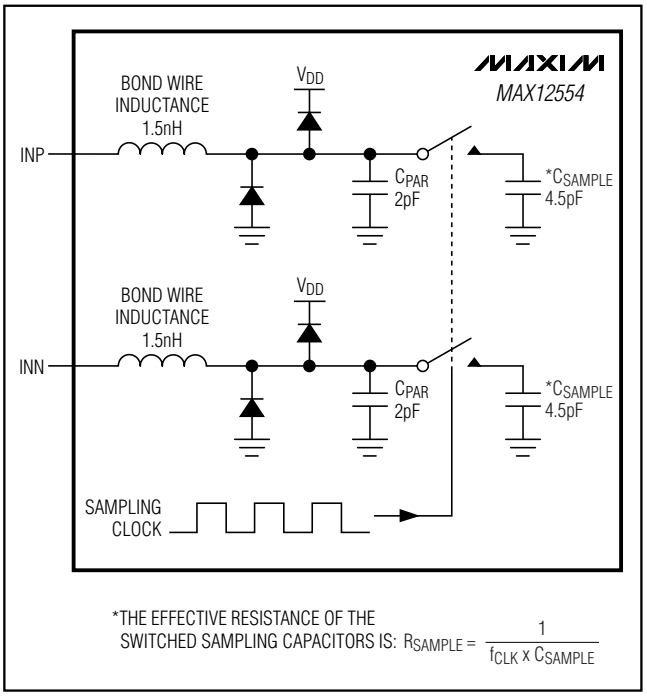


Figure 3. Simplified Input T/H Circuit

capacitors must be charged to one-half LSB accuracy within one-half of a clock cycle.

The analog input of the MAX12554 supports differential or single-ended input drive. For optimum performance with differential inputs, balance the input impedance of INP and INN and set the common-mode voltage to mid-supply (V_{DD} / 2). The MAX12554 provides the optimum common-mode voltage of V_{DD} / 2 through the COM output when operating in internal reference mode and buffered external reference mode. This COM output voltage can be used to bias the input network as shown in Figures 10, 11, and 12.

Reference Output (REFOUT)

An internal bandgap reference is the basis for all the internal voltages and bias currents used in the MAX12554. The power-down logic input (PD) enables and disables the reference circuit. The reference circuit requires 10ms to power up and settle when power is applied to the MAX12554 or when PD transitions from high to low. REFOUT has approximately 17kΩ to GND when the MAX12554 is in power-down.

The internal bandgap reference and its buffer generate V_{REFOUT} to be 2.048V. The reference temperature coefficient is typically +50ppm/°C. Connect an external ≥0.1µF bypass capacitor from REFOUT to GND for stability.

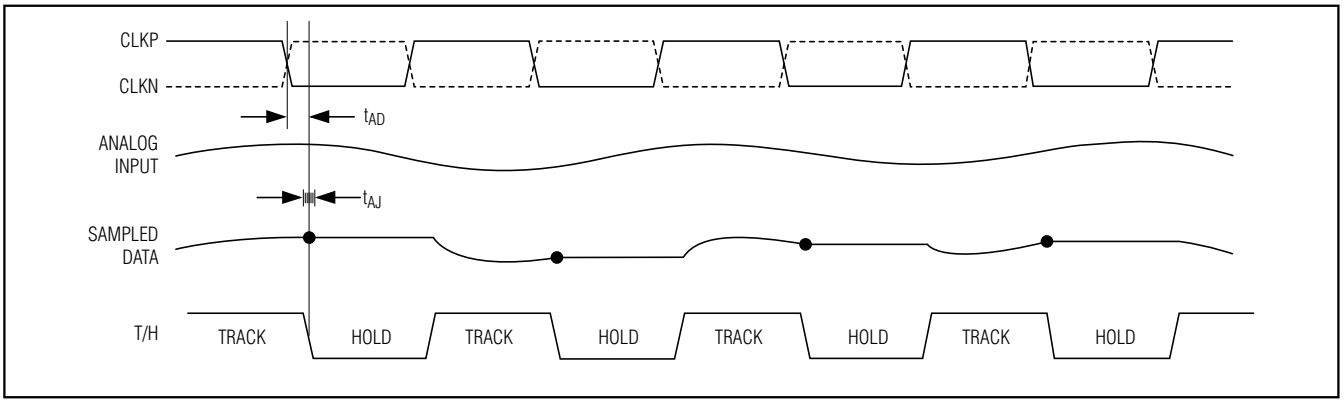


Figure 4. T/H Aperture Timing

REFOUT sources up to 1.0mA and sinks up to 0.1mA for external circuits with a load regulation of 35mV/mA. Short-circuit protection limits I_{REFOUT} to a 2.1mA source current when shorted to GND and a 0.24mA sink current when shorted to V_{DD}.

Analog Inputs and Reference Configurations

The MAX12554 full-scale analog input range is adjustable from ±0.35V to ±1.10V with a V_{DD} / 2 ±0.5V common-mode input range. The MAX12554 provides three modes of reference operation. The voltage at REFIN (V_{REFIN}) sets the reference operation mode (Table 1).

To operate the MAX12554 with the internal reference, connect REFOUT to REFIN either with a direct short or through a resistive divider. In this mode, COM, REFP, and REFN are low-impedance outputs with V_{COM} = V_{DD} / 2, V_{REFP} = V_{DD} / 2 + V_{REFIN} x 3/8, and V_{REFN} = V_{DD} / 2 - V_{REFIN} x 3/8. The REFIN input impedance is very large (>50MΩ). When driving REFIN through a resistive divider, use resistances ≥10kΩ to avoid loading REFOUT.

Buffered external reference mode is virtually identical to internal reference mode except that the reference source is derived from an external reference and not the MAX12554 REFOUT. In buffered external reference mode, apply a stable 0.7V to 2.2V source at REFIN. In this mode, COM, REFP, and REFN are low-impedance outputs with V_{COM} = V_{DD} / 2, V_{REFP} = V_{DD} / 2 + V_{REFIN} x 3/8, and V_{REFN} = V_{DD} / 2 - V_{REFIN} x 3/8.

To operate the MAX12554 in unbuffered external reference mode, connect REFIN to GND. Connecting REFIN to GND deactivates the on-chip reference buffers for COM, REFP, and REFN. With the respective buffers deactivated, COM, REFP, and REFN become high-impedance inputs and must be driven through separate, external reference sources. Drive V_{COM} to V_{DD} / 2 ±5%, and drive REFP and REFN so V_{COM} = (V_{REFP} + V_{REFN}) / 2. The full-scale analog input range is ±(V_{REFP} - V_{REFN}) x 2/3.

Table 1. Reference Modes

V_{REFIN}	REFERENCE MODE
35% V_{REFOUT} to 100% V_{REFOUT}	**Internal Reference Mode.** Drive REFIN with REFOUT either through a direct short or a resistive divider. The full-scale analog input range is ±V_{REFIN} / 2: V_{COM} = V_{DD} / 2 V_{REFP} = V_{DD} / 2 + V_{REFIN} x 3/8 V_{REFN} = V_{DD} / 2 - V_{REFIN} x 3/8
0.7V to 2.2V	**Buffered External Reference Mode.** Apply an external 0.7V to 2.2V reference voltage to REFIN. The full-scale analog input range is ±V_{REFIN} / 2: V_{COM} = V_{DD} / 2 V_{REFP} = V_{DD} / 2 + V_{REFIN} x 3/8 V_{REFN} = V_{DD} / 2 - V_{REFIN} x 3/8
<0.4V	**Unbuffered External Reference Mode.** Drive REFP, REFN, and COM with external reference sources. The full-scale analog input range is ±(V_{REFP} - V_{REFN}) x 2/3.

All three modes of reference operation require the same bypass capacitor combinations. Bypass COM with a 2.2µF capacitor to GND. Bypass REFP and REFN each with a 0.1µF capacitor to GND. Bypass REFP to REFN with a 1µF capacitor in parallel with a 10µF capacitor. **Place the 1µF capacitor as close to the device as possible on the same side of the PC board.** Bypass REFIN and REFOUT to GND with a 0.1µF capacitor.

For detailed circuit suggestions, see Figure 13 and Figure 14.

Clock Input and Clock Control Lines (CLKP, CLKN, CLKTYP)

The MAX12554 accepts both differential and single-ended clock inputs. For single-ended clock input operation, connect CLKTYP to GND, CLKN to GND, and drive CLKP with the external single-ended clock signal. For differential clock input operation, connect CLKTYP to OV_{DD} or V_{DD}, and drive CLKP and CLKN with the external differential clock signal. To reduce clock jitter, the external single-ended clock must have sharp falling edges. Consider the clock input as an analog input and route it away from any other analog inputs and digital signal lines.

CLKP and CLKN are high impedance when the MAX12554 is powered down (Figure 5).

Low clock jitter is required for the specified SNR performance of the MAX12554. Analog input sampling occurs on the falling edge of the clock signal, requiring this edge to have the lowest possible jitter. Jitter limits the maximum SNR performance of any ADC according to the following relationship:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \, f_{IN} \times t_J}\right)$$

where f_{IN} represents the analog input frequency and t_J is the total system clock jitter. Clock jitter is especially critical for undersampling applications. For example, assuming that clock jitter is the only noise source, to obtain the specified 70.9dB of SNR with a 175MHz input frequency, the system must have less than 0.26ps of clock jitter. In actuality, there are other noise sources such as thermal noise and quantization noise that contribute to the system noise, requiring the clock jitter to be less than 0.14ps to obtain the specified 70.9dB of SNR at 175MHz.

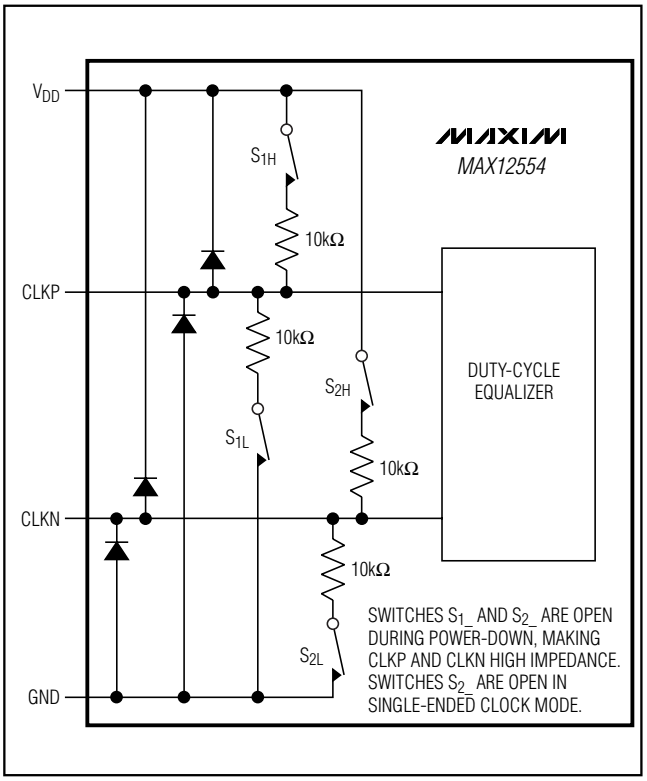


Figure 5. Simplified Clock Input Circuit

Clock Duty-Cycle Equalizer (DCE)

Connect DCE high to enable the clock duty-cycle equalizer (DCE = OV_{DD} or V_{DD}). Connect DCE low to disable the clock duty-cycle equalizer (DCE = GND). With the clock duty-cycle equalizer enabled, the MAX12554 is insensitive to the duty cycle of the signal applied to CLKP and CLKN. Duty cycles from 35% to 65% are acceptable with the clock duty-cycle equalizer enabled.

The clock duty-cycle equalizer uses a delay-locked loop (DLL) to create internal timing signals that are duty-cycle independent. Due to this DLL, the MAX12554 requires approximately 100 clock cycles to acquire and lock to new clock frequencies.

Although not recommended, disabling the clock duty-cycle equalizer reduces the analog supply current by 1.5mA. With the clock duty-cycle equalizer disabled, the MAX12554's dynamic performance varies depending on the duty cycle of the signal applied to CLKP and CLKN.

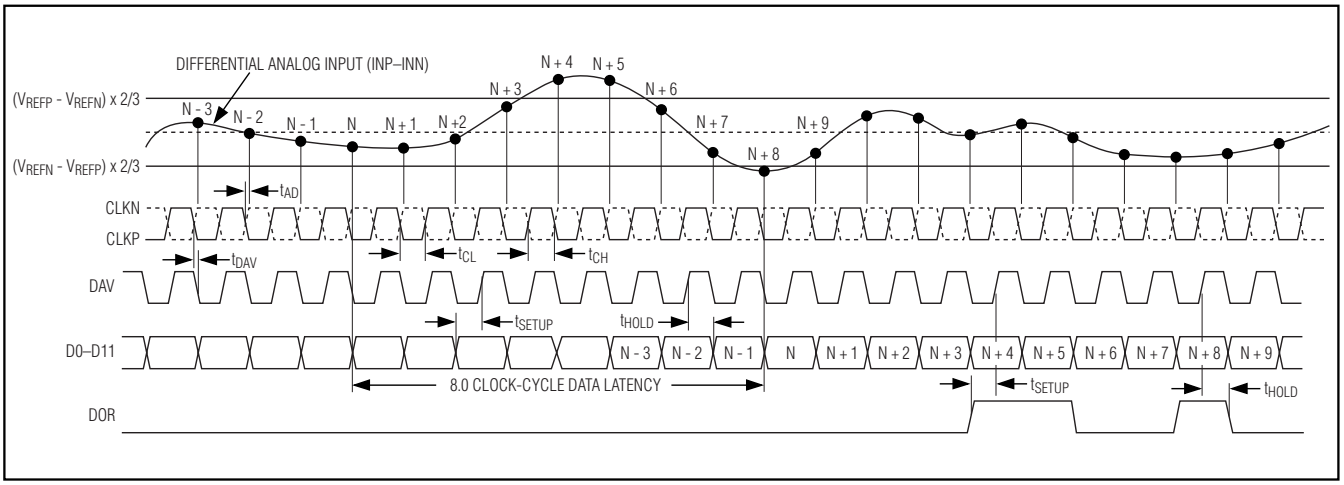


Figure 6. System Timing Diagram

System-Timing Requirements

Figure 6 shows the relationship between the clock, analog inputs, DAV indicator, DOR indicator, and the resulting output data. The analog input is sampled on the falling edge of the clock signal and the resulting data appears at the digital outputs 8.0 clock cycles later.

The DAV indicator is synchronized with the digital output and optimized for use in latching data into digital back-end circuitry. Alternatively, digital back-end circuitry can be latched with the rising edge of the conversion clock (CLKP-CLKN).

Data-Valid Output (DAV)

DAV is a single-ended version of the input clock (CLKP) with a delay (t_{DAV}). Output data changes on the falling edge of DAV, and DAV rises once output data is valid (Figure 6).

The state of the duty-cycle equalizer input (DCE) changes the waveform at DAV. With the duty-cycle equalizer disabled (DCE = low), the DAV signal is a single-ended version of CLKP delayed by 5.2ns (t_{DAV}). With the duty-cycle equalizer enabled (DCE = high), the DAV signal has a fixed pulse width that is independent of CLKP. In either case, with DCE high or low, output data at D13–D0 and DOR are valid from 5.5ns before the rising edge of DAV to 5.5ns after the rising edge of DAV, and the rising edge of DAV is synchronized to have a 5.2ns (t_{DAV}) delay from the falling edge of CLKP.

DAV is high impedance when the MAX12554 is in power-down (PD = high). DAV is capable of sinking and sourcing 600µA and has three times the drive strength of D13–D0 and DOR. DAV is typically used to latch the MAX12554 output data into an external back-end digital circuit.

Keep the capacitive load on DAV as low as possible (<25pF) to avoid large digital currents feeding back into the analog portion of the MAX12554 and degrading its dynamic performance. An external buffer on DAV isolates it from heavy capacitive loads. Refer to the MAX12555 evaluation kit schematic for an example of DAV driving back-end digital circuitry through an external buffer.

Data Out-of-Range Indicator (DOR)

The DOR digital output indicates when the analog input voltage is out of range. When DOR is high, the analog input is out of range. When DOR is low, the analog input is within range. The valid differential input range is from (V_{REFP} - V_{REFN}) x 3/4 to (V_{REFN} - V_{REFP}) x 3/4. Signals outside this valid differential range cause DOR to assert high as shown in Table 2 and Figure 6.

DOR is synchronized with DAV and transitions along with the output data D13–D0. There is an 8.0 clock-cycle latency in the DOR function as is with the output data (Figure 6).

DOR is high impedance when the MAX12554 is in power-down (PD = high). DOR enters a high-impedance state within 10ns after the rising edge of PD and becomes active 10ns after PD's falling edge.

Digital Output Data (D13–D0), Output Format (G/$\overline{T}$)

The MAX12554 provides a 14-bit, parallel, tri-state output bus. D13–D0 and DOR update on the falling edge of DAV and are valid on the rising edge of DAV.

The MAX12554 output data format is either Gray code or two's complement, depending on the logic input G/$\overline{T}$. With G/$\overline{T}$ high, the output data format is Gray code. With G/$\overline{T}$ low, the output data format is two's complement. See Figure 9 for a binary-to-Gray and Gray-to-binary code-conversion example.

The following equations, Table 2, Figure 7, and Figure 8 define the relationship between the digital output and the analog input:

$$V_{INP} - V_{INN} = (V_{REFP} - V_{REFN}) \times \frac{4}{3} \times \frac{CODE_{10} - 8192}{16384}$$

for Gray code (G/$\overline{T}$ = 1).

$$V_{INP} - V_{INN} = (V_{REFP} - V_{REFN}) \times \frac{4}{3} \times \frac{CODE_{10}}{16384}$$

for two's complement (G/$\overline{T}$ = 0).

where $CODE_{10}$ is the decimal equivalent of the digital output code as shown in Table 2.

Digital outputs D13–D0 are high impedance when the MAX12554 is in power-down (PD = high). D13–D0 transition high 10ns after the rising edge of PD and become active 10ns after PD's falling edge.

Keep the capacitive load on the MAX12554 digital outputs D13–D0 as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX12554 and degrading its dynamic performance. The addition of external digital buffers on the digital outputs isolates the MAX12554 from heavy capacitive loading. To improve the dynamic performance of the MAX12554, add 220Ω resistors in series with the digital outputs close to the MAX12554. Refer to the MAX12555 evaluation kit schematic for an example of the digital outputs driving a digital buffer through 220Ω series resistors.

Power-Down Input (PD)

The MAX12554 has two power modes that are controlled with the power-down digital input (PD). With PD low, the MAX12554 is in normal operating mode. With PD high, the MAX12554 is in power-down mode.

The power-down mode allows the MAX12554 to efficiently use power by transitioning to a low-power state when conversions are not required. Additionally, the MAX12554 parallel output bus is high impedance in power-down mode, allowing other devices on the bus to be accessed.

Table 2. Output Codes vs. Input Voltage

GRAY-CODE OUTPUT CODE ($G/\overline{T}$ = 1)				TWO'S-COMPLEMENT OUTPUT CODE ($G/\overline{T}$ = 0)				$V_{INP} - V_{INN}$ (V_{REFP} = 2.418V, V_{REFN} = 0.882V)
BINARY D13 → D0	DOR	HEXADECIMAL EQUIVALENT OF D13 → D0	DECIMAL EQUIVALENT OF D13 → D0 ($CODE_{10}$)	BINARY D13 → D0	DOR	HEXADECIMAL EQUIVALENT OF D13→ D0	DECIMAL EQUIVALENT OF D13 → D0 ($CODE_{10}$)	
10 0000 0000 0000	**1**	0x2000	+16383	01 1111 1111 1111	**1**	0x1FFF	+8191	>+1.023875V (DATA OUT OF RANGE)
10 0000 0000 0000	0	0x2000	+16383	01 1111 1111 1111	0	0x1FFF	+8191	+1.023875V
10 0000 0000 0001	0	0x2001	+16382	01 1111 1111 1110	0	0x1FFE	+8190	+1.023750V
11 0000 0000 0011	0	0x3003	+8194	00 0000 0000 0010	0	0x0002	+2	+0.000250V
11 0000 0000 0001	0	0x3001	+8193	00 0000 0000 0001	0	0x0001	+1	+0.000125V
11 0000 0000 0000	0	0x3000	+8192	00 0000 0000 0000	0	0x0000	0	+0.000000V
01 0000 0000 0000	0	0x1000	+8191	11 1111 1111 1111	0	0x3FFF	-1	-0.000125V
01 0000 0000 0001	0	0x1001	+8190	11 1111 1111 1110	0	0x3FFE	-2	-0.000250V
00 0000 0000 0001	0	0x0001	+1	10 0000 0000 0001	0	0x2001	-8191	-1.023875V
00 0000 0000 0000	0	0x0000	0	10 0000 0000 0000	0	0x2000	-8192	-1.024000V
00 0000 0000 0000	**1**	0x0000	0	10 0000 0000 0000	**1**	0x2000	-8192	<-1.024000V (DATA OUT OF RANGE)

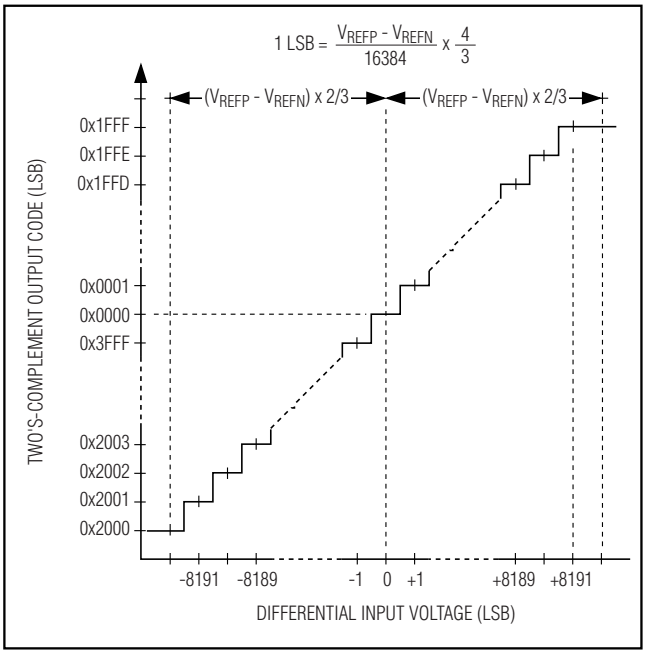


Figure 7. Two's-Complement Transfer Function (G/$\overline{T}$ = 0)

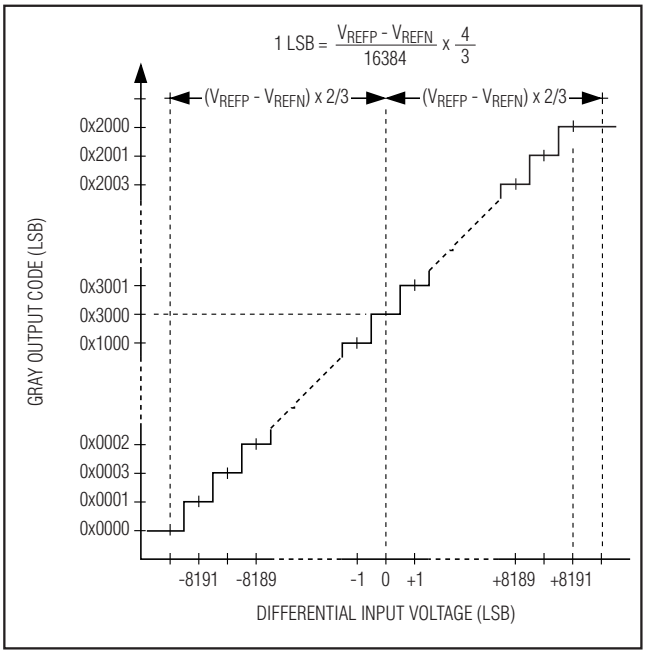


Figure 8. Gray-Code Transfer Function (G/$\overline{T}$ = 1)

In power-down mode, all internal circuits are off, the analog supply current reduces to 0.1mA, and the digital supply current reduces to 0.008mA. The following list shows the state of the analog inputs and digital outputs in power-down mode:

- INP, INN analog inputs are disconnected from the internal input amplifier (Figure 3).
- REFOUT has approximately 17kΩ to GND.
- REFP, COM, REFN go high impedance with respect to V_{DD} and GND, but there is an internal 4kΩ resistor between REFP and COM, as well as an internal 4kΩ resistor between REFN and COM.
- D13–D0, DOR, and DAV go high impedance.
- CLKP, CLKN go high impedance (Figure 5).

The wake-up time from power-down mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 10ms with the recommended capacitor array (Figure 13). When operating in unbuffered external reference mode, the wake-up time is dependent on the external reference drivers.

Applications Information

Using Transformer Coupling

In general, the MAX12554 provides better SFDR and THD performance with fully differential input signals as opposed to single-ended input drive. In differential input mode, even-order harmonics are lower as both inputs are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended input mode.

An RF transformer (Figure 10) provides an excellent solution to convert a single-ended input source signal to a fully differential signal, required by the MAX12554 for optimum performance. Connecting the center tap of the transformer to COM provides a V_{DD} / 2 DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion. The configuration of Figure 10 is good for frequencies up to Nyquist (f_{CLK} / 2).

The circuit of Figure 11 converts a single-ended input signal to fully differential just as Figure 10. However, Figure 11 utilizes an additional transformer to improve the common-mode rejection, allowing high-frequency

BINARY-TO-GRAY-CODE CONVERSION

1) THE MOST SIGNIFICANT GRAY-CODE BIT IS THE SAME AS THE MOST SIGNIFICANT BINARY BIT.

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 1	1 0 1 1	0 1 0 0	1 1 0 0		BINARY
↓					
0					GRAY CODE

2) SUBSEQUENT GRAY-CODE BITS ARE FOUND ACCORDING TO THE FOLLOWING EQUATION:

$GRAY_X = BINARY_X \oplus BINARY_{X+1}$

WHERE $\oplus$ IS THE EXCLUSIVE OR FUNCTION (SEE TRUTH TABLE BELOW) AND X IS THE BIT POSITION.

$GRAY_{12} = BINARY_{12} \oplus BINARY_{13}$

$GRAY_{12} = 1 \oplus 0$

$GRAY_{12} = 1$

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 ⊕ 1	1 0 1 1	0 1 0 0	1 1 0 0		BINARY
↓					
0 1					GRAY CODE

3) REPEAT STEP 2 UNTIL COMPLETE.

$GRAY_{11} = BINARY_{11} \oplus BINARY_{12}$

$GRAY_{11} = 1 \oplus 1$

$GRAY_{11} = 0$

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 1 ⊕ 1	0 1 1	0 1 0 0	1 1 0 0		BINARY
↓					
0 1 0					GRAY CODE

4) THE FINAL GRAY-CODE CONVERSION IS:

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 1	1 0 1 1	0 1 0 0	1 1 0 0		BINARY
0 1	0 1 1 0	1 1 1 0	1 0 1 0		GRAY CODE

GRAY-TO-BINARY-CODE CONVERSION

1) THE MOST SIGNIFICANT BINARY BIT IS THE SAME AS THE MOST SIGNIFICANT GRAY-CODE BIT.

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 1	0 1 1 0	1 1 1 0	1 0 1 0		GRAY CODE
↓					
0					BINARY

2) SUBSEQUENT BINARY BITS ARE FOUND ACCORDING TO THE FOLLOWING EQUATION:

$BINARY_X = BINARY_{X+1} \oplus GRAY_X$

WHERE $\oplus$ IS THE EXCLUSIVE OR FUNCTION (SEE TRUTH TABLE BELOW) AND X IS THE BIT POSITION.

$BINARY_{12} = BINARY_{13} \oplus GRAY_{12}$

$BINARY_{12} = 0 \oplus 1$

$BINARY_{12} = 1$

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 1	0 1 1 0	1 1 1 0	1 0 1 0		GRAY CODE
⊕					
0 1					BINARY

3) REPEAT STEP 2 UNTIL COMPLETE.

$BINARY_{11} = BINARY_{12} \oplus GRAY_{11}$

$BINARY_{11} = 1 \oplus 0$

$BINARY_{11} = 1$

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 1	0 1 1 0	1 1 1 0	1 0 1 0		GRAY CODE
⊕					
0 1 1					BINARY

4) THE FINAL GRAY-CODE CONVERSION IS:

D13 →	D11 →	D7 →	D3 →	D0	BIT POSITION
0 1	0 1 1 0	1 1 1 0	1 0 1 0		GRAY CODE
0 1	1 0 1 1	0 1 0 0	1 1 0 0		BINARY

EXCULSIVE OR TRUTH TABLE

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Figure 9. Binary-to-Gray and Gray-to-Binary Code Conversion

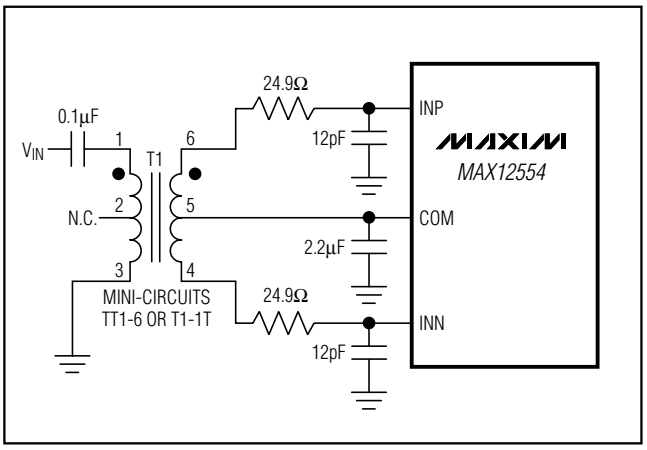


Figure 10. Transformer-Coupled Input Drive for Input Frequencies Up to Nyquist

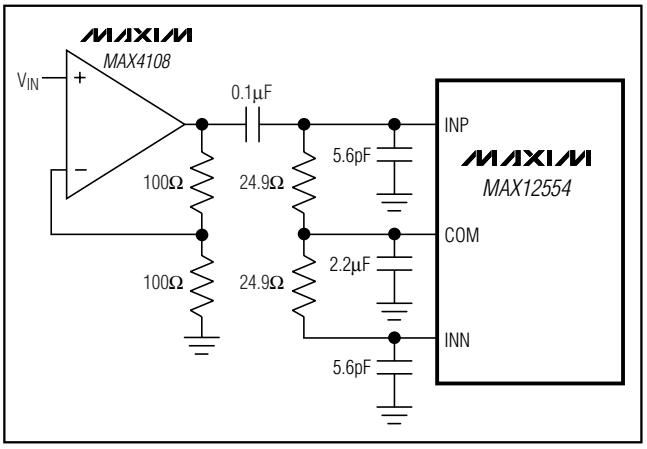


Figure 12. Single-Ended, AC-Coupled Input Drive

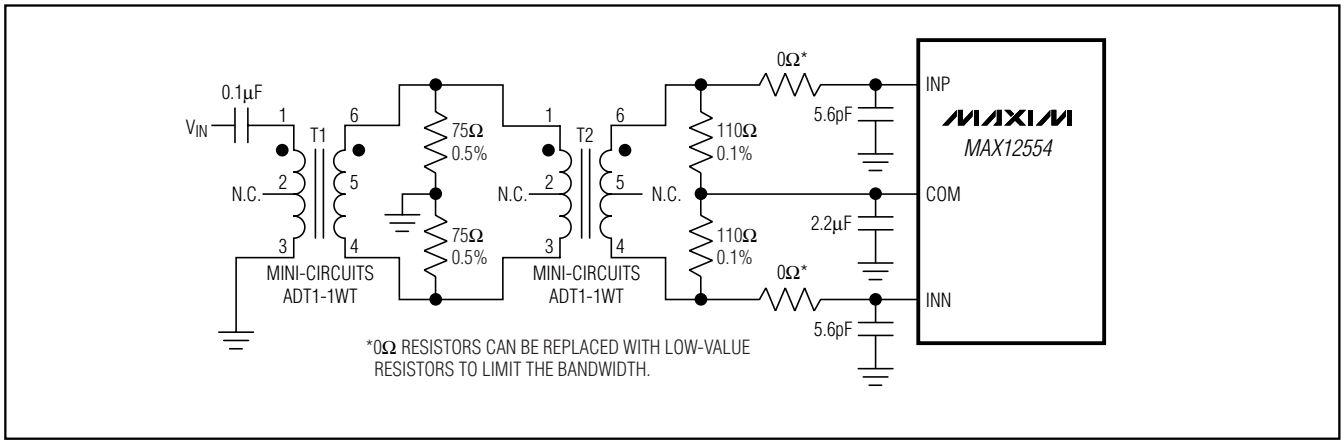


Figure 11. Transformer-Coupled Input Drive for Input Frequencies Beyond Nyquist

signals beyond the Nyquist frequency. The two sets of termination resistors provide an equivalent 50Ω termination to the signal source. The second set of termination resistors connects to COM, providing the correct input common-mode voltage. Two 0Ω resistors in series with the analog inputs allow high IF input frequencies. These 0Ω resistors can be replaced with low-value resistors to limit the input bandwidth.

Single-Ended, AC-Coupled Input Signal

Figure 12 shows an AC-coupled, single-ended input application. The MAX4108 provides high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity.

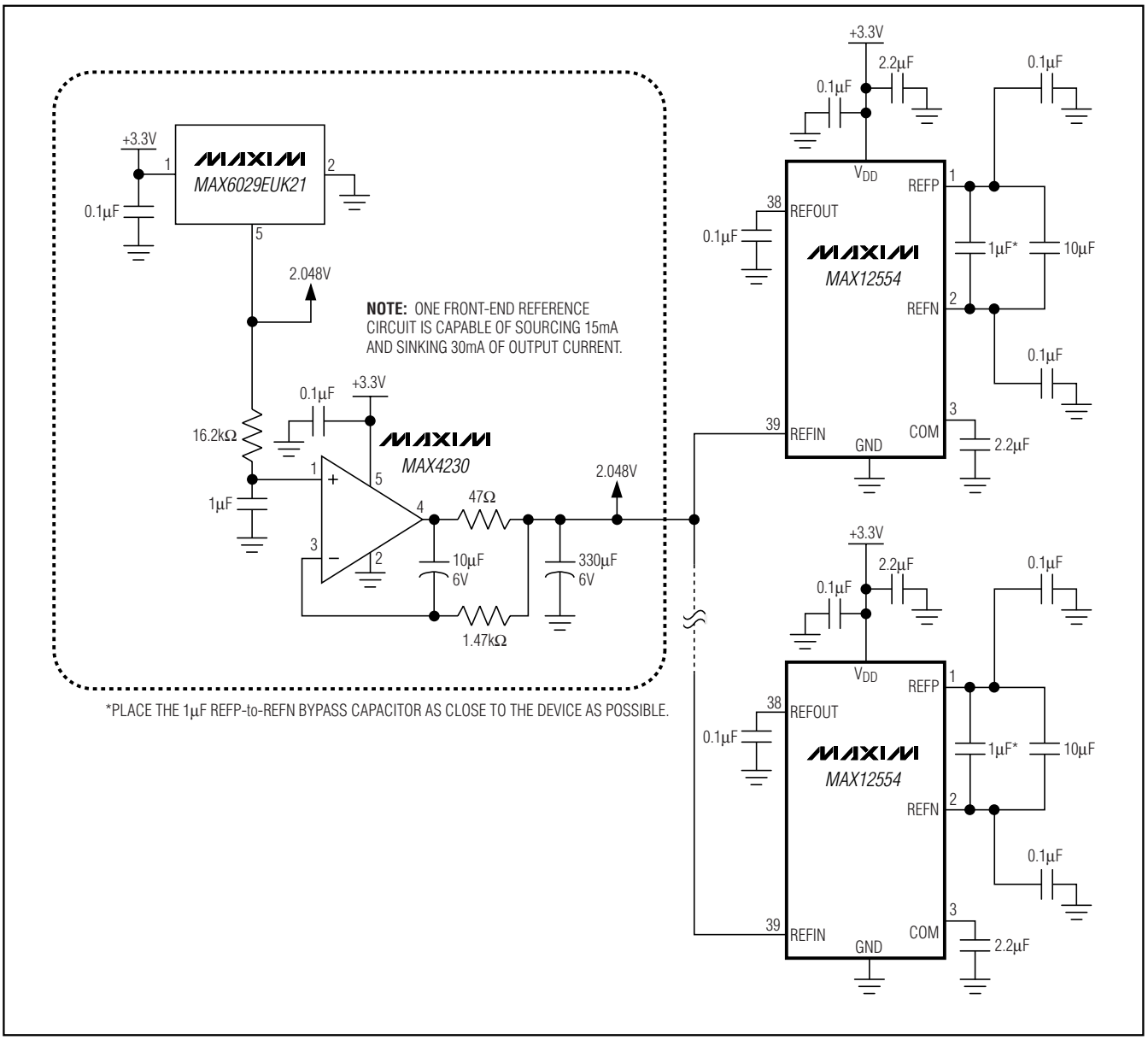


Figure 13. External Buffered Reference Driving Multiple ADCs

Buffered External Reference Drives Multiple ADCs

The buffered external reference mode allows for more control over the MAX12554 reference voltage and allows multiple converters to use a common reference. The REFIN input impedance is >50MΩ.

Figure 13 uses the MAX6029EUK21 precision 2.048V reference as a common reference for multiple converters. The 2.048V output of the MAX6029 passes through a one-pole 10Hz lowpass filter to the MAX4230. The MAX4230 buffers the 2.048V reference and provides additional 10Hz lowpass filtering before its output is applied to the REFIN input of the MAX12554.

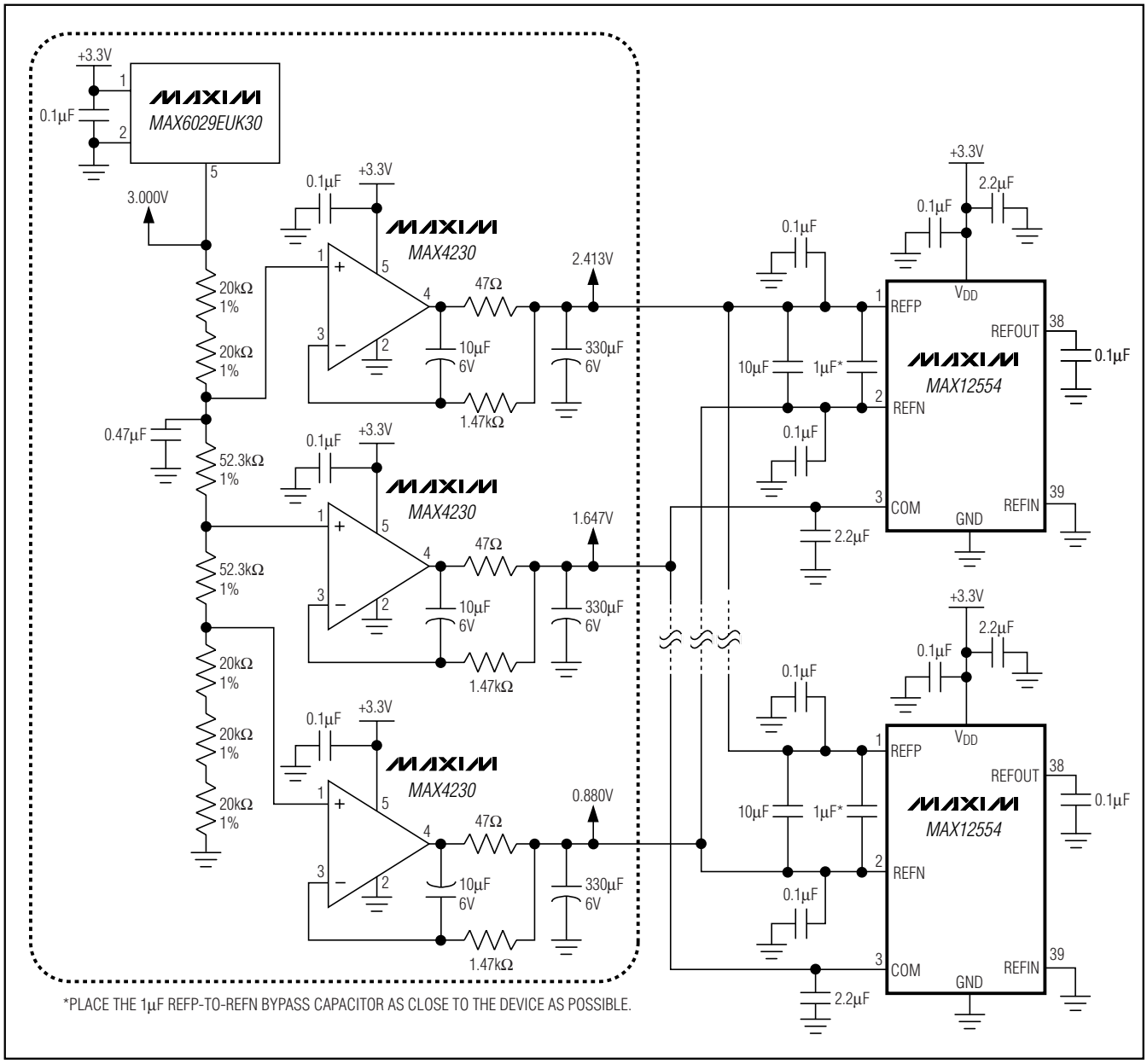


Figure 14. External Unbuffered Reference Driving Multiple ADCs

Unbuffered External Reference Drives Multiple ADCs

The unbuffered external reference mode allows for precise control over the MAX12554 reference and allows multiple converters to use a common reference. Connecting REFIN to GND disables the internal reference, allowing REFP, REFN, and COM to be driven directly by a set of external reference sources.

Figure 14 uses the MAX6029EUK30 precision 3.000V reference as a common reference for multiple converters. A seven-component resistive divider chain follows the MAX6029 voltage reference. The 0.47µF capacitor along this chain creates a 10Hz lowpass filter. Three MAX4230 operational amplifiers buffer taps along this resistor chain providing 2.413V, 1.647V, and 0.880V to the MAX12554's REFP, COM, REFN reference inputs,

respectively. The feedback around the MAX4230 op amps provides additional 10Hz lowpass filtering. The 2.413V and 0.880V reference voltages set the full-scale analog input range to ±1.022V = ±(VREFP - VREFN) x 2/3. A common power source for all active components removes any concern regarding power-supply sequencing when powering up or down.

Grounding, Bypassing, and Board Layout

The MAX12554 requires high-speed board layout design techniques. Refer to the MAX12555 evaluation kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side of the board as the ADC, using surface-mount devices for minimum inductance. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a 2.2µF ceramic capacitor. Bypass OV_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a 2.2µF ceramic capacitor.

Multilayer boards with ample ground and power planes produce the highest level of signal integrity. All MAX12554 GNDs and the exposed back-side paddle must be connected to the same ground plane. The MAX12554 relies on the exposed back-side paddle connection for a low-inductance ground connection. Use multiple vias to connect the top-side ground to the bottom-side ground. Isolate the ground plane from any noisy digital system ground planes such as a DSP or output buffer ground.

Route high-speed digital signal traces away from the sensitive analog traces. Keep all signal lines short and free of 90° turns.

Ensure that the differential analog input network layout is symmetric and that all parasitics are balanced equally. Refer to the MAX12555 evaluation kit data sheet for an example of symmetric input layout.

Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. For the MAX12554, this straight line is between the end points of the transfer function, once offset and gain errors have been nullified. INL deviations are measured at every step of the transfer function and the worst-case deviation is reported in the *Electrical Characteristics* table.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX12554, DNL deviations are measured at every step of the transfer function and the worst-case deviation is reported in the *Electrical Characteristics* table.

Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. Ideally the midscale MAX12554 transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The slope of the actual transfer function is measured between two data points: positive full scale and negative full scale. Ideally, the positive full-scale MAX12554 transition occurs at 1.5 LSBs below positive full scale, and the negative full-scale transition occurs at 0.5 LSB above negative full scale. The gain error is the difference of the measured transition points minus the difference of the ideal transition points.

Small-Signal Noise Floor (SSNF)

Small-signal noise floor is the integrated noise and distortion power in the Nyquist band for small-signal inputs. The DC offset is excluded from this noise calculation. For this converter, a small signal is defined as a single tone with an amplitude less than -35dBFS. This parameter captures the thermal and quantization noise characteristics of the converter and can be used to help calculate the overall noise figure of a receive channel. Go to www.maxim-ic.com for application notes on thermal + quantization noise floor.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{[max]} = 6.02 \times N + 1.76$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the

fundamental, the first six harmonics (HD2–HD7), and the DC offset:

$$SNR = 20 \times \log\left(\frac{SIGNAL_{RMS}}{NOISE_{RMS}}\right)$$

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus the RMS distortion. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset. RMS distortion includes the first six harmonics (HD2–HD7):

$$SINAD = 20 \times \log\left(\frac{SIGNAL_{RMS}}{\sqrt{NOISE_{RMS}^2 + DISTORTION_{RMS}^2}}\right)$$

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02}\right)$$

Single-Tone Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS amplitude of the next-largest spurious component, excluding DC offset.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_7 are the amplitudes of the 2nd- through 7th-order harmonics (HD2–HD7).

Intermodulation Distortion (IMD)

IMD is the ratio of the RMS sum of the intermodulation products to the RMS sum of the two fundamental input tones. This is expressed as:

$$MD = 20 \times \log\left(\frac{\sqrt{V_{IM1}^2 + V_{IM2}^2 + \ldots\ldots + V_{IM13}^2 + V_{IM14}^2}}{\sqrt{V_1^2 + V_2^2}}\right)$$

The fundamental input tone amplitudes (V_1 and V_2) are at -7dBFS. Fourteen intermodulation products ($V_{IM_}$) are used in the MAX12554 IMD calculation. The intermodulation products are the amplitudes of the output spectrum at the following frequencies, where f_{IN1} and f_{IN2} are the fundamental input tone frequencies:

- Second-order intermodulation products:
  $f_{IN1} + f_{IN2}$, $f_{IN2} - f_{IN1}$
- Third-order intermodulation products:
  $2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$, $2 \times f_{IN2} + f_{IN1}$
- Fourth-order intermodulation products:
  $3 \times f_{IN1} - f_{IN2}$, $3 \times f_{IN2} - f_{IN1}$, $3 \times f_{IN1} + f_{IN2}$, $3 \times f_{IN2} + f_{IN1}$
- Fifth-order intermodulation products:
  $3 \times f_{IN1} - 2 \times f_{IN2}$, $3 \times f_{IN2} - 2 \times f_{IN1}$, $3 \times f_{IN1} + 2 \times f_{IN2}$, $3 \times f_{IN2} + 2 \times f_{IN1}$

Third-Order Intermodulation (IM3)

IM3 is the total power of the third-order intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_{IN1} and f_{IN2}. The individual input tone levels are at -7dBFS. The third-order intermodulation products are $2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$, $2 \times f_{IN2} + f_{IN1}$.

Two-Tone Spurious-Free Dynamic Range ($SFDR_{TT}$)

$SFDR_{TT}$ represents the ratio, expressed in decibels, of the RMS amplitude of either input tone to the RMS amplitude of the next-largest spurious component in the spectrum, excluding DC offset. This spurious component can occur anywhere in the spectrum up to Nyquist and is usually an intermodulation product or a harmonic.

Aperture Delay

The MAX12554 samples data on the falling edge of its sampling clock. In actuality, there is a small delay between the falling edge of the sampling clock and the actual sampling instant. Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken (Figure 4).

Aperture Jitter

Figure 4 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Output Noise (n_{OUT})

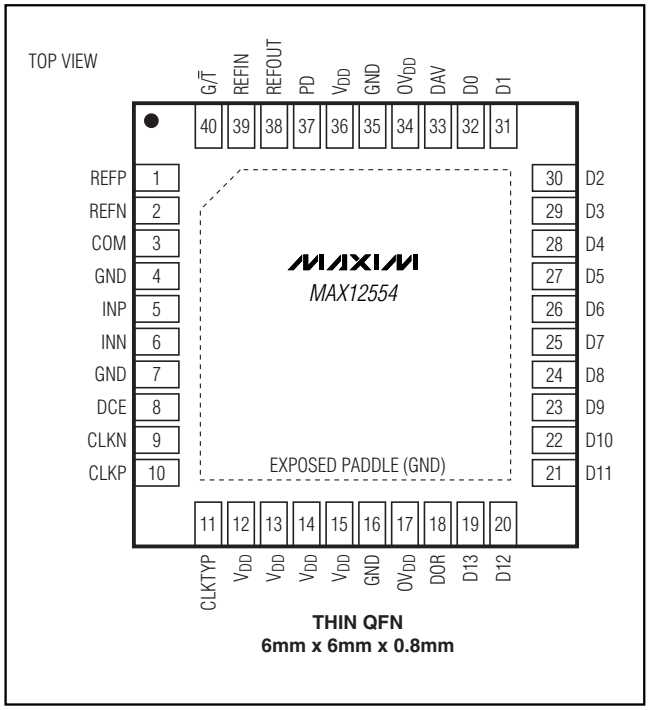
The output noise (n_{OUT}) parameter is similar to the thermal + quantization noise parameter and is an indication of the ADC's overall noise performance.

No fundamental input tone is used to test for n_{OUT}; INP, INN, and COM are connected together and 1024k data points collected. n_{OUT} is computed by taking the RMS value of the collected data points after the mean is removed.

Overdrive Recovery Time

Overdrive recovery time is the time required for the ADC to recover from an input transient that exceeds the full-scale limits. The MAX12554 specifies overdrive recovery time using an input transient that exceeds the full-scale limits by ±10%.

Pin Configuration

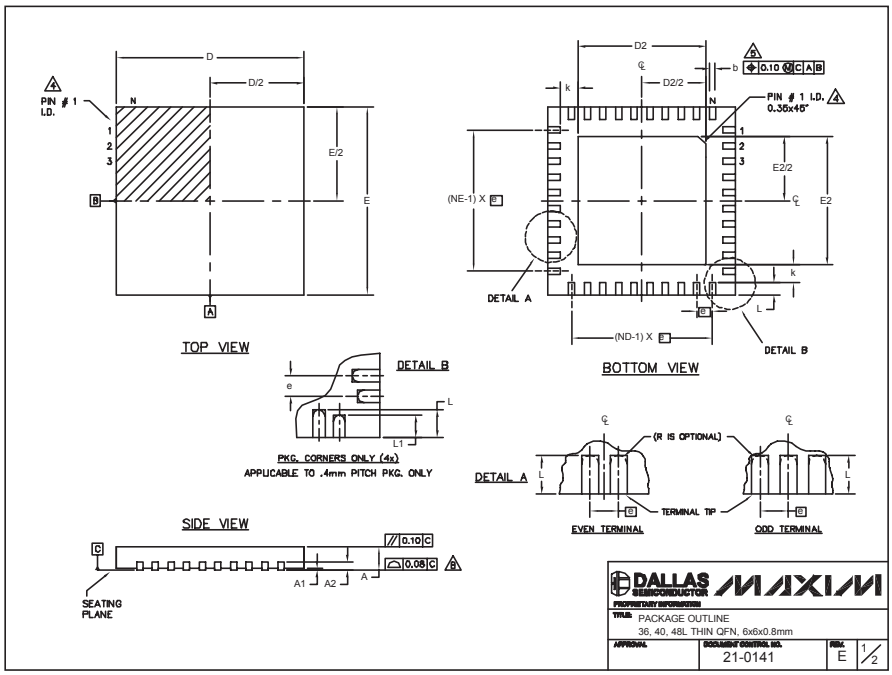


14-Bit, 80Msps, 3.3V ADC

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 6x6x0.8.EPS



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm
DOCUMENT CONTROL NO. 21-0141
REV. E
2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2004 Maxim Integrated Products Printed USA MAXIM is a registered trademark of Maxim Integrated Products.