ISLA214P12

High Performance 14-Bit, 125MSPS ADC

FN7982
Rev.4.0
Jul 6, 2021

The ISLA214P12 is a high performance 14-bit 125MSPS analog-to-digital converter offering very high dynamic range and low power consumption. It is part of a pin-compatible family of 12- to 16-bit A/Ds with maximum sample rates ranging from 125 to 500MSPS. This allows a design using the ISLA214P12 to accommodate any of the other pin-compatible A/Ds with minimal changes.

The ISLA214P12 is very flexible and can be designed into a wide variety of systems. A Serial Peripheral Interface (SPI) port allows access to its extensive configurability and provides digital control over various analog parameters such as input gain and offset. Digital output data is presented in selectable LVDS or CMOS formats and can be configured as full-width, Single Data Rate (SDR) or half-width, Double Data Rate (DDR). Operating from a 1.8V supply, performance is specified across the full industrial temperature range (-40°C to +85°C).

Applications

- Radar array processing
- Software defined radio
- Broadband communications
- High performance data acquisition
- Communications test equipment

Features

- Multi-ADC Support
  - SPI programmable fine gain and offset control
  - Multiple ADC synchronization
  - Optimized output timing
- Clock duty cycle stabilizer
- Nap and Sleep modes
- Programmable built-in test patterns
- SDR/DDR LVDS-compatible or LVCMOS outputs
- Data output clock

Key Specifications

- SNR at 125MSPS
  - 74.9dBFS f_{IN} = 30MHz
  - 70.9dBFS f_{IN} = 363MHz
- SFDR at 125MSPS
  - 88dBc f_{IN} = 30MHz
  - 84dBc f_{IN} = 363MHz
- Total power consumption = 310mW

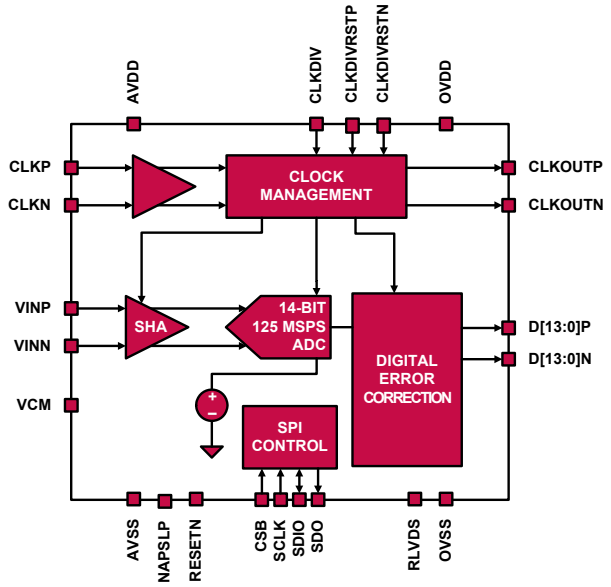

TABLE 1. PIN-COMPATIBLE FAMILY

MODEL	RESOLUTION	SPEED (MSPS)
ISLA216P25	16	250
ISLA216P20	16	200
ISLA216P13	16	130
ISLA214P50	14	500
ISLA214P25	14	250
ISLA214P20	14	200
ISLA214P13	14	130
ISLA212P50	12	500
ISLA212P25	12	250
ISLA212P20	12	200
ISLA212P13	12	130

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Ordering Information

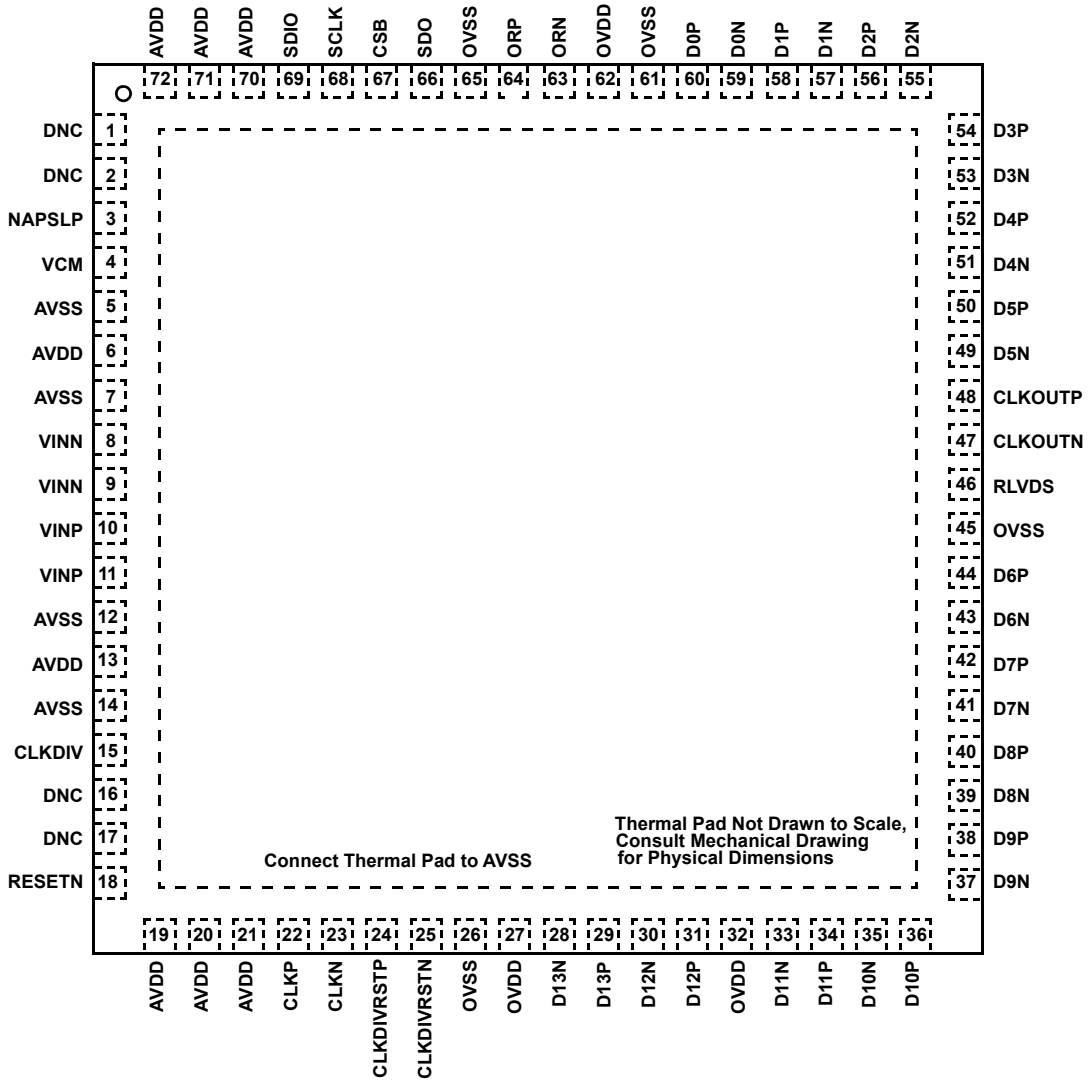
PART NUMBER (Notes 1, 2)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE	TEMP. RANGE
ISLA214P12IRZ	ISLA214P12 IRZ	72 Ld QFN	L72.10x10G	Tray	-40°C to +85°C
ISLA214IR72EV1Z	Evaluation Board - supports 125/130/200/250Msps grades				
KMB-001LEVALZ	LVDS Motherboard (Interfaces with ISLA214IR72EV1Z operating in LVDS Output mode)				
KMB-001CEVALZ	CMOS Motherboard (Interfaces with ISLA214IR72EV1Z operating in CMOS Output mode)				

NOTES:

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISLA214P12 device page. For more information about MSL, see TB363.

Pin Configuration - LVDS Mode

72 LD QFN
TOP VIEW



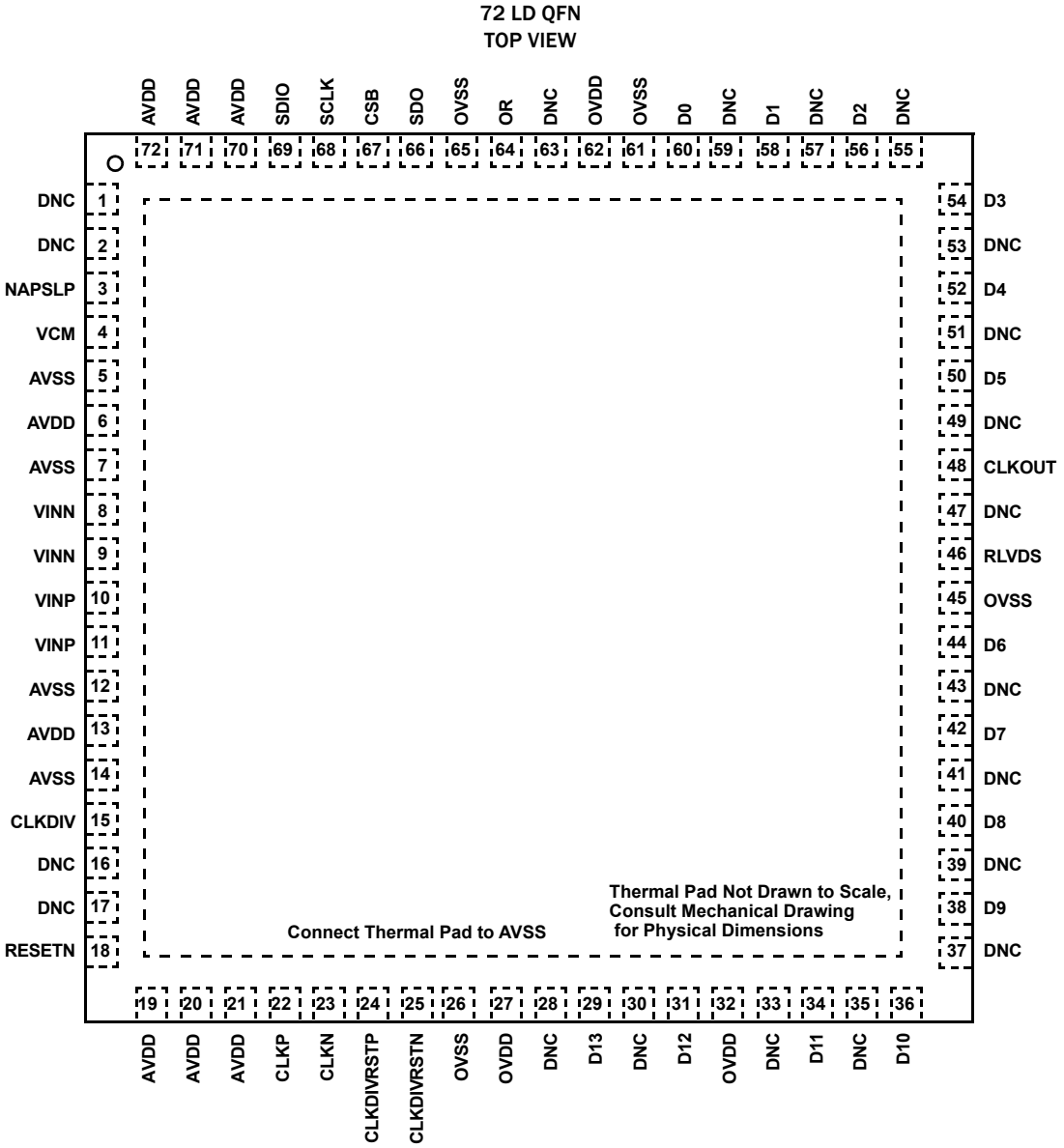
Pin Descriptions - 72 Ld QFN, LVDS Mode

PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION	DDR MODE COMMENTS
1, 2, 16, 17	DNC	Do Not Connect	
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply	
5, 7, 12, 14	AVSS	Analog Ground	
27, 32, 62	OVDD	1.8V Output Supply	
26, 45, 61, 65	OVSS	Output Ground	
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)	
4	VCM	Common Mode Output	
8, 9	VINN	Analog Input Negative	
10, 11	VINP	Analog Input Positive	
15	CLKDIV	Tri-Level Clock Divider Control	
18	RESETN	Power On Reset (Active Low)	
22, 23	CLKP, CLKN	Clock Input True, Complement	
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement	
28	D13N	LVDS Bit 13(MSB) Output Complement	NC in DDR Mode
29	D13P	LVDS Bit 13 (MSB) Output True	NC in DDR Mode
30	D12N	LVDS Bit 12 Output Complement	DDR Logical Bits 12, 13
31	D12P	LVDS Bit 12 Output True	DDR Logical Bits 12, 13
33	D11N	LVDS Bit 11 Output Complement	NC in DDR Mode
34	D11P	LVDS Bit 11 Output True	NC in DDR Mode
35	D10N	LVDS Bit 10 Output Complement	DDR Logical Bits 10, 11
36	D10P	LVDS Bit 10 Output True	DDR Logical Bits 10, 11
37	D9N	LVDS Bit 9 Output Complement	NC in DDR Mode
38	D9P	LVDS Bit 9 Output True	NC in DDR Mode
39	D8N	LVDS Bit 8 Output Complement	DDR Logical Bits 8, 9
40	D8P	LVDS Bit 8 Output True	DDR Logical Bits 8, 9
41	D7N	LVDS Bit 7 Output Complement	NC in DDR Mode
42	D7P	LVDS Bit 7 Output True	NC in DDR Mode
43	D6N	LVDS Bit 6 Output Complement	DDR Logical Bits 6, 7
44	D6P	LVDS Bit 6 Output True	DDR Logical Bits 6, 7
46	RLVDS	LVDS Bias Resistor (Connect to OVSS with 1% 10kΩ)	
47, 48	CLKOUTN, CLKOUTP	LVDS Clock Output Complement, True	
49	D5N	LVDS Bit 5 Output Complement	NC in DDR Mode
50	D5P	LVDS Bit 5 Output True	NC in DDR Mode
51	D4N	LVDS Bit 4 Output Complement	DDR Logical Bits 4, 5
52	D4P	LVDS Bit 4 Output True	DDR Logical Bits 4, 5
53	D3N	LVDS Bit 3 Output Complement	NC in DDR Mode
54	D3P	LVDS Bit 3 Output True	NC in DDR Mode
55	D2N	LVDS Bit 2 Output Complement	DDR Logical Bits 2, 3
56	D2P	LVDS Bit 2 Output True	DDR Logical Bits 2, 3
57	D1N	LVDS Bit 1 Output Complement	NC in DDR Mode
58	D1P	LVDS Bit 1 True	NC in DDR Mode

Pin Descriptions - 72 Ld QFN, LVDS Mode (Continued)

PIN NUMBER	LVDS PIN NAME	LVDS PIN FUNCTION	DDR MODE COMMENTS
59	D0N	LVDS Bit 0 (LSB) Output Complement	DDR Logical Bits 0, 1
60	D0P	LVDS Bit 0 (LSB) Output True	DDR Logical Bits 0, 1
63, 64	ORN, ORP	LVDS Over Range Complement, True	DDR Over Range
66	SDO	SPI Serial Data Output	
67	CSB	SPI Chip Select (active low)	
68	SCLK	SPI Clock	
69	SDIO	SPI Serial Data Input/Output	
Exposed Paddle	AVSS	Analog Ground	

Pin Configuration - CMOS Mode



Pin Descriptions - 72 Ld QFN, CMOS Mode

PIN NUMBER	CMOS PIN NAME	CMOS PIN FUNCTION	DDR MODE COMMENTS
1, 2, 16, 17, 28, 30, 33, 35, 37, 39, 41, 43, 47, 49, 51, 53, 55, 57, 59, 63	DNC	Do Not Connect	
6, 13, 19, 20, 21, 70, 71, 72	AVDD	1.8V Analog Supply	
5, 7, 12, 14	AVSS	Analog Ground	
27, 32, 62	OVDD	1.8V Output Supply	
26, 45, 61, 65	OVSS	Output Ground	
3	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)	
4	VCM	Common Mode Output	
8, 9	VINN	Analog Input Negative	
10, 11	VINP	Analog Input Positive	
15	CLKDIV	Tri-Level Clock Divider Control	
18	RESETN	Power On Reset (Active Low)	
22, 23	CLKP, CLKN	Clock Input True, Complement	
24, 25	CLKDIVRSTP, CLKDIVRSTN	Synchronous Clock Divider Reset True, Complement	
29	D13	CMOS Bit 13 (MSB) Output	NC in DDR Mode
31	D12	CMOS Bit 12 Output	DDR Logical Bits 12, 13
34	D11	CMOS Bit 11 Output	NC in DDR Mode
36	D10	CMOS Bit 10 Output	DDR Logical Bits 10, 11
38	D9	CMOS Bit 9 Output	NC in DDR Mode
40	D8	CMOS Bit 8 Output	DDR Logical Bits 8, 9
42	D7	CMOS Bit 7 Output	NC in DDR Mode
44	D6	CMOS Bit 6 Output	DDR Logical Bits 6, 7
46	RLVDS	LVDS Bias Resistor (connect to OVSS with 1% 10kΩ)	
48	CLKOUT	CMOS Clock Output	
50	D5	CMOS Bit 5 Output	NC in DDR Mode
52	D4	CMOS Bit 4 Output	DDR Logical Bits 4, 5
54	D3	CMOS Bit 3 Output	NC in DDR Mode
56	D2	CMOS Bit 2 Output	DDR Logical Bits 2, 3
58	D1	CMOS Bit 1 Output	NC in DDR Mode
60	D0	CMOS Bit 0 (LSB) Output	DDR Logical Bits 0, 1
64	OR	CMOS Over Range	DDR Over Range
66	SDO	SPI Serial Data Output	
67	CSB	SPI Chip Select (active low)	
68	SCLK	SPI Clock	
69	SDIO	SPI Serial Data Input/Output	
Exposed Paddle	AVSS	Analog Ground	

Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS . . . . . -0.3V to 0.3V
Analog Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS . . . . . -0.4V to OVDD + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2kV
Charged Device Model (Tested per JESD22-C101D) 200V
Latch-Up (Tested per JESD-78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
72 Ld QFN (Notes 3, 4)	23	0.9

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (Typical specifications at +25°C), A_{IN} = -1dBFS, f_{SAMPLE} = 125Msps. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
DC SPECIFICATIONS (Note 6)						
Analog Input						
Full-Scale Analog Input Range	V_{FS}	Differential	**1.95**	2.0	**2.1**	V_{P-P}
Input Resistance	R_{IN}	Differential		600		Ω
Input Capacitance	C_{IN}	Differential		4.5		pF
Full Scale Range Temperature Drift	A_{VTC}	Full temperature		74		ppm/°C
Input Offset Voltage	V_{OS}		**-5.0**	-1.7	**5.0**	mV
Common-Mode Output Voltage	V_{CM}			0.94		V
Common-Mode Input Current (per pin)	I_{CM}			2.6		µA/MSPS
Clock Inputs						
Inputs Common-Mode Voltage				0.9		V
CLKP, CLKN Input Swing (Note 7)				1.8		V
Power Requirements						
1.8V Analog Supply Voltage	AVDD		**1.7**	1.8	**1.9**	V
1.8V Digital Supply Voltage	OVDD		**1.7**	1.8	**1.9**	V
1.8V Analog Supply Current	I_{AVDD}			152	**161**	mA
1.8V Digital Supply Current (Note 6)	I_{OVDD}	3mA LVDS (SDR)		68.5	**77**	mA
Power Supply Rejection Ratio	PSRR	30MHz, 30mV_{P-P} signal on AVDD		40		dB
Total Power Dissipation						
Normal Mode	P_D	CMOS (DDR)		310		mW
		CMOS (SDR)		313		mW
		2mA LVDS (SDR)		369		mW
		3mA LVDS (DDR)		360		mW
		3mA LVDS (SDR)		397	**428**	mW

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (Typical specifications at +25°C), A_{IN} = -1dBFS, f_{SAMPLE} = 125Msps. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
Nap Mode	P_D			48.6	**53**	mW
Sleep Mode	P_D	CSB at logic high		6	**10**	mW
Nap/Sleep Mode Wakeup Time		Sample clock running		630		µs
AC SPECIFICATIONS						
Differential Nonlinearity	DNL	f_{IN} = 105MHz		±0.25		LSB
Integral Nonlinearity	INL	f_{IN} = 105MHz		±2.5		LSB
Minimum Conversion Rate (Note 8)	f_S MIN				**40**	MSPS
Maximum Conversion Rate	f_S MAX		**125**			MSPS
Signal-to-Noise Ratio (Note 9)	SNR	f_{IN} = 30MHz		74.9		dBFS
		f_{IN} = 105MHz	73.0	74.3		dBFS
		f_{IN} = 190MHz		73.3		dBFS
		f_{IN} = 363MHz		70.9		dBFS
		f_{IN} = 461MHz		69.5		dBFS
		f_{IN} = 605MHz		67.8		dBFS
Signal-to-Noise and Distortion (Note 9)	SINAD	f_{IN} = 30MHz		74.6		dBFS
		f_{IN} = 105MHz	70.8	73.6		dBFS
		f_{IN} = 190MHz		72.2		dBFS
		f_{IN} = 363MHz		70.6		dBFS
		f_{IN} = 461MHz		65.9		dBFS
		f_{IN} = 605MHz		61.1		dBFS
Effective Number of Bits (Note 9)	ENOB	f_{IN} = 30MHz		12.10		Bits
		f_{IN} = 105MHz	11.47	11.93		Bits
		f_{IN} = 190MHz		11.70		Bits
		f_{IN} = 363MHz		11.44		Bits
		f_{IN} = 461MHz		10.65		Bits
		f_{IN} = 605MHz		9.86		Bits
Spurious-Free Dynamic Range (Note 9)	SFDR	f_{IN} = 30MHz		88		dBc
		f_{IN} = 105MHz	70	83		dBc
		f_{IN} = 190MHz		78		dBc
		f_{IN} = 363MHz		84		dBc
		f_{IN} = 461MHz		68		dBc
		f_{IN} = 605MHz		61		dBc
Spurious-Free Dynamic Range Excluding H2, H3	SFDRX23	f_{IN} = 30MHz		99		dBc
		f_{IN} = 105MHz		95		dBc
		f_{IN} = 190MHz		91		dBc
		f_{IN} = 363MHz		95		dBc
		f_{IN} = 461MHz		94		dBc
		f_{IN} = 605MHz		87		dBc

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (Typical specifications at +25°C), A_{IN} = -1dBFS, f_{SAMPLE} = 125Msps. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
Intermodulation Distortion	IMD	f_{IN} = 70MHz		-85		dBFS
		f_{IN} = 170MHz		-105		dBFS
Word Error Rate	WER			10^{-12}		
Full Power Bandwidth	FPBW			700		MHz

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
6. Digital Supply Current is dependent upon the capacitive loading of the digital outputs. I_{OVDD} specifications apply for 10pF load on each digital output.
7. See "Clock Input" on page 19.
8. The DLL Range setting must be changed for low-speed operation.
9. Minimum specification ensured when calibrated at +85°C.

Digital Specifications

Boldface limits apply across the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
INPUTS (Note 10)						
Input Current High (RESETN)	I_{IH}	V_{IN} = 1.8V	**0**	1	**10**	µA
Input Current Low (RESETN)	I_{IL}	V_{IN} = 0V	**-25**	-12	**-8**	µA
Input Current High (SDIO)	I_{IH}	V_{IN} = 1.8V		4	**12**	µA
Input Current Low (SDIO)	I_{IL}	V_{IN} = 0V	**-600**	-415	**-300**	µA
Input Current High (CSB)	I_{IH}	V_{IN} = 1.8V	**40**	58	**75**	µA
Input Current Low (CSB)	I_{IL}	V_{IN} = 0V		5	**10**	µA
Input Current High (CLKDIV)	I_{IH}		**16**	25	**34**	µA
Input Current Low (CLKDIV)	I_{IL}		**-34**	-25	**-16**	µA
Input Voltage High (SDIO, RESETN)	V_{IH}		**1.17**			V
Input Voltage Low (SDIO, RESETN)	V_{IL}				**0.63**	V
Input Capacitance	C_{DI}			4		pF
LVDS INPUTS (CLKDIVRSTP, CLKDIVRSTN)						
Input Common-Mode Range	V_{ICM}		**825**		**1575**	mV
Input Differential Swing (peak-to-peak, single-ended)	V_{ID}		**250**		**450**	mV
CLKDIVRSTP Input Pull-Down Resistance	R_{Ipd}			100		kΩ
CLKDIVRSTN Input Pull-Up Resistance	R_{Ipu}			100		kΩ
LVDS OUTPUTS						
Differential Output Voltage (Note 11)	V_T	3mA mode		612		mV_{P-P}
Output Offset Voltage	V_{OS}	3mA mode	**1120**	1150	**1200**	mV
Output Rise Time	t_R			240		ps
Output Fall Time	t_F			240		ps
CMOS OUTPUTS						
Voltage Output High	V_{OH}	I_{OH} = -500µA	**OVDD - 0.3**	OVDD - 0.1		V
Voltage Output Low	V_{OL}	I_{OL} = 1mA		0.1	**0.3**	V

Digital Specifications Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
Output Rise Time	t_R			1.8		ns
Output Fall Time	t_F			1.4		ns

NOTES:

10. The tri-level inputs internal switching thresholds are approximately 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
11. The voltage is expressed in peak-to-peak differential swing. The peak-to-peak singled-ended swing is 1/2 of the differential swing.

Timing Diagrams

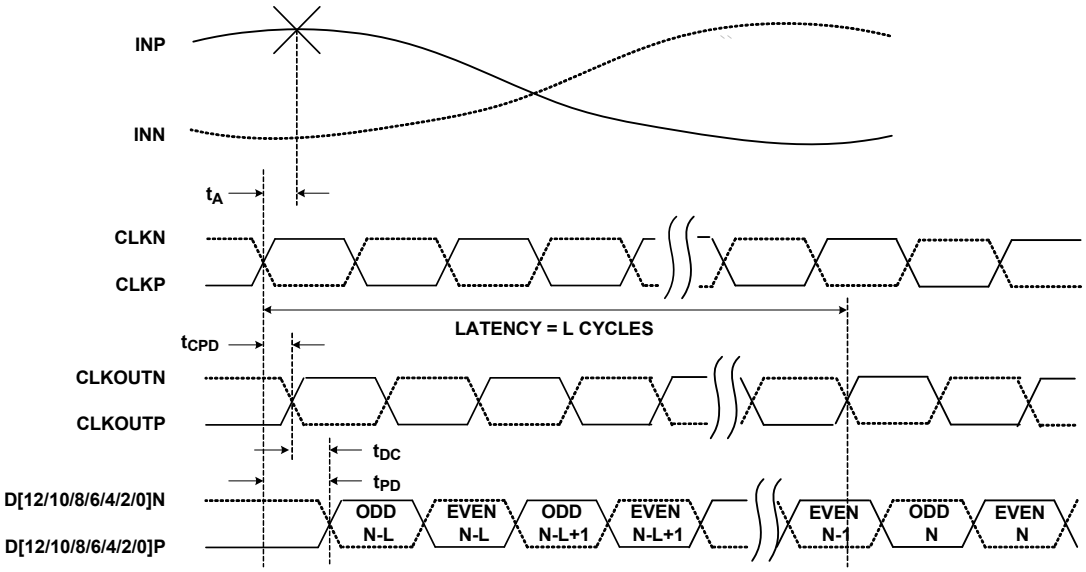


FIGURE 1A. LVDS DDR

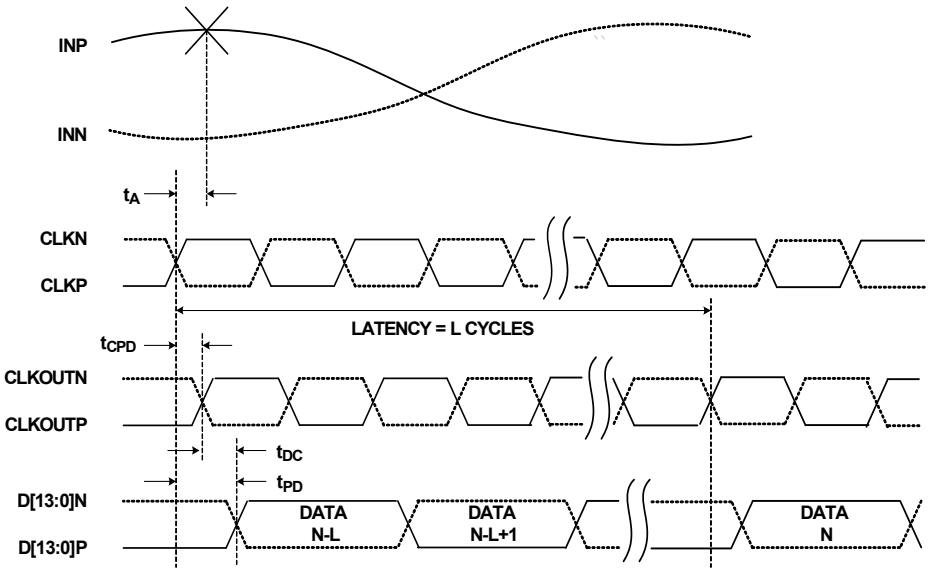


FIGURE 1B. LVDS SDR

FIGURE 1. LVDS TIMING DIAGRAMS

Timing Diagrams (Continued)

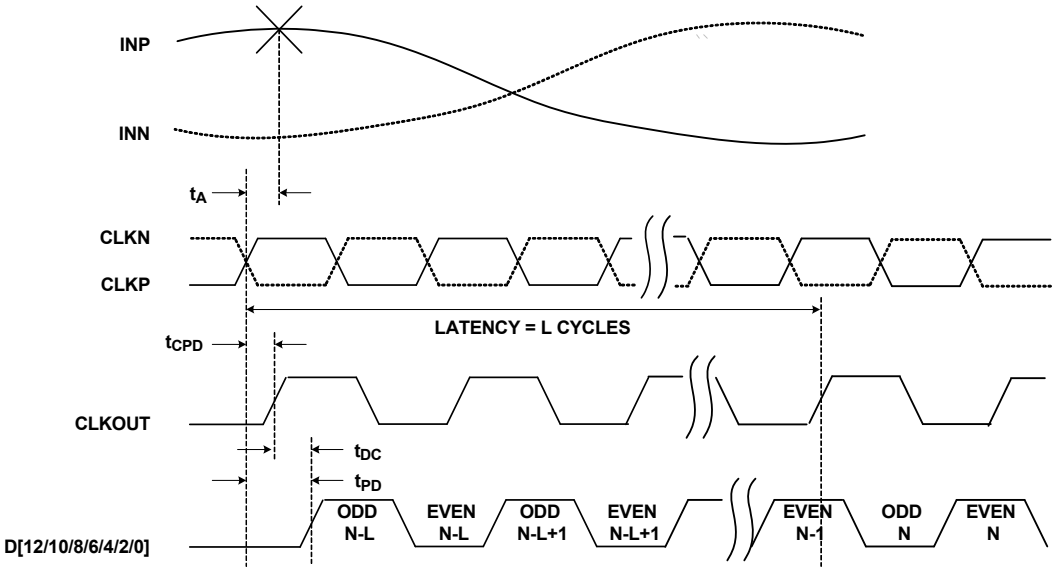


FIGURE 2A. CMOS DDR

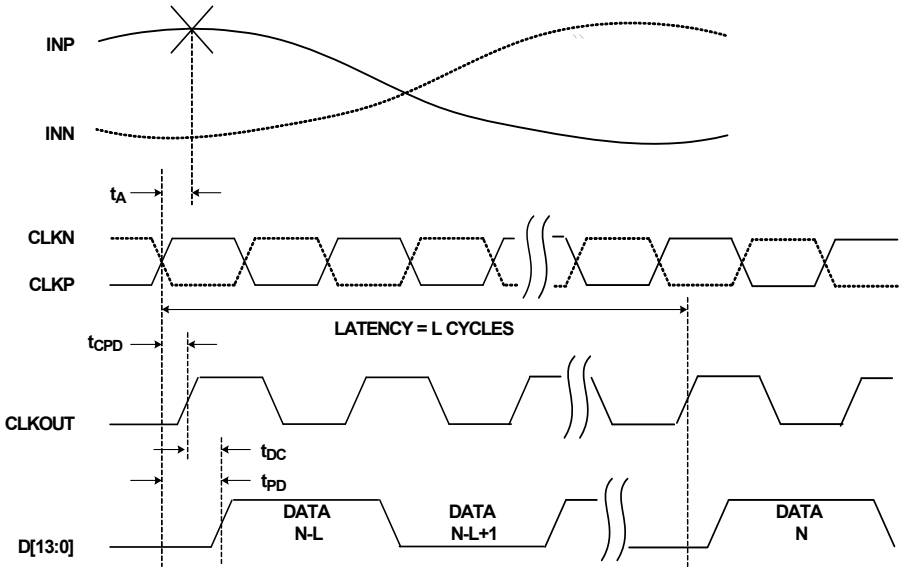


FIGURE 2B. CMOS SDR

FIGURE 2. CMOS TIMING DIAGRAMS

Switching Specifications

Boldface limits apply across the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITION	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
ADC OUTPUT						
Aperture Delay	t_A			114		ps
RMS Aperture Jitter	j_A			75		fs
Input Clock to Output Clock Propagation Delay	t_{CPD}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	**1.65**	2.4	**3**	ns
	t_{CPD}	AVDD, OVDD = 1.8V, T_A = +25°C	**1.9**	2.3	**2.75**	ns
Relative Input Clock to Output Clock Propagation Delay (Note 12)	dt_{CPD}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	**-450**		**450**	ps
Input Clock to Data Propagation Delay	t_{PD}		**1.65**	2.4	**3.5**	ns
Output Clock to Data Propagation Delay, LVDS Mode	t_{DC}	Rising/falling edge	**-0.1**	0.16	**0.5**	ns
Output Clock to Data Propagation Delay, CMOS Mode	t_{DC}	Rising/falling edge	**-0.1**	0.2	**0.65**	ns
Synchronous Clock Divider Reset Setup Time (with respect to the positive edge of CLKP)	t_{RSTS}		**0.4**	0.06		ns
Synchronous Clock Divider Reset Hold Time (with respect to the positive edge of CLKP)	t_{RSTH}			0.02	**0.35**	ns
Synchronous Clock Divider Reset Recovery Time	t_{RSTRT}	DLL recovery time after Synchronous Reset (sample clock not interrupted)		30		cycles
Latency (Pipeline Delay)	L			10		cycles
Overvoltage Recovery	t_{OVR}			1		cycles
SPI INTERFACE (Notes 13, 14)						
SCLK Period	t_{CLK}	Write operation	**16**			cycles
	t_{CLK}	Read operation	**16**			cycles
CSB↓ to SCLK↑ Setup Time	t_S	Read or Write	**28**			cycles
CSB↑ after SCLK↑ Hold Time	t_H	Write	**5**			cycles
CSB↑ after SCLK↓ Hold Time	t_{HR}	Read	**16**			cycles
Data Valid to SCLK↑ Setup Time	t_{DS}	Write	**6**			cycles
Data Valid after SCLK↑ Hold Time	t_{DH}	Read or Write			**4**	cycles
Data Valid after SCLK↓ Time	t_{DVR}	Read			**5**	cycles

NOTES:

12. The relative propagation delay is the difference in propagation time between any two devices that are matched in temperature and voltage, and is specified across the full operating temperature and voltage range.
13. SPI Interface timing is directly proportional to the ADC sample period (t_S). Values above reflect multiples of a 4ns sample period, and must be scaled proportionally for lower sample rates. ADC sample clock must be running for SPI communication.
14. The SPI may operate asynchronously with respect to the ADC sample clock.

Typical Performance Curves

All typical performance characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 125MSPS.

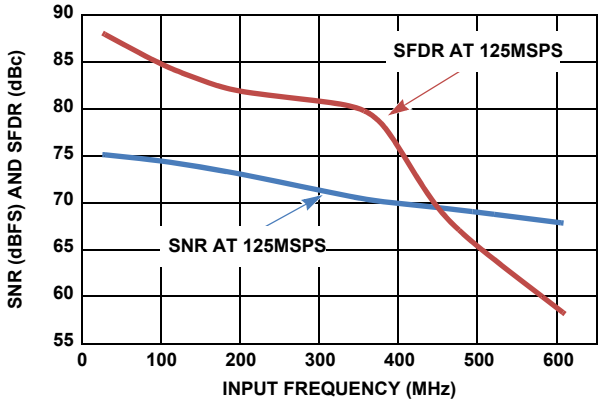


FIGURE 3. SNR AND SFDR vs f_{IN}

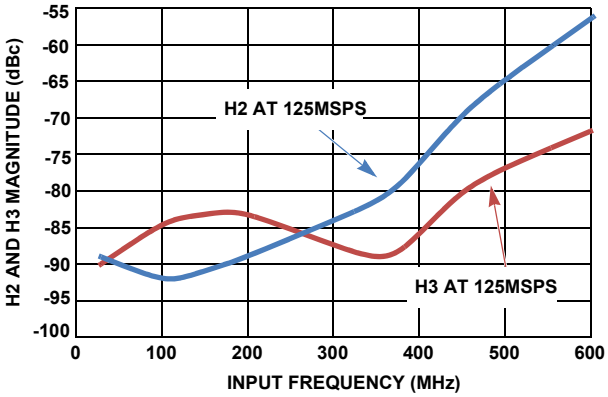


FIGURE 4. HD2 AND HD3 vs f_{IN}

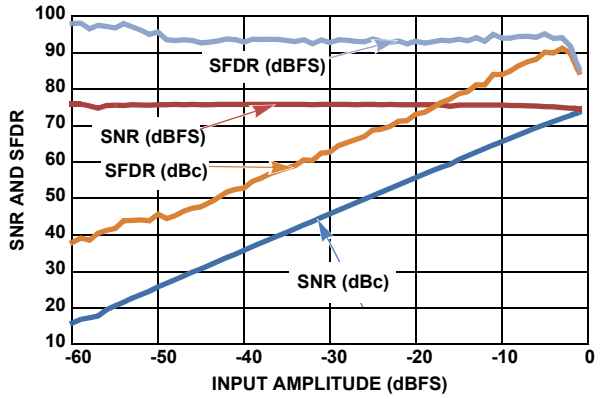


FIGURE 5. SNR AND SFDR vs A_{IN}

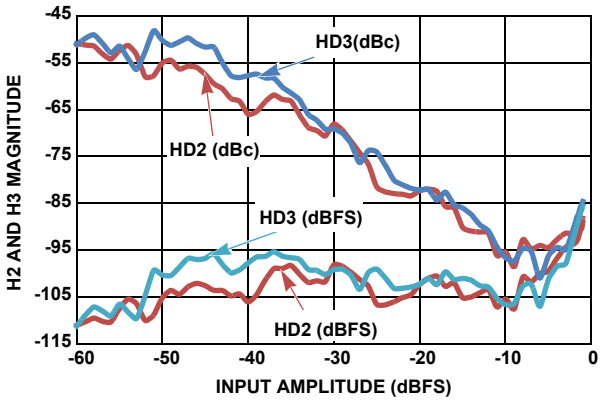


FIGURE 6. HD2 AND HD3 vs A_{IN}

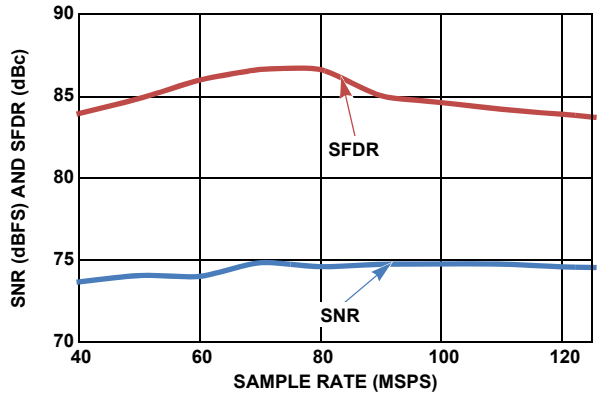


FIGURE 7. SNR AND SFDR vs f_{SAMPLE}

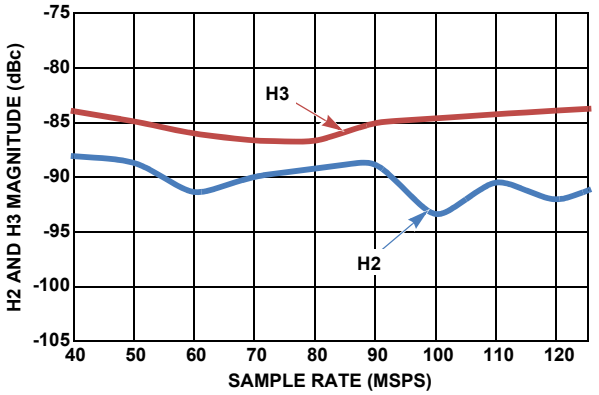


FIGURE 8. HD2 AND HD3 vs f_{SAMPLE}

Typical Performance Curves

All typical performance characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 125MSPS. **(Continued)**

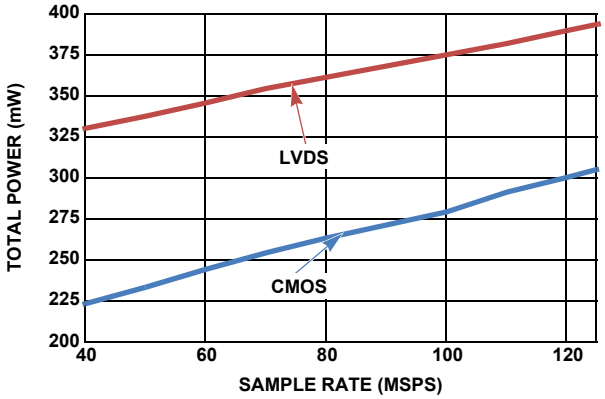


FIGURE 9. POWER vs f_{SAMPLE} IN 3mA LVDS MODE (SDR) AND CMOS MODE (DDR)

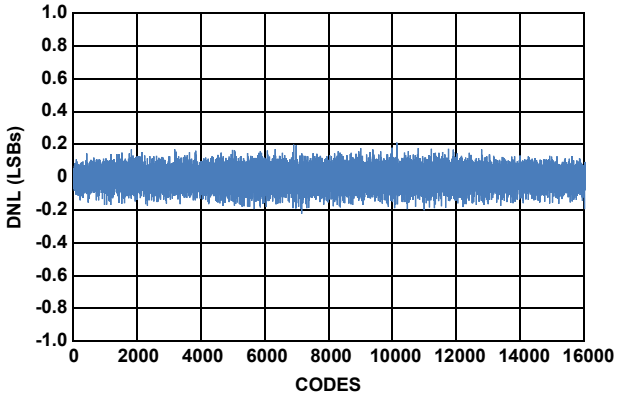


FIGURE 10. DIFFERENTIAL NONLINEARITY

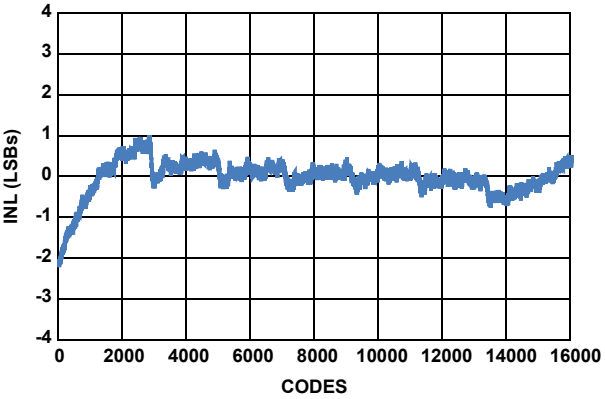


FIGURE 11. INTEGRAL NONLINEARITY

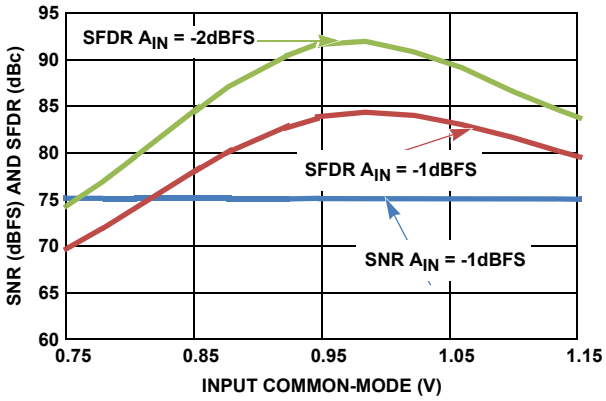


FIGURE 12. SNR AND SFDR vs VCM

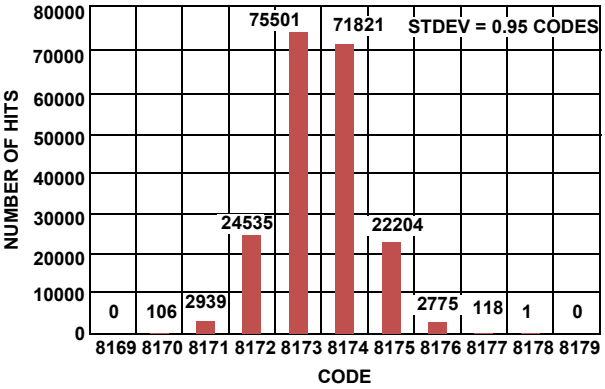


FIGURE 13. NOISE HISTOGRAM

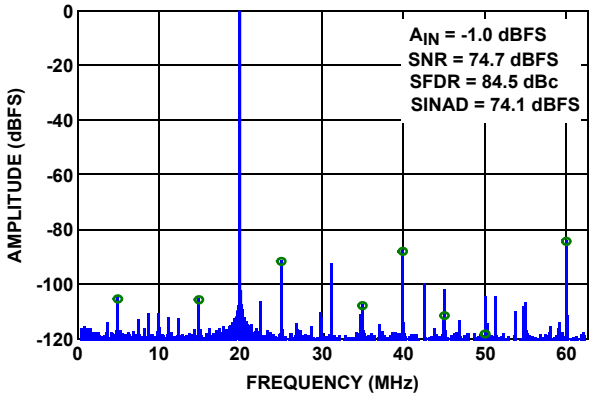


FIGURE 14. SINGLE-TONE SPECTRUM AT 105MHz

Typical Performance Curves

All typical performance characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 125MSPS. **(Continued)**

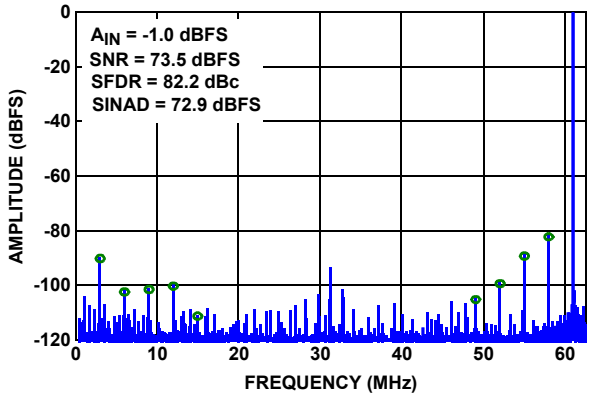


FIGURE 15. SINGLE-TONE SPECTRUM AT 190MHz

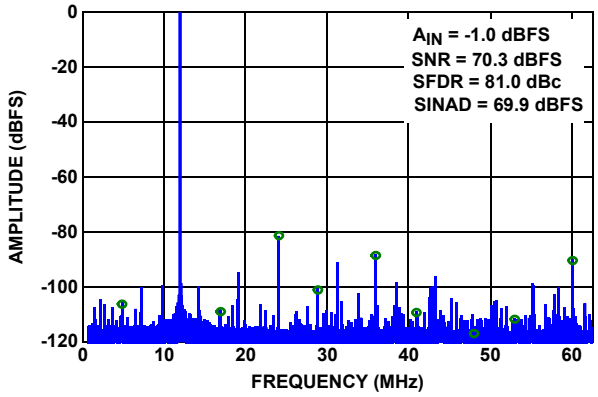


FIGURE 16. SINGLE-TONE SPECTRUM AT 363MHz

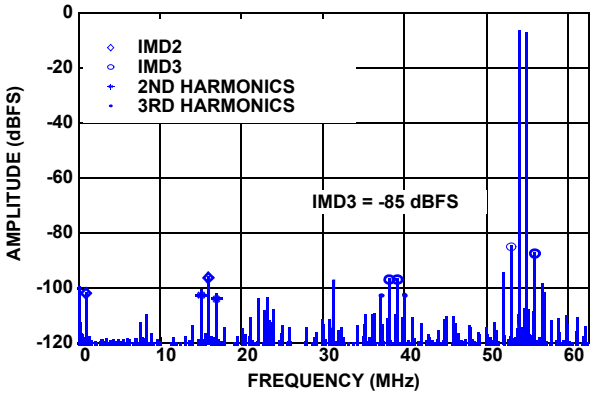


FIGURE 17. TWO-TONE SPECTRUM (F1 = 70MHz, F2 = 71MHz AT -7dBFS)

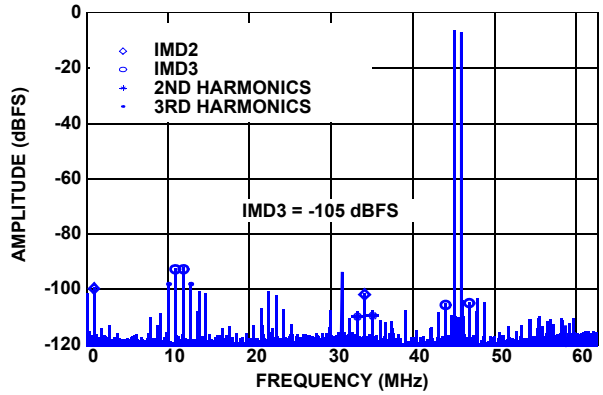


FIGURE 18. TWO-TONE SPECTRUM (F1 = 170MHz, F2 = 171MHz AT -7dBFS)

Theory of Operation

Functional Description

The ISLA214P12 is based on a 14-bit, 125MSPS A/D converter core that uses a pipelined successive approximation architecture (see Figure 19). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied, resulting in a total latency of 10 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

Power-On Calibration

As mentioned previously, the cores perform a self-calibration at start-up. An internal Power-On Reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be followed to for the power-on calibration to execute successfully.

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the previous conditions cannot be met at power-up.

After the power supply has stabilized, the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 20 on page 17. Calibration status can be determined by reading the cal_status bit (LSB) at 0xB6. This bit is ‘0’ during calibration and goes to a logic ‘1’ when calibration is complete. The data outputs produce 0xCCCC during calibration; this can also be used to determine calibration status.

While RESETN is low, the output clock (CLKOUTP/CLKOUTN) is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is de-asserted. At 125MSPS the nominal calibration time is 560ms, while the maximum calibration time is 1000ms.

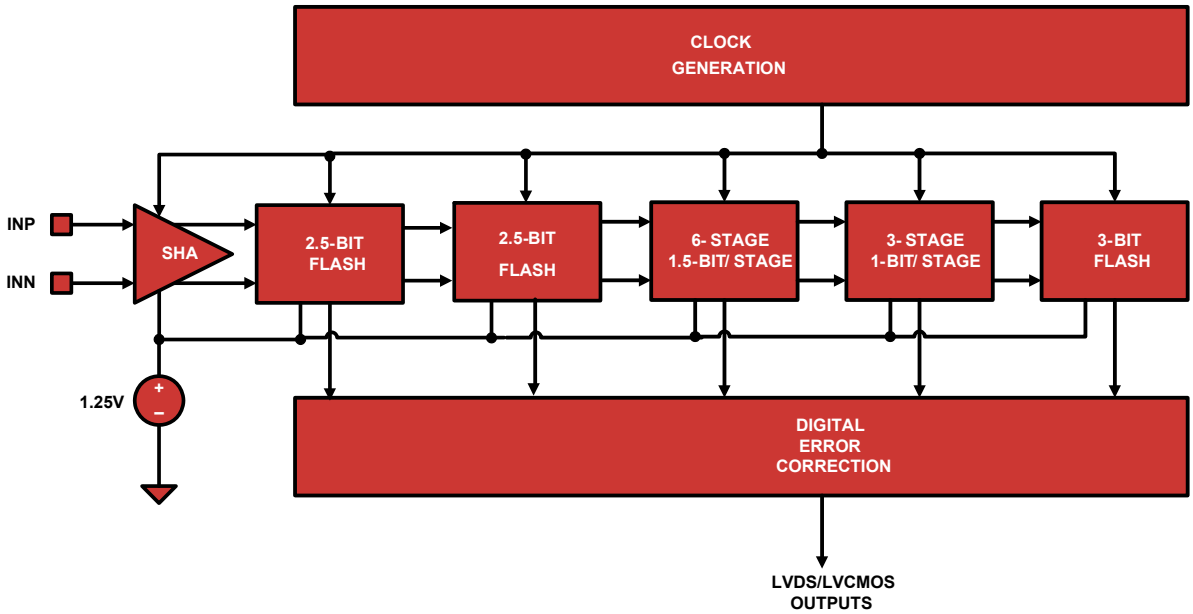


FIGURE 19. A/D CORE BLOCK DIAGRAM

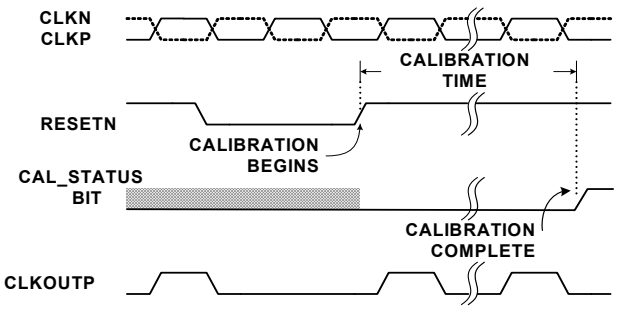


FIGURE 20. CALIBRATION TIMING

User Initiated Reset

Recalibration of the A/D can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA214P12 changes with variations in temperature, supply voltage, or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance is achieved by recalibrating the A/D under the environmental conditions at which it operates.

A supply voltage variation of <100mV generally results in an SNR change of <0.5dBFS and SFDR change of <3dBc.

In situations where the sample rate is not constant, best results are obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS typically results in an SNR change of <0.5dBFS and an SFDR change of <3dBc.

Figures 21 through 26 show the effect of temperature on SNR and SFDR performance with power-on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power-on calibration at -40°C, +25°C, and +85°C. Best performance is typically achieved by a user-initiated power-on calibration at the operating conditions, as stated earlier. However, it can be seen that performance drift with temperature is not a very strong function of the temperature at which the power-on calibration is performed.

Temperature Calibration

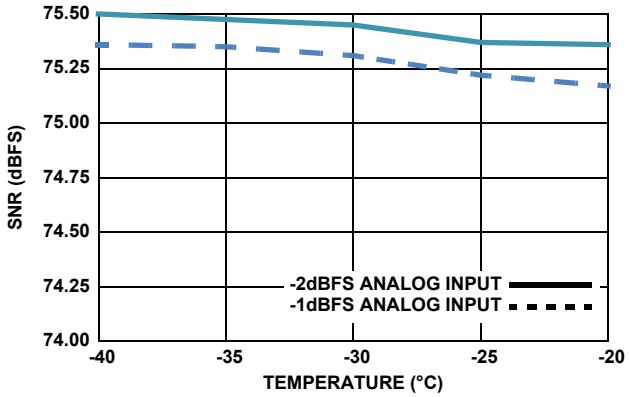


FIGURE 21. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40°C, f_{IN} = 105MHz

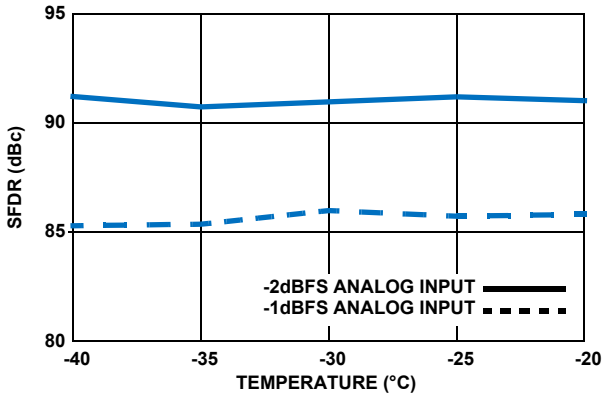


FIGURE 22. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40°C, f_{IN} = 105MHz

Temperature Calibration (Continued)

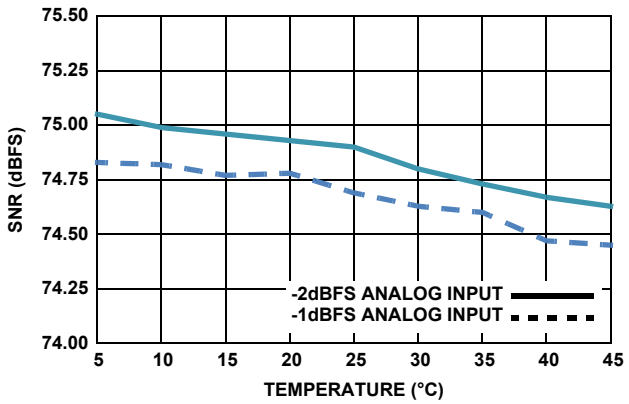


FIGURE 23. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, f_{IN} = 105MHz

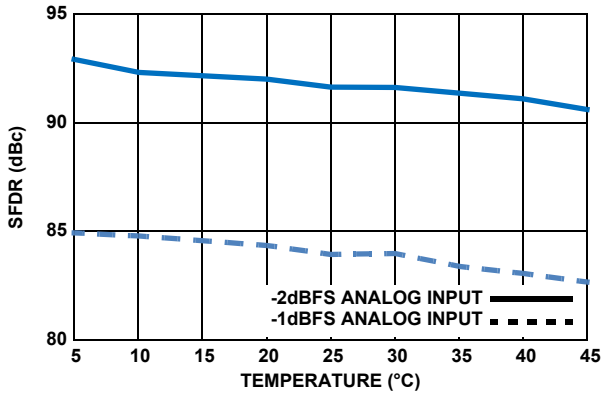


FIGURE 24. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, f_{IN} = 105MHz

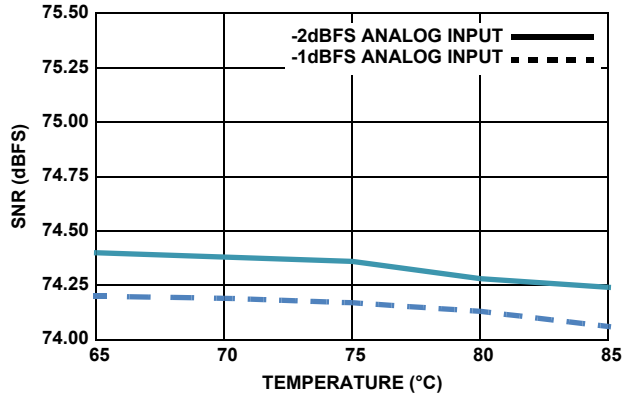


FIGURE 25. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, f_{IN} = 105MHz

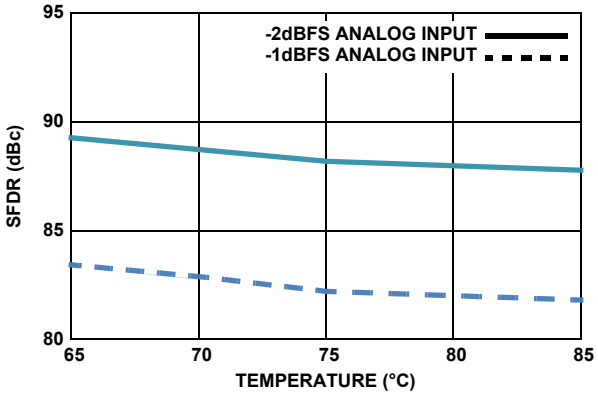


FIGURE 26. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, f_{IN} = 105MHz

Analog Input

A single fully differential input (VINP/VINN) connects to the Sample and Hold Amplifier (SHA) of each unit A/D. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage of 0.94V as shown in Figure 27.

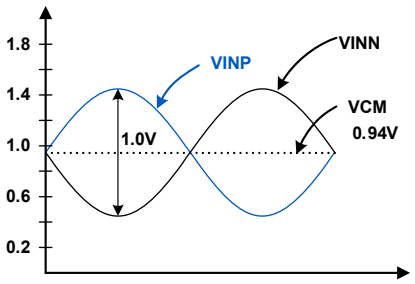


FIGURE 27. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 28 through 30. An RF transformer gives the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 28 and 29.

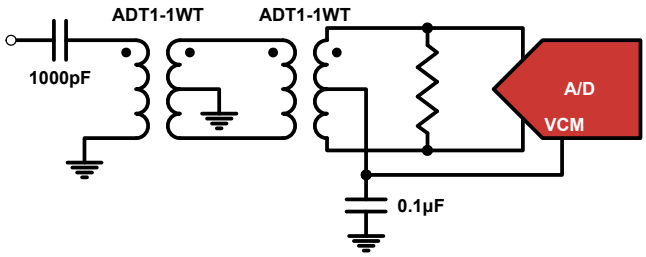


FIGURE 28. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

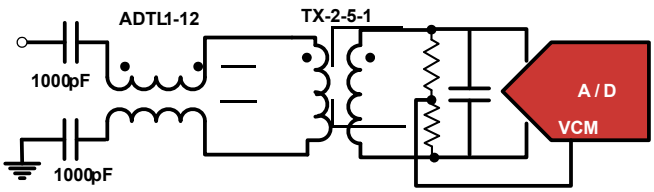


FIGURE 29. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA214P12 is 600Ω.

The SHA design uses a switched capacitor input stage (see Figure 43 on page 30), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the next sampling point. Lower source impedance results in faster settling and improved performance. Therefore a 2:1 or 1:1 transformer and low shunt resistance are recommended for optimal performance.

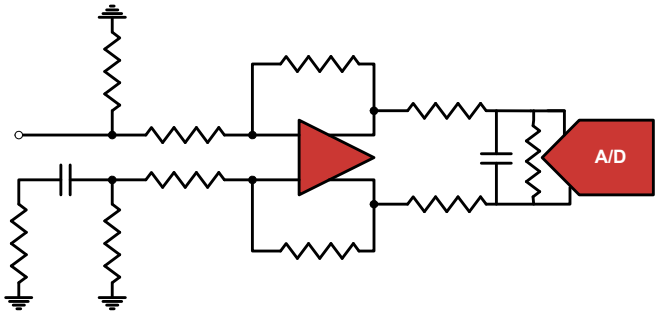


FIGURE 30. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in the simplified block diagram in Figure 30, can be used in applications that require DC-coupling. In this configuration, the amplifier typically dominates the achievable SNR and distortion performance. The ISL552xx differential amplifier family can also be used in certain AC applications with minimal performance degradation.

Clock Input

The clock input circuit is a differential pair (see Figure 44 on page 30). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave provides the lowest jitter performance. A transformer with 4:1 impedance ratio provides increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 31. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this reduces the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate AC coupling.

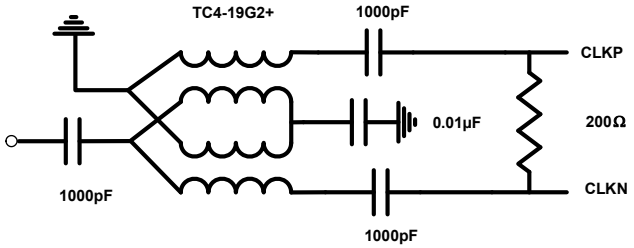


FIGURE 31. RECOMMENDED CLOCK DRIVE

A selectable 2x or 4x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate or in 4x mode with a sample clock equal to four times the desired sample rate. This allows the use of the Phase Slip feature, which enables synchronization of multiple ADCs. The Phase Slip feature can be used as an alternative to using the CLKDIVRST pins to synchronize ADCs in a multiple ADC system.

TABLE 2. CLKDIV PIN SETTINGS

CLKDIV PIN	DIVIDE RATIO
AVSS	2
Float	1
AVDD	4

The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. See "SPI Physical Interface" on page 24 A Delay-Locked Loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to 100µs to regain lock at 125MSPS. The lock time is inversely proportional to the sample rate.

The DLL has two ranges of operation, slow and fast. The slow range can be used for sample rates between 40MSPS and 100MSPS, while the default fast range can be used from 80MSPS to the maximum specified sample rate.

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 32.

$$SNR = 20\log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

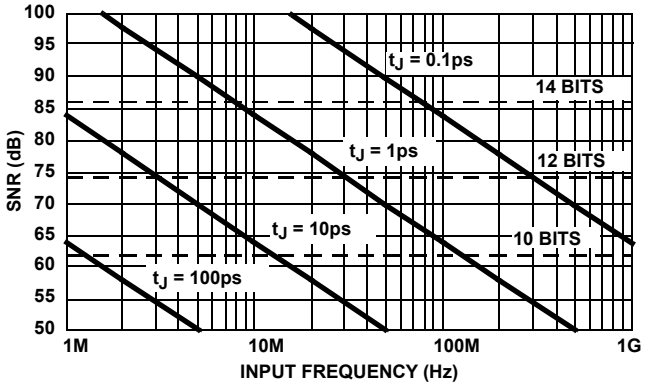


FIGURE 32. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter, and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure 1A on page 10. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

Digital Outputs

Output data is available as a parallel bus in LVDS-compatible (default) or CMOS modes. In either case, the data is presented in either Double Data Rate (DDR) or single data rate (default) format. Figures 1A and 1B show the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3mA (default) or a power-saving 2mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the A/D. The applicability of this setting is dependent upon the PCB layout, therefore the user should experiment to determine if performance degradation is observed. Note that a far-end termination resistor is required in LVDS mode for correct operation.

The output mode can be controlled through the SPI port, by writing to address 0x73, see "Serial Peripheral Interface" on page 24.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDS pin to OVSS.

Over-Range Indicator

The Over-Range (OR) bit is asserted when the magnitude of the analog input exceeds positive or negative fullscale of the ADC. The output code does not wrap around during an over-range condition. The OR bit is updated at the sample rate.

Power Dissipation

The power dissipated by the ISLA214P12 is primarily dependent on the sample rate and the output modes: LVDS vs CMOS and DDR vs SDR. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation changes to a lesser degree in LVDS mode, but is more strongly related to the clock frequency in CMOS mode.

Nap/Sleep

Portions of the device can be shut down to save power during times when operation of the A/D is not required. Two power saving modes are available: Nap and Sleep. Nap mode reduces power dissipation to <60mW while Sleep mode reduces power dissipation to 9mW typically.

All digital outputs (Data, CLKOUT, and OR) are placed in a high impedance state during Nap or Sleep. The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. Recovery time from Nap mode increases if the clock is stopped, since the internal DLL can take up to 100µs to regain lock at 125MSPS.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 3.

TABLE 3. NAPSLP PIN SETTINGS

NAPSLP PIN	MODE
AVSS	Normal
Float	Sleep
AVDD	Nap

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in "Serial Peripheral Interface" on page 24.

Data Format

Output data can be presented in three formats: two's complement (default), Gray code, and offset binary. The data format can be controlled through the SPI port, by writing to address 0x73. Details are shown in "Serial Peripheral Interface" on page 24.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit

position and the next most significant bit. Figure 33 shows this operation.

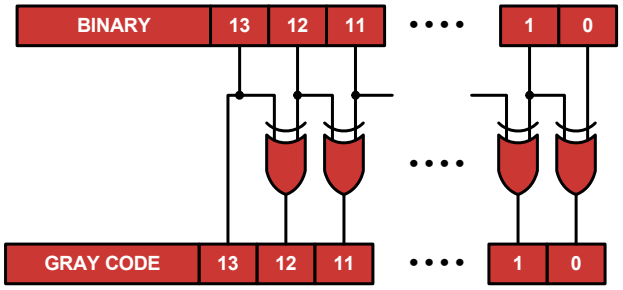


FIGURE 33. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 34.

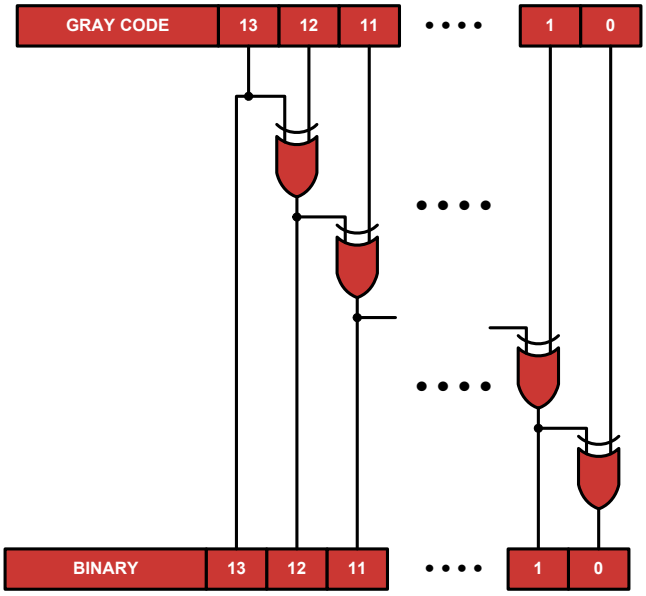


FIGURE 34. GRAY CODE TO BINARY CONVERSION

Mapping of the input voltage to the various data formats is shown in Table 4.

TABLE 4. INPUT VOLTAGE TO OUTPUT CODE MAPPING

INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT	GRAY CODE
–Full Scale	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000
–Full Scale + 1LSB	00 0000 0000 0001	10 0000 0000 0001	00 0000 0000 0001
Mid–Scale	10 0000 0000 0000	00 0000 0000 0000	11 0000 0000 0000
+Full Scale – 1LSB	11 1111 1111 1110	01 1111 1111 1110	10 0000 0000 0001
+Full Scale	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000

Clock Divider Synchronous Reset

An output clock (CLKOUTP, CLKOUTN) is provided to facilitate latching of the sampled data. The output clock frequency is equal to the input clock frequency divided by the internal clock divider setting (see "Clock Input" on page 19).

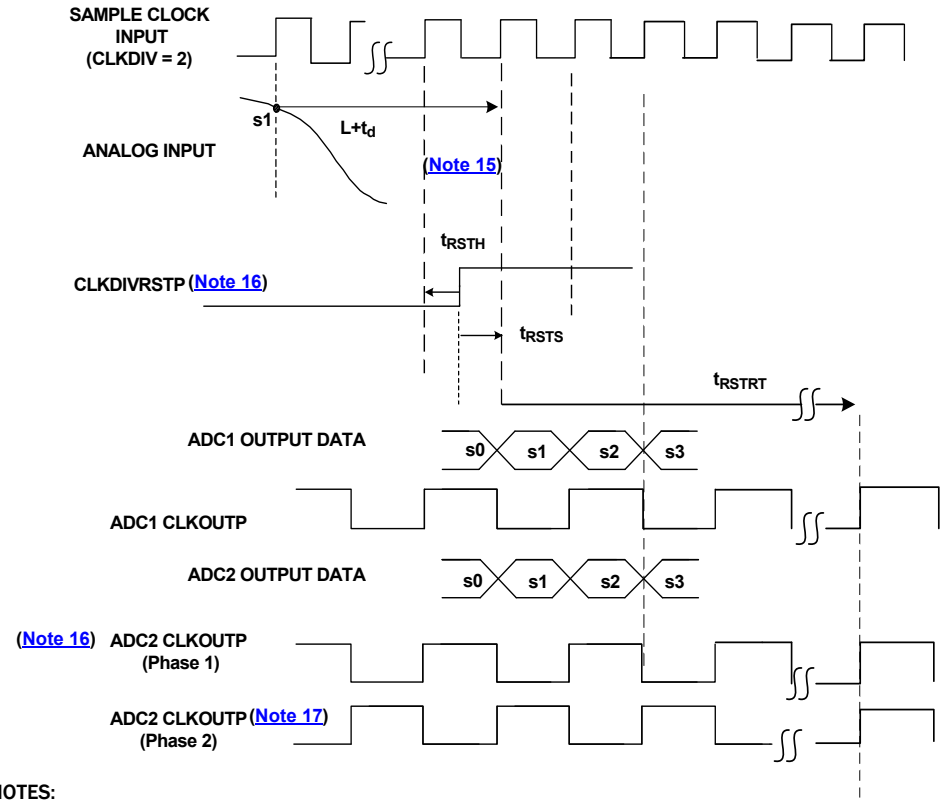
For clock divide settings >'1', the absolute phase of the output clocks for multiple A/Ds is indeterminate - there is a phase ambiguity between the output clocks of ADCs in a multiple ADC system. The CLKDIVRST feature allows the phase of multiple A/Ds to be synchronized (see Figure 35 on page 22) when the internal clock divider is used, greatly simplifying data capture in systems employing multiple A/Ds. For clock divide setting = '1', there is no phase ambiguity between clock outputs in a multiple ADC system and CLKDIVRST can be left as a DNC (do not connect).

The CLKDIVRST signal must be well-timed with respect to the sample clock (see "Switching Specifications" on page 12). Figure 35 shows assertion of CLKDIVRSTP by a positive edge (CLKDIVRSTN must be driven but is not shown); CLKDIVRSTP can remain high indefinitely after a synchronization event. CLKDIVRSTP can also be a pulse if needed, with CLKDIVRSTP returning to a logic '0' after assertion; in this case the CLKDIVRST pulse width should be a minimum of three input sample clock periods. In applications where multiple CLKDIVRST pulse events are required, a user should wait a minimum of 30 clock cycles before starting a second CLKDIVRST pulse event.

It takes a maximum of 30 input clock cycles to attain synchronization (t_{RSTRT}) in applications where the input clock is not interrupted. If the input clock is interrupted, CLKOUT is static or indeterminate until synchronization is attained.

In some applications, interrupting the input sample clock briefly (~ 150 cycles max) can simplify the timing requirements for synchronization using CLKDIVRST), in this case the total CLKDIVRST recovery time increases by the number of input clock cycles the sample clock is held static. Valid data is available (after recovery) in all cases after the normal pipeline latency. Assertion of CLKDIVRST resets.

AN1604 describes the synchronization of multiple ISLA1xxP50s. This document discusses the topic of synchronization in more detail and can be used to better understand the ISLA2XXPxx ADCs' operation.



NOTES:

15. Delay equals fixed pipeline latency (L cycles) plus fixed analog propagation delay t_d.
16. CLKDIVRSTP setup and hold times are with respect to input sample clock rising edge. CLKDIVRSTN is not shown, but must be driven, and is the compliment of CLKDIVRSTP.
17. Either Output Clock Phase (Phase 1 or Phase 2) equally likely prior to synchronization.

FIGURE 35. SYNCHRONOUS RESET OPERATION

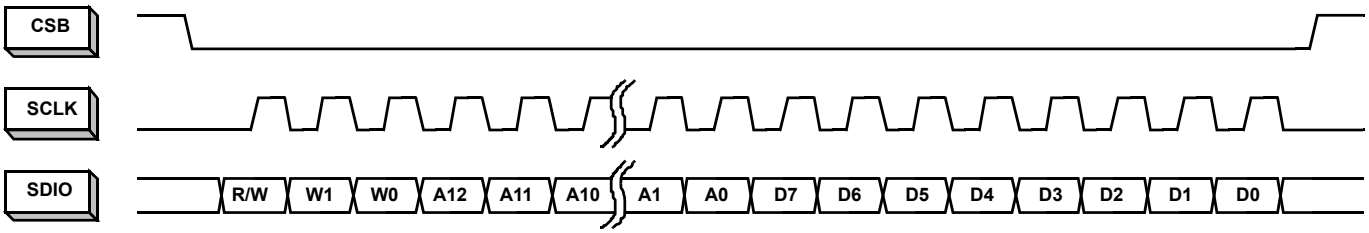


FIGURE 36. MSB-FIRST ADDRESSING

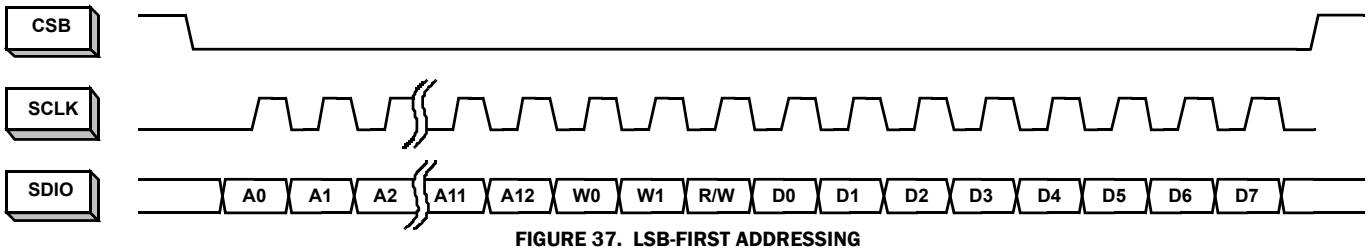


FIGURE 37. LSB-FIRST ADDRESSING

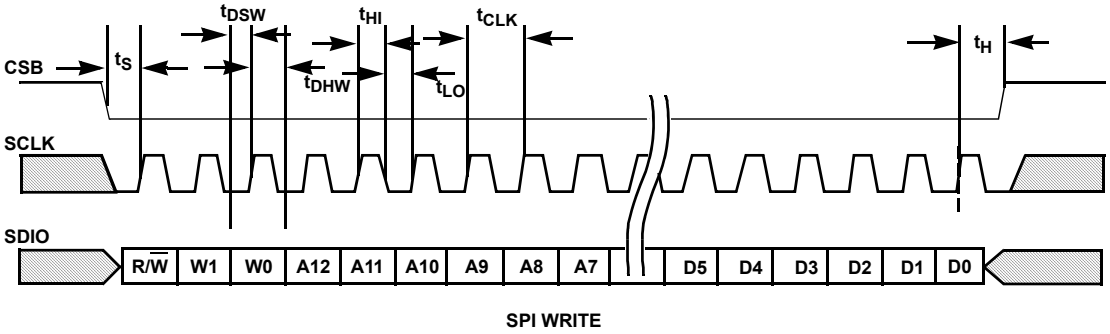


FIGURE 38. SPI WRITE

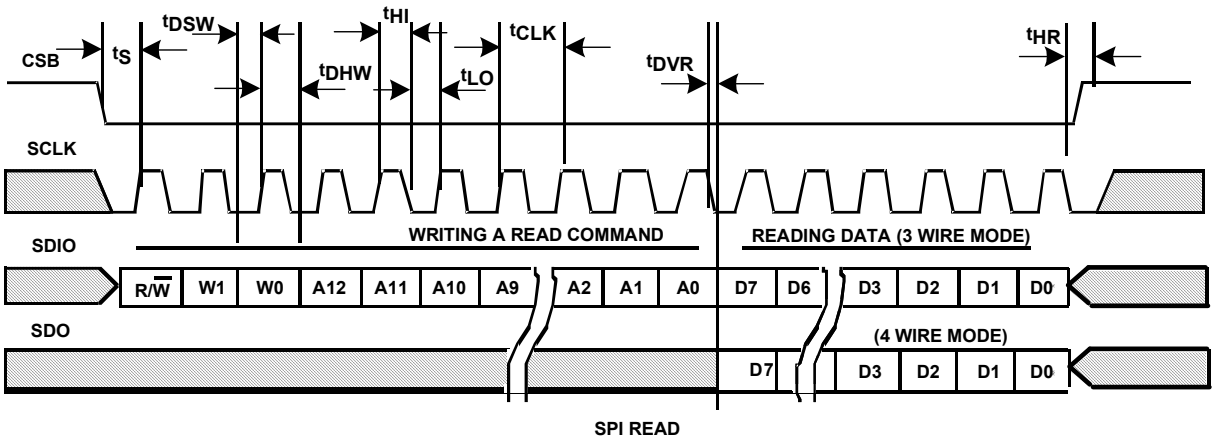


FIGURE 39. SPI READ

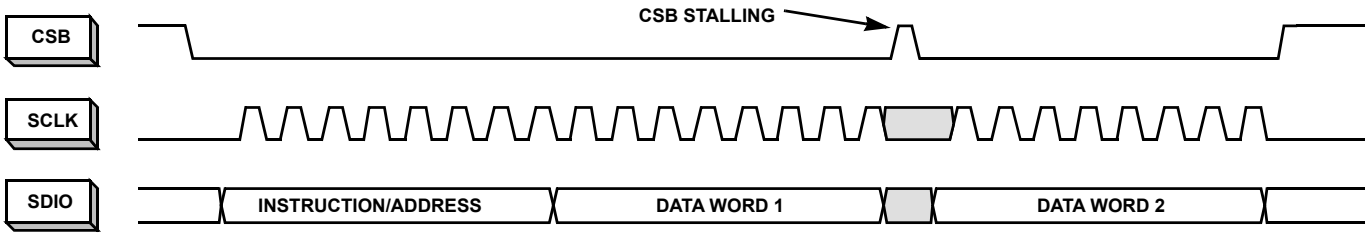


FIGURE 40. 2-BYTE TRANSFER

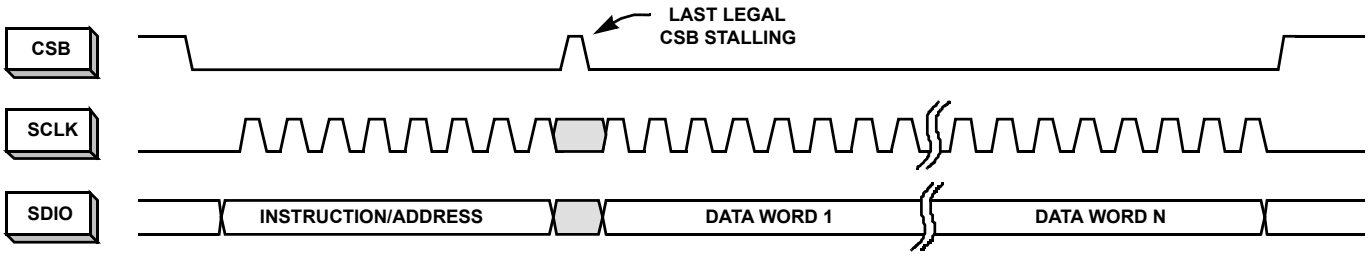


FIGURE 41. N-BYTE TRANSFER

Serial Peripheral Interface

A Serial Peripheral Interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), Serial Clock (SCLK) Serial Data Output (SDO), and Serial Data Input/Output (SDIO). The maximum SCLK rate is equal to the A/D sample rate (f_{SAMPLE}) divided by 16 for both write operations and read operations. At f_{SAMPLE} = 125MHz, maximum SCLK is 7.8125MHz for writing and read operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

SPI Physical Interface

The SCLK pin provides synchronization for the data transfer. By default, all data is presented on the SDIO pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated SDO pin can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ISLA214P12 functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The Chip-Select Bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results are indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high-to-low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 36 and 37 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it is decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 5). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 38, and timing values are given in “Switching Specifications” on page 12.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the A/D (based on the R/W bit status). The data transfer continues as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine resets and terminates the data transfer.

TABLE 5. BYTE TRANSFER SELECTION

[W1:W0]	BYTES TRANSFERRED
00	1
01	2
10	3
11	4 or more

Figures 40 and 41 on page 23 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

SPI Configuration

ADDRESS 0X00: CHIP_PORT_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various microcontrollers.

Bit 7 SDO Active

Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved

This bit should always be set high.

Bits 3:0 These bits should always mirror Bits 4:7 to avoid ambiguity in bit ordering.

ADDRESS 0X02: BURST_END

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. The burst is ended by pulling the CSB pin high. Setting the burst_end address determines the end of the transfer; during a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.

Device Information

ADDRESS 0X08: CHIP_ID

ADDRESS 0X09: CHIP_VERSION

The generic die identifier and a revision number, respectively, can be read from these two registers.

Device Configuration/Control

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Renesas A/D products. Single core ADCs use ADC0, while multiple-core devices use both ADC0 and ADC1.

ADDRESS 0X20: OFFSET_COARSE_ADC0

ADDRESS 0X21: OFFSET_FINE_ADC0

The input offset of the A/D core can be adjusted in fine and coarse steps. Both adjustments are made using an 8-bit word as detailed in Table 6. The data format is twos complement. Bit 0 in register 0xFE must be set high to enable updates written to 0x20 and 0x21 to be used by the ADC (see "Address 0xFE: OFFSET/GAIN_ADJUST_Enable" on page 27).

The default value of each register is the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 6. OFFSET ADJUSTMENTS

PARAMETER	0x20[7:0] COARSE OFFSET	0x21[7:0] FINE OFFSET
Steps	255	255
–Full Scale (0x00)	-133LSB (-47mV)	-5LSB (-1.75mV)
Mid–Scale (0x80)	0.0LSB (0.0mV)	0.0LSB
+Full Scale (0xFF)	+133LSB (+47mV)	+5LSB (+1.75mV)
Nominal Step Size	1.04LSB (0.37mV)	0.04LSB (0.014mV)

ADDRESS 0X22: GAIN_COARSE_ADC0

ADDRESS 0X23: GAIN_MEDIUM_ADC0

ADDRESS 0X24: GAIN_FINE_ADC0

Gain of the A/D core can be adjusted in coarse, medium, and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple coarse gain bits can be set for a total adjustment range of ±4.2%. ('0011' ≅ -4.2% and '1100' ≅ +4.2%) It is recommended to use one of the coarse gain settings (-4.2%, -2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 0x23 and 0x24.

The default value of each register is the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, you should first read the register value then write the incremented or decremented value back to the same register. Bit 0 in register 0xFE must be set high to enable updates written to 0x23 and 0x24 to be used by the ADC (see "Address 0xFE: OFFSET/GAIN_ADJUST_Enable" on page 27).

TABLE 7. COARSE GAIN ADJUSTMENT

0x22[3:0] core 0	NOMINAL COARSE GAIN ADJUST (%)
Bit3	+2.8
Bit2	+1.4
Bit1	-2.8
Bit0	-1.4

TABLE 8. MEDIUM AND FINE GAIN ADJUSTMENTS

PARAMETER	0x23[7:0] MEDIUM GAIN	0x24[7:0] FINE GAIN
Steps	256	256
–Full Scale (0x00)	-2%	-0.20%
Mid–Scale (0x80)	0.00%	0.00%
+Full Scale (0xFF)	+2%	+0.2%
Nominal Step Size	0.016%	0.0016%

ADDRESS 0X25: MODES

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, Nap, or Sleep modes (refer to"Nap/Sleep" on page 20). This functionality can be overridden and controlled through the SPI. This is an indexed function when controlled from the SPI, but a global function when driven from the pin. This register is not changed by a soft reset.

TABLE 9. POWER-DOWN CONTROL

VALUE	0x25[2:0] POWER DOWN MODE
000	Pin Control
001	Normal Operation
010	Nap Mode
100	Sleep Mode

Global Device Configuration/Control

ADDRESS 0X71: PHASE_SLIP

The output data clock is generated by dividing down the A/D input sample clock. Some systems with multiple A/Ds can more easily latch the data from each A/D by controlling the phase of the output data clock. This control is accomplished through the use of the phase_slip SPI feature, which allows the rising edge of the output data clock to be advanced by one input clock period, as shown in the Figure 42 on page 26. Execution of a phase_slip command is accomplished by first writing a '0' to bit 0 at address 0x71, followed by writing a '1' to bit 0 at address 0x71.

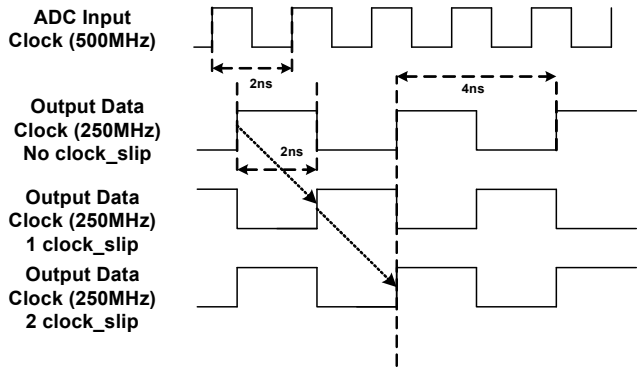


FIGURE 42. PHASE SLIP

ADDRESS 0X72: CLOCK_DIVIDE

The ISLA214P12 has a selectable clock divider that can be set to divide by four, two, or one (no division). By default, the tri-level CLKDIV pin selects the divisor. This functionality can be overridden and controlled through the SPI, as shown in Table 10. This register is not changed by a soft reset.

TABLE 10. CLOCK DIVIDER SELECTION

VALUE	0x72[2:0] CLOCK DIVIDER
000	Pin Control
001	Divide by 1
010	Divide by 2
100	Divide by 4
other	Not Allowed

ADDRESS 0X73: OUTPUT_MODE_A

The output_mode_A register controls the physical output format of the data, as well as the logical coding. The ISLA214P12 can present output data in two physical formats: LVDS (default) or LVCMOS. Additionally, the drive strength in LVDS mode can be set high (default, 3mA or low (2mA).

TABLE 11. OUTPUT MODE CONTROL

VALUE	0x73[7:5] OUTPUT MODE
000	LVDS 3mA (Default)
001	LVDS 2mA
100	LVCMOS

Data can be coded in three possible formats: two's complement (default), Gray code, or offset binary, see Table 12.

This register is not changed by a soft reset.

TABLE 12. OUTPUT FORMAT CONTROL

VALUE	0x73[2:0] OUTPUT FORMAT
000	Two's Complement (Default)
010	Gray Code
100	Offset Binary

ADDRESS 0X74: OUTPUT_MODE_B

Bit 6 DLL Range

This bit sets the DLL operating range to fast (default) or slow.

Internal clock signals are generated by a delay-locked loop (DLL), which has a finite operating range. Table 13 shows the allowable sample rate ranges for the slow and fast settings.

Bit 4 DDR Enable

Set to a '1' to enable DDR.

TABLE 13. DLL RANGES

DLL RANGE	MIN	MAX	UNIT
Slow	40	100	MSPS
Fast	80	125	MSPS

ADDRESS 0XB6: CALIBRATION STATUS

The LSB at address 0xB6 can be read to determine calibration status. The bit is '0' during calibration and goes to a logic '1' when calibration is complete. This register is unique in that it can be read after POR at calibration, unlike the other registers on chip, which can't be read until calibration is complete.

DEVICE TEST

The ISLA214P12 can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A user can pick from preset built-in patterns by writing to the output test mode field [7:4] at 0xC0 or user defined patterns by writing to the user test mode field [2:0] at 0xC0. The user defined patterns should be loaded at address space 0xC1 through 0xD0, see the "SPI Memory Map" on page 27 for more detail. The predefined patterns are shown in Table 14 on page 27. The test mode is enabled asynchronously to the sample clock, therefore several sample clock cycles may elapse before the data is present on the output bus.

ADDRESS 0XC0: TEST_IO

Bits 7:4 Output Test Mode

These bits set the test mode according to Table 14. Other values are reserved. User test patterns loaded at 0xC1 through 0xD0 are also available by writing '1000' to [7:4] at 0xC0 and a pattern depth value to [2:0] at 0xC0. See the memory map.

Bits 2:0 User Test Mode

The three LSBs in this register determine the test pattern in combination with registers 0xC1 through 0xD0, see the SPI Memory Map on page 27.

TABLE 14. OUTPUT TEST MODES

VALUE	0xC0[7:4] OUTPUT TEST MODE	WORD 1	WORD 2
0000	Off		
0001	Midscale	0x8000	N/A
0010	Positive Full-Scale	0xFFFF	N/A
0011	Negative Full-Scale	0x0000	N/A
0100	SDR/DDR Dependent	N/A	N/A
0101	Reserved	N/A	N/A
0110	Reserved	N/A	N/A
0111	SDR/DDR Dependent	N/A	N/A
1000	User Pattern	user_patt1	user_patt2
1001	Reserved	N/A	N/A
1010	Ramp	N/A	N/A

ADDRESS 0XC1: USER_PATT1_LSB

ADDRESS 0XC2: USER_PATT1_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 1.

ADDRESS 0XC3: USER_PATT2_LSB

ADDRESS 0XC4: USER_PATT2_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 2.

ADDRESS 0XC5: USER_PATT3_LSB

ADDRESS 0XC6: USER_PATT3_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 3.

ADDRESS 0XC7: USER_PATT4_LSB

ADDRESS 0XC8: USER_PATT4_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 4.

ADDRESS 0XC9: USER_PATT5_LSB

ADDRESS 0XCA: USER_PATT5_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 5.

ADDRESS 0XCB: USER_PATT6_LSB

ADDRESS 0XCC: USER_PATT6_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 6.

ADDRESS 0XCD: USER_PATT7_LSB

ADDRESS 0XCE: USER_PATT7_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 7.

ADDRESS 0XCF: USER_PATT8_LSB

ADDRESS 0XD0: USER_PATT8_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined Pattern 8.

ADDRESS 0XFE: OFFSET/GAIN_ADJUST_ENABLE

Bit 0 at this register must be set high to enable adjustment of offset coarse and fine adjustments (0x20 and 0x21) and gain medium and gain fine adjustments (0x23 and 0x24). It is recommended that new data be written to the offset and gain adjustment registers (0x20, 0x21, 0x23, 0x24) while Bit 0 is a ‘0’. Subsequently, Bit 0 should be set to ‘1’ to allow the values written to the aforementioned registers to be used by the ADC. Bit 0 should be set to a ‘0’ upon completion.

SPI Memory Map

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (Hex)
SPI Config/Control	00	Port_config	SDO Active	LSB First	Soft Reset			Mirror (Bit 5)	Mirror (Bit 6)	Mirror (Bit 7)	00h
	01	Reserved	Reserved								
	02	Burst_end	Burst end address [7:0]								00h
	03-07	Reserved	Reserved								
DUT Info	08	Chip_id	Chip ID #								Read only
	09	Chip_version	Chip Version #								Read only
	0A-0F	Reserved	Reserved								

SPI Memory Map (Continued)

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (Hex)
Device Config/Control	10-1F	Reserved	Reserved								
	20	Offset_coarse_adc0	Coarse Offset								cal. value
	21	Offset_fine_adc0	Fine Offset								cal. value
	22	Gain_coarse_adc0	Reserved				Coarse Gain				cal. value
	23	Gain_medium_adc0	Medium Gain								cal. value
	24	Gain_fine_adc0	Fine Gain								cal. value
	25	Modes_adc0	Reserved					Power Down Mode ADC0 [2:0] 000 = Pin Control 001 = Normal Operation 010 = Nap 100 = Sleep Other codes = Reserved			00h NOT reset by Soft Reset
	26	Offset_coarse_adc1	Coarse Offset								cal. value
	27	Offset_fine_adc1	Fine Offset								cal. value
	28	Gain_coarse_adc1	Reserved				Coarse Gain				cal. value
	29	Gain_medium_adc1	Medium Gain								cal. value
	2A	Gain_fine_adc1	Fine Gain								cal. value
	2B	Modes_adc1	Reserved					Power Down Mode ADC1 [2:0] 000 = Pin Control 001 = Normal Operation 010 = Nap 100 = Sleep Other codes = Reserved			00h NOT reset by Soft Reset
	2C-2F	Reserved	Reserved								
	33-4A	Reserved	Reserved								
	4B	Reserved						Reserved			Read only
	4C	Reserved	Reserved								Read only
	4D	Reserved		Enable	PD	Reset	Divider [2:0]			Select	00h
	4E-6F	Reserved	Reserved								
	70	Skew_diff	Differential Skew								80h
	71	Phase_slip	Reserved							Next Clock Edge	00h
	72	Clock_divide						Clock Divide [2:0] 000 = Pin Control 001 = Divide by 1 010 = Divide by 2 100 = Divide by 4 Other codes = Reserved			00h NOT reset by Soft Reset
Device Config/Control	73	Output_mode_A	Output Mode [7:5] 000 = LVDS 3mA (Default) 001 = LVDS 2mA 100 = LVCMOS Other codes = Reserved					Output Format [2:0] 000 = Two's Complement (Default) 010 = Gray Code 100 = Offset Binary Other codes = Reserved			00h NOT reset by Soft Reset
	74	Output_mode_B		DLL Range 0 = Fast 1 = Slow Default = '0'		DDR Enable					00h NOT reset by Soft Reset
	75-B5	Reserved	Reserved								
	B6	Cal_status								Calibration Done	Read Only
	B7-BF	Reserved									

SPI Memory Map (Continued)

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (Hex)
Device Test	C0	Test_io	Output Test Mode [7:4]					User Test Mode [2:0]			00h
			Part in SDR Mode 0 = Off (Note 15) 1 = Midscale Short 2 = +FS Short 3 = -FS Short 4 = Checkerboard Output (0xAAAA, 0x5555) (Note 16) 7 = 0xFFFF, 0x0000 all on pattern (Note17) 8 = User Pattern (1 to 8 deep, MSB Justified) 10 = Ramp 5, 6, 9, 11-15 = Reserved **Part in DDR Mode** 0 = Off (Note 15) 1 = Midscale Short 2 = +FS Short 3 = -FS Short 4 = Reserved (Note 16) 7 = Reserved (Note 17) 8 = User Pattern (1 to 4 deep, MSB Justified) 10 = Ramp 5, 6, 9, 11-15 = Reserved					**Part in SDR Mode** 0 = User pattern 1 only 1 = Cycle pattern 1 through 2 2 = Cycle pattern 1 through 3 3 = Cycle pattern 1 through 4 4 = Cycle pattern 1 through 5 5= Cycle pattern 1 through 6 6 = Cycle pattern 1 through7 7 = Cycle pattern 1 through 8 **Part in DDR Mode** 0 = User pattern 1 only 1 = Cycle pattern 1,3 2 = Cycle pattern 1,3,5 3 = Cycle pattern 1,3,5,7 4-7 = NA			
	C1	User_patt1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	0x00
	C2	User_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C3	User_patt2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C4	User_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C5	User_patt3_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C6	User_patt3_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C7	User_patt4_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C8	User_patt4_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C9	User_patt5_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CA	User_patt5_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CB	User_patt6_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CC	User_patt6_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CD	User_patt7_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CE	User_patt7_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CF	User_patt8_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	D0	User_patt8_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	D1-FD	Reserved	Reserved								
	FE	Offset/Gain_Adjust_Enable	Reserved							Enable '1' = Enable	00h
	FF	Reserved	Reserved								

NOTES:

15. During Calibration xCCCC (MSB justified) is presented at the output data bus, toggling on the LSB (and higher) data bits occurs at completion of calibration. This behavior can be used as an option to determine calibration state.
16. Use test_io = 0x80 and User Pattern 1 = 0x9999 for Checkerboard outputs in DDR mode. In SDR mode, write '0x41' to test_io for Checkerboard outputs.
17. Use test_io = 0x80 and User Pattern 1 = 0xAAAA for all ones/zeroes outputs in DDR mode. In SDR mode, write '0x71' to test_io for all ones/zeroes outputs.

Equivalent Circuits

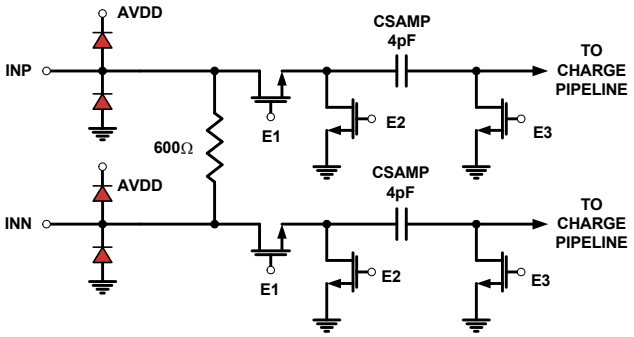


FIGURE 43. ANALOG INPUTS

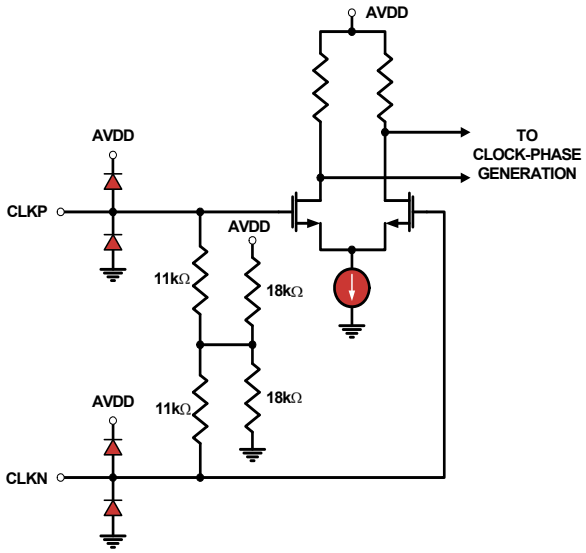


FIGURE 44. CLOCK INPUTS

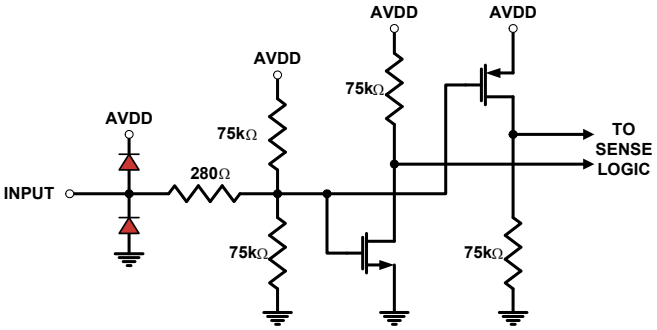


FIGURE 45. TRI-LEVEL DIGITAL INPUTS

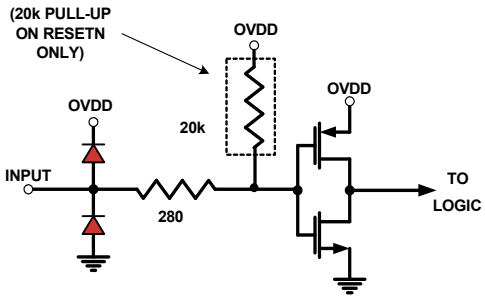


FIGURE 46. DIGITAL INPUTS

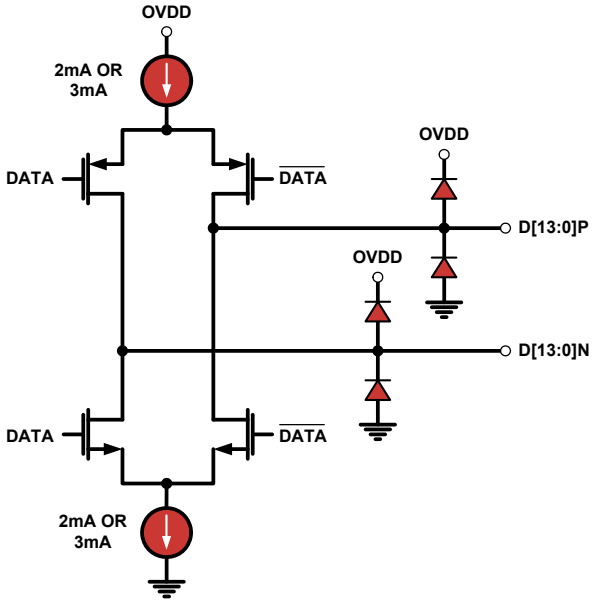


FIGURE 47. LVDS OUTPUTS

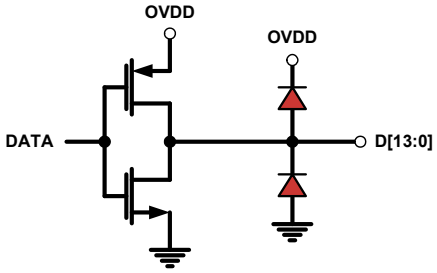


FIGURE 48. CMOS OUTPUTS

Equivalent Circuits (Continued)

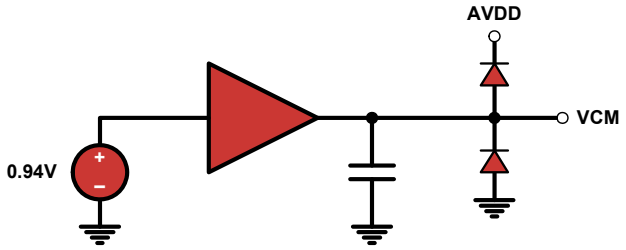


FIGURE 49. VCM_OUT OUTPUT

A/D Evaluation Platform

Renesas offers an A/D Evaluation platform which can be used to evaluate any of Renesas's high speed A/D products. The platform consists of an FPGA based data capture motherboard and a family of A/D daughtercards. This USB based platform allows a user to quickly evaluate the A/D's performance at a user's specific application frequency requirements. More information is available on our website.

Layout Considerations

Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins. Longer traces increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

LVDS Outputs

Output traces and connections must be designed for 50Ω (100Ω differential) characteristic impedance. Keep traces direct and minimize bends where possible. Avoid crossing ground and power-plane breaks with signal traces.

LVCMOS Outputs

Output traces and connections must be designed for 50Ω characteristic impedance.

Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which are not operated do not require connection to ensure optimal A/D performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP) accept a floating input as a valid state, and therefore should be biased according to the desired functionality.

Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.

Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD - 1.76)/6.02

Gain Error is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage less than 2 LSB. It is typically expressed in percent.

I2E The Interleave Engine. This highly configurable circuitry performs estimates of offset, gain, and sample time skew mismatches between the core converters, and updates analog adjustments for each to minimize interleave spurs.

Integral Non-Linearity (INL) is the maximum deviation of the A/D's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N-1)$ where N is the resolution in bits.

Missing Codes are output codes that are skipped and never appear at the A/D output. These codes cannot be reached with any input value.

Most Significant Bit (MSB) is the bit that has the largest value or weight.

Pipeline Delay is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

Power Supply Rejection Ratio (PSRR) is the ratio of the observed magnitude of a spur in the A/D FFT, caused by an AC signal superimposed on the power supply voltage.

Signal to Noise-and-Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

Signal-to-Noise Ratio (without Harmonics) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

SNR and SINAD are either given in units of dB when the power of the fundamental is used as the reference, or dBFS (dB to full scale) when the converter's full-scale input power is used as the reference.

Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the largest spurious spectral component. The largest spurious spectral component may or may not be a harmonic.

Revision History

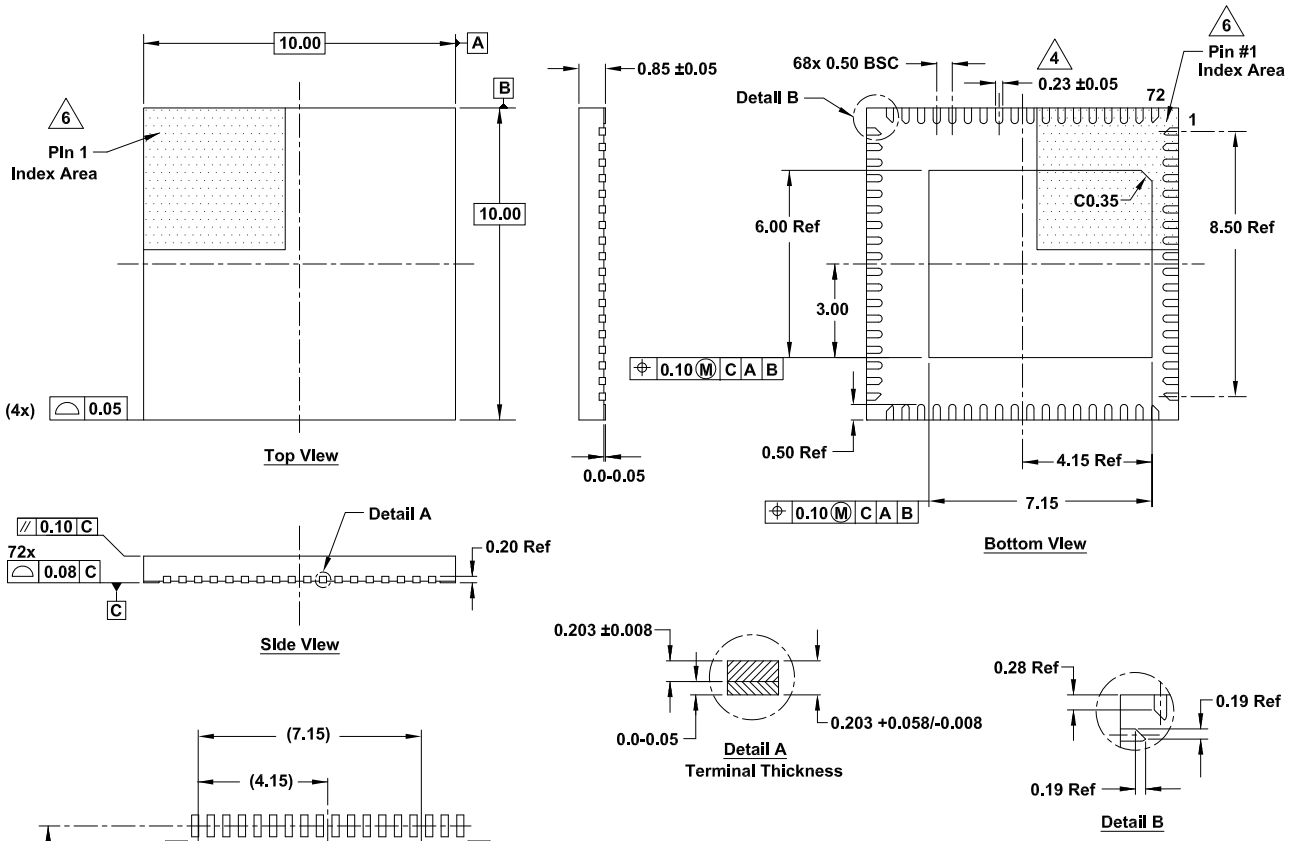
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
Jul 6, 2021	4.0	Updated links throughout. Removed Related Literature section. Updated Ordering Information table format and updated applicable notes. Changed POD from L72.10x10E to L72.10x10G.
Nov 29, 2018	3.0	Applied new formatting standards throughout document. Updated features list Updated fist paragraph on page 1. Added related literature section. Added ESD rating information. Updated revision history section. Removed products section. Updated disclaimer.
Jun 27, 2012	2.0	Removed DNL Min Spec from Spec Table on Page 9.
May 25, 2012	1.0	Removed Max spec "1.4" in Differential Nonlinearity
Mar 27, 2012	0.0	Initial Release

Package Outline Drawing

For the most recent package outline drawing, see L72.10x10G.

L72.10x10G
72 Lead Quad Flat No-Lead Plastic Package (QFN)
Rev 0, 4/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.10
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Package outline compliant to JESD-M0220.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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