ISL26102, ISL26104

Low-Noise 24-bit Delta Sigma ADC

FN7608
Rev 0.00
October 12, 2012

The ISL26102 and ISL26104 provide a low-noise programmable gain amplifier along with a 24-bit Delta-Sigma Analog-to-Digital Converter with two channel (ISL26102) or four channel (ISL26104) differential, multiplexed inputs. The devices feature exceptional noise performance for conversion rates ranging from 2.5Sps to 4kSps.

The on-chip low-noise programmable-gain amplifier provides gains ranging from 1 to 128, which supports ±19.5mVFS from a 5V reference. The high input impedance allows direct connection of sensors such as load cell bridges to ensure the specified measurement accuracy without additional circuitry.

The Delta-Sigma ADC features a 3rd-order modulator providing up to 21.5 bit noise-free performance (10Sps), with user-selectable word rates. The converter can be operated from an external clock source, an external crystal (typically 4.9152MHz), or the on-chip oscillator.

The ISL26102 and ISL26104 offer a simple-to-use serial interface.

The ISL26102 and ISL26104 are available in a Thin Shrink Small Outline Package (TSSOP). The devices are specified for operation over the automotive temperature range (-40°C to +105°C).

Features

- Programmable gain amplifier with gains of 1 to 128
- Low noise: 7nV/√Hz @ PGA = 128
- Linearity error: 0.0002% FS
- Output word rates up to 4kSps
- Low-side switch for load cell power management
- +5V analog and +2.7V to +5V digital supplies
- ISL26102 in 24 Ld TSSOP
- ISL26104 in 28 Ld TSSOP
- ESD 7.5kV - HBM

Applications

- Weigh scales
- Temperature monitors and controls
- Load safety systems
- Industrial process control
- Pressure sensors

Related Literature

AN1704, "Precision Signal Path Data Acquisition System"

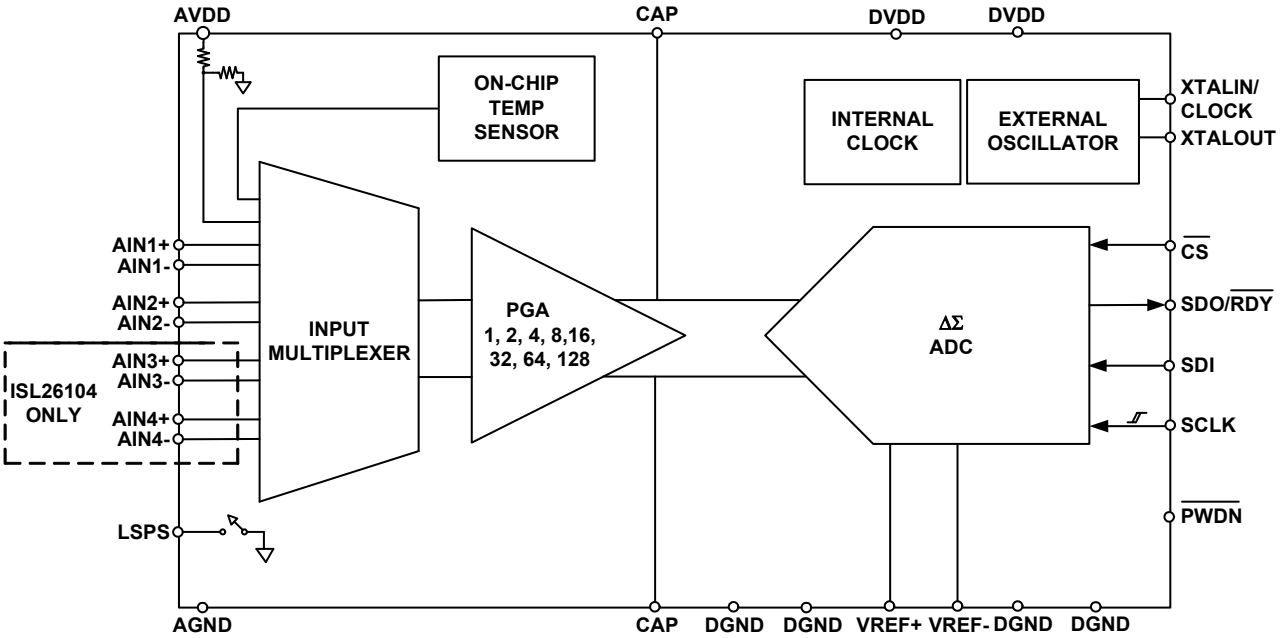


FIGURE 1. BLOCK DIAGRAM

Ordering Information

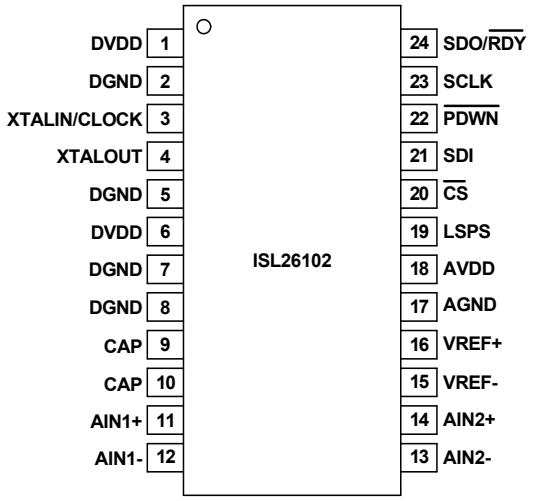
PART NUMBER (Notes 1, 2, 3)	PART MARKING	DESCRIPTION	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL26102AVZ	26102 AVZ	2 Channel ADC	-40 to +105	24 Ld TSSOP	M24.173
ISL26104AVZ	26104 AVZ	4 Channel ADC	-40 to +105	28 Ld TSSOP	M28.173
ISL26104AV28EV1Z	Evaluation Board				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pbfree products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL26102, ISL26104. For more information on MSL please see techbrief TB363.

Pin Configurations

ISL26102
(24 LD TSSOP)
TOP VIEW



ISL26104
(28 LD TSSOP)
TOP VIEW

Pin Descriptions (TSSOP)

PIN NAME	PIN NUMBER		ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
	ISL26102	ISL26104		
DVDD	1, 6	1, 6	Digital	Digital Power Supply (2.7V to 5.25V)
DGND	2, 5, 7, 8	2, 5, 7, 8	Digital	Digital Ground
XTALIN/CLOCK	3	3	Digital/Digital Input	External Clock Input: Typically 4.9152MHz. Tie low to activate internal oscillator. Can also use external crystal across XTALIN/CLOCK and XTALOUT pins.
XTALOUT	4	4	Digital	External Crystal Connection
CAP	9, 10	9, 10	Analog	PGA Filter Capacitor
AIN1+	11	11	Analog Input	Positive Analog Input Channel 1
AIN1-	12	12	Analog Input	Negative Analog Input Channel 1
AIN3+	-	13	Analog Input	Positive Analog Input Channel 3
AIN3-	-	14	Analog Input	Negative Analog Input Channel 3
AIN4-	-	15	Analog Input	Negative Analog Input Channel 4
AIN4+	-	16	Analog Input	Positive Analog Input Channel 4
AIN2-	13	17	Analog Input	Negative Analog Input Channel 2
AIN2+	14	18	Analog Input	Positive Analog Input Channel 2
VREF-	15	19	Analog Input	Negative Reference Input
VREF+	16	20	Analog Input	Positive Reference Input
AGND	17	21	Analog Input	Analog Ground
AVDD	18	22	Analog Input	Analog Power Supply 4.75V to 5.25V
LSPS	19	23	Digital Output	Low-Side Power Switch (Open Drain)
$\overline{CS}$	20	24	Digital Input	Chip Select (Active Low)
SDI	21	25	Digital Input	Serial Data Input
$\overline{PDWN}$	22	26	Digital Input	Device Power Down (Active Low)
SCLK	23	27	Digital Input	Serial Port Clock
SDO/$\overline{RDY}$	24	28	Digital Output	Data Ready signal (conversion complete) and Serial Data Output

Absolute Maximum Ratings

A_{GND} to D_{GND} . . . . . -0.3V to +0.3V
Analog In to A_{GND} . . . . . -0.3 to A_{VDD}+0.3V
Digital In to D_{GND} . . . . . -0.3 to D_{VDD}+0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 7.5kV
Machine Model (Per JESD22-A115) 450V
Charged Device Model (Per JESD22-C101) 2000V
Input Current
Momentary 100mA
Continuous 10mA
Latch-up
(Per JEDEC, JESD-78C; Class 2, Level A) . . . . 100mA @ +25°C and +105°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld TSSOP Package (Notes 4, 5)	65	18
28 Ld TSSOP Package (Notes 4, 5)	63	18

Maximum Power Dissipation 80mW
Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C

Operating Conditions

Temperature Range . . . . . -40°C to +105°C
A_{VDD} to A_{GND} . . . . . 4.75V to +5.25V
D_{VDD} to D_{GND} . . . . . 2.7V to +5.25V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{REF}+ = 5.0V, V_{REF}- = 0V, A_{VDD} = 5V, D_{VDD} = 5V XTALIN/CLOCK = 4.9152MHz (Note 6) T_A = -40°C to +105°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

SYMBOL	PARAMETER	TEST LEVEL OR NOTES	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
ANALOG INPUTS						
V_{IN}	Differential Input Voltage Range			±0.5V_{REF}/ Gain		V
	Input Voltage Range: Common Mode + Signal	Gain = 1	**A_{GND} + 0.1**		**A_{VDD} - 0.1**	V
		Gain = 2, 4, 8, 16, 32, 64, 128	**A_{GND} + 1.5**		**A_{VDD} - 1.5**	V
	Input Bias Current; AIN+, AIN-	Gain = 1		300		nA
		Gain = 2, 4, 8, 16, 32, 64, 128		3		nA
	Input Offset Current; AIN+, AIN-	Gain = 1		±20		nA
		Gain = 2, 4, 8, 16, 32, 64, 128		±1		nA
SYSTEM PERFORMANCE						
	Resolution	No Missing Codes	**24**			Bits
INL	Integral Nonlinearity	Gain = 1		±0.0002	**±0.001**	% FSR
		Gain = 2 to 128		±0.0004		% FSR
	Offset	Gain = 1		±0.4		ppm of FS
	Offset Drift	Gain = 1		±300		nV/°C
		Gain = 2 to 128		±300/Gain ± 10		nV/°C
	Full Scale Error	Gain = 1		±0.007		%
		Gain = 2 to 128		±0.02		%
	Full Scale Drift	Gain = 1		±0.1		ppm/°C
		Gain = 64		±3.5		ppm/°C
		Gain = 128		±3.5		ppm/°C
CMRR	Common Mode Rejection Ratio	Gain of 1	**85**	110		dB
		Gain of 128		130		dB
PSRR	Power Supply Rejection Ratio	Gain of 1		100		dB
		Gain of 128	**100**	125		dB
OWR	Output Word Rate (Note 8)		**2.5**		**4000**	SPS

Electrical Specifications

$V_{REF}+$ = 5.0V, $V_{REF}-$ = 0V, A_{VDD} = 5V, D_{VDD} = 5V XTALIN/CLOCK = 4.9152MHz (Note 6) T_A = -40°C to +105°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

SYMBOL	PARAMETER	TEST LEVEL OR NOTES	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VOLTAGE REFERENCE INPUT						
VREF	Voltage Reference Input	VREF = VREF+ - VREF-	**1.5**	5.0	**A_{VDD} + 0.1**	V
VREF+	Positive Voltage Reference Input		**V_{REF-} + 1.5**		**A_{VDD} + 0.1**	V
VREF-	Negative Voltage Reference Input		**A_{GND} - 0.1**		**V_{REF+} - 1.5**	V
VREFI	Voltage Reference Input Current			350		nA
Low-Side Power Switch						
r_{ON}	ON-resistance				**10**	Ω
	Continuous Current				**30**	mA
Power Supply Requirements						
A_{VDD}	Analog Supply Voltage		**4.75**	5.0	**5.25**	V
D_{VDD}	Digital Supply Voltage		**2.7**	5.0	**5.25**	V
A_{IDD}	Analog Supply Current	Gain of 1		6	**10**	mA
		Gain = 2 to 128		9	**12**	mA
		Power-down		0.2	**2.5**	µA
		Standby		0.3		µA
D_{IDD}	Digital Supply Current	Gain of 1		750	**950**	µA
		Gain = 2 to 128		750	**950**	µA
		Power-down		1	**26**	µA
		Standby		1.8		µA
	Power	Normal				
		Gain = 1		33.75	**54.75**	
		Gain = 2 to 128		48.75	**64.75**	mW
		Power-down		6		µW
		Standby		10.5		µW
Digital Inputs						
V_{IH}			**0.7 D_{VDD}**			V
V_{IL}					**0.2 D_{VDD}**	V
V_{OH}		I_{OH} = -1mA	**D_{VDD} - 0.4**			V
V_{OL}		I_{OL} = 1mA			**0.2 D_{VDD}**	V
	Input Leakage Current				**±10**	µA
	External Clock Input Frequency		**0.3**	4.9152		MHz
	Serial Clock Input Frequency (Note 9)				**4**	MHz

NOTES:

6. If the device is driven with an external clock, best performance will be achieved if the rise and fall times of the clock are slowed to less than 20ns (10% to 90% rise/fall time).
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Output word rates (MIN and MAX in the table) are specified using 4.9152MHz clock. If a different clock frequency is used, or if the internal oscillator is used as the clock source for the converter, the output word rates will scale proportionally to the change in the clock frequency.
9. The OWR (Output Word Rate) setting dictates the rate at which the SDO/$\overline{RDY}$ signal will fall. To read every conversion word, reading of the conversion word should begin immediately after SDO/$\overline{RDY}$ falls and the SCLK rate should be fast enough to read all 24 data bits of the conversion word before the next falling edge of SDO/$\overline{RDY}$ that indicates that a new conversion word is available.

TABLE 1. INPUT REFERRED NOISE (nV, RMS)

OUTPUT WORD RATE (Note 10)	PGA GAIN							
	1	2	4	8	16	32	64	128
2.5	187.1	101.8	52.0	25.0	14.5	8.8	6.6	6.5
5	209.2	112.2	55.9	28.5	16.3	10.5	8.4	8.2
10	253.6	133.0	63.8	35.5	20.0	13.9	11.9	11.6
20	308.3	157.7	77.6	43.8	25.0	18.1	15.7	15.2
40	417.7	207.1	105.1	60.2	35.1	25.3	23.3	22.4
80	547.2	264.6	140.1	78.2	46.8	34.9	31.6	30.1
100	607.0	292.7	159.4	87.5	52.2	39.7	35.4	34.3
160	780.3	368.2	203.0	110.6	68.0	52.3	46.2	45.2
200	845.1	405.5	222.2	119.7	74.2	57.3	50.6	49.5
320	1030.6	517.0	284.5	147.2	93.2	72.5	64.1	62.5
400	1169.0	591.7	318.1	165.3	105.2	81.9	72.6	70.5
640	1476.0	756.0	398.0	211.0	129.7	102.4	90.2	87.4
800	1632.0	857.9	445.0	237.2	139.5	114.7	101.0	98.9
1000	1806.1	958.6	489.5	267.0	157.8	126.8	112.4	107.7
1280	2018.0	1089.0	557.0	297.6	180.2	143.7	124.3	123.5
1600	2289.0	1234.0	632.0	328.0	202.3	163.4	134.0	132.0
2000	2572.5	1380.4	708.8	365.8	230.2	176.0	147.6	145.8
2560	2945.0	1538.0	801.0	423.7	259.0	201.0	162.3	161.3
3200	3287.0	1711.0	891.0	478.0	285.0	221.0	178.0	174.3
4000	3708.2	1876.9	955.1	545.1	316.6	242.8	196.0	194.9

NOTE:

10. The ADC has a programmable $SINC^4$ filter. The -3dB bandwidth of the filter for a given word rate is 0.239 x OWR.

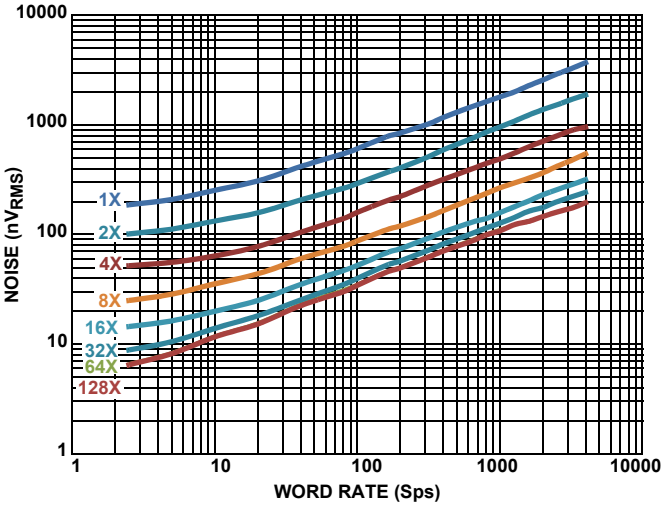


FIGURE 2. NOISE vs GAIN AND WORD RATE SETTINGS

TABLE 2. NOISE FREE BITS

OUTPUT WORD RATE (Note 11)	NOISE-FREE BITS							
	1	2	4	8	16	32	64	128
2.5	21.9	21.8	21.8	21.9	21.6	21.4	20.8	19.8
5	21.8	21.7	21.7	21.7	21.5	21.1	20.4	19.5
10	21.5	21.4	21.5	21.3	21.2	20.7	19.9	19.0
20	21.2	21.2	21.2	21.0	20.9	20.3	19.5	18.6
40	20.8	20.8	20.8	20.6	20.4	19.8	19.0	18.0
80	20.4	20.4	20.4	20.2	19.9	19.4	18.5	17.6
100	20.3	20.3	20.2	20.0	19.8	19.2	18.4	17.4
160	19.9	20.0	19.8	19.7	19.4	18.8	18.0	17.0
200	19.8	19.8	19.7	19.6	19.3	18.7	17.8	16.9
320	19.5	19.5	19.3	19.3	19.0	18.3	17.5	16.5
400	19.3	19.3	19.2	19.1	18.8	18.1	17.3	16.4
640	19.0	18.9	18.9	18.8	18.5	17.8	17.0	16.0
800	18.8	18.8	18.7	18.6	18.4	17.7	16.8	15.9
1000	18.7	18.6	18.6	18.4	18.2	17.5	16.7	15.7
1280	18.5	18.4	18.4	18.3	18.0	17.3	16.5	15.5
1600	18.3	18.2	18.2	18.1	17.8	17.1	16.4	15.5
2000	18.2	18.1	18.0	18.0	17.7	17.0	16.3	15.3
2560	18.0	17.9	17.9	17.8	17.5	16.8	16.2	15.2
3200	17.8	17.8	17.7	17.6	17.3	16.7	16.0	15.1
4000	17.6	17.6	17.6	17.4	17.2	16.6	15.9	14.9

NOTE:

11. Noise-free resolution in Table 2 is calculated as LOG ((Input Span)/(RMS Noise x 6.6))/LOG(2). The result is rounded to the nearest tenth of a bit. The Input Span is equivalent to ±0.5VREF/GAIN, V_{REF} = 5V. The RMS noise is selected from Table 1 for the desired Output Word Rate and Gain option.

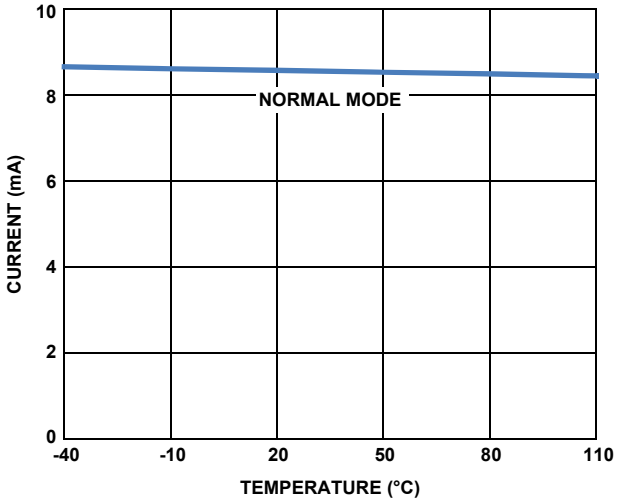


FIGURE 3. ANALOG CURRENT vs TEMPERATURE (GAIN = 2 TO 128)

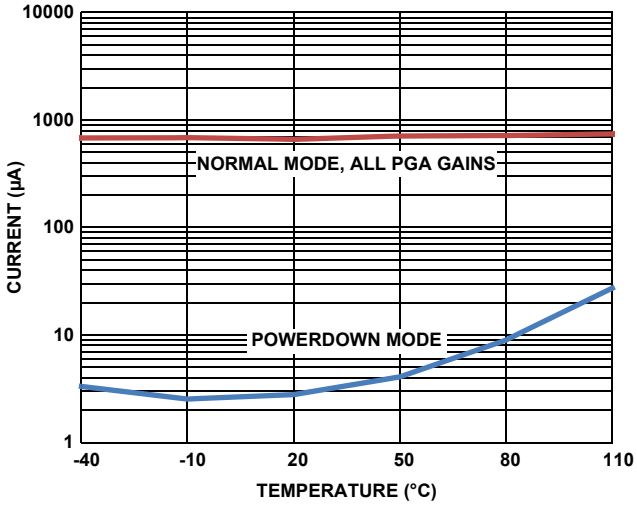


FIGURE 4. DIGITAL CURRENT vs TEMPERATURE

Typical Characteristics

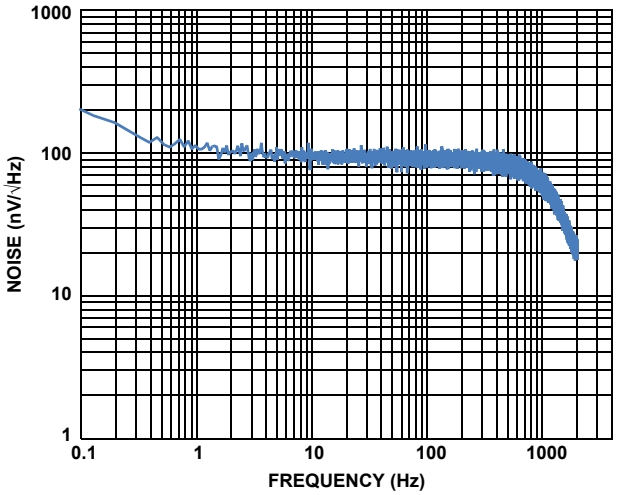


FIGURE 5. NOISE SPECTRAL DENSITY, 4kSPS, PGA GAIN = 1

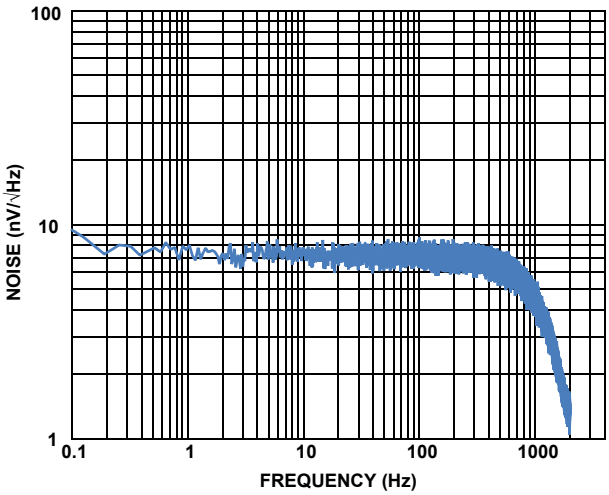


FIGURE 6. NOISE SPECTRAL DENSITY, 4kSPS, PGA GAIN = 128

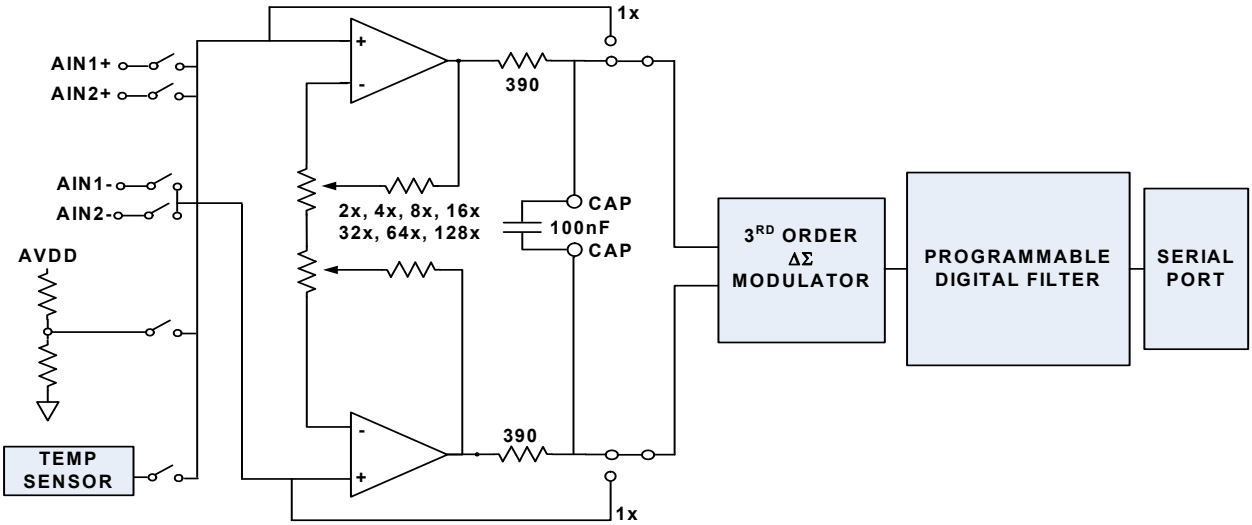


FIGURE 7. ISL26102 (2 CHANNEL) BLOCK DIAGRAM

Circuit Description

A key element in the ISL26102/ISL26104 A/D converters is its low noise chopper-stabilized programmable gain amplifier. The amplifier features seven gain settings (2x, 4x, 8x, 16x, 32x, 64x, and 128x). On these gain settings, the amplifier has very high input impedance but has restricted common mode range, which does not extend all the way to the power supply rails. When the gain of 1x is selected, the chopper-stabilized amplifier is bypassed. The modulator input, which is used directly in 1x gain, has a common mode range that extends to the supply rails. But, because of this greater common mode range on the 1x gain setting, the input current is higher than on the other gain settings.

The ISL26102 provides the user with two fully differential signal inputs at the multiplexer plus two other internal channel selections, which allow the user to monitor the analog supply voltage of the chip, and the on-chip temperature sensor. The ISL26104 provides the user with two additional fully differential inputs on the multiplexer.

The programmable gain amplifier has a passive RC filter on its output. The resistors are located inside the chip on the outputs of the differential amplifier stages. The capacitor (nominally a 100nF C0G ceramic or PPS film (Polyphenylene sulfide)) for the filter is connected to the two CAP pins of the chip. The outputs of the differential amplifier stages of the PGA are filtered before their signals are presented to the delta-sigma modulator. This filter reduces the amount of noise by limiting the signal bandwidth and eliminating the chopping artifacts of the chopped PGA stage.

Figure 7 illustrates a block diagram of the programmable gain amplifier.

Functional Description

Analog Input Span

The input span of the A/D converter is determined by the magnitude of the voltage reference and the gain setting selection. The voltage reference magnitude is determined by the voltage difference between the VREF+ and the VREF- pins. This voltage may be as low as 1.5V or as great as the analog supply voltage to the chip. The voltage on the VREF pins is scaled to accept a voltage into the A/D converter on 1x gain of ±0.5 VREF/GAIN where gain is 1. An illustration of the input span when using a 5V V_{REF} is in Figure 8. The figure illustrates that with a V_{REF} = 5V and a gain setting of 1x, the input span will be ±2.5V, which is a fully differential signal. If the programmable gain amplifier gain is set to another value other than 1x, the input span will be reduced by the gain scale factor. With a V_{REF} = 5V and the PGA gain set at 128x, the input span into the ADC will be [±(0.5)5V]/128 = ±19.53mV on a fully differential basis.

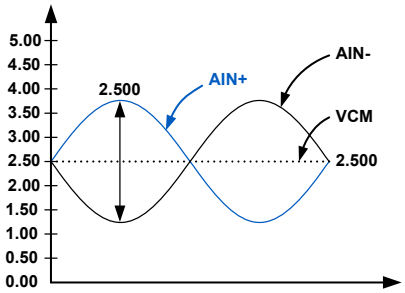


FIGURE 8. DIFFERENTIAL INPUT FOR V_{REF} = 5V, GAIN = 1X

Digital Filter

The output of the delta-sigma modulator in the A/D converter is filtered with a $Sinc^4$ digital filter that includes programmable decimation to achieve a wide range of output word rates. The transfer function of the $Sinc^4$ filter is illustrated in Figure 9. Figure 9 is normalized to 1 being the output word rate. The output word rate can be selected by setting bits in the OWR (Output Word Rate) Register. The converter provides a wide selection of word rates as shown in Table 3. Note that the word rates are based upon an XTALIN/CLOCK of 4.9152MHz. If the clock is a different frequency than 4.9152MHz, the actual output word rate will scale proportionally.

TABLE 3. OUTPUT WORD RATE REGISTER SETTINGS

DATA RATE (Sps)	REGISTER CODE (Hex)
2.5	00
5	01
10	02
20	03
40	04
80	05
100	0B
160	06
200	0C
320	07
400	0D
640	08
800	0E
1000	11
1280	09
1600	0F
2000	12
2560	0A
3200	10
4000	13

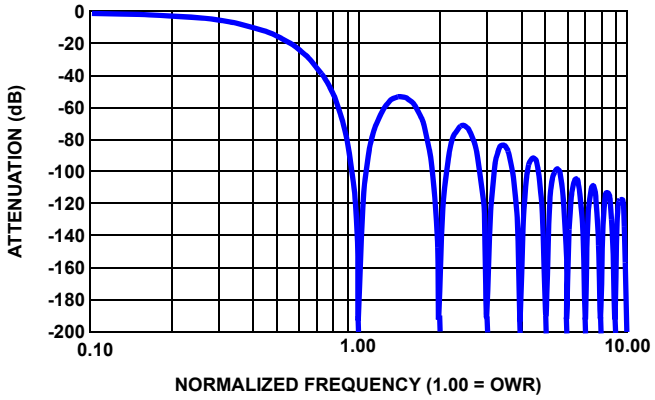


FIGURE 9. TRANSFER FUNCTION OF SINC^4 NORMALIZED TO 1 = OUTPUT WORD RATE

Digital Filter Settling Time

If the Input Mux Selection register is written into to select a new channel, the modulator and the digital filter are reset and the converter begins computing a new output word when the new mux selection is made. The first conversion word output from the A/D after a new mux channel is selected, or after the PGA gain is changed, will be delayed to allow the filter to fully settle. A Sinc^4 filter takes four conversion times to fully settle, therefore the SDO/$\overline{\text{RDY}}$ signal will not fall until a time of four normal conversion periods has elapsed. The SDO/$\overline{\text{RDY}}$ output falls to signal that an output conversion word is ready to be read.

Whenever the input signal has a large step change in value, it may take as many as six output conversions for the output word to accurately represent the new input value.

Clock Sources

The ISL26102/ISL26104 can operate from an internal oscillator, and external clock source, or from a crystal connected between the XTALIN/CLOCK and XTALOUT pins. See the block diagram for the clock system in Figure 10. When the converter is powered up, the CLOCK DETECT block determines if an external clock source is present. If a clock signal greater than 300kHz is present on the XTALIN/CLOCK pin, the circuitry will disable the internal oscillator and use the external clock as the clock to drive the chip circuitry. If the ADC is to be operated from the internal oscillator the XTALIN/CLOCK pin should be grounded. If the ADC is to be driven with an external clock there should be a 100Ω resistor placed in series with the clock signal to the XTALIN/CLOCK pin. This helps slow the rise and fall time edges, which can impact converter performance. If the ADC is to be operated with a crystal, the crystal should be located very close to the A/D converter package pins. Note that loading capacitors for the crystal are not required as there are loading capacitors built into the silicon, although the capacitor values are optimized for operation with a 4.9152MHz crystal.

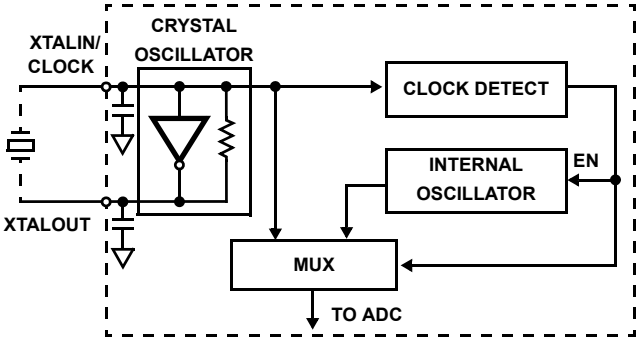


FIGURE 10. CLOCK GENERATOR BLOCK DIAGRAM

Overview of Registers and A/D Converter Operation

The ISL26102, ISL26104 devices are controlled via their serial port by accessing various on-chip registers. Communication to the A/D via the serial port occurs by writing a command byte followed by a data byte. All registers in the converter are accessed or written as 8-bit wide registers, even though some data words may be up to three bytes in length. The converter has offset registers (three bytes wide) associated with each PGA gain setting. These registers hold the offset calibration word, a three byte twos complement word, for each gain selection. When power is first applied to the converter these registers are reset to zero. Note that the ISL26102, ISL26104 converters do not have gain calibration registers for the PGA gains. This is because the gain for each PGA gain setting is calibrated at the factory.

Table 4 list the registers inside the ADC. When power is first applied the Offset Array Registers, registers which hold the offset calibration words for each PGA gain, are set to zero.

The **Chip ID register** has a bit, which allows the user to identify whether the chip is an ISL26102 (2 channel) or an ISL26104 (4 Channel) device. This register also has a code, which is assigned to reveal the revision of the chip.

The **SDO/LSPS register** allows the user to control the behavior of the SDO (Serial Data Output) output. If bit (b1) is set to logic 0, the SDO/$\overline{\text{RDY}}$ output will go low when conversions are completed and output the 24-bit conversion word if $\overline{\text{CS}}$ is taken high and 24 SCLKs are issued to the SCLK pin. If the SDO bit in this register is set to logic 1, the SDO output will be set to a tri-state condition (high output impedance). This allows another device, such as another A/D converter, to be connected to this same signal line going to the microcontroller.

The LSPS (Low-Side Power Switch) bit allows the user to toggle a switch via the LSPS pin that can be used to enable power to a load cell or other circuitry. When the LSPS bit is logic 0 the LSPS switch is open. When the LSPS bit is logic 1, the switch is closed. The LSPS bit is set back to a logic 0 if the chip is put into Standby via the Standby Register, or if the $\overline{\text{PDWN}}$ signal is activated. See data sheet tables for the current capability of the switch.

The **Standby register** has a bit which when set to logic 1, the chip enters the standby mode. In standby mode, the chip enters a low power state. Only the crystal oscillator is left powered (if used) to enable a quick return to full operation when bit (b0) is set back to logic 0. If the crystal is not being used, it is not powered. In this

case, there is no difference in power consumption for standby or power-down modes.

The **Output Word Rate register** allows the user to set the rate at which the converter performs conversions. Table 3 lists the output word rate options.

The **Input Mux Selection register** defines the input signal that will be used when conversions are performed. The signals include either 2 (ISL26102) or 4 (ISL26104) differential input channels, an on-chip temperature sensor, or the monitor node for the AVDD supply voltage. Note that if the temperature sensor or the AVDD monitor are selected the PGA gain is internally set for 1x gain.

The **PGA Gain register** allows the user to set the PGA gain setting for the channel pointed to by the Channel Pointer register. The PGA provides gain settings of 1x (in this gain setting the programmable gain amplifier is actually bypassed and the signal goes directly to the modulator), 2x, 4x, 8x, 16x, 32x, 64x, and 128x.

The **Conversion Control register** provides the means to initiate offset calibration, or initiate single or continuous conversions. If bit b2 of this register is set to a logic 1, an offset calibration will be performed and the states of bits b1 and b0 are ignored. The state of bit b2 will be set back to a logic 0 after the offset calibration is complete.

If the b1b0 bits are set to 01, a single conversion will be performed. When the conversion is completed, the bits will be set back to 00, the SDO/$\overline{\text{RDY}}$ pin will be taken low (note that the $\overline{\text{CS}}$ pin must be a logic 1 for SDO/$\overline{\text{RDY}}$ to fall) and the conversion data will be held in a register. If the user enables $\overline{\text{CS}}$ (held at logic 1) and provides 24 SCLKs to the SCLK pin, the data word will be shifted out of the SDO/$\overline{\text{RDY}}$ pin as a 24-bit two's complement word, starting with the MSB. Data bits are clocked out on the rising edge of SCLK. If the entire 24-bit data word is not read before the completion of the next conversion, it will be overwritten with the new conversion word.

If the b1b0 bits are set to 10, conversions will be performed continuously until bits b1b0 are set to either 00 or 01, Standby mode is activated, or the $\overline{\text{PDWN}}$ pin is taken low. Refer to "Reading Conversion Data" on page 14.

The **Delay Timer register** allows the user to program a delay time, which will be inserted between the time that the user selects an input to be converted via the Input Mux Selection register and when the conversion is started. If continuous conversions are selected via the Conversion Control register, the Input Mux Selection register can be changed without needing to stop conversions. The Delay Timer register allows the user to insert a delay between when the mux is changed and when a new conversion is started. If the Delay Timer register is set to all 0's the minimum delay will be 100µs.

Any time the PGA Gain setting is changed, the channel selection is changed, or a command is given to start conversion(s), the user can expect a delay before the SDO/$\overline{\text{RDY}}$ signal will fall. This delay is defined by Equation 1:

$$[4\text{ms} + (\text{Delay Timer Register Setting} * 4\text{ms}) + 100\mu\text{s}) + 4*(1/\text{OWR})] \quad \text{(EQ. 1)}$$

The first 4ms is for the PGA to settle. This delay cannot be changed. The Delay Timer register setting is user controllable, and it dictates the majority of the second section of the equation. The 4*(1/OWR) term is the time required for the filter to settle at the OWR (Output Word Rate), which has been selected in the Output Word Rate register.

The **PGA Offset Array registers** hold the calibration results for the offset calibration done for each of the PGA gain settings. The result of an offset calibration is a 24-bit twos complement word. There are eight high byte registers, eight mid byte registers and eight low byte registers. When reading or writing to one of the PGA Offset Array byte registers, the register selected will be determined by the PGA Pointer Register.

The PGA Pointer register contains the pointer to the PGA Offset register array bytes associated with a specific PGA gain.

TABLE 4. CONTROL REGISTERS

NAME	ADDRESS		DATA BITS	NOTES
	Write	Read	b7 b6 b5 b4 b3 b2 b1 b0	Registers are Accessed by Address Byte followed by Register Data Byte
Chip ID	N/A	00h	b4 0 = ISL26104 1 = ISL26102 b3-b0 Revision Code	
SDO/LSPS	82h	02h	b1 1= Disable SDO 0 = Enable SDO b0 1 = LSPS ON 0 = LSPS OFF	 0 is default 0 is default
Standby	83h	03h	b0 1 = Enable Standby 0 = Disable	 0 is default
Output Word Rate	85h	05h	See Table 3 on page 9	0 is default, 2.5Sps
Input Mux Selection	87h	07h	ISL26104 b2 b1 b0 000 = Channel 1 001 = Channel 2 010 = Channel 3 011 = Channel 4 100 = Analog Supply Monitor 101 = Temperature Sensor 110 = Not used 111 = Not used ISL26102 b2 b1 b0 000 = Channel 1 001 = Channel 2 010 = Analog Supply Monitor 011 = Temperature Sensor 100 = Not used 101 = Not used 110 = Not used 111 = Not used	
Channel Pointer	88h	08h	ISL26104 b2 b1 b0 000 = Channel 1 001 = Channel 2 010 = Channel 3 011 = Channel 4 100 = Analog Supply Monitor 101 = Temperature Sensor 110 = Not used 111 = Not used ISL26102 b2 b1 b0 000 = Channel 1 001 = Channel 2 010 = Analog Supply Monitor 011 = Temperature Sensor 100 = Not used 101 = Not used 110 = Not used 111 = Not used	

TABLE 4. CONTROL REGISTERS (Continued)

NAME	ADDRESS		DATA BITS	NOTES
PGA Gain	97h	17h	b2 b1 b0 000 = 1x 001 = 2x 010 = 4x 011 = 8x 100 = 16x 101 = 32x 110 = 64x 111 = 128x	PGA Gain Setting for Channel Pointed to by the Channel Pointer Register. Whenever the Analog Supply Monitor or the Temp Sensor are selected, the PGA gain is set to 1x.
Conversion Control	84h	04h	b2 0 = Off 1 = Perform Offset Calibration b1 b0 00 = Stop Conversions 01 = Perform Single Conversion 10 = Perform Continuous Conversions 11 = Not Used	Performing Offset Calibration has priority over instructions from bits b1b0
Delay Timer	C2h	42h	b7-b0 The start of conversion is delayed by: Delay = Register Word*4ms + 100µs	
PGA Offset Array (High Byte)	BDh	3Dh	Offset Calibration Result Most Significant Byte	For PGA Pointed to by PGA Pointer Register
PGA Offset Array (Mid Byte)	BEh	3Eh	Offset Calibration Result Middle Byte	For PGA Pointed to by PGA Pointer Register
PGA Offset Array (Low Byte)	BFh	3Fh	Offset Calibration Result Low Byte	For Channel Pointed to by Channel Pointer Register
PGA Monitor	Bch	3ch	b2 b1 b0 000 = 1x 001 = 2x 010 = 4x 011 = 8x 100 = 16x 101 = 32x 110 = 64x 111 = 128x	This register points to the offset register associated with the PGA gain selection

Writing to On-chip Registers

Writing into a register on the chip involves writing an address byte followed by a data byte. The lead bit of the address byte is always a logic 1 to indicate that data is to be written. The remaining seven bits of the address byte contain the address of the register that is to be written. To begin the write cycle, $\overline{CS}$ must first be taken low with SCLK low. This should occur at least 125ns before SCLK goes high. This is shown as t_{cs} in the timing diagram of Figure 11. Once $\overline{CS}$ is low, the user must then present the lead bit to the SDI port. The data bits will be latched into the port by rising edges of SCLK. The data set-up time (t_{ds}) of the data bits to the rising edge of SCLK is 50ns (Note that one half clock cycle of the highest SCLK rate is 1/(2*4 MHz) = 125ns). Data hold time (t_{dh}) is also 50ns. Data bits should be advanced to the next bit on falling edges of SCLK. Once the eight data bits have been written, $\overline{CS}$ should be returned to high. ($\overline{CS}$ must be high to read conversion data words from the port). When $\overline{CS}$ goes high the user should ignore any activity on the SDO/$\overline{RDY}$ pin for at least 10 cycles of the master clock, which is driving the ADC.

See Figure 11 for an illustration of the timing to write on-chip registers.

If multiple registers are to be written, $\overline{CS}$ should be taken high after each address byte/data byte combination and remain high for at least a period of time equal to 6*1/(Xtal/Clock) frequency. If the chip is operating from a 4.9152MHz master clock, this would mean that $\overline{CS}$ should remain high between write cycles for at least 6*1/4.9152MHz = 1.22µs.

Lower frequency master clock rates (minimum master clock rate can be as low as 300kHz) will require $\overline{CS}$ to remain high for a longer period of time between register write cycles.

Each time an address/data byte combination is written into the port, the master clock is used to place the data into the register after $\overline{CS}$ returns high. This is required because the data transfer must be synchronized to the clock that is driving the modulator/filter circuitry.

Reading from On-chip Registers

Reading from a register on the chip begins by writing an address byte into the SDI port. The lead bit of the address byte is always a logic 0 to indicate that data is to be read from an on-chip register. The remaining seven bits of the address byte contains the address of the register that is to be read. To begin the read cycle, $\overline{CS}$ must first be taken low with SCLK low and be low for at least 125ns before SCLK is taken high to latch the first data bit. The eight address bits will be latched into the port by rising edges of SCLK. The data set-up time (t_{ds}) of the data bits to the rising edge of SCLK is 50ns (one half clock cycle of the highest SCLK rate is 1/(2*4MHz) = 125ns). Data hold time (t_{dh}) is also 50ns. Address bits should be advanced to the next bit on falling edges of SCLK. Once the address byte has been written, the port will output a byte from the selected 8-bit register onto the SDO pin. A total of 16 SCLKs are required to write the address byte and then read the 8-bit register output. The timing for reading from on-chip registers is illustrated in Figure 12.

Reading Conversion Data

Reading conversion data is done in a different manner than when reading on-chip registers. After writing into the Conversion Control register to instruct the A/D to start conversions, the user will then wait for the SDO/$\overline{RDY}$ signal to fall. Once the SDO/$\overline{RDY}$ signal falls, the 24-bit conversion data word becomes available to the port. To read the conversion word, the $\overline{CS}$ signal should be left in the logic 1 state and 24 SCLKs issued to the SCLK pin. The first rising SCLK edge will make the MSB data bit of the 24-bit word become available. The falling edge of the first SCLK will latch the bit into the external receiving logic device. Subsequent rising edges of SCLK will cause the port output to advance to the next data bit. Once the last data bit is read, the SCLK signal should remain low until another conversion word is available or until a command to write or read an on-chip register is performed.

SDO/$\overline{RDY}$ goes low to signal that a conversion has been performed and that the conversion word is available. If the analog input signal goes over range this may cause the modulator to become unstable. If this condition occurs the modulator resets itself. The output code will be held at full scale but the effect of the modulator being reset will cause the SDO/$\overline{RDY}$ signal to fall at only one fourth of its word rate. This occurs because when the modulator is reset, the digital filter is also reset and it takes four conversion periods for the filter to accumulate enough modulator bit stream information to produce an accurate conversion result.

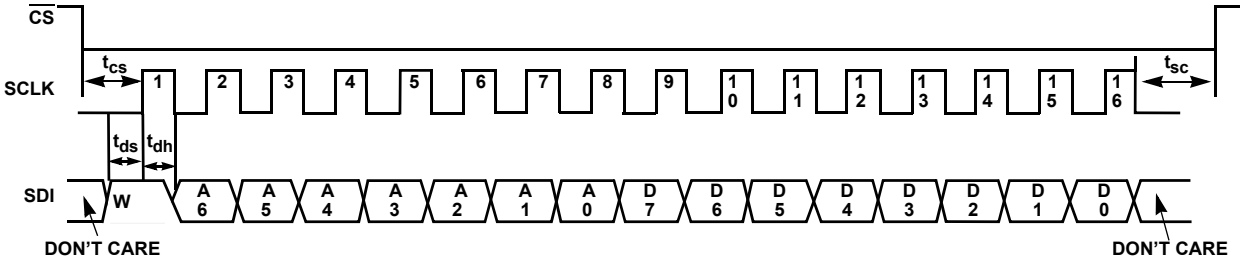


FIGURE 11. WRITE ON-CHIP REGISTER WAVEFORMS

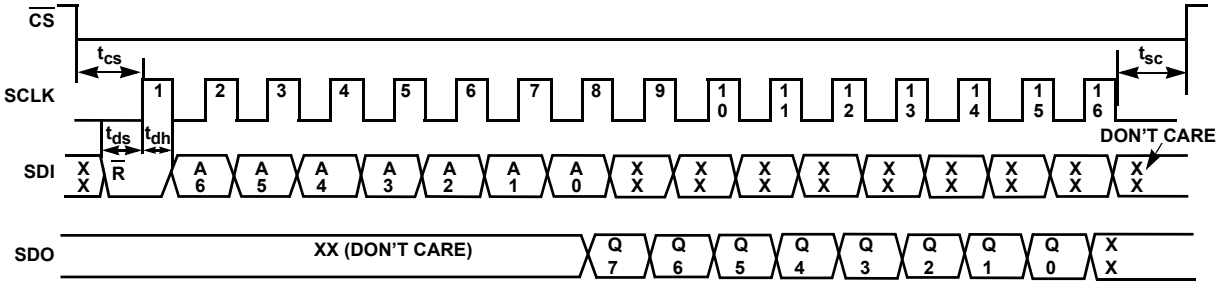


FIGURE 12. READ ON-CHIP REGISTER WAVEFORMS

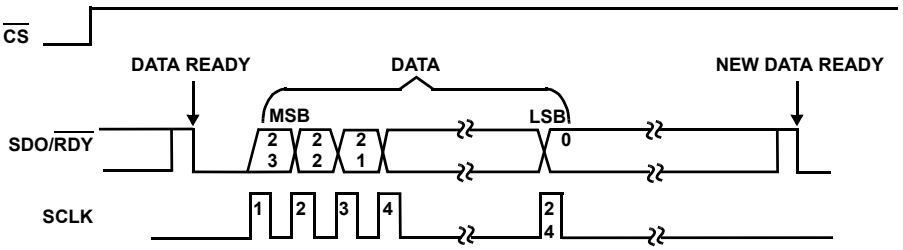


FIGURE 13. READING CONVERSION DATA WORD WAVEFORMS

Output Data Format

The converter outputs data in twos complement format in accordance with coding shown in Table 5.

TABLE 5. OUTPUT CODES CORRESPONDING TO INPUT

INPUT SIGNAL	DESCRIPTION	OUTPUT CODE (HEX)
$\geq + 0.5V_{REF}/GAIN$	+ Over-range	7FFFFF
$0.5V_{REF}/[GAIN*(2^{23} - 1)]$	+ 1 LSB	000001
0	Zero Input	000000
$-0.5V_{REF}/[GAIN*(2^{23}-1)]$	- 1 LSB	FFFFFF
$\leq - 0.5V_{REF}/GAIN$	- Over-range	800000

Operation of $\overline{PDWN}$

When power is first applied to the converter, the $\overline{PDWN}$ pin must transition from Low to High after both power supplies have settled to specified levels in order to initiate a correct internal power-on reset. A means of controlling the $\overline{PDWN}$ pin with a simple RC delay circuit is illustrated in Figure 14. If AVDD and DVDD are different supplies, be certain that AVDD is fully established before $\overline{PDWN}$ goes high.

The $\overline{PDWN}$ pin can be taken low at any time to reduce power consumption. When $\overline{PDWN}$ is taken low, all circuitry is shut down, including the crystal oscillator. When coming out of power-down, $\overline{PDWN}$ is brought high to resume operation. There will be some delay before the chip begins operation. The delay will depend upon the source of the clock being used. If the XTALIN/CLOCK pin is driven by an external clock, the delay will be minimal. If the crystal oscillator is the clock source, the oscillator must start before the chip can function. Using the on chip crystal oscillator amplifier with an attached 4.9152MHz clock will typically require about 20ms to start-up.

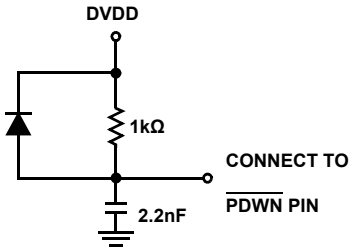


FIGURE 14. $\overline{PDWN}$ DELAY CIRCUIT

Standby Mode Operation

The A/D converter can be placed in the standby mode by writing to the Standby register. Standby mode causes the converter to enter a low power state except for the crystal oscillator amplifier. If the converter is operated with a crystal connected to the XTALIN/CLOCK and XTALOUT pins the crystal will continue to oscillate. This reduces start-up time when the Standby register bit is written back to logic 0 to exit standby mode.

Low Side Power Switch

The ADC includes a low side power switch. The LSPS pin is an open drain connection to a transistor, which can be turned on or off via bit control in the SDO/LSPS register. The LSPS switch can be used to enable/disable excitation to external systems, such as a load cell. Figure 15 illustrates the typical connection of the ADC in a load cell measurement system. The LSPS pin is connected to the low side of the load cell.

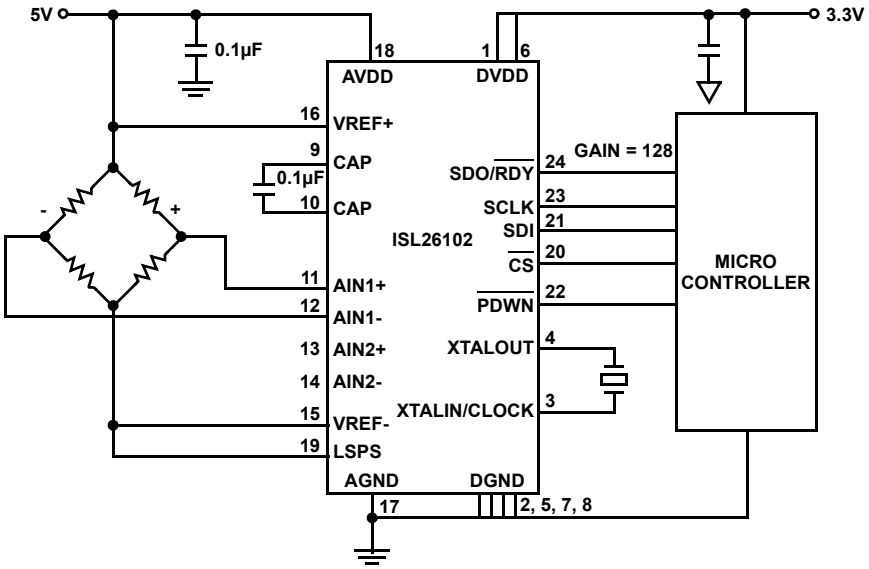


FIGURE 15. A LOAD CELL MEASUREMENT APPLICATION USING THE ISL26102

Device Supply and Temperature Monitoring

One of the multiplexer input selections is the AVDD Monitor. This option allows the A/D converter to measure a divided down value of the AVDD voltage. The nominal output code from AVDD monitor is given by (2^{23})*AVDD/(2*VREF). Table 6 provides a listing of the nominal count of the A/D converter associated with supply voltage values between 4.75 and 5.25V. Table 6 is based on V_{REF} = 5V.

If a V_{REF} of 2.5V is used, the output code from the A/D converter will stay at +Full Scale when AVDD > 5V. Thus, the AVDD monitor will not be able to check the voltages greater than 5V, but it will provide proper readings for AVDD voltages below 5V.

TABLE 6. ANALOG SUPPLY MONITOR OUTPUT CODES OVER SUPPLY VOLTAGES (V_{REF} = 5.0V)

AVDD (V)	OUTPUT CODE (±5%)
5.25	4407063
5.10	4281464
5.00	4197996
4.90	4114662
4.75	3989915

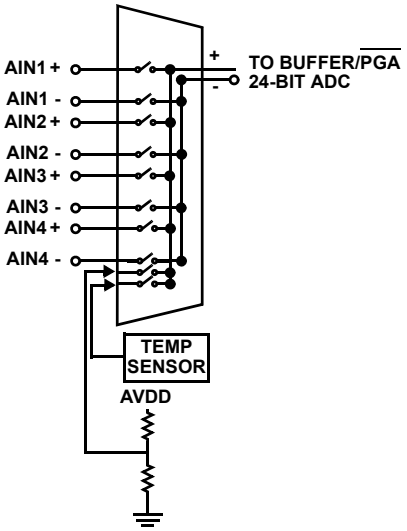


FIGURE 16. INPUT MULTIPLEXER BLOCK DIAGRAM

When the Input Mux Selection register is instructed to select the on-chip temperature sensor signal, the A/D measures a differential voltage produced between two diodes that are biased at different operating currents. The differential voltage is defined by Equation 2:

$$\Delta V = 102.2\ \text{mV} + (379\mu V * T(^\circ C)) \quad \text{(EQ. 2)}$$

Whenever the temperature sensor is selected in the Input Mux Selection Register, the Gain is set to 1x.

At a temperature of +25°C the measured voltage will be approximately 111.7mV. The actual output code from the converter will depend upon the magnitude of the VREF signal. The 111.7mV signal will be a portion of the span set by the VREF voltage using a gain setting of 1x. If V_{REF} is 5V, one code in the converter will be $\pm 0.5(V_{REF})/2^{23}$ = 298nV. Since the converter span is bipolar, and its span represents ± 8.338 million codes, the +111.7mV will output of a code of approximately 374,800 counts.

The on-chip temperature will typically be about 3° hotter than ambient because the device's power consumption is about 50 mW and the thermal impedance from die to ambient is about 63°/W; (0.05)*63 = 3.15°.

Getting Started

When power is first applied to the converter, the $\overline{PDWN}$ pin should be held low until the power supplies and the voltage reference are stable. Then $\overline{PDWN}$ should be taken high. When this occurs the serial port logic and other logic in the chip will have been reset. The chip contains factory calibration data stored in on-chip non-volatile memory. When $\overline{PDWN}$ goes positive this data is transferred into the appropriate working registers. This initialization can take up to 12.6ms. If an external clock or the internal oscillator are used as the clock for the chip, then this 12.6ms time includes the time necessary for these to be functional. But, if the crystal oscillator is used, the crystal may take 20ms to start up before the 12.6ms initialization occurs. Writing into or reading from the serial port should be delayed until the clock source and the initialization period have elapsed.

Once the clock source and initialization period have elapsed, the user should configure the ADC by writing into the appropriate registers. The commands and the corresponding data bytes that are to be placed into each of the registers are shifted into the SDI pin with $\overline{CS}$ held low. $\overline{CS}$ should be taken high for at least six cycles of the master clock after each command/data byte combination. This allows the control logic to properly synchronize the writing of the register with the master clock that controls the modulator/filter system. Each command/data byte combination should have its own $\overline{CS}$ cycle of $\overline{CS}$ going low, shifting the data, then $\overline{CS}$ going high, and remaining high for at least six cycles of the master clock.

Even though the device has been powered up, reset, and its register settings have been configured, the programmable gain amplifier and modulator portions of the ADC remain in a low power state until a command to start conversions is written into the Conversion Control register. To minimize drift in the device due to self-heating, it is recommended that after all registers are initialized to their initial condition, the command to start continuous conversions be issued as soon as is practical. Subsequent changes to registers, such as selecting another mux channel, should be performed with continuous conversions active. The proper method of writing to the other registers when continuous conversions are active is to wait for SDO/$\overline{RDY}$ to fall, read the conversion data, then take $\overline{CS}$ low and issue the command and the data byte that is to be written into a register, then return $\overline{CS}$ high. If multiple registers are to be written, $\overline{CS}$ should be toggled low and high to frame each command/data byte combination. Whenever any of the following registers [SDO/LSPS, Output Word Rate, Input Mux Selection, PGA Gain, Delay Timer, PGA Offset Array, or Offset Calibration] are written with continuous conversions in progress, the digital filter will be reset and there will be a delay determined by Equation 1 on page 11. The delay will begin when $\overline{CS}$ returns and remains high. When the delay has elapsed, the SDO/$\overline{RDY}$ signal will go low to

signal that a conversion data word is available. The Chip ID register (read only), the Channel Pointer register, and the PGA Monitor register can be read or written without any effect to the filter, and therefore there will be no delay in SDO/$\overline{\text{RDY}}$ falling. If the Standby register is enabled, conversions will be stopped.

Performing Calibration

The offset calibration function in the A/D converter removes the offset associated with the PGA (Programmable Gain Amplifier) in a specific gain setting. There are eight gain settings (1x, 2x, 4x, 8x, 16x, 32x, 64x, and 128x) and there is an array of eight sets of three byte registers which hold the high, middle, and low bytes of a 24-bit calibration word. The word is stored in twos complement format.

When calibration is performed it is to correct the PGA offset and is not actually associated with a given input channel. When a calibration is executed, its result is based upon the results of the converter performing a conversion with the input to the PGA shorted internally to the chip. The conversion result will have an uncertainty due to the peak-to-peak noise of the converter on the word rate in which the calibration is performed. Lower word rates have lower signal bandwidth and therefore will have less peak to peak variation in the output result when a calibration is performed. Therefore, it can improve calibration accuracy if the calibration is performed with the lowest word rate acceptable to the user.

Perform a PGA Offset Calibration

1. Write to the Output Word Rate register (85h) and select a word rate.
2. Write to the Input Mux Selection register (87h) and select an input channel (AIN1 to AIN4, not AVDD monitor or Temperature Sensor). Note that the channel will actually be shorted internally so it need not be a specific channel.
3. Write to the Channel Pointer register (88h) with the same selection written into the Mux Selection register.
4. Write the PGA gain selection into the PGA Gain register (97h).
5. Write bits b1 and b0 of the Conversion Control Register (84h) setting b1 to logic 1 and bit b2 to logic 0 to Perform Continuous Conversions.
6. Allow some delay and then write bit b2 of the Conversion Control Register (84h) to logic 1 to start the calibration process. The calibration time will be a function of the selection made in the Output Word Rate register. To determine when the calibration cycle is completed the user has two options. One is to monitor SDO/$\overline{\text{RDY}}$ for a falling edge as this signals the completion of conversion. A second approach would be to introduce a wait timer for at least the period of five conversion times at the word rate selected. [Example: If the word rate is 10Sps the calibration should be completed at 5x 1/10s or 500ms. After this time, the microcontroller can poll bit 2 of the Conversion Control Register. Bit b2 will be set back to logic 0 when the calibration has completed. It is best not to poll the register continuously because the added activity on the serial port may introduce noise and impact the calibration result.

Read Offset Calibration Registers

After an offset calibration has been performed, the calibration result, which is a 24-bit (3 bytes) two's complement word, is stored in the PGA Offset Arrays. Some user applications prefer to calibrate their system in the factory, then off load the calibration data and write it into non-volatile memory. Then when the product is powered up, this data is written back into the registers of the ADC.

1. Write into the PGA Pointer register (BCh) the selection wanted for the Gain of the PGA.
2. Read the three different PGA Offset Array registers, High byte (3Dh), Mid byte(3Eh), and Low byte(3Fh). Note that they can be read in any order, just understand that the three bytes represent a two's complement 24-bit word with the byte in order, high, mid and low.

Write Offset Calibration Registers

Upon power-up the offset registers are initialized to zero. After an offset calibration is performed the registers associated with that selected PGA gain will contain a valid 24-bit two's complement number.

This number can be saved into non-volatile memory and then written back to the PGA Offset Array register.

1. Write into the PGA Pointer register (BCh) the selection for the Gain setting of the PGA for which offset data is to be written.
2. Write the three different PGA Offset Array registers, High byte (BDh), Mid byte (BEh), and Low byte (BFh). Note that they can be written in any order, just understand that the three bytes represent a two's complement 24-bit word with the byte in order, high, mid and low.

The value written will be subtracted from the conversion data before it is output from the converter whenever that particular PGA Gain setting is used. Offset values up to the equivalent of full scale of the converter can be written but realize that this can consume dynamic range for the actual signal if the offset value is set to a large number.

Example Command Sequence

Table 7 illustrates an example command sequence to set up the ADC once power supplies are active. The sequence of commands, Set Channel Pointer, Set PGA Gain Setting, Set Mux Selection, Set Data Rate, and Start Continuous Conversions, can be written into the ADC as a sequence, each framed with $\overline{\text{CS}}$ going low at the beginning of each command and returning high at the end of the associated data byte (the rising edge of $\overline{\text{CS}}$ is the signal that actually writes the data byte to the control register). After continuous conversions are started, it is best if a time delay occur before the Perform Offset Calibration is issued. There is no specific amount of delay time as this depends upon the gain selection and the accuracy required. When the command to perform the offset calibration is issued, the continuous conversions in progress will be paused and the conversion sequence will be performed as necessary to perform the calibration. Once the calibration is completed, continuous conversions will be automatically restarted. Any subsequent commands which write into registers [SDO/LSPS, Output Word Rate, Input Mux Selection, PGA Gain, Delay Timer, PGA Offset Array, or Offset Calibration] while continuous conversions are in progress will reset the digital filter and introduce a delay determined by Equation 1 on page 11, after which, the SDO/$\overline{\text{RDY}}$ signal will toggle low to signal the availability of a conversion word.

TABLE 7. EXAMPLE COMMAND SEQUENCE

OPERATION	REGISTER	ADDRESS (WRITE)	DATA	COMMENTS
Set Channel Pointer	Channel Pointer	88h	01h	Set to select channel 2 (AIN2+, AIN2-)
Set PGA Gain Setting	PGA Gain	97h	06h	Sets PGA gain to 64x. This PGA gain is applied to the signal channel pointed to by the Channel Pointer set above.
Set Mux Selection	Input Mux Selection	87h	00h	Mux selection determines which channel is connected to the ADC. This step selects mux input 1 (AIN1+, AIN1-).
Set Data Rate	OWR	85h	11h	Sets output word rate to 1kSps. See Table 3 for other data rate options.
Start Continuous Conversions	Conversion Control	84h	02h	Set bits (b1-b0) of the Conversion Control register to '10' to start continuous conversions.
Perform Offset Calibration	Conversion Control	84h	04h	Set bit (b2) of the Conversion Control register to 1 to initiate an offset calibration of the PGA gain setting selected above. Note that bit (b3) will return to 0 when the calibration is completed.
Set Mux Selection	Input Mux Selection	87h	01h	Mux selection determines which channel is connected to the ADC. This step selects mux input 2 (AIN2+, AIN2-).

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 12, 2012	FN7608.0	Initial release.

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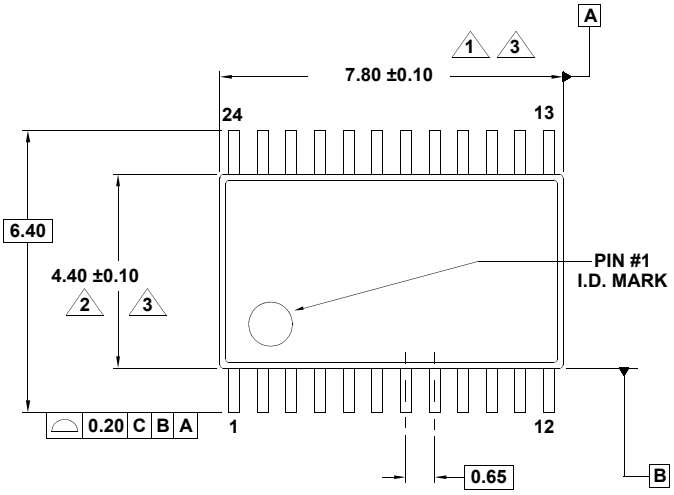
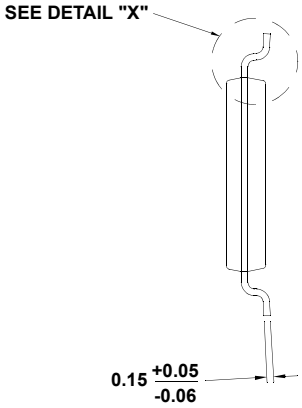
Package Outline Drawing

M24.173

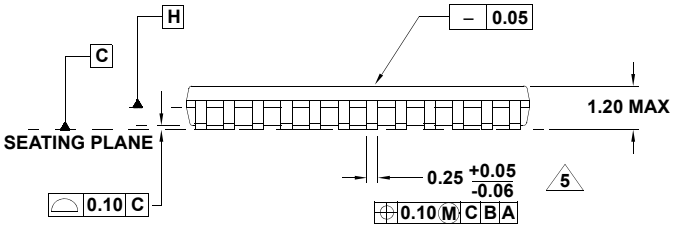
24 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10



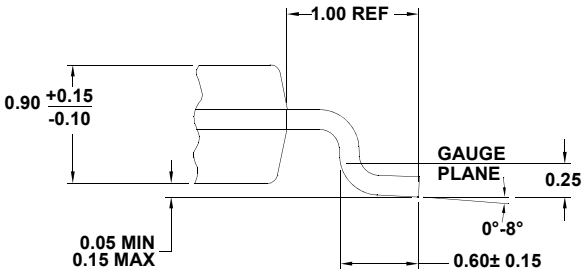
TOP VIEW



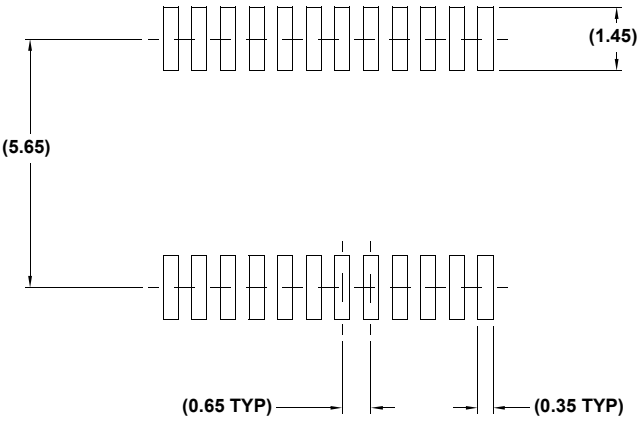
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

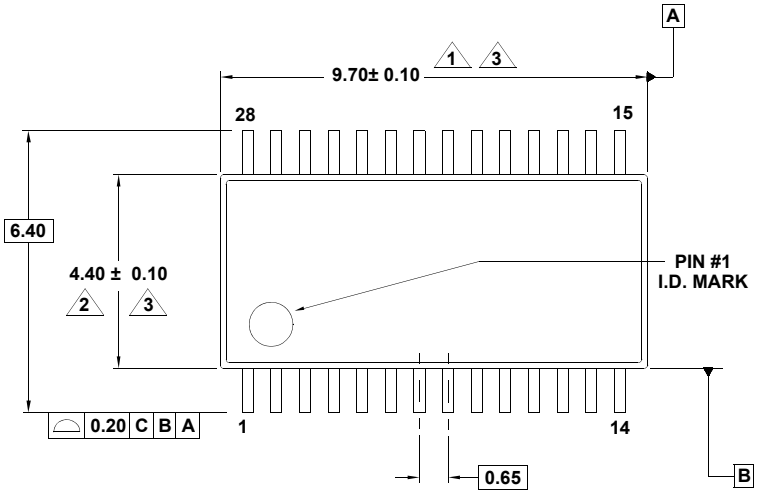
NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

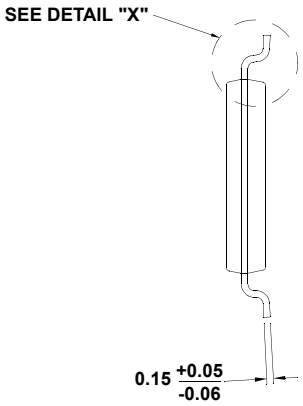
Package Outline Drawing

M28.173

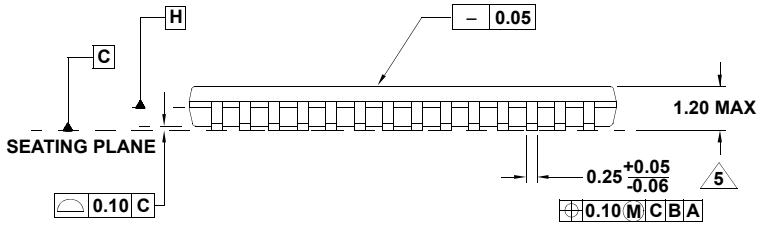
28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10



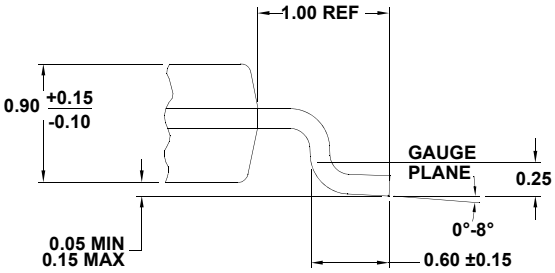
TOP VIEW



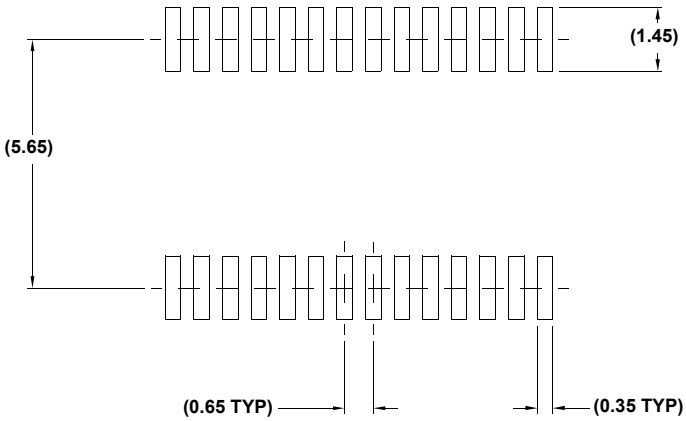
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

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3. Dimensions are measured at datum plane H.
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6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.