ISLA110P50

10-Bit, 500MSPS A/D Converter

FN7606
Rev.3.0
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The ISLA110P50 is a low-power, high-performance, 500MSPS analog-to-digital converter designed with Renesas' proprietary *FemtoCharge*™ technology on a standard CMOS process. The ISLA110P50 is part of a pin-compatible portfolio of 8, 10 and 12-bit A/Ds. This device is an upgrade of the KAD551XP-50 product family and is pin similar.

The device utilizes two time-interleaved 250MSPS unit A/Ds to achieve the ultimate sample rate of 500MSPS. A single 500MHz conversion clock is presented to the converter, and all interleave clocking is managed internally. The proprietary Interleave Engine (I2E) performs automatic fine correction of offset, gain, and sample time skew mismatches between the unit A/Ds to optimize performance. No external interleaving algorithm is required.

A serial peripheral interface (SPI) port allows for extensive configurability of the A/D. The SPI also controls the interleave correction circuitry, allowing the system to issue continuous calibration commands as well as configure many dynamic parameters.

Digital output data is presented in selectable LVDS or CMOS formats. The ISLA110P50 is available in a 72 Ld QFN package with an exposed paddle. Performance is specified over the full industrial temperature range (-40°C to +85°C).

Features

- 1.15GHz Analog Input Bandwidth
- 90fs Clock Jitter
- Automatic Fine Interleave Correction Calibration
- Multiple Chip Time Alignment Support via the Synchronous Clock Divider Reset
- Programmable Gain, Offset and Skew Control
- Over-Range Indicator
- Clock Phase Selection
- Nap and Sleep Modes
- Two's Complement, Gray Code or Binary Data Format
- DDR LVDS-Compatible or LVCMOS Outputs
- Programmable Test Patterns and Internal Temperature Sensor

Key Specifications

- SNR = 60.6dBFS for f_{IN} = 190MHz (-1dBFS)
- SFDR = 80dBc for f_{IN} = 190MHz (-1dBFS)
- Total Power Consumption = 441mW

Applications

- Radar and Electronic/Signal Intelligence
- Broadband Communications
- High-Performance Data Acquisition

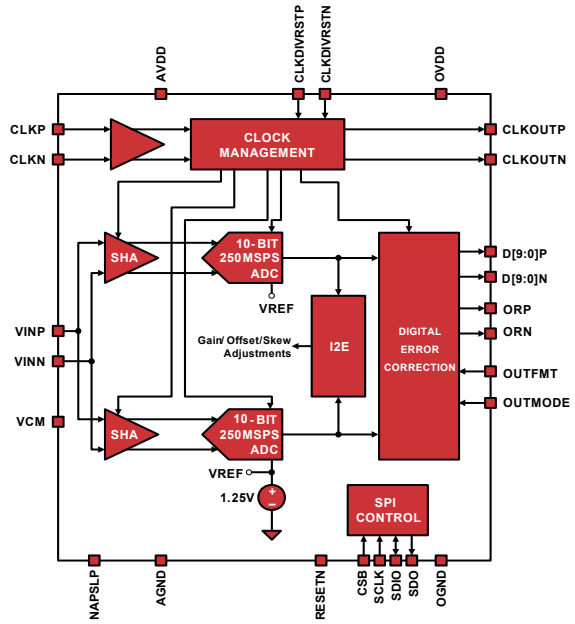

FIGURE 1A. BLOCK DIAGRAM

TABLE 1. PIN-COMPATIBLE FAMILY

MODEL	RESOLUTION	SPEED (MSPS)
ISLA112P50	12	500
ISLA110P50	10	500
ISLA118P50	8	500

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Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	SPEED (MSPS)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE	TEMP. RANGE
ISLA110P50IRZ	ISLA110P50 IRZ	500	72 Ld QFN	L72.10x10J	Tray	-40 to +85°C

NOTES:

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISLA110P50. For more information on MSL please see TB363.

Pin Configuration

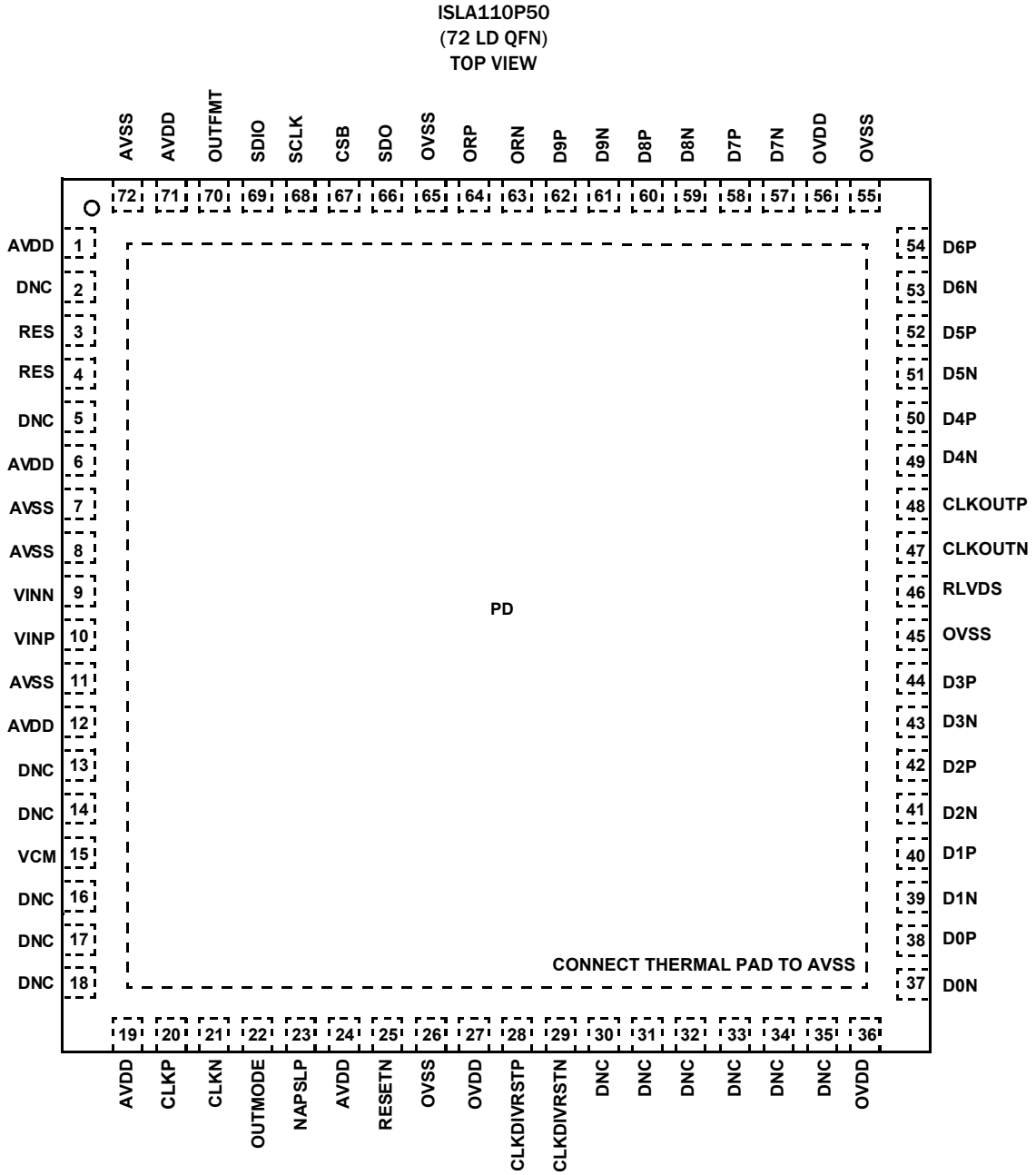


FIGURE 2. PIN CONFIGURATION

Pin Descriptions

PIN NUMBER	LVDS [LVCMOS] NAME	LVDS [LVCMOS] FUNCTION
1, 6, 12, 19, 24, 71	AVDD	1.8V Analog Supply
2, 5, 13, 14, 16, 17, 18, 30, 31, 32, 33, 34, 35	DNC	Do Not Connect
3, 4	RES	Reserved. **(4.7kΩ pull-up to OVDD is required for each of these pins)**
7, 8, 11, 72	AVSS	Analog Ground
9, 10	VINN, VINP	Analog Input Negative, Positive
15	VCM	Common Mode Output
20, 21	CLKP, CLKN	Clock Input True, Complement
22	OUTMODE	Tri-Level Output Mode (LVDS, LVCMOS)
23	NAPSLP	Tri-Level Power Control (Nap, Sleep modes)
25	RESETN	Power-on Reset (Active Low)
26, 45, 55, 65	OVSS	Output Ground
27, 36, 56	OVDD	1.8V Output Supply
28, 29	CLKDIVRSTP, CLKDIVRSTN	Sample Clock Synchronous Divider Reset Positive, Negative
37, 38	D0N, D0P [NC, D0]	LVDS Bit 0 Output Complement, True [NC, LVCMOS Bit 0]
39, 40	D1N, D1P [NC, D1]	LVDS Bit 1 Output Complement, True [NC, LVCMOS Bit 1]
41, 42	D2N, D2P [NC, D2]	LVDS Bit 2 Output Complement, True [NC, LVCMOS Bit 2]
43, 44	D3N, D3P [NC, D3]	LVDS Bit 3 Output Complement, True [NC, LVCMOS Bit 3]
46	RLVDS	LVDS Bias Resistor (connect to OVSS with a 10kΩ, 1% resistor)
47, 48	CLKOUTN, CLKOUTP [NC, CLKOUT]	LVDS Clock Output Complement, True [NC, LVCMOS CLKOUT]
49, 50	D4N, D4P [NC, D4]	LVDS Bit 4 Output Complement, True [NC, LVCMOS Bit 4]
51, 52	D5N, D5P [NC, D5]	LVDS Bit 5 Output Complement, True [NC, LVCMOS Bit 5]
53, 54	D6N, D6P [NC, D6]	LVDS Bit 6 Output Complement, True [NC, LVCMOS Bit 6]
57, 58	D7N, D7P [NC, D7]	LVDS Bit 7 Output Complement, True [NC, LVCMOS Bit 7]
59, 60	D8N, D8P [NC, D8]	LVDS Bit 8 Output Complement, True [NC, LVCMOS Bit 8]
61, 62	D9N, D9P [NC, D9]	LVDS Bit 9 (MSB) Output Complement, True [NC, LVCMOS Bit 9]
63, 64	ORN, ORP [NC, OR]	LVDS Over-Range Complement, True [NC, LVCMOS Over-Range]
66	SDO	SPI Serial Data Output **(4.7kΩ pull-up to OVDD is required)**
67	CSB	SPI Chip Select (active low)
68	SCLK	SPI Clock
69	SDIO	SPI Serial Data Input/Output
70	OUTFMT	Tri-Level Output Data Format (Two's Comp., Gray Code, Offset Binary)
PD	AVSS	Exposed Paddle. Analog Ground

NOTE: LVCMOS Output Mode Functionality is shown in brackets (NC = No Connection)

Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS . . . . . -0.3V to 0.3V
Analog Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS . . . . . -0.4V to OVDD + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
72 Ld QFN (Notes 3, 4, 5)	23	0.75

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. For solder stencil layout and reflow guidelines, see TB389.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -1dBFS, F_{IN} = 105MHz, f_{SAMPLE} = 500MSPS, after completion of I2E calibration.

PARAMETER	SYMBOL	CONDITIONS	ISLA110P50 (Note 6) MIN	TYP	MAX	UNITS
DC SPECIFICATIONS (Note 6)						
Analog Input						
Full-Scale Analog Input Range	V_{FS}	Differential	1.41	1.45	1.52	V_{P-P}
Input Resistance	R_{IN}	Differential		500		Ω
Input Capacitance	C_{IN}	Differential		1.9		pF
Full Scale Range Temp. Drift	A_{VTC}	Full Temp		325		ppm/°C
Input Offset Voltage	V_{OS}		-10	±2.0	10	mV
Gain Error	E_G			±2.0		%
Common-Mode Output Voltage	V_{CM}		435	535	635	mV
Clock Inputs						
Inputs Common Mode Voltage				0.9		V
CLKP, CLKN Input Swing			0.2	1.8		V
Power Requirements						
1.8V Analog Supply Voltage	AVDD		1.7	1.8	1.9	V
1.8V Digital Supply Voltage	OVDD		1.7	1.8	1.9	V
1.8V Analog Supply Current	IAVDD			173	186	mA
1.8V Digital Supply Current (Note 7)	I_{OVDD}	3mA LVDS, I2E powered down, Notch Filter powered down		79	86	mA
		3mA LVDS, I2E On, Notch Filter On		124		mA
Power Supply Rejection Ratio	PSRR	30MHz, 200mV_{P-P}		-36		dB
Total Power Dissipation						
Normal Mode	P_D	2mA LVDS, I2E powered down, Notch Filter powered down		441		mW
		3mA LVDS, I2E powered down, Notch Filter powered down		454	490	mW
		3mA LVDS, I2E On, Notch Filter powered down		520		mW
		3mA LVDS, I2E On, Notch Filter On		535		mW
Nap Mode	P_D			164	179	mW

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -1dBFS, F_{IN} = 105MHz, f_{SAMPLE} = 500MSPS, after completion of I2E calibration. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA110P50 (Note 6) MIN	TYP	MAX	UNITS
Sleep Mode	P_D			28	34	mW
Nap Mode Wakeup Time (Note 8)		Sample Clock Running		2.75		µs
Sleep Mode Wakeup Time (Note 8)		Sample Clock Running		1		ms
AC SPECIFICATIONS (Note 9)						
Differential Nonlinearity	DNL		-0.35	±0.15	0.35	LSB
Integral Nonlinearity	INL		-0.5	±0.2	0.5	LSB
Minimum Conversion Rate (Note 10)	f_S MIN				80	MSPS
Maximum Conversion Rate	f_S MAX		500			MSPS
Signal-to-Noise Ratio (Notes 11, 12)	SNR	f_{IN} = 10MHz		60.7		dBFS
		f_{IN} = 105MHz	59.9	60.7		dBFS
		f_{IN} = 190MHz		60.6		dBFS
		f_{IN} = 364MHz		60.3		dBFS
		f_{IN} = 495MHz		60.1		dBFS
		f_{IN} = 605MHz		59.7		dBFS
		f_{IN} = 995MHz		58.6		dBFS
Signal-to-Noise and Distortion (Notes 11, 12)	SINAD	f_{IN} = 10MHz		60.7		dBFS
		f_{IN} = 105MHz	59.8	60.7		dBFS
		f_{IN} = 190MHz		60.5		dBFS
		f_{IN} = 364MHz		60.0		dBFS
		f_{IN} = 495MHz		59.4		dBFS
		f_{IN} = 605MHz		57.9		dBFS
		f_{IN} = 995MHz		48.2		dBFS
Effective Number of Bits (Notes 11, 12)	ENOB	f_{IN} = 10MHz		9.79		Bits
		f_{IN} = 105MHz	9.60	9.79		Bits
		f_{IN} = 190MHz		9.77		Bits
		f_{IN} = 364MHz		9.68		Bits
		f_{IN} = 495MHz		9.58		Bits
		f_{IN} = 605MHz		9.33		Bits
		f_{IN} = 995MHz		7.71		Bits
Spurious-Free Dynamic Range (Notes 11, 12)	SFDR	f_{IN} = 10MHz		84		dBc
		f_{IN} = 105MHz	70	86		dBc
		f_{IN} = 190MHz		80		dBc
		f_{IN} = 364MHz		74		dBc
		f_{IN} = 495MHz		68		dBc
		f_{IN} = 605MHz		63		dBc
		f_{IN} = 995MHz		48		dBc
Intermodulation Distortion	IMD	f_{IN} = 70MHz		89		dBc
		f_{IN} = 170MHz		87		dBc
Word Error Rate	WER			10^{-12}		
Full Power Bandwidth	FPBW			1.15		GHz

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -1dBFS, F_{IN} = 105MHz, f_{SAMPLE} = 500MSPS, after completion of I2E calibration. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA110P50 (Note 6) MIN	TYP	MAX	UNITS
I2E SPECIFICATIONS						
Offset mismatch-induced spurious power		No I2E Calibration performed		-70		dBFS
		Active Run state enabled		-81		dBFS
I2E Settling Times	I2Epost_t	Calibration settling time for Active Run state			1000	ms
Minimum Duration of Valid Analog Input (Note 13)	t_{TE}	Allow one I2E iteration of Offset, Gain and Phase correction			500	µs
Largest Interleave Spur		f_{IN} = 10MHz to 240MHz, Active Run State enabled, in Track Mode		-94		dBc
		f_{IN} = 10MHz to 240MHz, Active Run State enabled and previously settled, in Hold Mode		-82		dBc
		f_{IN} = 260MHz to 490MHz, Active Run State enabled, in Track Mode		-89		dBc
		f_{IN} = 260MHz to 490MHz, Active Run State enabled and previously settled, in Hold Mode		-79		dBc
Total Interleave Spurious Power		Active Run State enabled, in Track Mode, f_{IN} is a broadband signal in the 1st Nyquist zone		-90		dBc
		Active Run State enabled, in Track Mode, f_{IN} is a broadband signal in the 2nd Nyquist zone		-85		dBc
Sample Time Mismatch Between Unit A/Ds		Active Run State enabled, in Track Mode		30		fs
Gain Mismatch Between Unit A/Ds				0.01		%
Offset Mismatch Between Unit A/Ds				1		mV

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Digital Supply Current is dependent upon the capacitive loading of the digital outputs. I_{OVDD} specifications apply for 10pF load on each digital output.
8. See “Nap/Sleep” for more detail.
9. AC Specifications apply after internal calibration of the A/D is invoked at the given sample rate and temperature. Refer to “Power-On Calibration” and “User Initiated Reset” for more detail.
10. The DLL Range setting must be changed for low speed operation.
11. The offset mismatch-induced spur energy, which occurs at $f_{SAMPLE}/2$, is not included in any specification unless otherwise noted.
12. This specification only applies when I2E is in Active Run state, and in Track Mode.
13. Limits are specified over the full operating temperature and voltage range and are established by characterization and not production tested.

Digital Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS INPUTS						
Input Current High (SDIO, RESETN, CSB, SCLK)	I_{IH}	V_{IN} = 1.8V	0	1	10	µA
Input Current Low (SDIO, RESETN, CSB, SCLK)	I_{IL}	V_{IN} = 0V	-25	-12	-5	µA
Input Voltage High (SDIO, RESETN, CSB, SCLK)	V_{IH}		1.17			V
Input Voltage Low (SDIO, RESETN, CSB, SCLK)	V_{IL}				0.63	V

Digital Specifications (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current High (OUTMODE, NAPSLP, OUTFMT) (Note 14)	I_{IH}		15	25	40	µA
Input Current Low (OUTMODE, NAPSLP, OUTFMT)	I_{IL}		-40	25	-15	µA
Input Capacitance	C_{DI}			3		pF
LVDS INPUTS (ClkdivrstP, ClkdivrstN)						
Input Common Mode Range	V_{ICM}		825		1575	mV
Input Differential Swing (peak to peak, single ended)	V_{ID}		250		450	mV
Input Pull-up and Pull-down Resistance	R_{Ipu}			1		MΩ
LVDS OUTPUTS						
Differential Output Voltage (Note 15)	V_T	3mA Mode		620		mV_{P-P}
Output Offset Voltage	V_{OS_LVDS}	3mA Mode	950	965	980	mV
Output Rise Time	t_R			625		ps
Output Fall Time	t_F			625		ps
CMOS OUTPUTS						
Voltage Output High	V_{OH}	I_{OH} = -500µA	OVDD - 0.3	OVDD - 0.1		V
Voltage Output Low	V_{OL}	I_{OL} = 1mA		0.1	0.3	V
Output Rise Time	t_R			2		ns
Output Fall Time	t_F			2		ns

Timing Diagrams

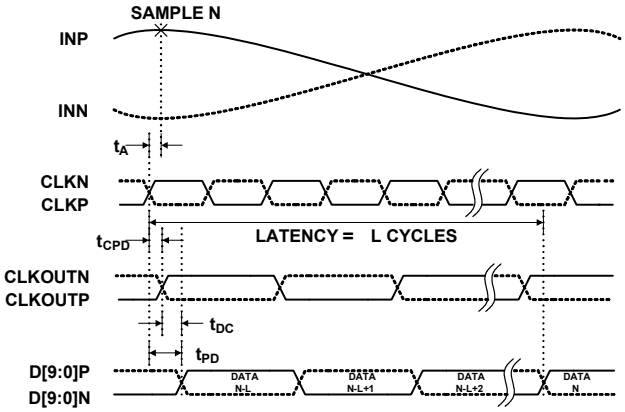


FIGURE 3. LVDS TIMING DIAGRAM

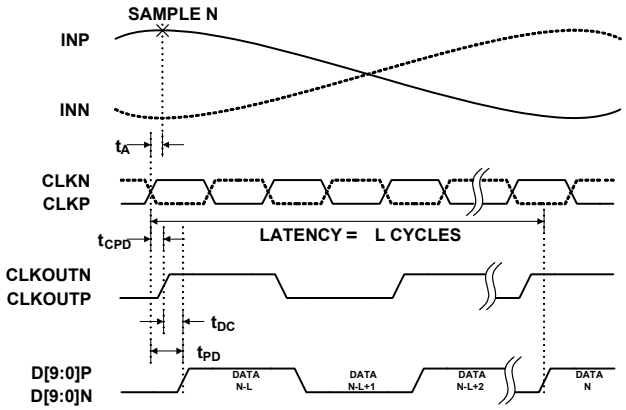


FIGURE 4. CMOS TIMING DIAGRAM

Switching Specifications

PARAMETER	CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
A/D OUTPUT						
Aperture Delay		t_A		375		ps
RMS Aperture Jitter		j_A		90		fs
Input Clock to Output Clock Propagation Delay	AVDD, OVDD = 1.8V, T_A = +25°C	t_{CPD}	2.6	2.9	3.3	ns
	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	t_{CPD}	2.0	2.6	3.6	ns
Relative Input Clock to Output Clock Propagation Delay Matching (Note 16)	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	dt_{CPD}	-450		450	ps
Input Clock to Data Propagation Delay, LVDS Mode		t_{PD}	1.74	2.6	3.83	ns
Output Clock to Data Propagation Delay (Note 13)	LVDS or CMOS Mode	t_{DC}	-250	0	250	ps
Synchronous Clock Divider Reset Setup Time (with respect to the positive edge of CLKP)		t_{RSTS}	300	75		ps
Synchronous Clock Divider Reset Hold Time (with respect to the positive edge of CLKP)		t_{RSTH}	450	150		ps
Synchronous Clock Divider Reset Recovery Time	DLL recovery time after Synchronous Reset	t_{RSTRT}			52	µs
Latency (Pipeline Delay) (Note 17)		L		17		cycles
Overvoltage Recovery		t_{OVR}		1		cycles
SPI INTERFACE (Notes 18, 19)						
SCLK Period	Write Operation	t_{CLK}	32			cycles (Note 18)
	Read Operation	t_{CLK}	132			cycles
CSB↓ to SCLK↑ Setup Time	Read or Write	t_S	2			cycles
CSB↑ after SCLK↑ Hold Time	Read or Write	t_H	11			cycles
Data Valid to SCLK↑ Setup Time	Write	t_{DSW}	2			cycles
Data Valid after SCLK↑ Hold Time	Write	t_{DHW}	8			cycles
Data Valid after SCLK↓ Time	Read	t_{DVR}			33	cycles
Data Invalid after SCLK↑ Time	Read	t_{DHR}	6			cycles
Sleep Mode CSB↓ to SCLK↑ Setup Time (Note 20)	Read or Write in Sleep Mode	t_S	150			µs

NOTES:

14. The Tri-Level Inputs internal switching thresholds are approximately 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
15. The voltage is expressed in peak-to-peak differential swing. The peak-to-peak singled-ended swing is 1/2 of the differential swing.
16. The relative propagation delay is the timing of the output clock of any A/D with respect to the nominal timing of any other A/D, given that all devices are clocked at the same time and are matched in temperature and voltage. It is specified over the full operating temperature and voltage range, and is established by characterization and not production tested.
17. The pipeline latency of this converter is fixed.
18. SPI Interface timing is directly proportional to the A/D sample period (t_{SAMPLE}).
19. The SPI may operate asynchronously with respect to the A/D sample clock.
20. The CSB setup time increases in sleep mode due to the reduced power state, CSB setup time in Nap mode is equal to normal mode CSB setup time (4ns min).

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS.

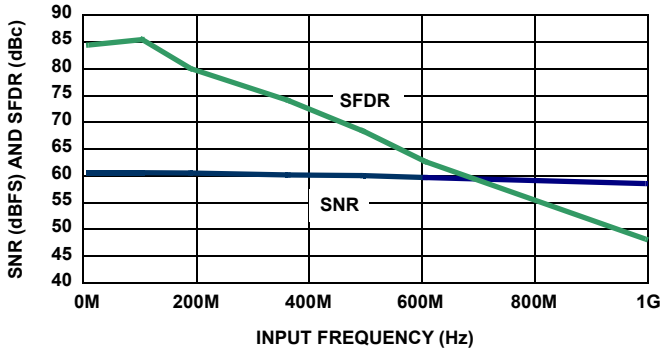


FIGURE 5. SNR AND SFDR vs f_{IN}

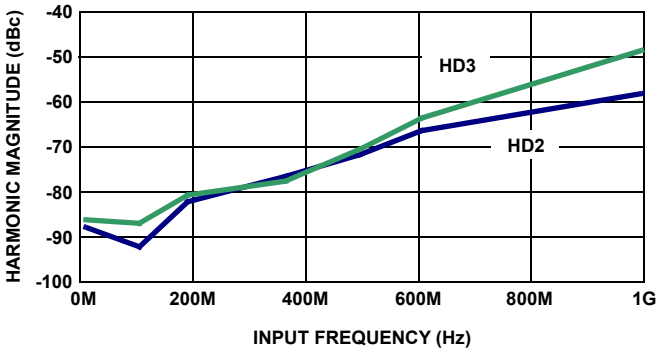


FIGURE 6. HD2 AND HD3 vs f_{IN}

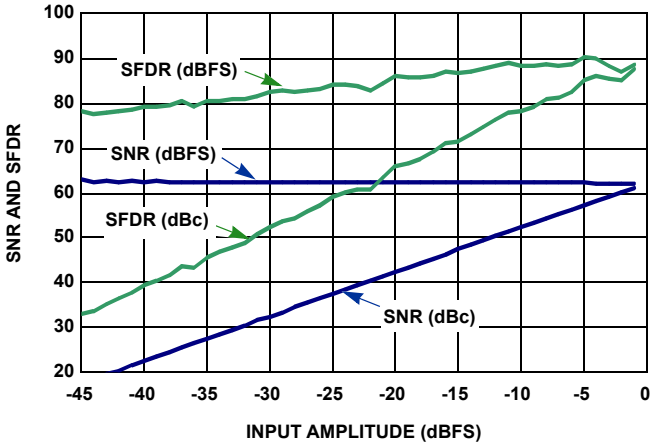


FIGURE 7. SNR AND SFDR vs A_{IN}

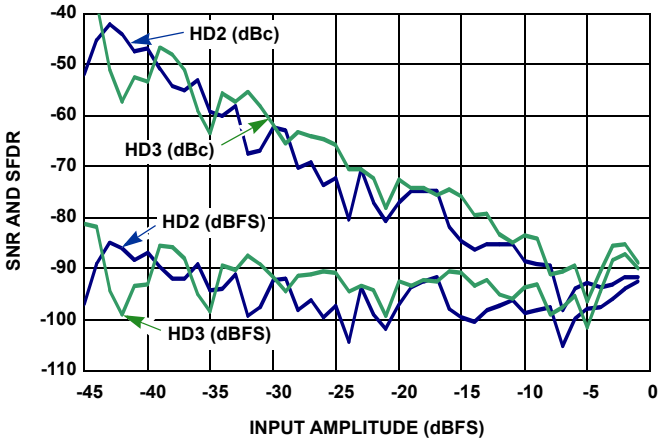


FIGURE 8. HD2 AND HD3 vs A_{IN}

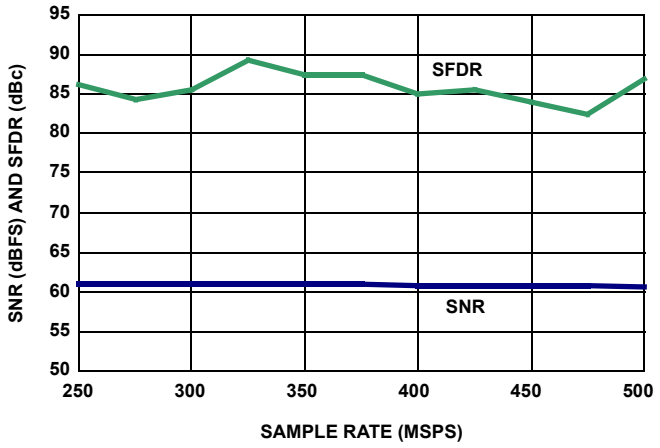


FIGURE 9. SNR AND SFDR vs f_{SAMPLE}

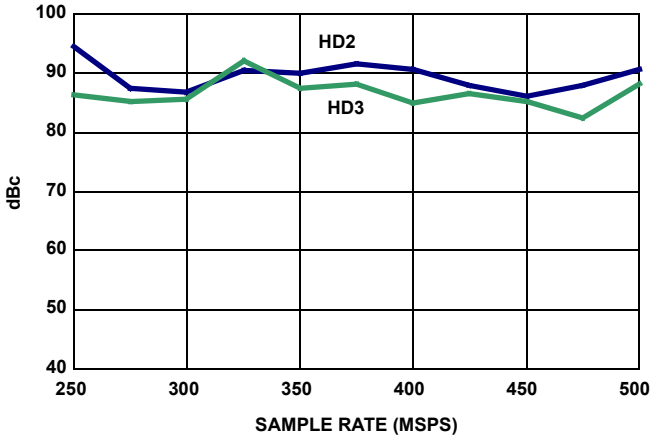


FIGURE 10. HD2 AND HD3 vs f_{SAMPLE}

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

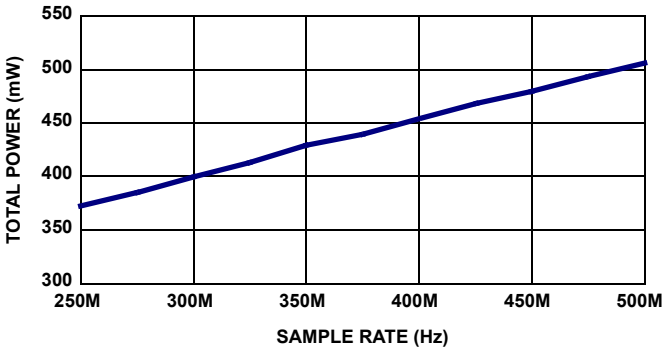


FIGURE 11. POWER vs f_{SAMPLE} IN 3mA LVDS MODE

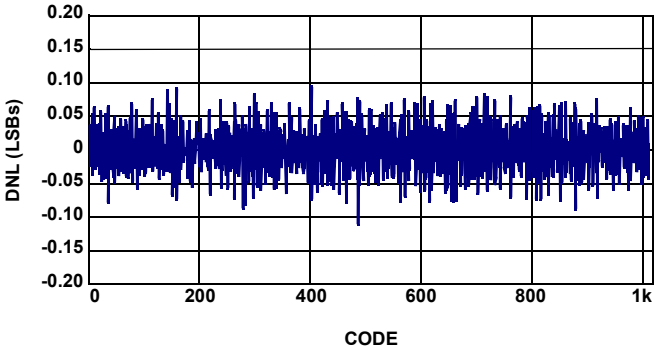


FIGURE 12. DIFFERENTIAL NONLINEARITY

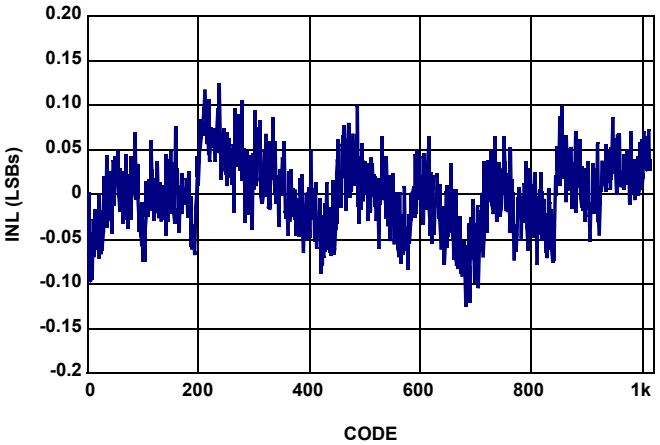


FIGURE 13. INTEGRAL NONLINEARITY

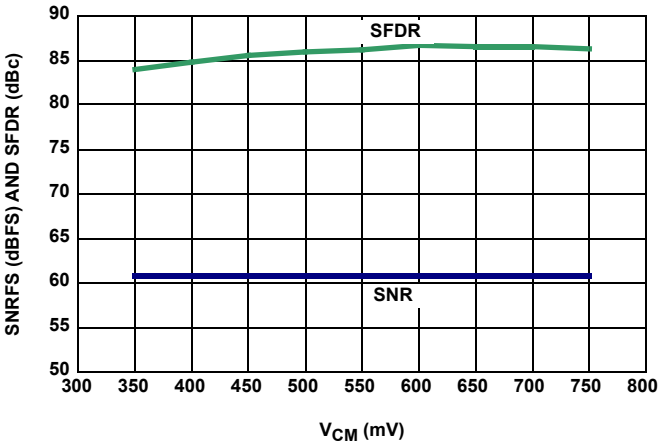


FIGURE 14. SNR AND SFDR vs VCM

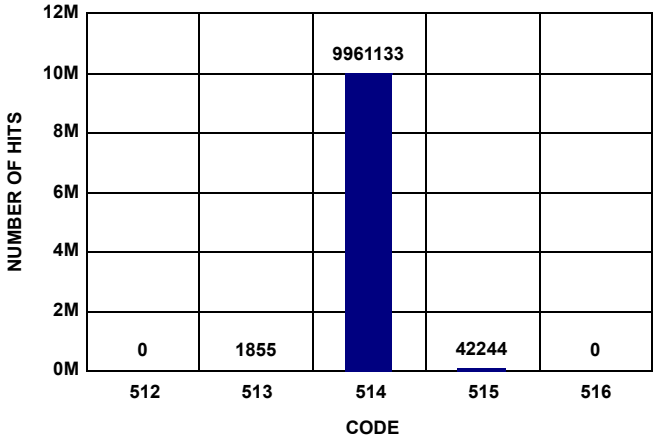


FIGURE 15. NOISE HISTOGRAM

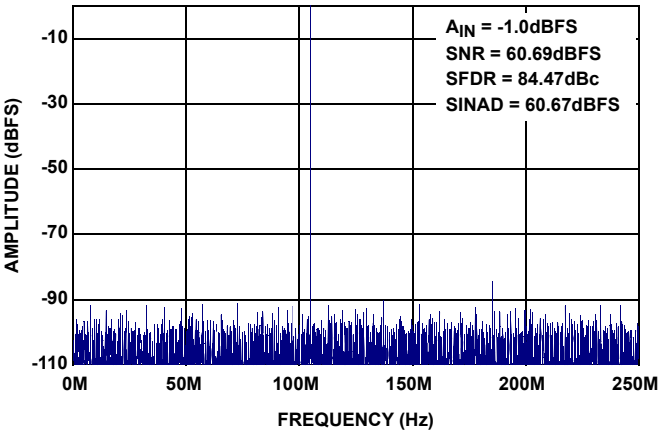


FIGURE 16. SINGLE-TONE SPECTRUM @ 105MHz

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

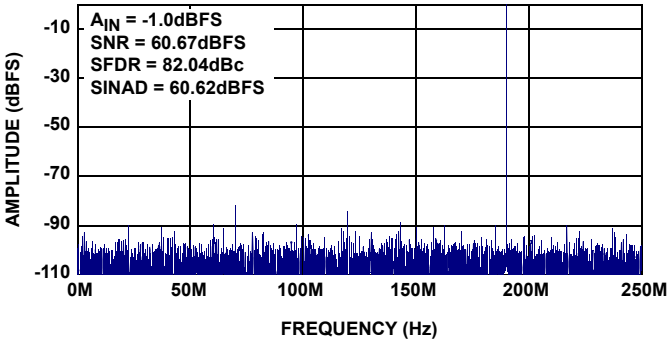


FIGURE 17. SINGLE-TONE SPECTRUM @ 190MHz

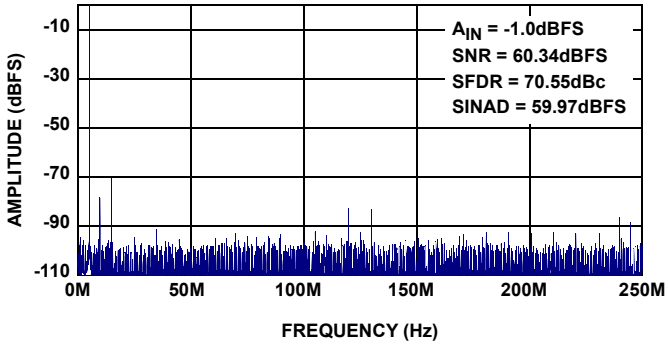


FIGURE 18. SINGLE-TONE SPECTRUM @ 495MHz

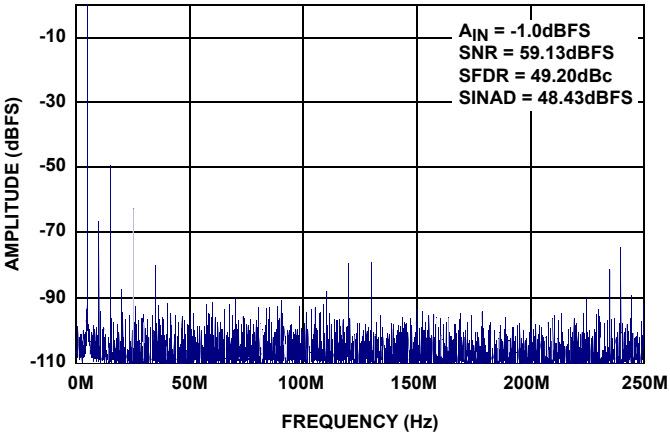


FIGURE 19. SINGLE-TONE SPECTRUM @ 995MHz

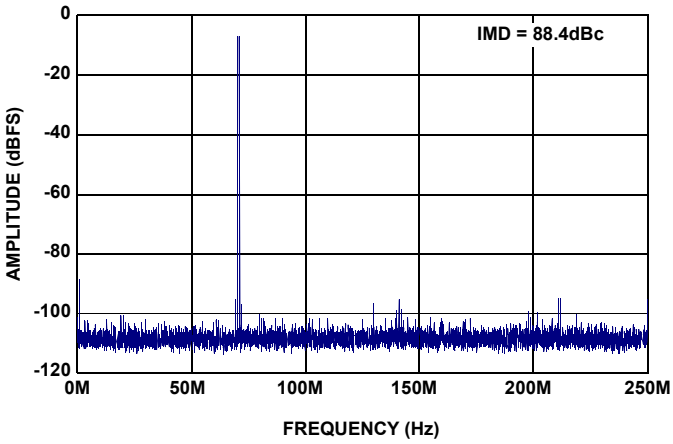


FIGURE 20. TWO-TONE SPECTRUM @ 70MHz (1MHz SPACING)

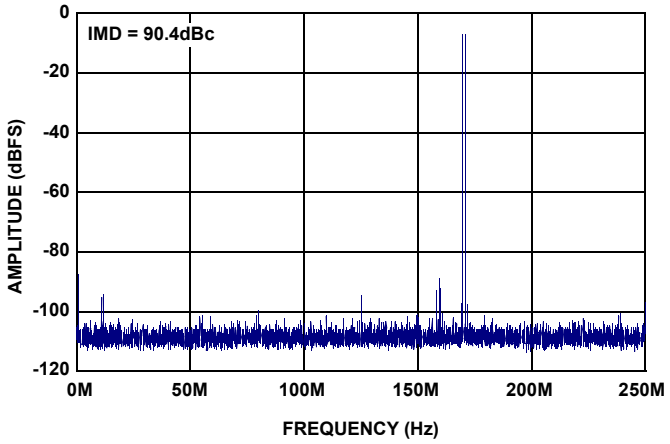


FIGURE 21. TWO-TONE SPECTRUM @ 170MHz (1MHz SPACING)

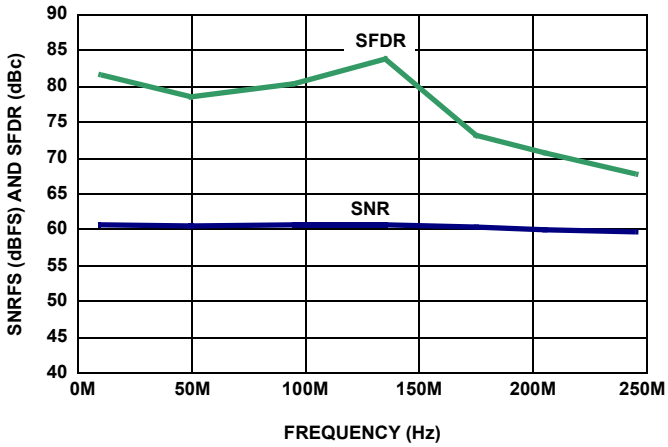


FIGURE 22. INPUT FREQUENCY SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED @ 105MHz

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -1dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

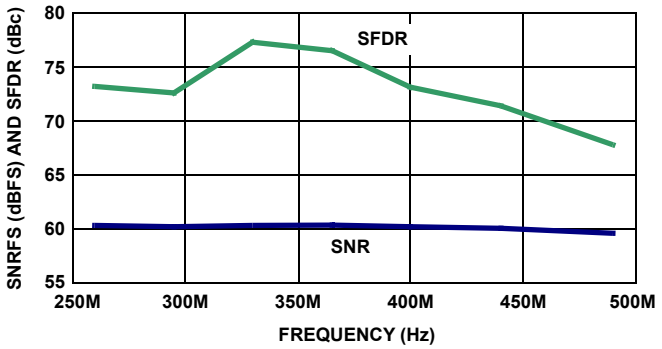


FIGURE 23. INPUT FREQUENCY SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED @ 330MHz

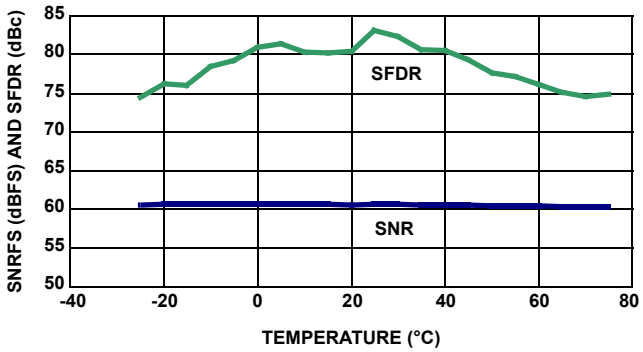


FIGURE 24. TEMPERATURE SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED

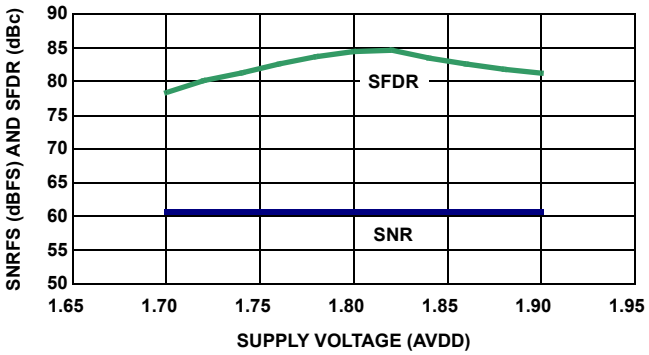


FIGURE 25. ANALOG SUPPLY VOLTAGE SWEEP WITH I2E FROZEN, I2E PREVIOUSLY CALIBRATED

Theory of Operation

Functional Description

The ISLA110P50 is based upon a 12-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (Figure 26). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. The converter pipeline requires twelve samples to produce a result. Digital error correction is also applied, resulting in a total latency of 17 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

The device contains two core A/D converters with carefully matched transfer characteristics. The cores are clocked on alternate clock edges, resulting in a doubling of the sample rate.

Time–interleaved A/D systems can exhibit non–ideal artifacts in the frequency domain if the individual core A/D characteristics are not well matched. Gain, offset and timing skew mismatches are of primary concern.

The Interleave Engine (I2E) performs automatic interleave calibration for the offset, gain, and sample time skew mismatch between the core A/Ds. The I2E circuitry also adjusts in real-time for temperature and voltage variations.

Residual gain and sample time skew mismatch result in fundamental image spurs at $f_{NYQUIST} \pm f_{IN}$. Offset mismatches create spurs at DC and multiples of $f_{NYQUIST}$.

Power-On Calibration

As mentioned previously, the cores perform a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO (pin 66) must be high
- RESETN (pin 25) must begin low
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

Pins 3, 4, and SDO require an external 4.7kΩ pull-up to OVDD. If these pins are pulled low externally during power-up, calibration will not be executed properly.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with a drive strength in its high impedance state of less than 0.5mA.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 27. The over-range output (OR) is set high once RESETN is pulled low, and remains in that state until calibration is complete. The OR output returns to normal operation at that time, so it is important that the analog input be within the converter's full-scale range to observe the transition. If the input is in an over-range condition the OR pin will stay high, and it will not be possible to detect the end of the calibration cycle.

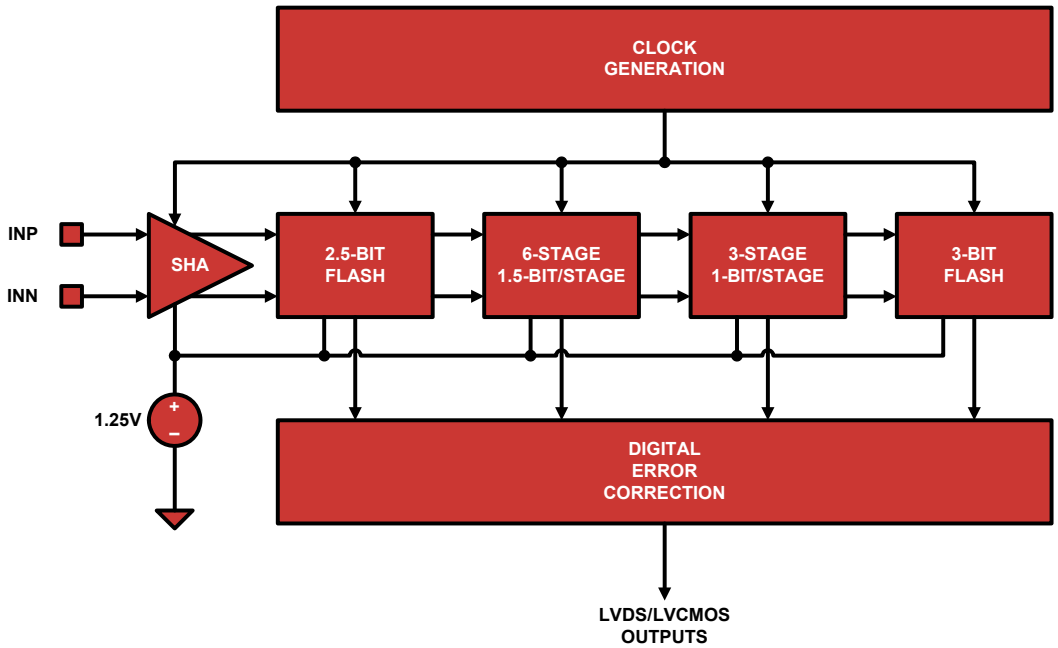


FIGURE 26. A/D CORE BLOCK DIAGRAM

While RESETN is low, the output clock (CLKOUTP/CLKOUTN) is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is deasserted. At 500MSPS the nominal calibration time is 200ms, while the maximum calibration time is 550ms.

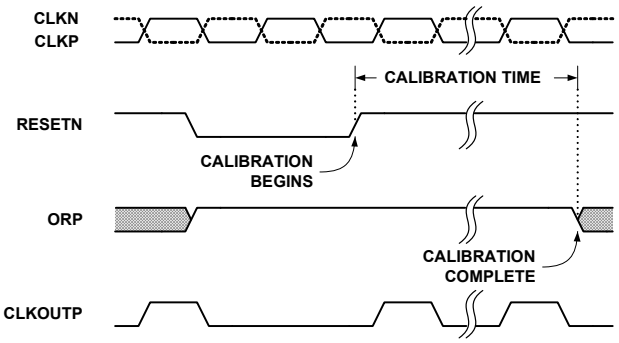


FIGURE 27. CALIBRATION TIMING

User Initiated Reset

Recalibration of the A/D can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, the SDO, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA110P50 changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the A/D under the environmental conditions at which it will operate.

A supply voltage variation of less than 100mV will generally result in an SNR change of less than 0.5dBFS and SFDR change of less than 3dBc.

In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS will typically result in an SNR change of less than 0.5dBFS and an SFDR change of less than 3dBc.

Figures 28 and 29 show the effect of temperature on SNR and SFDR performance with power-on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power-on calibration at -40°C, +25°C and +85°C. Best performance is typically achieved by a user-initiated power-on calibration at the operating conditions, as stated earlier. However, it can be seen that performance drift with temperature is not a very strong function of the temperature at which the power-on calibration is performed. To achieve the performance demonstrated in the SFDR plot, I2E must be in Track mode.

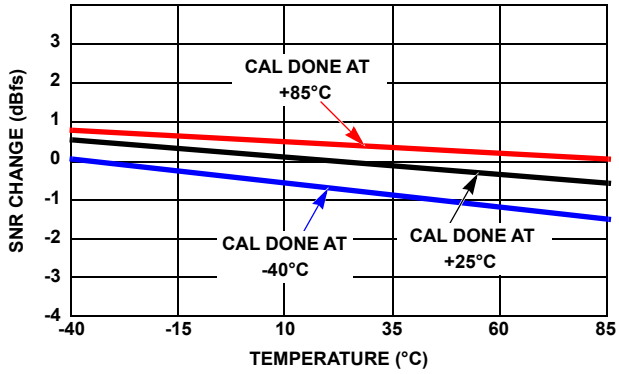


FIGURE 28. SNR PERFORMANCE vs TEMPERATURE AFTER +25°C CALIBRATION

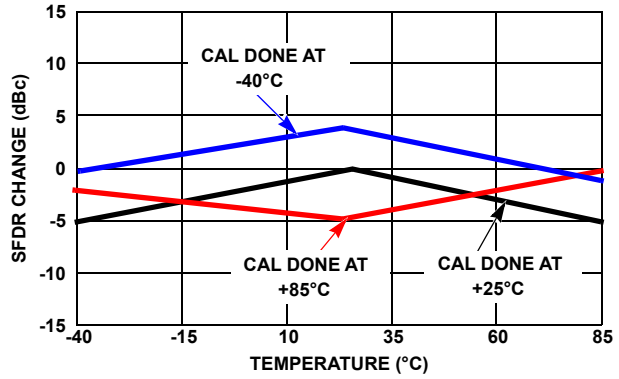


FIGURE 29. SFDR PERFORMANCE vs TEMPERATURE AFTER +25°C CALIBRATION

Analog Input

A single fully differential input (VINP/VINN) connects to the sample and hold amplifier (SHA) of each unit A/D. The ideal full-scale input voltage is 1.45V, centered at the VCM voltage of 0.535V as shown in Figure 30.

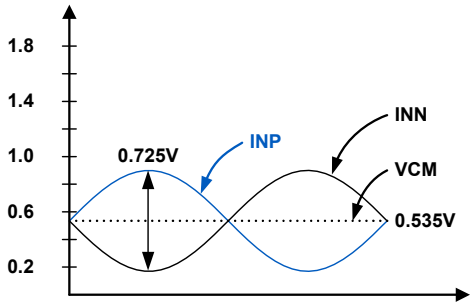


FIGURE 30. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 31 through 33. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 31 and 32.

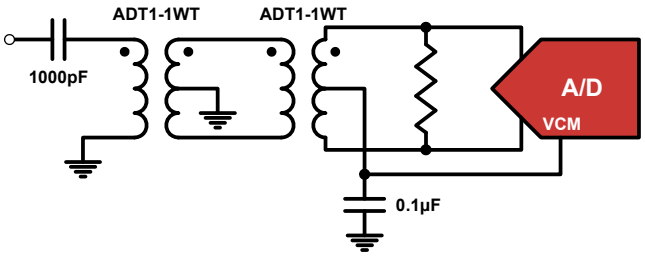


FIGURE 31. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

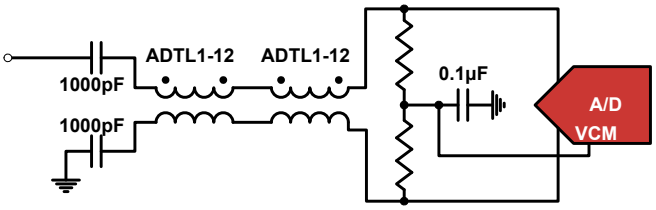


FIGURE 32. TRANSMISSION LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA110P50 is 500Ω.

The SHA design uses a switched capacitor input stage (see Figure 47), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 1:1 transformer and low shunt resistance are recommended for optimal performance.

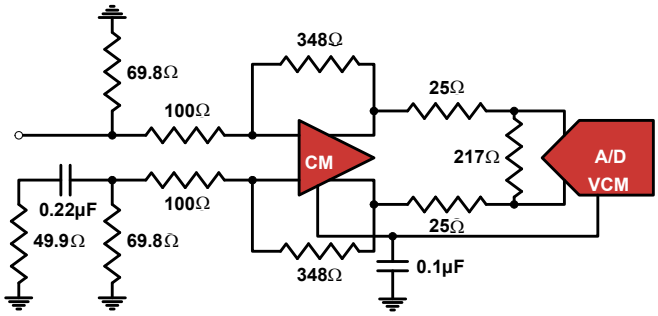


FIGURE 33. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in Figure 33, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance.

Clock Input

The clock input circuit is a differential pair (see Figure 48). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 34. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate AC coupling.

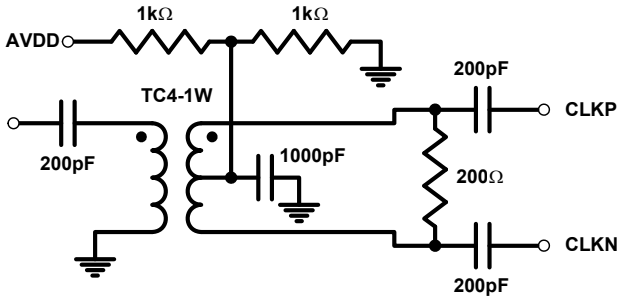


FIGURE 34. RECOMMENDED CLOCK DRIVE

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 35.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

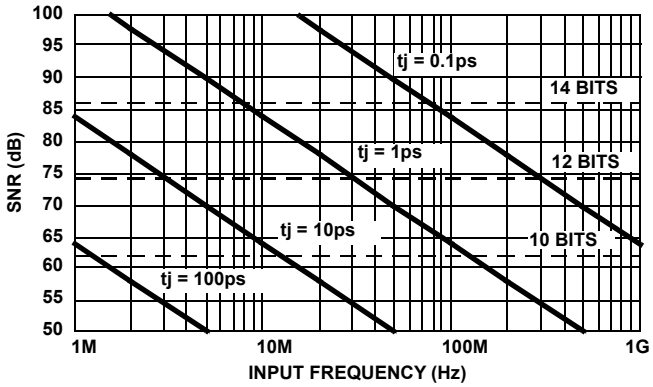


FIGURE 35. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure 3. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Voltage Reference

A temperature compensated voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

Digital Outputs

Output data is available as a parallel bus in LVDS-compatible or CMOS modes. In either case, the data is presented in double data rate (DDR) format. Figures 3 and 4 show the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3mA or a power-saving 2mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the A/D. The applicability of this setting is dependent upon the PCB layout, therefore the user should experiment to determine if performance degradation is observed.

The output mode and LVDS drive current are selected via the OUTMODE pin as shown in Table 2.

TABLE 2. OUTMODE PIN SETTINGS

OUTMODE PIN	MODE
AVSS	LVCMOS
Float	LVDS, 3mA
AVDD	LVDS, 2mA

The output mode can also be controlled through the SPI port, which overrides the OUTMODE pin setting. Details on this are contained in "Serial Peripheral Interface" on page 22.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDS pin to OVSS.

Over-Range Indicator

The over-range (OR) bit is asserted when the output code reaches positive full-scale (e.g., 0xFFF in offset binary mode). The output code does not wrap around during an over-range condition. The OR bit is updated at the sample rate.

Power Dissipation

The power dissipated by the ISLA110P50 is primarily dependent on the sample rate and the output modes: LVDS vs CMOS and DDR vs SDR. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation changes to a lesser degree in LVDS mode, but is more strongly related to the clock frequency in CMOS mode.

Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the A/D is not required. Two power saving modes are available: Nap and Sleep. Nap mode reduces power dissipation to less than 164mW and recovers to normal operation in approximately 2.75µs. Sleep mode reduces power dissipation to less than 6mW but requires approximately 1ms to recover from a sleep command.

Wake-up time from sleep mode is dependent on the state of CSB; in a typical application CSB would be held high during sleep, requiring a user to wait 150µs max after CSB is asserted (brought low) prior to writing '001x' to SPI Register 25. The device would be fully powered up, in normal mode 1ms after this command is written.

Wake-up from Sleep Mode Sequence (CSB high)

- Pull CSB Low
- Wait 150µs
- Write '001x' to Register 25
- Wait 1ms until A/D fully powered on

In an application where CSB was kept low in sleep mode, the 150µs CSB setup time is not required as the SPI registers are powered on when CSB is low, the chip power dissipation increases by ~15mW in this case. The 1ms wake-up time after the write of a '001x' to register 25 still applies. It is generally recommended to keep CSB high in sleep mode to avoid any unintentional SPI activity on the A/D.

All digital outputs (Data, CLKOUT and OR) are placed in a high impedance state during Nap or Sleep. The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to 52µs to regain lock at 250MSPS.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 3.

TABLE 3. NAPSLP PIN SETTINGS

NAPSLP PIN	MODE
AVSS	Normal
Float	Sleep
AVDD	Nap

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in "Serial Peripheral Interface" on page 22. This is an indexed function when controlled from the SPI, but a global function when driven from the pin.

Data Format

Output data can be presented in three formats: two's complement, Gray code and offset binary. The data format is selected via the OUTFMT pin as shown in Table 4.

TABLE 4. OUTFMT PIN SETTINGS

OUTFMT PIN	MODE
AVSS	Offset Binary
Float	Two's Complement
AVDD	Gray Code

The data format can also be controlled through the SPI port, which overrides the OUTFMT pin setting. Details on this are contained in "Serial Peripheral Interface" on page 22.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 36 shows this operation.

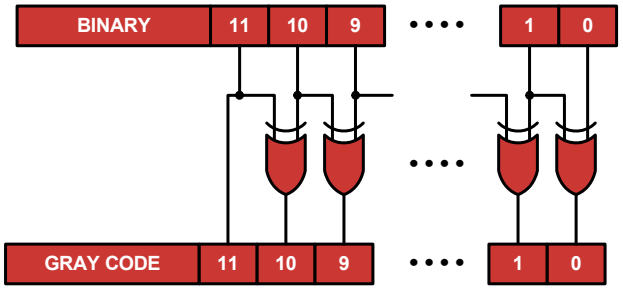


FIGURE 36. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 37.

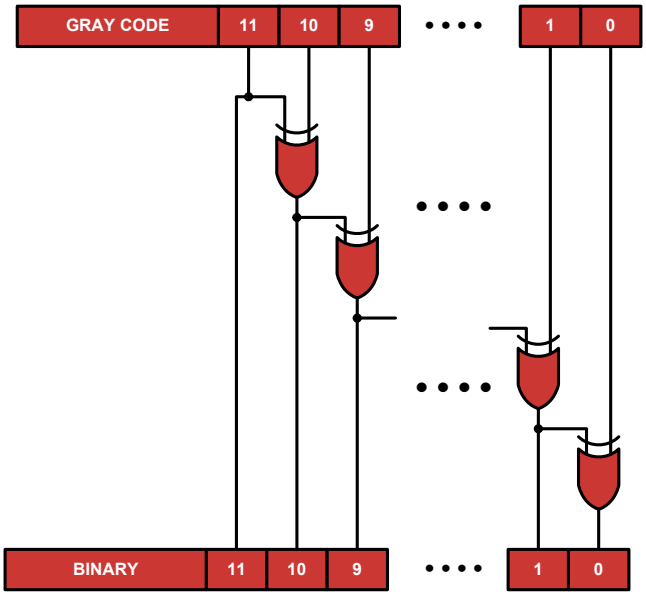


FIGURE 37. GRAY CODE TO BINARY CONVERSION

Mapping of the input voltage to the various data formats is shown in Table 5.

TABLE 5. INPUT VOLTAGE TO OUTPUT CODE MAPPING

INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT	GRAY CODE
-Full Scale	000 00 000 00 00	100 00 000 00 00	000 00 000 00 00
-Full Scale +1LSB	000 00 000 00 01	100 00 000 00 01	000 00 000 00 01
Mid–Scale	100 00 000 00 00	000 00 000 00 00	110 00 000 00 00
+Full Scale -1LSB	111 11 111 11 10	011 11 111 11 10	100 00 000 00 01
+Full Scale	111 11 111 11 11	011 11 111 111 1	100 00 000 00 00

I2E Requirements and Restrictions

Overview

I2E is a blind and background capable algorithm, designed to transparently eliminate interleaving artifacts. This circuitry eliminates interleave artifacts due to offset, gain, and sample time mismatches between unit A/Ds, and across supply voltage and temperature variations in real-time.

Differences in the offset, gain, and sample times of time-interleaved A/Ds create artifacts in the digital outputs. Each of these artifacts creates a unique signature that may be detectable in the captured samples. The I2E algorithm optimizes performance by detecting error signatures and adjusting each unit A/D using minimal additional power.

The I2E algorithm can be put in Active Run state via SPI. When the I2E algorithm is in Active Run state, it detects and corrects for offset, gain, and sample time mismatches in real time (see Track Mode description in the "Active Run State" section). However, certain analog input characteristics can obscure the estimation of these mismatches. The I2E algorithm is capable of detecting these obscuring analog input characteristics, and as long as they are present, I2E will stop updating the correction in real time. Effectively, this freezes the current correction circuitry to the last known good state (see Hold Mode description in the "Active Run State" section). Once the analog input signal stops obscuring the interleaved artifacts, the I2E algorithm will automatically start correcting for mismatch in real time again.

Active Run State

During the Active Run state the I2E algorithm actively suppresses artifacts due to interleaving based on statistics in the digitized data. I2E has two modes of operation in this state (described below), dynamically chosen in real-time by the algorithm based on the statistics of the analog input signal.

Track Mode refers to the default state of the algorithm, when all artifacts due to interleaving are actively being eliminated. To be in Track Mode the analog input signal to the device must adhere to the following requirements:

- Possess total power greater than -20dBFS, integrated from 1MHz to Nyquist but excluding signal energy in a 100kHz band centered at $f_S/4$

The criteria above assumes 500MSPS operation; the frequency bands should be scaled proportionally for lower sample rates. Note that the effect of excluding energy in the 100kHz band around of $f_S/4$ exists in every Nyquist zone. This band generalizes to the form ($N*f_S/4$-50kHz) to ($N*f_S/4$+50kHz), where N is any odd integer. An input signal that violates these criteria briefly (approximately 10µs), before and after which it meets this criteria, will not impact system performance.

The algorithm must be in Track Mode for approximately one second (defined as I2Epost_t in the specification table on page 7) after power-up before the specifications apply. Once this requirement has been met, the specifications of the device will continue to be met while I2E remains in Track Mode, even in the presence of temperature and supply voltage changes.

Hold Mode refers to the state of the I2E algorithm when the analog input signal does not meet the requirements specified above. If the algorithm detects that the signal no longer meets the criteria, it automatically enters Hold Mode. In Hold Mode, the I2E circuitry freezes the adjustment values based on the most recent set of valid input conditions. However, in Hold Mode, the I2E circuitry will not correct for new changes in interleave artifacts induced by supply voltage and temperature changes. The I2E circuitry will remain in Hold Mode until such time as the analog input signal meets the requirements for Track Mode.

Power Meter

The power meter calculates the average power of the analog input, and determines if it's within range to allow operation in Track Mode. Both AC RMS and total RMS power are calculated, and there are separate SPI programmable thresholds and hysteresis values for each.

Notch Filter

A digital filter removes the signal energy in a 100kHz band around $f_S/4$ before the I2E circuitry uses these samples for estimating offset, gain, and sample time mismatches (data samples produced by the A/D are unaffected by this filtering). This allows the I2E algorithm to continue in Active Run state while in the presence of a large amount of input energy near the $f_S/4$ frequency. This filter can be powered down if it's known that the signal characteristics won't violate the restrictions. Powering down the Notch filter will reduce power consumption by approximately 70mW.

Nyquist Zones

The I2E circuitry allows the use of any one Nyquist zone without configuration, but requires the use of only one Nyquist zone. Inputs that switch dynamically between Nyquist zones will cause poor performance for the I2E circuitry. For example, I2E will function properly for a particular application that has f_S = 500MSPS and uses the 1st Nyquist zone (0MHz to 250MHz). I2E will also function properly for an application that uses f_S = 500MSPS and the 2nd Nyquist zone (250MHz to 500MHz). I2E will not function properly for an application that uses f_S = 500MSPS, and input frequency bands from 150MHz to 210MHz and 250MHz to 290MHz simultaneously. There is no need to configure the I2E algorithm to use a particular Nyquist zone, but no dynamic switching between Nyquist zones is permitted while I2E is running.

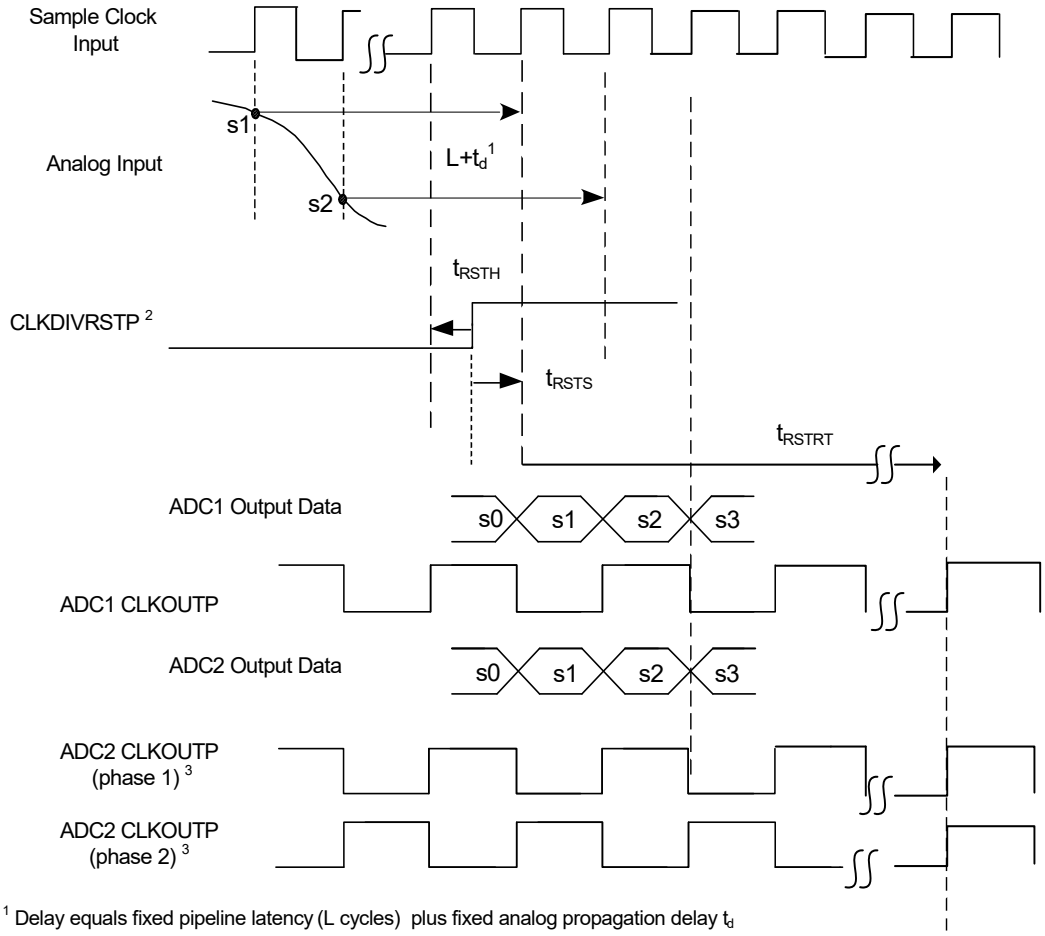
Configurability and Communication

I2E can respond to status queries, be turned on and turned off, and generally configured via SPI programmable registers. Configuring of I2E is generally unnecessary unless the application cannot meet the requirements of Track Mode on or after power up. Parameters that can be adjusted and read back include Notch filter threshold and status, Power Meter threshold and status, and initial values for the offset, gain, and sample time values to use when I2E starts.

Clock Divider Synchronous Reset

An output clock (CLKOUTP, CLKOUTN) is provided to facilitate latching of the sampled data. This clock is at half the frequency of the sample clock, and the absolute phase of the output clocks for multiple A/Ds is indeterminate. This feature allows the phase of multiple A/Ds to be synchronized (refer to Figure 38), which greatly simplifies data capture in systems employing multiple A/Ds.

The reset signal must be well-timed with respect to the sample clock (see “Switching Specifications” on page 9).



[1] Delay equals fixed pipeline latency (L cycles) plus fixed analog propagation delay t_d

[2] CLKDIVRSTP setup and hold times are with respect to input sample clock rising edge. CLKDIVRSTN is not shown, but must be driven, and is the compliment of CLKDIVRSTP

[3] Either Output Clock Phase (phase 1 or phase 2) equally likely prior to synchronization

FIGURE 38. SYNCHRONOUS RESET OPERATION

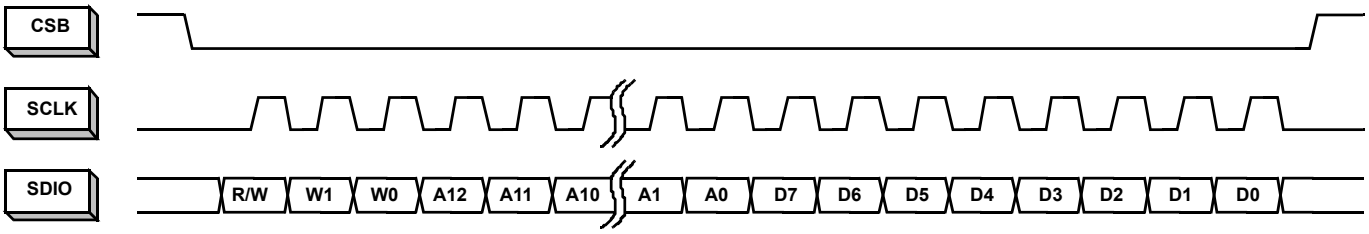


FIGURE 39. MSB-FIRST ADDRESSING

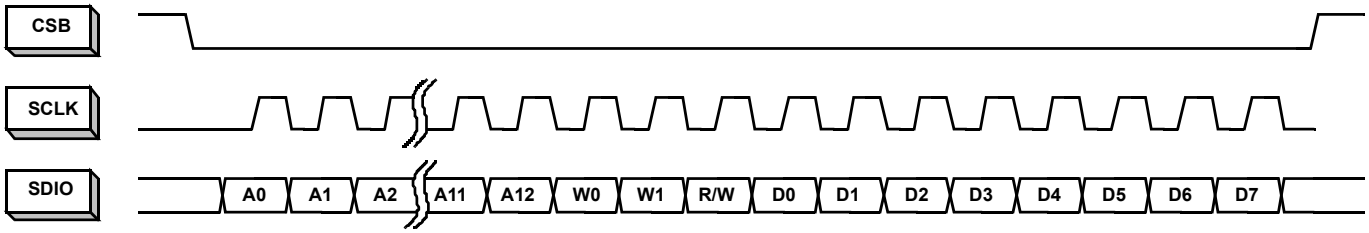


FIGURE 40. LSB-FIRST ADDRESSING

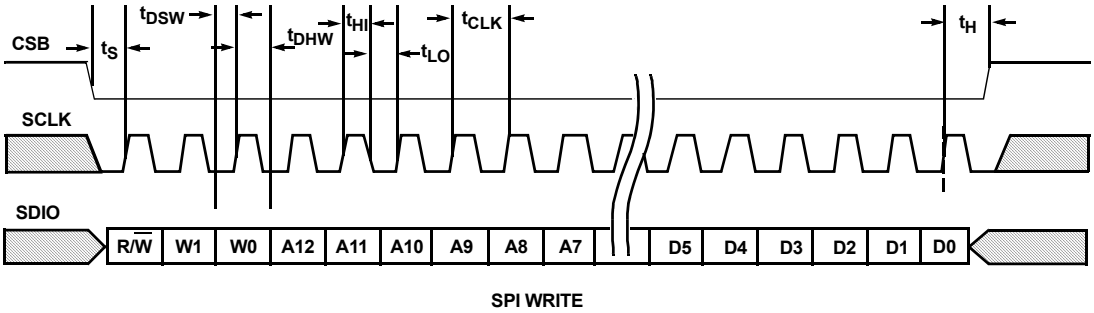


FIGURE 41. SPI WRITE

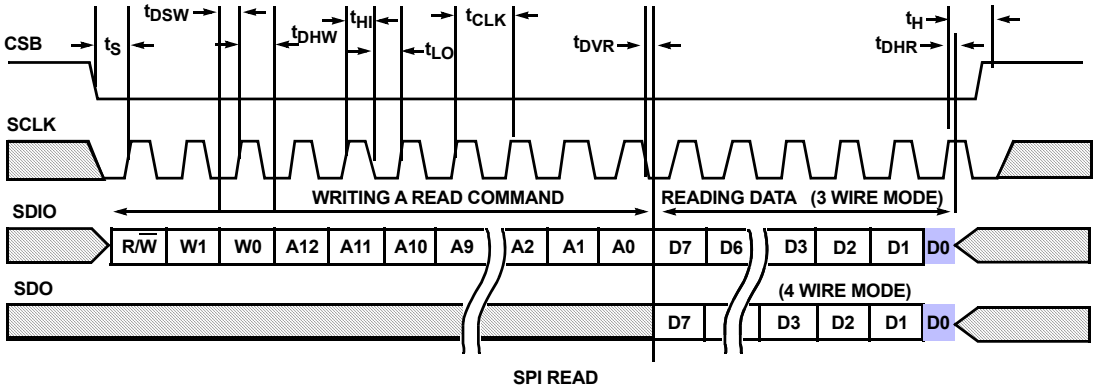


FIGURE 42. SPI READ

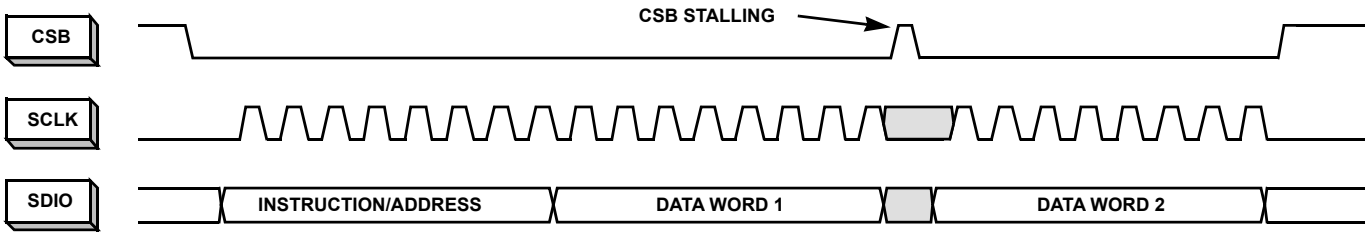


FIGURE 43. 2-BYTE TRANSFER

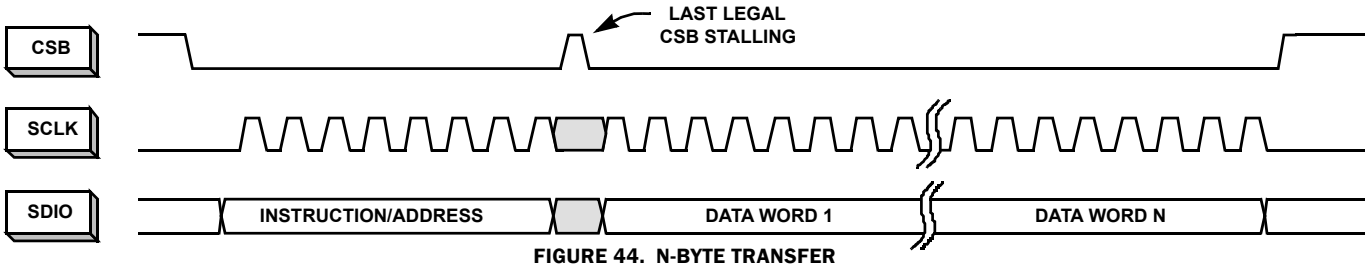


FIGURE 44. N-BYTE TRANSFER

Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data output (SDO), and serial data input/output (SDIO). The maximum SCLK rate is equal to the A/D sample rate (f_{SAMPLE}) divided by 32 for write operations and f_{SAMPLE} divided by 132 for reads. At f_{SAMPLE} = 250MHz, maximum SCLK is 15.63MHz for writing and 3.79MHz for read operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ISLA110P50 functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high to low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 39 and 40 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 6). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 41, and timing values are given in "Switching Specifications" on page 9.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the A/D (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

TABLE 6. BYTE TRANSFER SELECTION

[W1:W0]	BYTES TRANSFERRED
00	1
01	2
10	3
11	4 or more

Figures 43 and 44 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

SPI Configuration

ADDRESS 0X00: CHIP_PORT_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various micro controllers.

Bit 7 SDO Active

Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved

This bit should always be set high.

Bits 3:0 These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

ADDRESS 0X02: BURST_END

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. In 3-wire SPI mode the burst is ended by pulling the CSB pin high. If the device is operated in 2-wire mode the CSB pin is not available. In that case, setting the burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.

Device Information

ADDRESS 0X08: CHIP_ID

ADDRESS 0X09: CHIP_VERSION

The generic die identifier and a revision number, respectively, can be read from these two registers.

Indexed Device Configuration/Control

ADDRESS 0X10: DEVICE_INDEX_A

Bits 1:0 ADC01, ADC00

Determines which A/D is addressed. Valid states for this register are 0x01 or 0x10. The two A/D cores cannot be adjusted concurrently.

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Renesas A/D products. Certain configuration commands (identified as Indexed in the SPI map) can be executed on a per-converter basis. This register determines which converter is being addressed for an Indexed command. It is important to note that only a single converter can be addressed at a time.

This register defaults to 00h, indicating that no A/D is addressed. Error code ‘AD’ is returned if any indexed register is read from without properly setting device_index_A.

ADDRESS 0X20: OFFSET_COARSE

ADDRESS 0X21: OFFSET_FINE

The input offset of the A/D core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in Table 7. The data format is two’s complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 7. OFFSET ADJUSTMENTS

PARAMETER	0x20[7:0] COARSE OFFSET	0x21[7:0] FINE OFFSET
Steps	255	255
–Full Scale (0x00)	-133LSB (-47mV)	-5LSB (-1.75mV)
Mid–Scale (0x80)	0.0LSB (0.0mV)	0.0LSB
+Full Scale (0xFF)	+133LSB (+47mV)	+5LSB (+1.75mV)
Nominal Step Size	1.04LSB (0.37mV)	0.04LSB (0.014mV)

ADDRESS 0X22: GAIN_COARSE

ADDRESS 0X23: GAIN_MEDIUM

ADDRESS 0X24: GAIN_FINE

Gain of the A/D core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2%. (‘0011’ ≅ -4.2% and ‘1100’ ≅ +4.2%) It is recommended to use one of the coarse gain settings (-4.2%, -2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 23h and 24h.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 8. COARSE GAIN ADJUSTMENT

0x22[3:0]	NOMINAL COARSE GAIN ADJUST (%)
Bit3	+2.8
Bit2	+1.4
Bit1	-2.8
Bit0	-1.4

TABLE 9. MEDIUM AND FINE GAIN ADJUSTMENTS

PARAMETER	0x23[7:0] MEDIUM GAIN	0x24[7:0] FINE GAIN
Steps	256	256
–Full Scale (0x00)	-2%	-0.20%
Mid–Scale (0x80)	0.00%	0.00%
+Full Scale (0xFF)	+2%	+0.2%
Nominal Step Size	0.016%	0.0016%

ADDRESS 0X25: MODES

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes (refer to"Nap/Sleep" on page 17). This functionality can be overridden and controlled through the SPI. This is an indexed function when controlled from the SPI, but a global function when driven from the pin. This register is not changed by a Soft Reset.

TABLE 10. POWER-DOWN CONTROL

VALUE	0x25[2:0] POWER DOWN MODE
000	Pin Control
001	Normal Operation
010	Nap Mode
100	Sleep Mode

ADDRESS 0X30: I2E STATUS

The I2E general status register.

Bits 0 and 1 indicate if the I2E circuitry is in Active Run or Hold state. The state of the I2E circuitry is dependent on the analog input signal itself. If the input signal obscures the interleave mismatched artifacts such that I2E cannot estimate the mismatch, the algorithm will dynamically enter the Hold state. For example, a DC mid-scale input to the A/D does not contain sufficient information to estimate the gain and sample time skew mismatches, and thus the I2E algorithm will enter the Hold state. In the Hold state, the analog adjustments for interleave correction will be frozen and mismatch estimate calculations will cease until such time as the analog input achieves sufficient quality to allow the I2E algorithm to make mismatch estimates again.

Bit 0: 0 = I2E has not detected a low power condition. 1 = I2E has detected a low power condition, and the analog adjustments for interleave correction are frozen.

Bit 1: 0 = I2E has not detected a low AC power condition. 1 = I2E has detected a low AC power condition, and I2E will continue to correct with best known information but will not update its interleave correction adjustments until the input signal achieves sufficient AC RMS power.

Bit 2: When first started, the I2E algorithm can take a significant amount of time to settle (~1s), dependent on the characteristics of the analog input signal. 0 = I2E is still settling, 1 = I2E has completed settling.

ADDRESS 0X31: I2E CONTROL

The I2E general control register. This register can be written while I2E is running to control various parameters.

Bit 0: 0 = turn I2E off, 1= turn I2E on

Bit 1: 0 = no action, 1 = freeze I2E, leaving all settings in the current state. Subsequently writing a 0 to this bit will allow I2E to continue from the state it was left in.

Bit 2-4: Disable any of the interleave adjustments of offset, gain, or sample time skew

Bit 5: 0 = bypass notch filter, 1 = use notch filter on incoming data before estimating interleave mismatch terms

ADDRESS 0X32: I2E STATIC CONTROL

The I2E general static control register. This register must be written prior to turning I2E on for the settings to take effect.

Bit 1-4: Reserved, always set to 0

Bit 5: 0 = normal operation, 1 = skip coarse adjustment of the offset, gain, and sample time skew analog controls when I2E is first turned on. This bit would typically be used if optimal analog adjustment values for offset, gain, and sample time skew have been preloaded in order to have the I2E algorithm converge more quickly.

The system gain of the pair of interleaved core A/Ds can be set by programming the medium and fine gain of the reference A/D before turning I2E on. In this case, I2E will adjust the non-reference A/D's gain to match the reference A/D's gain.

Bit 7: Reserved, always set to 0

ADDRESS 0X4A: I2E POWER DOWN

This register provides the capability to completely power down the I2E algorithm and the Notch filter. This would typically be done to conserve power.

BIT 0: Power down the I2E Algorithm

BIT 1: Power down the Notch Filter

ADDRESS 0X50-0X55: I2E FREEZE THRESHOLDS

This group of registers provides programming access to configure I2E's dynamic freeze control. As with any interleave mismatch correction algorithm making estimates of the interleave mismatch errors using the digitized application input signal, there are certain characteristics of the input signal that can obscure the mismatch estimates. For example, a DC input to the A/D contains no information about the sample time skew mismatch between the core A/Ds, and thus should not be used by the I2E algorithm to update its sample time skew estimate. Under such circumstances, I2E enters Hold state. In the Hold state, the analog adjustments will be frozen and mismatch estimate calculations will cease until such time as the analog input achieves sufficient quality to allow the I2E algorithm to make mismatch estimates again.

These registers allow the programming of the thresholds of the meters used to determine the quality of the input signal. This can be used by the application to optimize I2E's behavior based on knowledge of the input signal. For example, if a specific

application had an input signal that was typically 30dB down from full scale, and was primarily concerned about analog performance of the A/D at this input power, lowering the RMS power threshold would allow I2E to continue tracking with this input power level, thus allowing it to track over voltage and temperature changes.

0x50 (LSBs), 0x51 (MSBs) RMS Power Threshold

This 16-bit quantity is the RMS power threshold at which I2E will enter Hold state. The RMS power of the analog input is calculated continuously by I2E on incoming data.

A 12-bit number squared produces a 24-bit result (for A/D resolutions under 12-bits, the A/D samples are MSB-aligned to 12-bit data). A dynamic number of these 24-bit results are averaged to compare with this threshold approximately every 1µs to decide whether or not to freeze I2E. The 24-bit threshold is constructed with bits 23 through 20 (MSBs) assigned to 0, bits 19 through 4 assigned to this 16-bit quantity, and bits 3 through 0 (LSBs) assigned to 0. As an example, if the application wanted to set this threshold to trigger near the RMS analog input of a -20dBFS sinusoidal input, the calculation to determine this register's value would be

$$RMS_{codes} = \frac{\sqrt{2}}{2} \times 10^{\left(\frac{-20}{20}\right)} \times 2^{12} \cong 290 codes \quad \text{(EQ. 2)}$$

$$hex(290^2) = 0x014884_{TruncateMSBandLSBhexdigit} = \mathbf{0x1488} \quad \text{(EQ. 3)}$$

Therefore, programming 0x1488 into these two registers will cause I2E to freeze when the signal being digitized has less RMS power than a -20dBFS sinusoid.

The default value of this register is 0x1000, causing I2E to freeze when the input amplitude is less than -21.2 dBFS.

The freezing of I2E by the RMS power meter threshold affects the gain and sample time skew interleave mismatch estimates, but not the offset mismatch estimate.

0x52 RMS Power Hysteresis

In order to prevent I2E from constantly oscillating between the Hold and Track state, there is hysteresis in the comparison described above. After I2E enters a frozen state, the RMS input power must achieve ≥ threshold value + hysteresis to again enter the Track state. The hysteresis quantity is a 24-bit value, constructed with bits 23 through 12 (MSBs) being assigned to 0, bits 11 through 4 assigned to this register's value, and bits 3 through 0 (LSBs) assigned to 0.

AC RMS Power Threshold

Similar to RMS power threshold, there must be sufficient AC RMS power (or dV/dt) of the input signal to measure sample time skew mismatch for an arbitrary input. This is clear from observing the effect when a high voltage (and therefore large RMS value) DC input is applied to the A/D input. Without sufficient dV/dt in the input signal, no information about the sample time skew between the core A/Ds can be determined from the digitized samples. The AC RMS Power Meter is implemented as a high-passed (via DSP) RMS power meter.

The writing of the AC RMS Power Threshold is different than other SPI registers, and these registers are not listed in the SPI memory map table. The required algorithm is documented below.

1. Write the value 0x80 to the Index Register (SPI address 0x10)
2. Write the MSBs of the 16-bit quantity to SPI Address 0x150
3. Write the LSBs of the 16-bit quantity to SPI Address 0x14F

A 12-bit number squared produces a 24-bit result (for A/D resolutions under 12-bits, the A/D samples are MSB-aligned to 12-bit data). A dynamic number of these 24-bit results are averaged to compare with this threshold approximately every 1µs to decide whether or not to freeze I2E. The 24-bit threshold is constructed with bits 23 through 20 (MSBs) assigned to 0, bits 19 through 4 assigned to this 16-bit quantity, and bits 3 through 0 (LSBs) assigned to 0. The calculation methodology to set this register is identical to the description in the RMS power threshold description.

The freezing of I2E when the AC RMS power meter threshold is not met affects the sample time skew interleave mismatch estimate, but not the offset or gain mismatch estimates.

0x55 AC RMS Power Hysteresis

In order to prevent I2E from constantly oscillating between the Hold and Track state, there is hysteresis in the comparison described above. After I2E enters a frozen state, the AC RMS input power must achieve ≥ threshold value + hysteresis to again enter the Track state. The hysteresis quantity is a 24-bit value, constructed with bits 23 through 12 (MSBs) being assigned to 0, bits 11 through 4 assigned to this register's value, and bits 3 through 0 (LSBs) assigned to 0.

ADDRESS 0X60-0X64: I2E INITIALIZATION

These registers provide access to the initialization values for each of offset, gain, and sample time skew that I2E programs into the target core A/D before adjusting to minimize interleave mismatch. They can be used by the system to, for example, reduce the convergence time of the I2E algorithm by programming in the optimal values before turning I2E on. In this case, I2E only needs to adjust for temperature and voltage-induced changes since the optimal values were recorded.

Global Device Configuration/Control

ADDRESS 0X70: SKEW_DIFF

The value in the skew_diff register adjusts the timing skew between the two A/D cores. The nominal range and resolution of this adjustment are given in Table 11. The default value of this register after power-up is 80h.

TABLE 11. DIFFERENTIAL SKEW ADJUSTMENT

PARAMETER	0x70[7:0] DIFFERENTIAL SKEW
Steps	256
–Full Scale (0x00)	-6.5ps
Mid–Scale (0x80)	0.0ps
+Full Scale (0xFF)	+6.5ps
Nominal Step Size	51fs

ADDRESS 0X71: PHASE_SLIP

The output data clock is generated by dividing down the A/D input sample clock. Some systems with multiple A/Ds can more easily latch the data from each A/D by controlling the phase of the output data clock. This control is accomplished through the use of the phase_slip SPI feature, which allows the rising edge of the output data clock to be advanced by one input clock period, as shown in the Figure 45. Execution of a phase_slip command is accomplished by first writing a '0' to bit 0 at address 0x71, followed by writing a '1' to bit 0 at address 0x71.

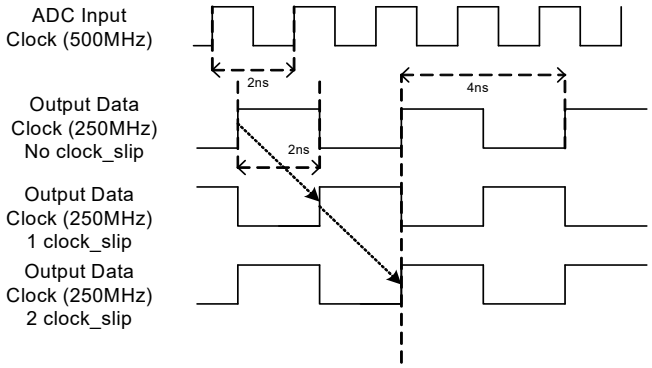


FIGURE 45. PHASE SLIP

ADDRESS 0X73: OUTPUT_MODE_A

The output_mode_A register controls the physical output format of the data, as well as the logical coding. The ISLA110P50 can present output data in two physical formats: LVDS or LVCMOS. Additionally, the drive strength in LVDS mode can be set high (3mA) or low (2mA). By default, the tri-level OUTMODE pin selects the mode and drive level (refer to "Digital Outputs" on page 17). This functionality can be overridden and controlled through the SPI, as shown in Table 12.

Data can be coded in three possible formats: two's complement, Gray code or offset binary. By default, the tri-level OUTFMT pin selects the data format (refer to "Data Format" on page 17). This functionality can be overridden and controlled through the SPI, as shown in Table 13.

This register is not changed by a Soft Reset.

TABLE 12. OUTPUT MODE CONTROL

VALUE	0x93[7:5] OUTPUT MODE
000	Pin Control
001	LVDS 2mA
010	LVDS 3mA
100	LVCMOS

TABLE 13. OUTPUT FORMAT CONTROL

VALUE	0x93[2:0] OUTPUT FORMAT
000	Pin Control
001	Two's Complement
010	Gray Code
100	Offset Binary

ADDRESS 0X74: OUTPUT_MODE_B

ADDRESS 0X75: CONFIG_STATUS

Bit 6 DLL Range

This bit sets the DLL operating range to fast (default) or slow.

Internal clock signals are generated by a delay-locked loop (DLL), which has a finite operating range. Table 14 shows the allowable sample rate ranges for the slow and fast settings.

TABLE 14. DLL RANGES

DLL RANGE	MIN	MAX	UNIT
Slow	80	200	MSPS
Fast	160	500	MSPS

The output_mode_B and config_status registers are used in conjunction to enable DDR mode and select the frequency range of the DLL clock generator. The method of setting these options is different from the other registers.

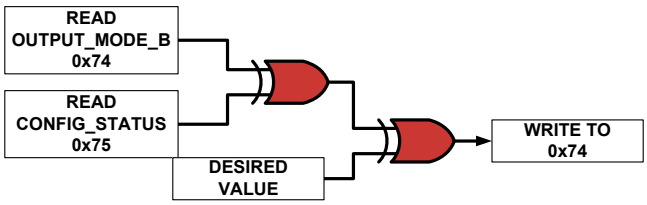


FIGURE 46. SETTING OUTPUT_MODE_B REGISTER

The procedure for setting output_mode_B is shown in Figure 46. Read the contents of output_mode_B and config_status and XOR them. Then XOR this result with the desired value for output_mode_B and write that XOR result to the register.

Device Test

The ISLA110P50 can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A static word can be placed on the output bus, or two different words can alternate. In the alternate mode, the values defined as Word 1 and Word 2 (as shown in Table 15) are set on the output bus on alternating clock phases. The test mode is enabled asynchronously to the sample clock, therefore several sample clock cycles may elapse before the data is present on the output bus.

ADDRESS 0XC0: TEST_IO

Bits 7:6 User Test Mode

These bits set the test mode to static (0x00) or alternate (0x01) mode. Other values are reserved.

The four LSBs in this register (Output Test Mode) determine the test pattern in combination with registers 0xC2 through 0xC5. Refer to "SPI Memory Map" on page 28.

TABLE 15. OUTPUT TEST MODES

VALUE	0xC0[3:0] OUTPUT TEST MODE	WORD 1	WORD 2
0000	Off		
0001	Midscale	0x8000	N/A
0010	Positive Full-Scale	0xFFFF	N/A
0011	Negative Full-Scale	0x0000	N/A
0100	Checkerboard	0xAAAA	0x5555
0101	Reserved	N/A	N/A
0110	Reserved	N/A	N/A
0111	One/Zero	0xFFFF	0x0000
1000	User Pattern	user_patt1	user_patt2

ADDRESS 0XC2: USER_PATT1_LSB

ADDRESS 0XC3: USER_PATT1_MSB

These registers define the lower and upper eight bits, respectively, of the first user-defined test word.

ADDRESS 0XC4: USER_PATT2_LSB

ADDRESS 0XC5: USER_PATT2_MSB

These registers define the lower and upper eight bits, respectively, of the second user-defined test word.

Digital Temperature Sensor

This set of registers provides digital access to an IPTAT-based temperature sensor, allowing the system to estimate the temperature of the die. This information is of particular interest for applications that do not keep I2E in Active Run state when in normal use, allowing easy access to information that can be used to decide when to recalibrate the A/D as needed. This set of registers is not included in the SPI memory map table.

The most accurate usage of this information requires knowledge of the temperature at which the digital value is first read (time = 0, T(0) = °C at time = 0, and register_value(0) = the digital value of the temperature registers at time = 0). Any future reading of the registers indicates temperature change according to Equation 4:

$$\Delta T = T(1) - T(0) = \frac{[\text{register_value}(1)] - [\text{register_value}(0)]}{[(T(0) - 216)/256]} \quad \text{(EQ. 4)}$$

A less accurate method for evaluating the temperature change does not require knowledge of the temperature at time = 0, and is given by Equation 5:

$$\Delta T = T(1) - T(0) = \frac{[\text{register_value}(1)] - [\text{register_value}(0)]}{(-0.72)} \quad \text{(EQ. 5)}$$

The digital temperature sensor is a weak function of the AVDD supply voltage, so to achieve best accuracy the AVDD supply voltage should be held fairly constant across the operating temperature range.

The algorithm to access this set of registers is as follows:

1. Write the value 0x80 to the Index Register (SPI address 0x10)
2. Write the value 0x88 to SPI address 0x120 to turn the temperature sensor on.
3. Read the register_value LSBs at SPI register 0x11E
4. Read the register_value MSBs at SPI register 0x11F
5. Write the value 0x60 to SPI address 0x120 to turn the temperature sensor off.

SPI Memory Map

TABLE 16. SPI MEMORY MAP

	ADDR (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (Hex)	INDEXED/GLOBAL
SPI Config	00	port_config	SDO Active	LSB First	Soft Reset			Mirror (bit5)	Mirror (bit6)	Mirror (bit7)	00h	G
	01	Reserved	Reserved									
	02	burst_end	Burst end address [7:0]								00h	G
	03-07	Reserved	Reserved									
Info	08	chip_id	Chip ID #								Read only	G
	09	chip_version	Chip Version #								Read only	G
Indexed Device Config/Control	10	device_index_A	Reserved						ADC01	ADC00	00h	I
	11-1F	Reserved	Reserved									
	20	offset_coarse	Coarse Offset								cal. value	I
	21	offset_fine	Fine Offset								cal. value	I
	22	gain_coarse	Reserved				Coarse Gain				cal. value	I
	23	gain_medium	Medium Gain								cal. value	I
	24	gain_fine	Fine Gain								cal. value	I
	25	modes	Reserved					**Power-Down Mode [2:0]** 000 = Pin Control 001 = Normal Operation 010 = Nap 100 = Sleep Other codes = Reserved			00h NOT affected by Soft Reset	I
	26-2F	Reserved	Reserved									I
I2E Control and Status	30	I2E Status				Reserved		I2E Settled	Low AC RMS Power	Low RMS Power	Read only	G
	31	I2E Control			Enable notch filter	Disable Offset	Disable Gain	Disable Skew	Freeze	Run	20h	G
	32	I2E Static Control	Reserved must be set to 0		Skip coarse adjustment	Reserved, must be set to 0					00h	G
	33-49	Reserved	Reserved									G
	4A	I2E Power Down							Notch Filter Power Down	I2E Power Down	00h	G
	4B-4F	Reserved	Reserved									G
	50	I2E RMS Power Threshold LSBs	RMS Power Threshold, LSBs								00h	G
	51	I2E RMS Power Threshold MSBs	RMS Power Threshold, MSBs								10h	G
	52	I2E RMS Hysteresis	RMS Power Hysteresis								FFh	G
	53-54	Reserved	Reserved									G

TABLE 16. SPI MEMORY MAP (Continued)

	ADDR (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (Hex)	INDEXED/GLOBAL
I2E Control and Status (continued)	55	I2E AC RMS Hysteresis	AC RMS Power Hysteresis								10h	G
	56-5F	Reserved	Reserved									G
	60	Coarse Offset Init	Coarse Offset Initialization value								80h	G
	61	Fine Offset Init	Fine Offset Initialization value								80h	G
	62	Medium Gain Init	Medium Gain Initialization value								80h	G
	63	Fine Gain Init	Fine Gain Initialization value								80h	G
	64	Sample Time Skew Init	Sample Time Skew Initialization value								80h	G
	65-6F	Reserved	Reserved									G
Global DeviceConfig/Control	70	skew_diff	Differential Skew								80h	G
	71	phase_slip	Reserved							Next Clock Edge	00h	G
	72	Reserved	Reserved					Reserved (must be 0)			00h NOT affected by Soft Reset	G
	73	output_mode_A	**Output Mode [2:0]** 000 = Pin Control 001 = LVDS 2mA 010 = LVDS 3mA 100 = LVCMOS other codes = reserved					**Output Format [2:0]** 000 = Pin Control 001 = Twos Complement 010 = Gray Code 100 = Offset Binary Other codes = Reserved			00h NOT affected by Soft Reset	G
	74	output_mode_B		**DLL Range** 0 = fast 1 = slow							00h NOT affected by Soft Reset	G
	75	config_status		XOR Result							Read Only	G
	76-BF	Reserved	Reserved									
Device Test	C0	test_io	**User Test Mode [1:0]** 00 = Single 01 = Alternate 10 = Reserved 11 = Reserved				**Output Test Mode [3:0]** 0 = Off 1 = Midscale Short 2 = +FS Short 3 = -FS Short 4 = Checker Board 5 = reserved 6 = reserved		7 = One/Zero Word Toggle 8 = User Input 9-15 = reserved		00h	G
	C1	Reserved	Reserved								00h	G
	C2	user_patt 1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h	G
	C3	user_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h	G
	C4	user_patt 2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h	G
	C5	user_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h	G
	C6-FF	Reserved	Reserved									

Equivalent Circuits

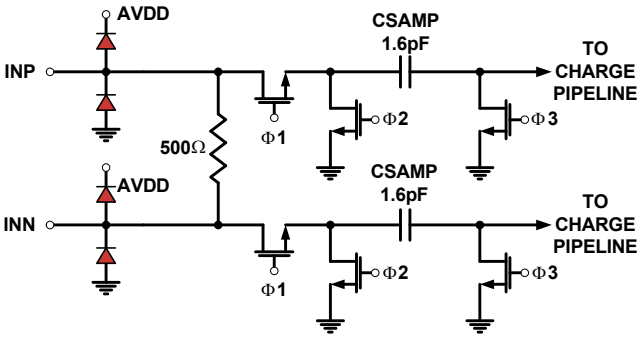


FIGURE 47. ANALOG INPUTS

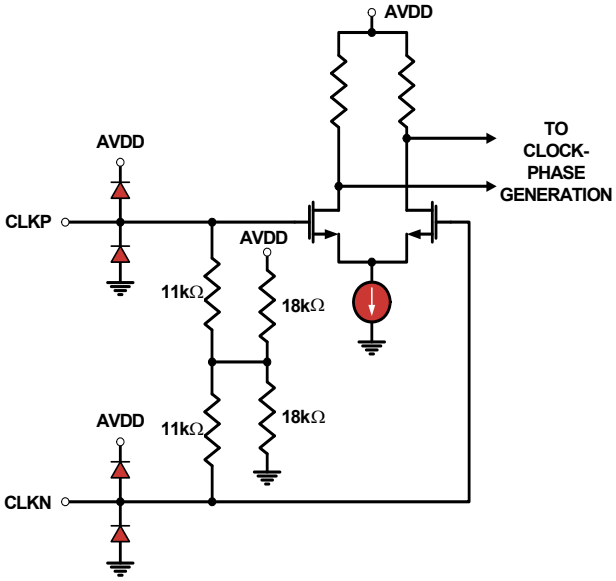


FIGURE 48. CLOCK INPUTS

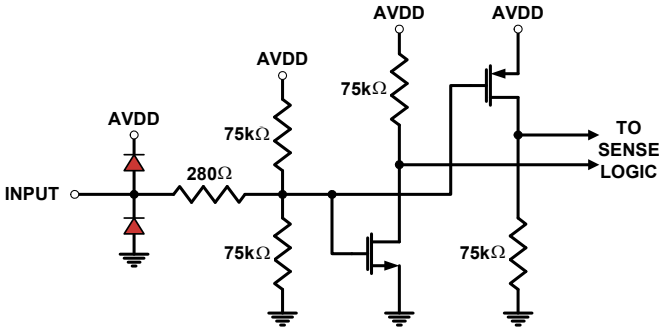


FIGURE 49. TRI-LEVEL DIGITAL INPUTS

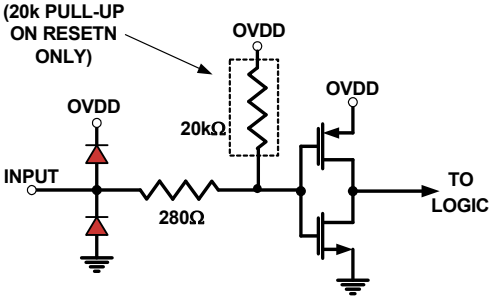


FIGURE 50. DIGITAL INPUTS

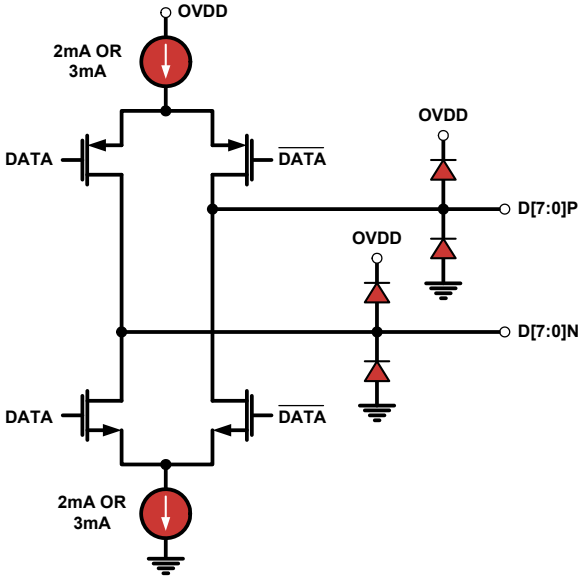


FIGURE 51. LVDS OUTPUTS

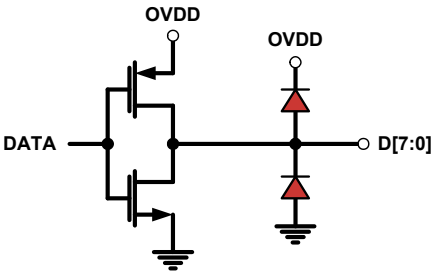


FIGURE 52. CMOS OUTPUTS

Equivalent Circuits (Continued)

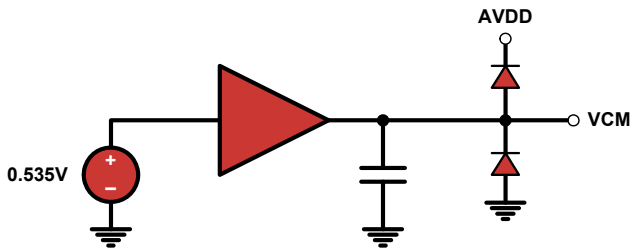


FIGURE 53. VCM_OUT OUTPUT

A/D Evaluation Platform

Renesas offers an A/D Evaluation platform which can be used to evaluate any of Renesas' high speed A/D products. The platform consists of an FPGA based data capture motherboard and a family of A/D daughter cards. This USB based platform allows a user to quickly evaluate the A/D's performance at a user's specific application frequency requirements. More information is available on the website.

Layout Considerations

Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins. Longer traces will increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

LVDS Outputs

Output traces and connections must be designed for 50Ω (100Ω differential) characteristic impedance. Keep traces direct and minimize bends where possible. Avoid crossing ground and power-plane breaks with signal traces.

LVCMOS Outputs

Output traces and connections must be designed for 50Ω characteristic impedance.

Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which will not be operated do not require connection to ensure optimal A/D performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP, OUTMODE, OUTFMT) accept a floating input as a valid state, and therefore should be biased according to the desired functionality.

Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.

Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD - 1.76)/6.02

Gain Error is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage less 2 LSB. It is typically expressed in percent.

I2E The Interleave Engine. This highly configurable circuitry performs estimates of offset, gain, and sample time skew mismatches between the core converters, and updates analog adjustments for each to minimize interleave spurs.

Integral Non-Linearity (INL) is the maximum deviation of the A/D's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N-1)$ where N is the resolution in bits.

Missing Codes are output codes that are skipped and will never appear at the A/D output. These codes cannot be reached with any input value.

Most Significant Bit (MSB) is the bit that has the largest value or weight.

Pipeline Delay is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

Power Supply Rejection Ratio (PSRR) is the ratio of the observed magnitude of a spur in the A/D FFT, caused by an AC signal superimposed on the power supply voltage.

Signal to Noise-and-Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

Signal-to-Noise Ratio (without Harmonics) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

SNR and SINAD are either given in units of dB when the power of the fundamental is used as the reference, or dBFS (dB to full scale) when the converter's full-scale input power is used as the reference.

Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the largest spurious spectral component. The largest spurious spectral component may or may not be a harmonic.

Revision History

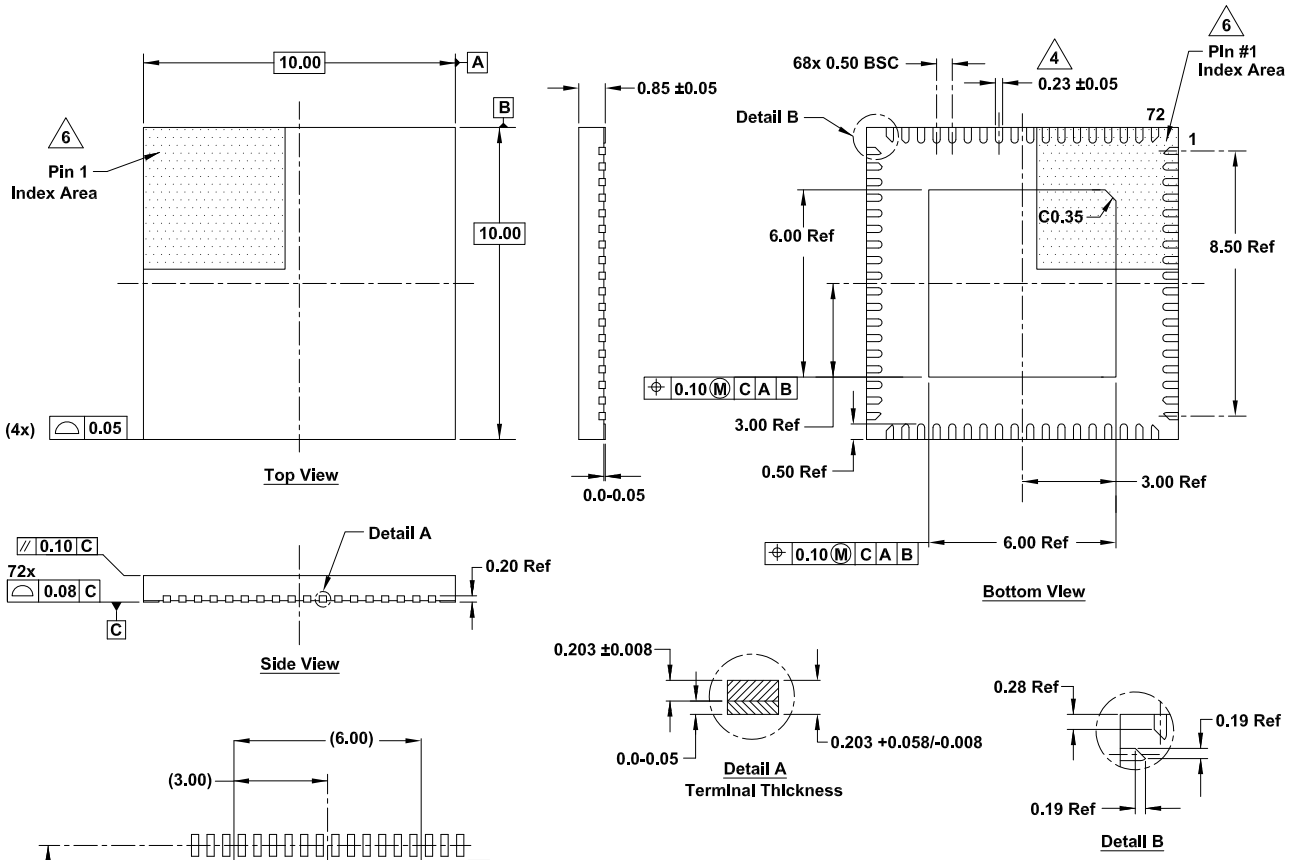
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

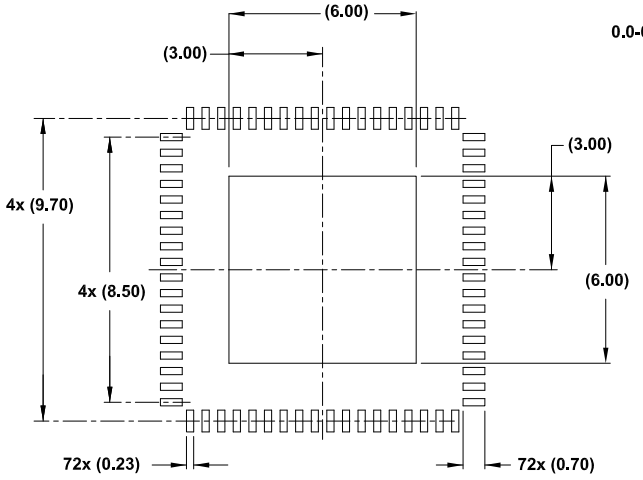
DATE	REVISION	CHANGE
Jul 6, 2021	3.0	Updated links throughout. Updated Ordering Information table format and updated applicable notes. Updated termination finish from Matte Sn (e3) to NiPdAu-Ag (e4). Changed POD from L72.10x10C to L72.10x10J. Removed Products section.
Jul 6, 2011	2.0	– Updated Intersil Trademark statement at bottom of page 1 per directive from Legal. – Converted to new datasheet template. – Replaced all occurrences of "Fs/4 filter" with "Notch filter". – Updated over temp note in Min Max column of spec tables from: Unless otherwise noted, parameters with Min and/or MAX limits are 100% production tested at their worst case temperature extreme (+85°C). To new standard: "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design."
May 19, 2010	1.0	– On page 1: Removed CLKDIV from key feature list (Selectable Clock Divider: ÷1 or ÷2) Removed CLKDIV pin from Block Diagram (was right nexto to CLKDIVRSTP pin) – On page 3: Removed CLKDIV pin from "Pin Configuration" diagram, replaced with a DNC pin (pin 16) – On page 4: Removed CLKDIV pin from "Pin Descriptions" list, added pin 16 to DNC list – On page 8: Under "CMOS INPUTS" in the "Digital Specifications" table, added CSB and SCLK to the CMOS pin list (in Parameter column) for I_IH, I_IL, V_IH, V_IL Removed CLKDIV reference from "Input Current High (OUTMODE, NAPSLP, OUTFMT) (Note 14)" and "Input Current Low (OUTMODE, NAPSLP, OUTFMT)" specs – On page 16: Removed text and table describing CLKDIV function – On page 20: Removed sentences referencing the "2GSPS" block diagram under the "Clock Divider Synchronous Reset" section as we no longer support this clock distribution block diagram, nor su/hold times to support closing timing at 1GHz input clock – On page 21: Removed Sync generation block diagram (former FIGURE 38. SYNCHRONIZATION SCHEME) because we no longer support this architecture – On page 26: Updated "Address 0x71: phase_slip" section to reflect functionality in the CLKDIV1 mode. New timing diagram Figure 45 to show functionality. Removed the "ADDRESS 0X72: CLOCK_DIVIDE" section and table for SPI address 0x72, clock_divide feature – On page 29: Removed the clock_divide SPI register from Table 16 under ADDR 72, replacing with Reserved (and indicating which bits must be set to 0) – On page 31: Removed the CLKDIV reference in "Unused Inputs" section
Mar 30, 2010	0.0	Initial Release of Production Datasheet

Package Outline Drawing

For the most recent package outline drawing, see L72.10x10J.

L72.10x10J
72 Lead Quad Flat No-Lead Plastic Package (QFN)
Rev 0, 4/20





Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.10
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Package outline compliant to JESD-M0220.

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(Rev.1.0 Mar 2020)

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