ISLA214S50

14-Bit, 500/350 MSPS JESD204B High Speed Serial Output ADC

FN7973
Rev 2.00
April 25, 2013

The ISLA214S50 is a series of low-power, high-performance, 14-bit, analog-to-digital converters. Designed with FemtoCharge™ technology on a standard CMOS process, the series supports sampling rates of up to 500MSPS. The ISLA214S50 is part of a pin-compatible family of 12-, 14-, and 16-bit A/Ds with maximum sample rates ranging from 125MSPS to 500MSPS. The family minimizes power consumption while providing state-of-the-art dynamic performance.

The device utilizes two time-interleaved 250MSPS unit ADCs to achieve the ultimate sample rate of 500MSPS. A single 500MHz conversion clock is presented to the converter, and all interleave clocking is managed internally. The proprietary Intersil Interleave Engine (I2E) performs automatic correction of offset, gain, and sample time mismatches between the unit ADCs to optimize performance.

The ISLA214S50 offers a highly configurable, JESD204B-compliant, high speed serial output link. The link offers data rates up to 4.375 Gbps per lane and multiple packing modes. The link can be configured to use two or three lanes to transmit the conversion data, allowing for flexibility in the receiver design. The JESD204 transmitter also provides deterministic latency and multi-chip time alignment support to satisfy complex synchronization requirements.

A serial peripheral interface (SPI) port allows for extensive configurability of the ADC and its JESD204B transmitter including access to its built-in link and transport-layer test patterns as well as the programmable clock divider, enabling 2x harmonic clocking.

The ISLA214S50 is available in a space-saving 7mmx7mm 48 Ld QFN package. The package features a thermal pad for improved thermal performance and is specified over the full industrial temperature range (-40°C to +85°C)

Features

- JESD204A/B High Speed Data Interface
  - JESD204A Compliant
  - JESD204B Device Subclass 0 Compliant
  - JESD204B Device Subclass 2 Compatible
  - Up to 3 JESD204 Output Lanes Running up to 4.375Gbps
  - Highly Configurable JESD204 Transmitter
- Multiple Chip Time Alignment and Deterministic Latency Support (JESD204B Device Subclass 2)
- SPI Programmable Debugging Features and Test Patterns
- 48-pin QFN 7mmx7mm Package

Key Specifications

- SNR @ 500/350MSPS
  73.1/74.1 dBFS f_{IN} = 30MHz
  71.0/71.6 dBFS f_{IN} = 363MHz
- SFDR @ 500/350MSPS
  87/87 dBc f_{IN} = 30MHz
  78/81 dBc f_{IN} = 363MHz
- Total Power Consumption: 1060mW @ 500MSPS

Applications

- Radar and Satellite Antenna Array Processing
- Broadband Communications and Microwave Receivers
- High-Performance Data Acquisition
- Communications Test Equipment
- High-Speed Medical Imaging

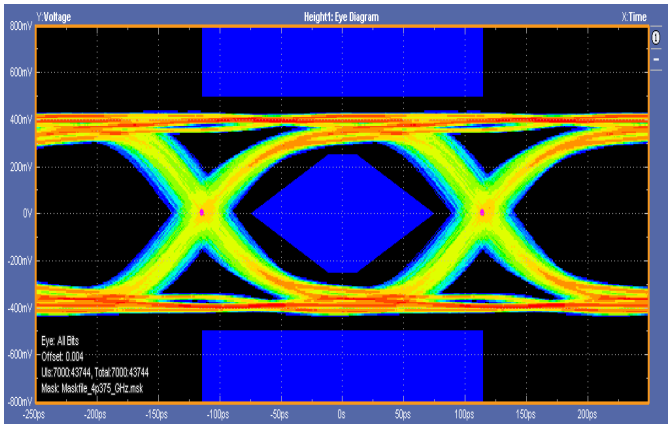


FIGURE 1. SERDES DATA EYE AT 4.375Gbps

Pin-Compatible Family

MODEL	RESOLUTION	SPEED (MSPS)	PRODUCT AVAILABILITY
ISLA214S50	14	500	Now
ISLA214S35	14	350	Soon

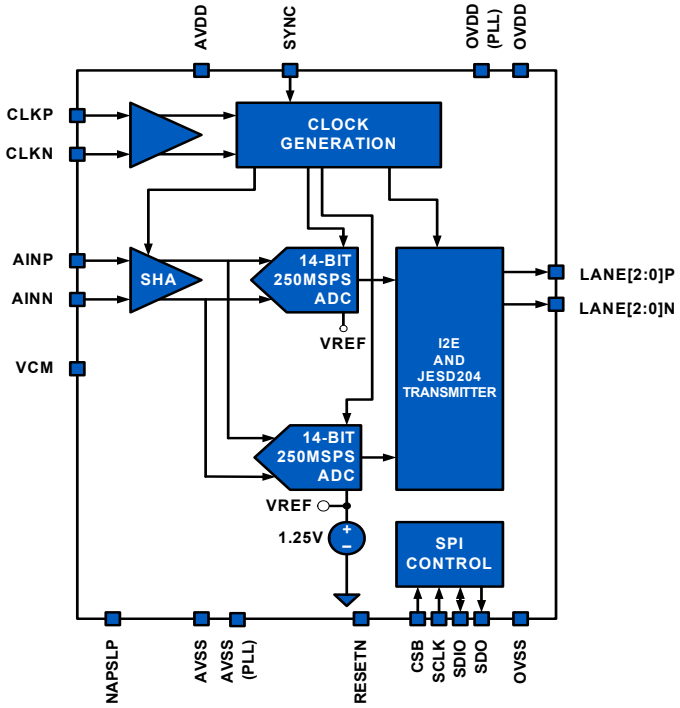
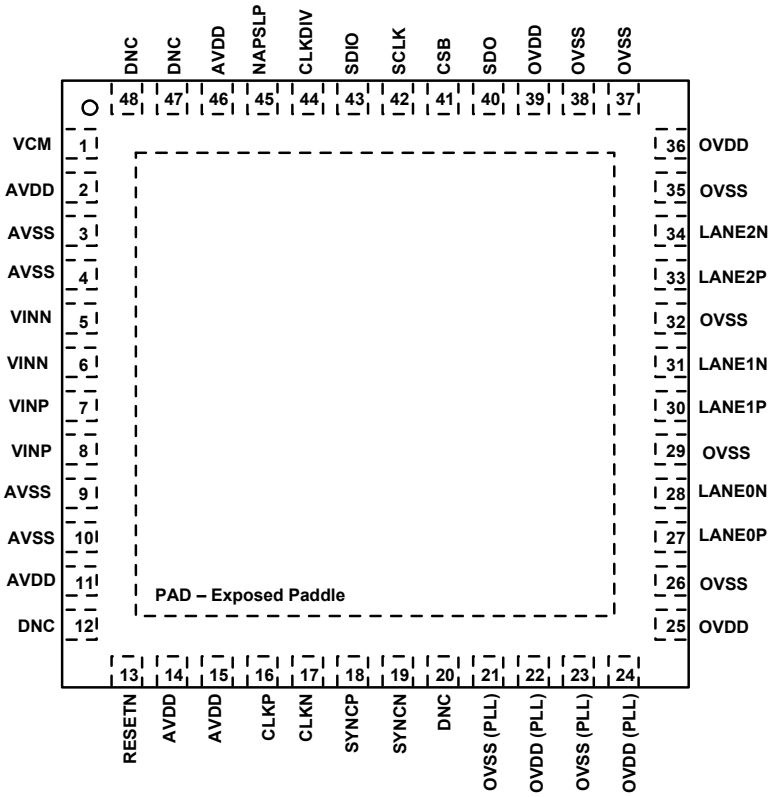


FIGURE 2. BLOCK DIAGRAM

Pin Configuration

ISLA214S50
(48 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	NAME	FUNCTION
2, 11, 14, 15, 46	AVDD	1.8V Analog Supply
12, 20, 47, 48	DNC	Do Not Connect
3, 4, 9, 10	AVSS	Analog Ground
7, 8	VINP	Analog Input Positive
5, 6	VINN	Analog Input Negative
1	VCM	Common Mode Output
44	CLKDIV	Clock Divider Control
16, 17	CLKP, CLKN	Clock Input True, Complement
45	NAPSLP	Power Control (Nap, Sleep modes)
13	RESETN	Power On Reset (Active Low)
26, 29, 32, 35, 37, 38	OVSS	Output Ground
25, 36, 39	OVDD	1.8V Digital Supply
22, 24	OVDD (PLL)	1.8V Analog Supply for SERDES PLL
21, 23	OVSS (PLL)	Analog Ground Supply for SERDES PLL
18, 19	SYNCP, SYNCN	JESD204 SYNC Input
27, 28	LANE0P, LANE0N	SERDES Lane 0
30, 31	LANE1P, LANE1N	SERDES Lane 1
33, 34	LANE2P, LANE2N	SERDES Lane 2
40	SDO	SPI Serial Data Output
41	CSB	SPI Chip Select (active low)
42	SCLK	SPI Clock
43	SDIO	SPI Serial Data Input/Output
PAD	AVSS	Exposed Paddle. Analog Ground (connect to AVSS)

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISLA214S50IR1Z	ISLA214S50 IR1Z	-40 to +85	48 Ld QFN	L48.7x7G
Coming Soon ISLA214S35IR1Z	ISLA214S35 IR1Z	-40 to +85	48 Ld QFN	L48.7x7G
Coming Soon ISLA214S50IR48EV1Z	Evaluation Board			

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISLA214S50, ISLA214S35. For more information on MSL please see techbrief TB363.

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Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS . . . . . -0.3V to 0.3V
Analog Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS . . . . . -0.4V to OVDD + 0.3V
Latchup (Tested per JESD-78C;Class 2,Level A 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN (Notes 3, 4, 5)	23	0.75

Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. For solder stencil layout and reflow guidelines, please see Tech Brief TB389.

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITIONS	ISLA214S50			ISLA214S35			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	
DC SPECIFICATIONS									
Analog Input									
Full-Scale Analog Input Range	V_{FS}	Differential	**1.95**	2.00	**2.15**	**1.95**	2.00	**2.15**	V_{P-P}
Input Resistance	R_{IN}	Differential		600			600		Ω
Input Capacitance	C_{IN}	Differential		13.3			13.3		pF
Full Scale Range Temp. Drift	A_{VTC}	Full Temp		100			100		ppm/°C
Input Offset Voltage	V_{OS}		**-5.0**	±1	**5.0**	**-5.0**	±1	**5.0**	mV
Gain Error	E_G			-2.6			-2.6		%
Common-Mode Output Voltage	V_{CM}			0.94			0.94		V
Common Mode Input Current (per pin)	I_{CM}			6.0			6.0		µA/MSPS
Clock Inputs									
Inputs Common Mode Voltage				0.9			0.9		V
CLKP, CLKN Swing				1.8			1.8		V
Power Requirements									
1.8V Analog Supply Voltage	AVDD		**1.7**	1.8	**1.9**	**1.7**	1.8	**1.9**	V
1.8V Digital Supply Voltage	OVDD		**1.7**	1.8	**1.9**	**1.7**	1.8	**1.9**	V
1.8V Analog Supply Current	I_{AVDD}			359	**385**		313		mA
1.8V Digital Supply Current	I_{OVDD}	I2E on, Fs/4 filter on, Minimum number of lanes active		222	**248**		159		mA

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA214S50			ISLA214S35			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	
Power Supply Rejection Ratio (Note 7)	PSRR	30MHz 200mV$_{P-P}$		41			41		dB
		1MHz 200mV$_{P-P}$		47			47		dB
Total Power Dissipation									
Normal Mode	P_D			1060	**1139**		857		mW
Nap Mode	P_D			421	**466**		352		mW
Sleep Mode	P_D	CSB at logic high		6	**12**		6		mW
Nap Mode Wakeup Time		Sample Clock Running		5			5		µs
Sleep Mode Wakeup Time		Sample Clock Running		1			1		ms
AC SPECIFICATIONS (Note 8)									
Differential Nonlinearity	DNL		**-1.0**	±0.35	**1.4**		±0.30		LSB
Integral Nonlinearity	INL			±2.4			±1.5		LSB
Minimum Conversion Rate (Note 9)	f_S MIN				**200**			**175**	MSPS
Maximum Conversion Rate	f_S MAX	Efficient Packing	**500**			**350**	500		MSPS
		Simple Packing				**310**			MSPS
Signal-to-Noise Ratio (Note 10)	SNR	f_{IN} = 30MHz		73.1			74.1		dBFS
		f_{IN} = 105MHz	70	72.9			73.8		dBFS
		f_{IN} = 190MHz		72.5			73.2		dBFS
		f_{IN} = 363MHz		71.0			71.6		dBFS
		f_{IN} = 495MHz		70.1			70.1		dBFS
		f_{IN} = 605MHz		68.9			68.9		dBFS
Signal-to-Noise and Distortion (Note 10)	SINAD	f_{IN} = 30MHz		73.0			73.9		dBFS
		f_{IN} = 105MHz	69.4	72.7			73.6		dBFS
		f_{IN} = 190MHz		72.1			72.9		dBFS
		f_{IN} = 363MHz		70.4			71.3		dBFS
		f_{IN} = 495MHz		67.9			68.4		dBFS
		f_{IN} = 605MHz		67.0			67.0		dBFS
Effective Number of Bits (Note 10)	ENOB	f_{IN} = 30MHz		11.8			12.0		Bits
		f_{IN} = 105MHz	11.23	11.8			11.9		Bits
		f_{IN} = 190MHz		11.7			11.8		Bits
		f_{IN} = 363MHz		11.4			11.6		Bits
		f_{IN} = 495MHz		11.0			11.1		Bits
		f_{IN} = 605MHz		10.8			10.8		Bits

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	ISLA214S50			ISLA214S35			UNITS
			MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	
Spurious-Free Dynamic Range (Note 10)	SFDR	f_{IN} = 30MHz		87			87		dBc
		f_{IN} = 105MHz	74	86			87		dBc
		f_{IN} = 190MHz		84			85		dBc
		f_{IN} = 363MHz		78			81		dBc
		f_{IN} = 495MHz		70			72		dBc
		f_{IN} = 605MHz		70			71		dBc
Spurious-Free Dynamic Range Excluding H2, H3 (Note 10)	SFDRX23	f_{IN} = 30MHz		89			93		dBc
		f_{IN} = 105MHz		89			91		dBc
		f_{IN} = 190MHz		87			86		dBc
		f_{IN} = 363MHz		81			81		dBc
		f_{IN} = 495MHz		79			76		dBc
		f_{IN} = 605MHz		76			75		dBc
Intermodulation Distortion	IMD	f_{IN} = 70MHz		83			83		dBFS
		f_{IN} = 170MHz		97			96		dBFS
Word Error Rate	WER			10^{-13}			10^{-13}		
Full Power Bandwidth	FPBW			500			500		MHz

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. PSRR is calculated by the equation 20*log10(A/B), where B is the amplitude of a disturber sinusoid on AVDD at the device pins, and A is the amplitude of the spur in the captured data at the frequency of the disturber sinusoid.
8. AC Specifications apply after internal calibration of the ADC is invoked at the given sample rate and temperature. Refer to “Power-On Calibration” on page 15 and “User Initiated Reset” on page 16 for more detail.
9. The DLL Range setting must be changed via SPI for ADC core sample rates below 160MSPS. The JESD204 transmitter can support ADC sample rates below 200MSPS, as long as the lane data rate is greater than or equal to 1Gbps.
10. Minimum specification guaranteed when calibrated at +85°C.

I2E Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Offset Mismatch-induced Spurious Power		No I2E Calibration performed		-65		dBFS
		Active Run state enabled		-70		dBFS
I2E Settling Times	I2Epost_t	Calibration settling time for Active Run state			**1000**	ms
Minimum Duration of Valid Analog Input	t_{TE}	Allow one I2E iteration of Offset, Gain and Phase correction			**100**	µs

I2E Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Largest Interleave Spur		f_{IN} = 10MHz to 240MHz, Active Run State enabled, in Track Mode		-99		dBc
		f_{IN} = 10MHz to 240MHz, Active Run State enabled and previously settled, in Hold Mode		-80		dBc
		f_{IN} = 260MHz to 490MHz, Active Run State enabled, in Track Mode		-95		dBc
		f_{IN} = 260MHz to 490MHz, Active Run State enabled and previously settled, in Hold Mode		-70		dBc
Total Interleave Spurious Power		Active Run State enabled, in Track Mode, f_{IN} is a broadband signal in the 1st Nyquist zone		-85		dBc
		Active Run State enabled, in Track Mode, f_{IN} is a broadband signal in the 2nd Nyquist zone		-75		dBc
Sample Time Mismatch Between Unit ADCs		Active Run State enabled, in Track Mode		25		fs
Gain Mismatch Between Unit ADCs				0.02		%FS
Offset Mismatch Between Unit ADCs				1		mV

Digital Specifications Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CMOS INPUTS						
Input Current High (RESETN)	I_{IH}	V_{IN} = 1.8V		1	**10**	µA
Input Current Low (RESETN)	I_{IL}	V_{IN} = 0V	**-25**	-12	**-7**	µA
Input Current High (SDIO, SCL, SDA SCLK)	I_{IH}	V_{IN} = 1.8V		4	**12**	µA
Input Current Low (SDIO, SCL, SDA SCLK)	I_{IL}	V_{IN} = 0V	**-600**	-400	**-300**	µA
Input Current High (CSB)	I_{IH}	V_{IN} = 1.8V	**40**	52	**70**	µA
Input Current Low (CSB)	I_{IL}	V_{IN} = 0V		1	**10**	µA
Input Voltage High (SDIO, RESETN)	V_{IH}		**1.17**			V
Input Voltage Low (SDIO, RESETN)	V_{IL}				**0.63**	V
Input Current High (NAPSLP, CLKDIV) (Note 11)	I_{IH}		**19**	25	**30**	µA
Input Current Low (NAPSLP, CLKDIV)	I_{IL}		**–30**	-25	**-19**	µA
Input Capacitance	C_{DI}			4		pF
LVDS INPUTS (SYNCP, SYNCN)						
Input Common Mode Range	V_{ICM}		**825**		**1575**	mV
Input Differential Swing (peak-to-peak, single-ended)	V_{ID}		**250**		**450**	mV
Input Pull-up and Pull-down Resistance	R_{Ipu}			100		kΩ
CML OUTPUTS						
Output Common Mode Voltage				1.14		mV

Switching Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
ADC OUTPUT						
Aperture Delay	t_A			240		ps
RMS Aperture Jitter	j_A			90		fs
Synchronous Clock Divider Reset Recovery Time (Note 12)	t_{RSTRT}	DLL recovery time after Synchronous Reset		250		µs
Latency (ADC Pipeline Delay)	L			20		cycles
Overvoltage Recovery	t_{OVR}			2		cycles
SERDES						
PLL Lock Time				250		µs
PLL Bandwidth				2.2		MHz
Added Random Jitter				5		ps RMS
Added Deterministic Jitter				7		ps P-P
Maximum Input Sample Clock Total Jitter to Maintain SERDES BER <1E-12		Integrated from 1kHz to 10MHz offset from carrier		5		ps rms
LVDS Inputs						
SYNCP, SYNCN Setup Time (with Respect to the Positive Edge of CLKP)	t_{RSTS}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	**400**	75		ps
SYNCP, SYNCN Hold Time (with Respect to the Positive Edge of CLKP)	t_{RSTH}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C		150	**350**	ps
CML Outputs						
Output Rise Time	t_R			165		ps
Output Fall Time	t_F			145		ps
Data Output Duty Cycle				50		%
Differential Output Resistance				100		Ω
Differential Output Voltage (Note 13)				760		mV_{P-P}
SPI INTERFACE (Notes 14, 15)						
SCLK Period	t_{CLK}	Write Operation	**14**			cycles
	t_{CLK}	Read Operation	**32**			cycles
CSB↓ to SCLK↑ Setup Time	t_S	Read or Write	**4**			cycles
CSB↑ after SCLK↑ Hold Time	t_H	Read or Write	**10**			cycles

Switching Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Data Valid to SCLK↑ Setup Time	t_{DS}	Read or Write	**12**			cycles
Data Valid after SCLK↑ Hold Time	t_{DH}	Read or Write	**8**			cycles
Data Valid after SCLK↓ Time	t_{DVR}	Read			**8**	cycles

NOTES:

11. The Tri-Level Inputs internal switching thresholds are approximately. 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
12. The synchronous clock divider reset function is available as a (SPI-programmable) overload on the SYNC input.
13. The voltage is expressed in peak-to-peak differential swing. The peak-to-peak single-ended swing is 1/2 of the differential swing.
14. The SPI interface timing is directly proportional to the ADC sample period (t_S). Values above reflect multiples of a 2ns sample period, and must be scaled proportionally for lower sample rates. ADC sample clock must be running for SPI communication.
15. The SPI may operate asynchronously with respect to the ADC sample clock.

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS.

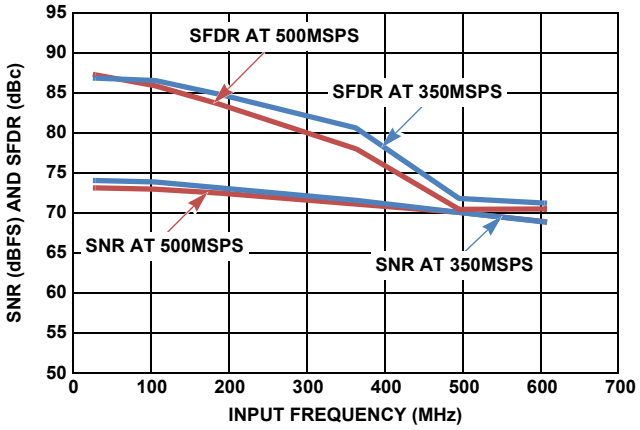


FIGURE 3. SNR AND SFDR vs f_{IN}

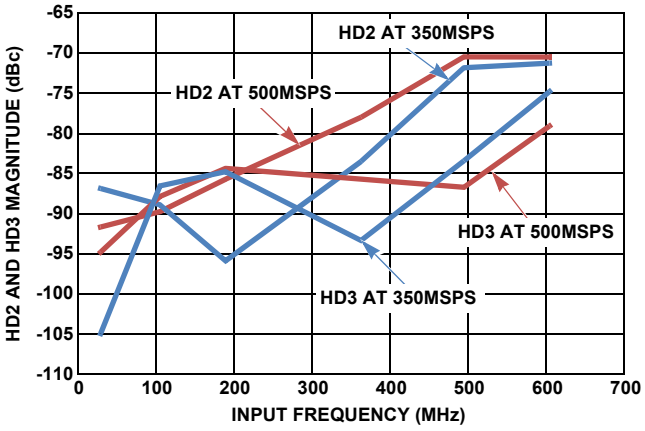


FIGURE 4. HD2 AND HD3 vs f_{IN}

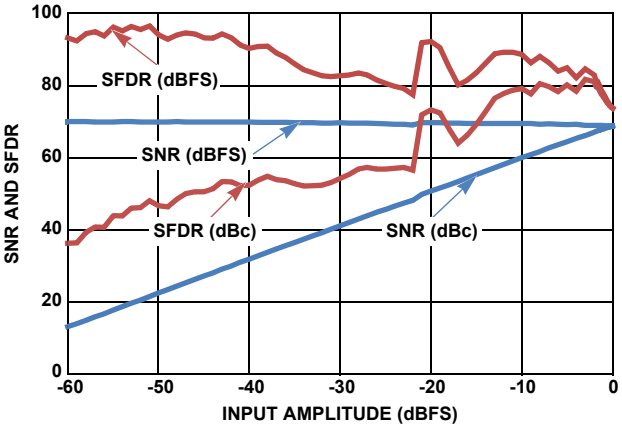


FIGURE 5. SNR AND SFDR vs A_{IN}

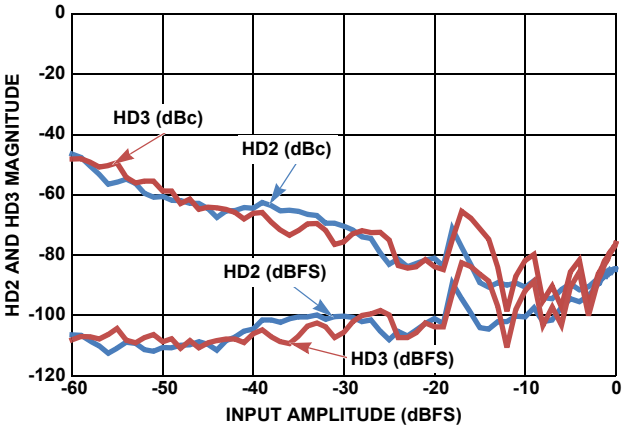


FIGURE 6. HD2 AND HD3 vs A_{IN}

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

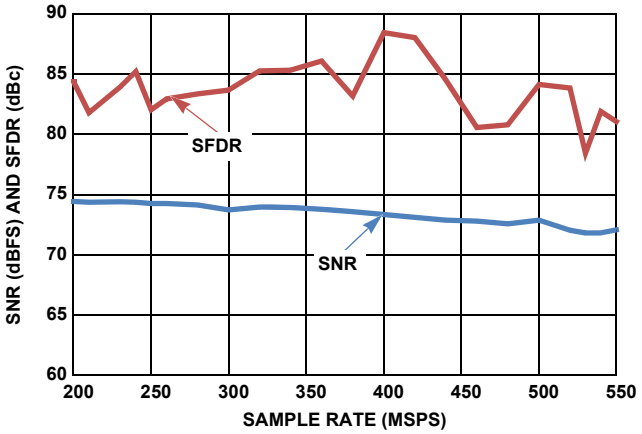


FIGURE 7. SNR AND SFDR vs f_{SAMPLE}

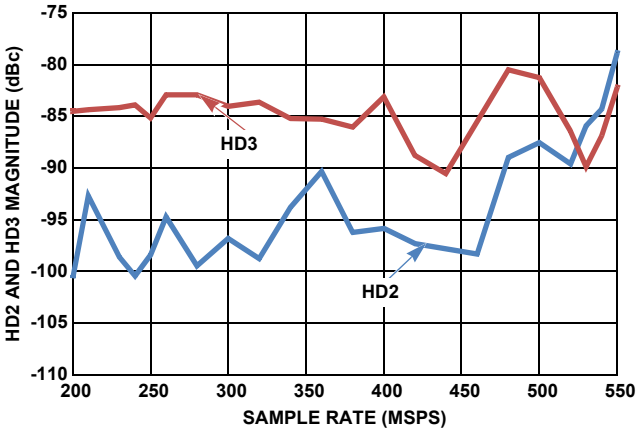


FIGURE 8. HD2 AND HD3 vs f_{SAMPLE}

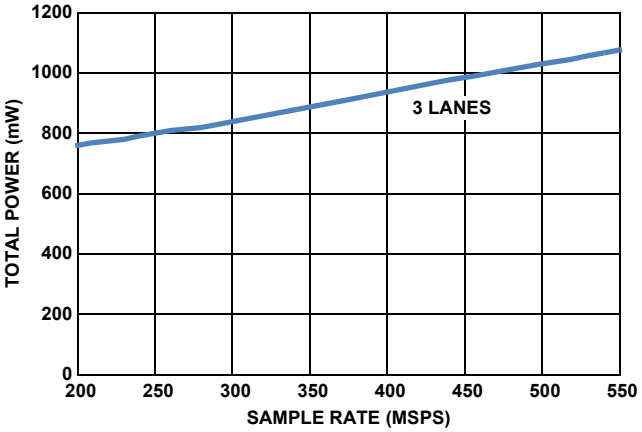


FIGURE 9. POWER vs f_{SAMPLE}

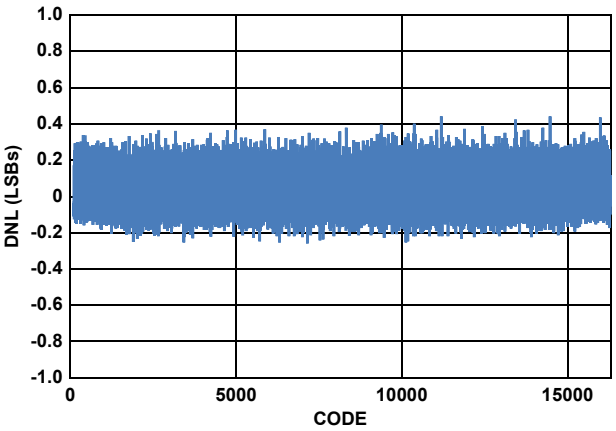


FIGURE 10. DIFFERENTIAL NONLINEARITY

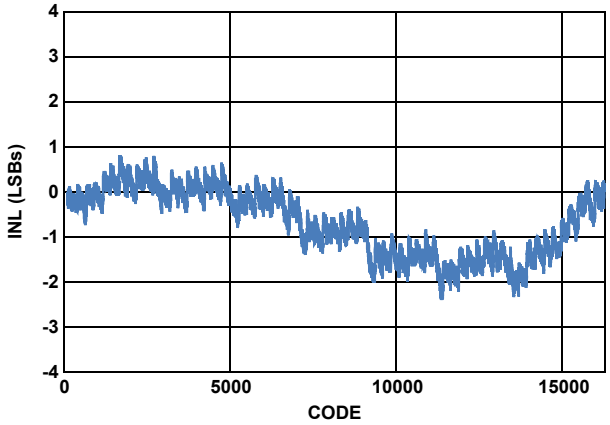


FIGURE 11. INTEGRAL NONLINEARITY

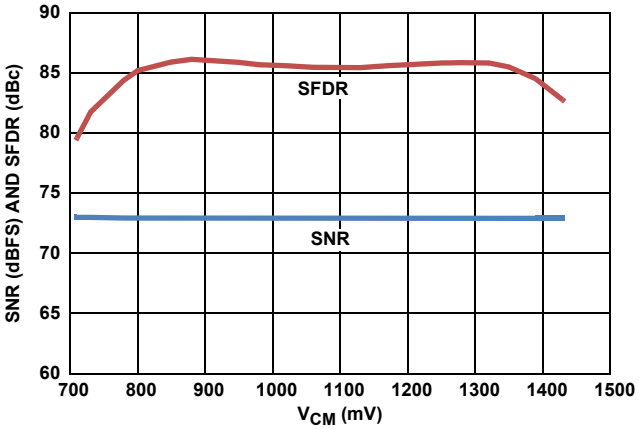


FIGURE 12. SNR AND SFDR vs V_{CM}

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

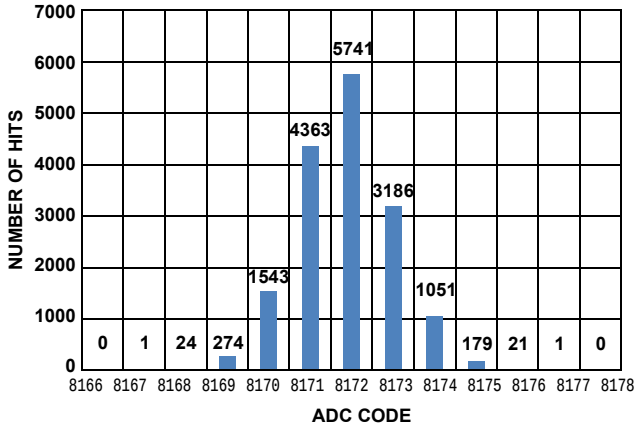


FIGURE 13. NOISE HISTOGRAM

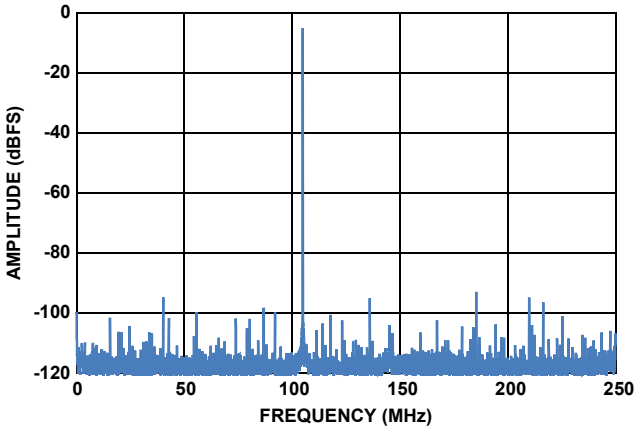


FIGURE 14. SINGLE-TONE SPECTRUM @ 105MHz

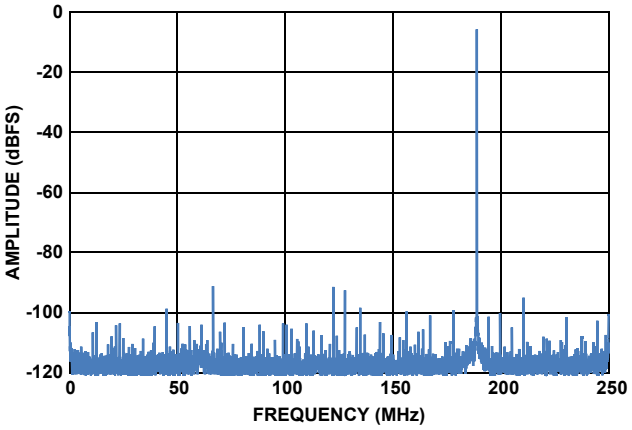


FIGURE 15. SINGLE-TONE SPECTRUM @ 190MHz

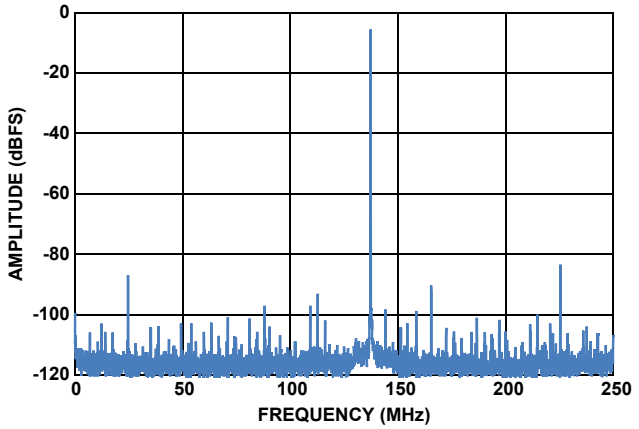


FIGURE 16. SINGLE-TONE SPECTRUM @ 363MHz

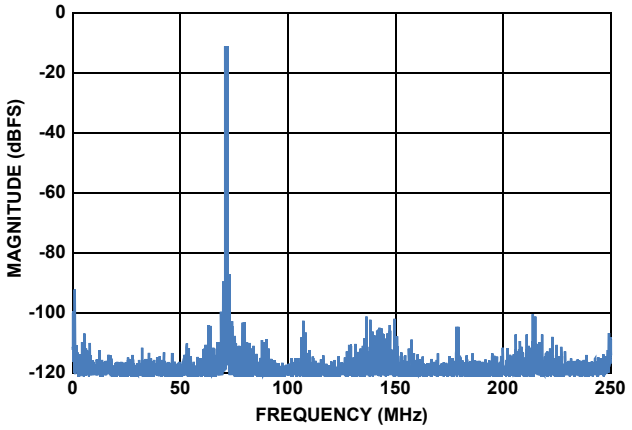


FIGURE 17. TWO-TONE SPECTRUM (F1 = 70MHz, F2 = 71MHz AT -7dBFS)

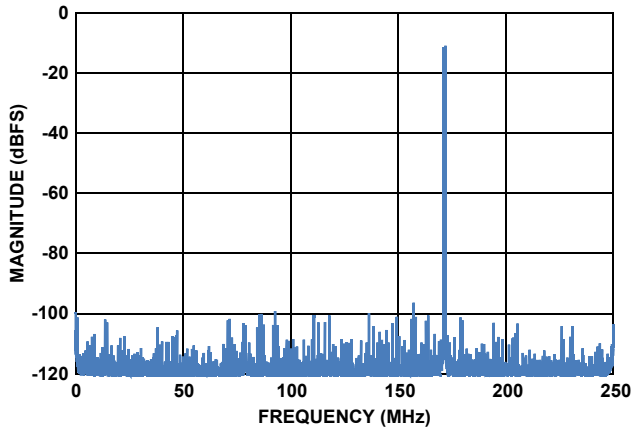


FIGURE 18. TWO-TONE SPECTRUM (F1 = 170MHz, F2 = 171MHz AT -7dBFS)

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

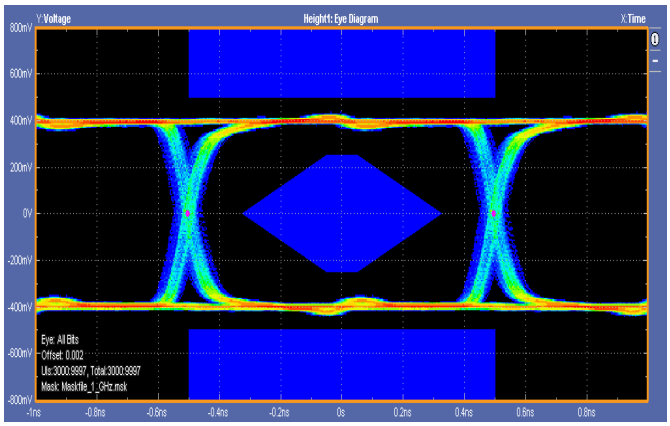


FIGURE 19. SERDES DATA EYE at 1.0Gbps

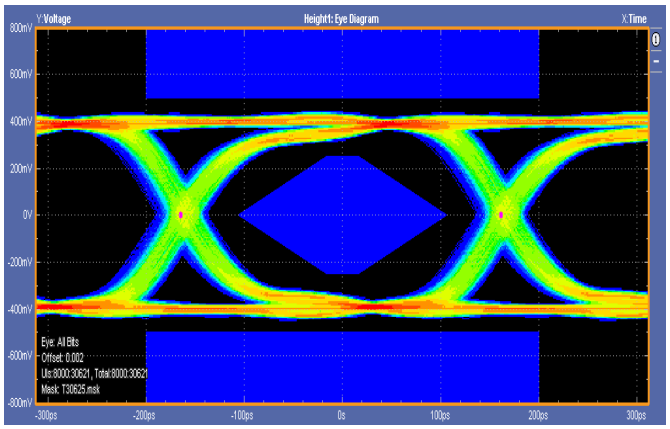


FIGURE 20. SERDES DATA EYE at 3.0Gbps

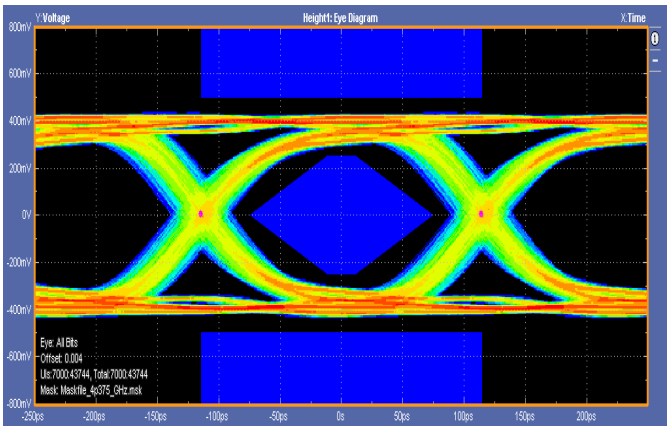


FIGURE 21. SERDES DATA EYE at 4.375Gbps

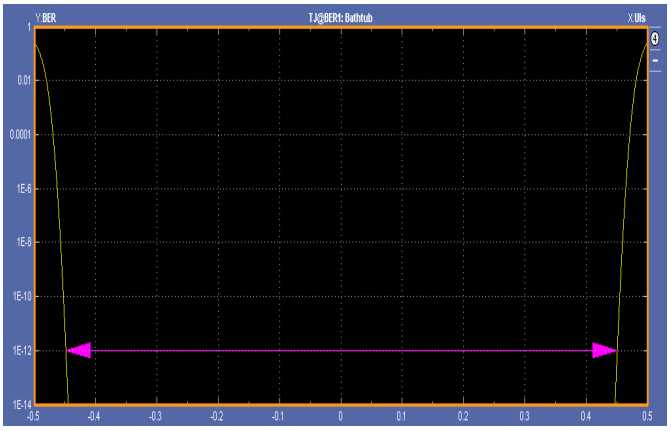


FIGURE 22. SERDES BATHTUB at 1.0Gbps

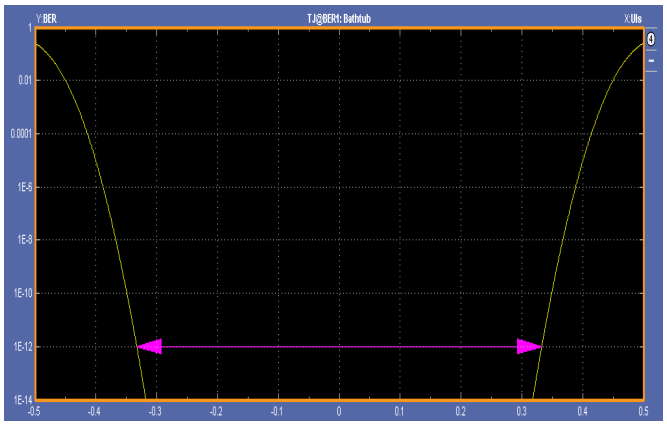


FIGURE 23. SERDES BATHTUB at 3.0Gbps

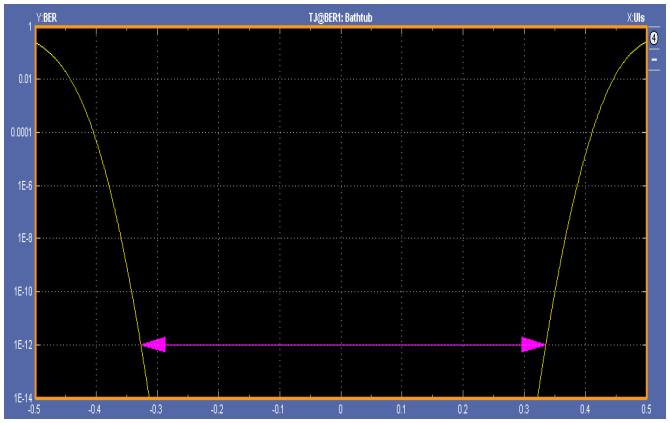


FIGURE 24. SERDES BATHTUB at 4.375Gbps

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 500MSPS. **(Continued)**

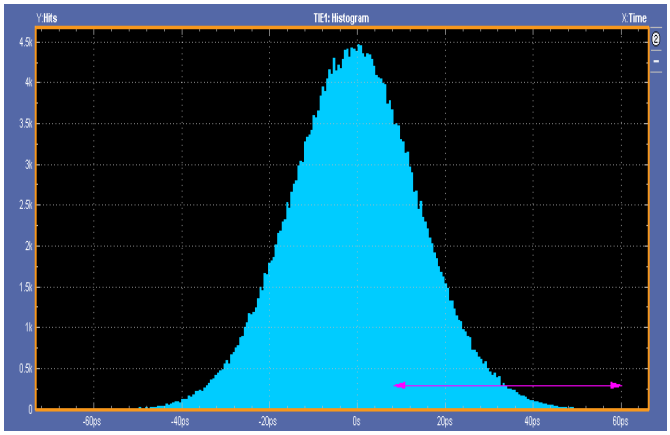


FIGURE 25. SERDES Histogram at 1.0Gbps

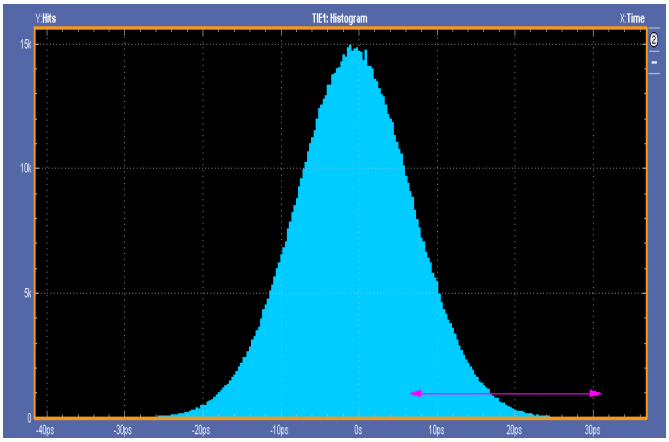


FIGURE 26. SERDES Histogram at 3.0Gbps

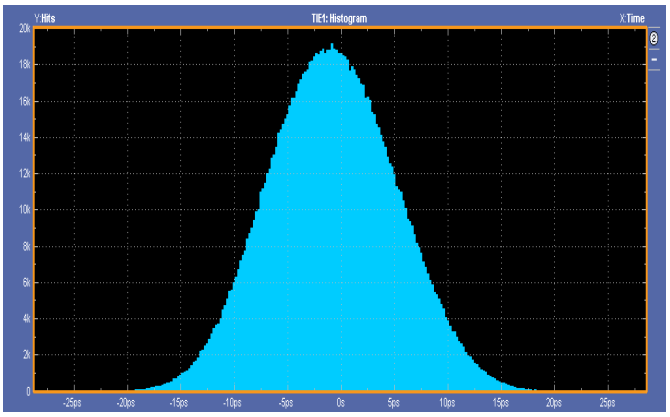


FIGURE 27. SERDES Histogram at 4.375Gbps

Theory of Operation

Functional Description

The device is based upon a 14-bit, 250MSPS ADC converter core that utilizes a pipelined successive approximation architecture (see Figure 28). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied.

Power-On Calibration

The ADC core(s) perform a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional.
- SPI communications must not be attempted during calibration, with the only exception of performing read operations on the cal_done register at address 0xB6.

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 29. Calibration status can be determined by reading the cal_status bit (LSB) at 0xB6. This bit is ‘0’ during calibration and goes to a logic ‘1’ when calibration is complete. During calibration the JESD204 transmitter PLL is not locked to the ADC sample clock, so the CML outputs will toggle at an undetermined rate. Normal operation is resumed once calibration is complete.

At 250MSPS the nominal calibration time is 280ms, while the maximum calibration time is 550ms.

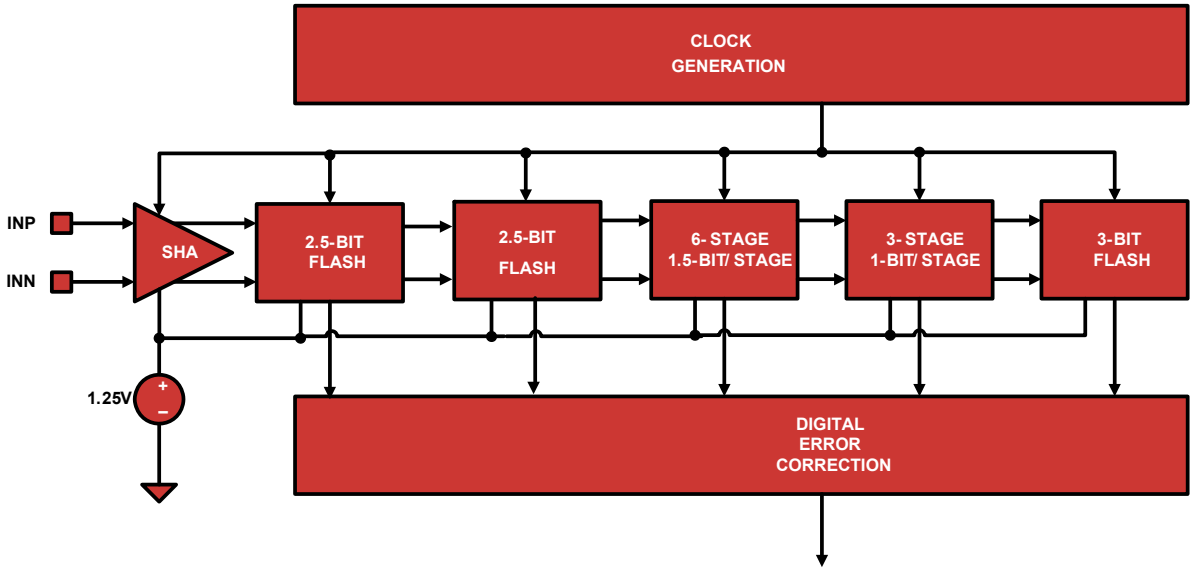


FIGURE 28. ADC CORE BLOCK DIAGRAM

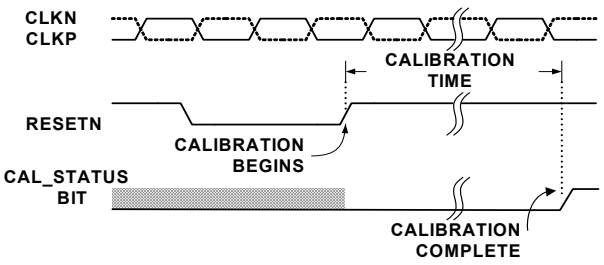


FIGURE 29. CALIBRATION TIMING

User Initiated Reset

Recalibration of the ADC can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA214S50 changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the ADC under the environmental conditions at which it will operate.

A supply voltage variation of <100mV will generally result in an SNR change of <0.5dBFS and SFDR change of <3dBc. In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS will typically result in an SNR change of <0.5dBFS and an SFDR change of <3dBc.

Figures 30 through 32 show the effect of temperature on SNR and SFDR performance with power on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power on calibration at -40°C, +25°C and +85°C. Best performance is typically achieved by a user-initiated power on calibration at the operating conditions, as stated earlier. However, it can be seen that performance drift with temperature is not a very strong function of the temperature at which the power on calibration is performed.

Temperature Calibration

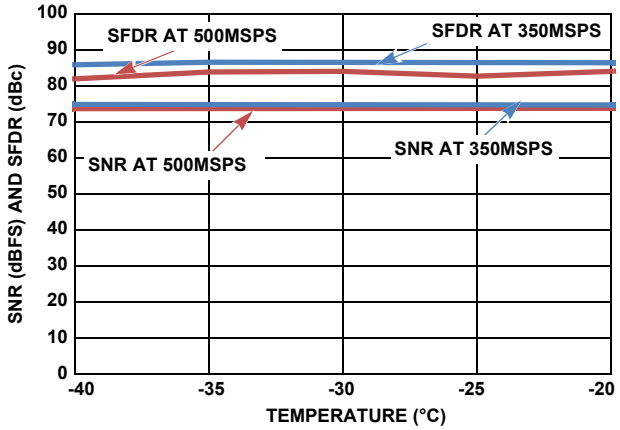


FIGURE 30. TYPICAL SNR AND SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40°C, f_{IN} = 105MHz

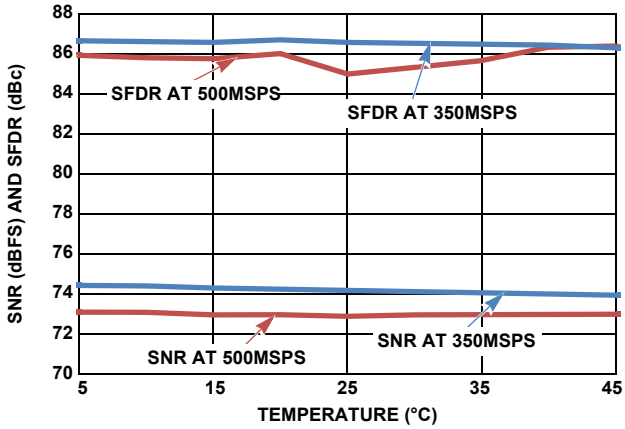


FIGURE 31. TYPICAL SNR AND SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, f_{IN} = 105MHz

Temperature Calibration (Continued)

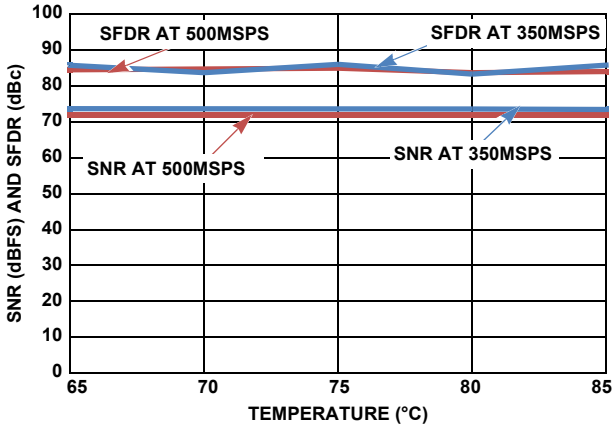


FIGURE 32. TYPICAL SNR AND SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, f_{IN} = 105MHz

Analog Input

A single fully differential input (VINP/VINN) connects to the sample and hold amplifier (SHA) of each unit ADC. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage as shown in Figure 33.

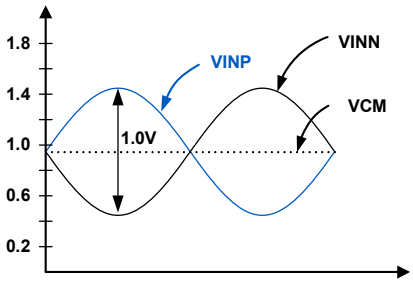


FIGURE 33. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 34 through 36. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 34 and 35.

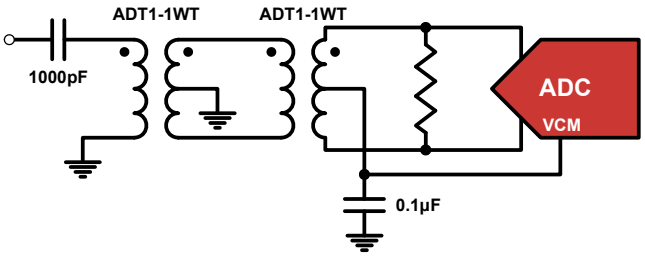


FIGURE 34. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

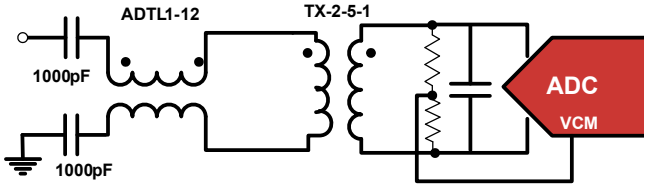


FIGURE 35. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA214S50 is 600Ω.

The SHA design uses a switched capacitor input stage (see Figure 48), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 2:1 or 1:1 transformer and low shunt resistance are recommended for optimal performance.

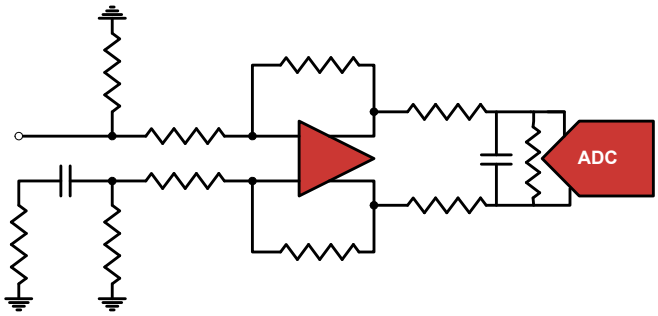


FIGURE 36. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in the simplified block diagram in Figure 36, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance. Intersil's new ISL552xx differential amplifier family can also be

used in certain AC applications with minimal performance degradation. Contact the factory for more information.

When an over range occurs, the data sample output bits are held at full scale (all 0's or all 1's), thus allowing the detection of this condition in the receiver device.

Clock Input

The clock input circuit is a differential pair (see Figure 49). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 37. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to $AV_{DD}/2$ through a Thevenin equivalent of 10kΩ to facilitate AC coupling.

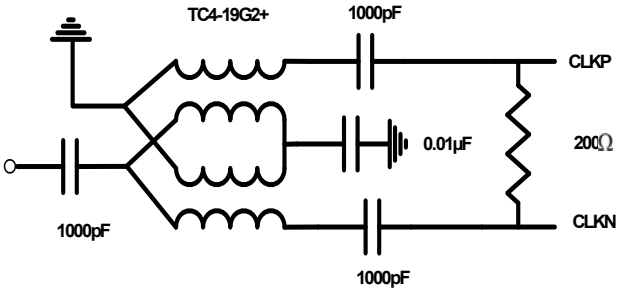


FIGURE 37. RECOMMENDED CLOCK DRIVE

A selectable 2x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate. Use of the 2x frequency divider enables the use of the Phase Slip feature, which enables the system to be able to select the phase of the divide by 2 that causes the ADC to sample the analog input.

TABLE 1. CLKDIV PIN SETTINGS

CLKDIV PIN	DIVIDE RATIO
AVSS	2
Float	1
AVDD	Not Allowed

The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. See "SPI Physical Interface" on page 26. A delay-locked loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to 52µs to regain lock at 500MSPS. The lock time is inversely proportional to the sample rate.

The DLL has two ranges of operation, slow and fast. The slow range can be used for ADC sample rates between 80MSPS and 200MSPS, while the default fast range can be used from 160MSPS to the maximum specified sample rate. The lane data rate is related to the ADC core sample rate by a relationship that is defined by the JESD204 transmitter configuration, and has additional frequency constraints; see"JESD204 Transmitter" on page 21 for additional details.

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 38.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

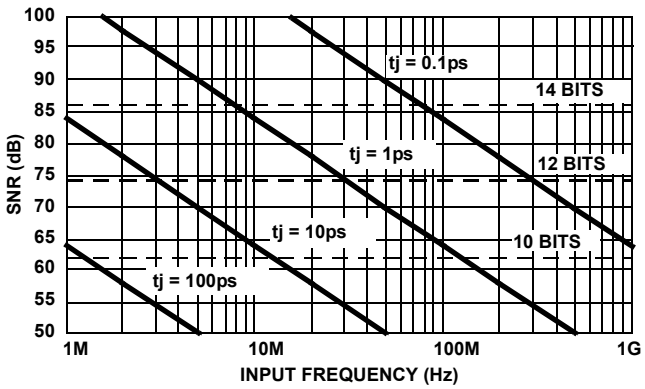


FIGURE 38. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise as well. Internal aperture jitter is the uncertainty in the sampling instant. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each ADC is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

Digital Outputs

The digital outputs are in CML format, and feature analog and digital characteristics compliant with the JESD204 standard requirements.

Power Dissipation

The power dissipated by the device is dependent on the ADC sample rate and the number of active lanes in the link. There is a fixed bias current drawn from the analog supply for the ADC, along with a fixed bias current drawn from the digital supply for each active lane. The remaining power dissipation is linearly related to the sample rate.

Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the ADC is not required. Two power saving modes are available: Nap, and Sleep. Nap mode reduces power dissipation significantly while taking a very short time to return to functionality. Sleep mode reduces power consumption drastically while taking longer to return to functionality.

In Nap mode the JESD204 lanes will continue to produce valid encoded data, allowing the link to remain active and thus return to a functional state quickly. The data transmitted over the lanes in nap mode is the last valid ADC sample, repeated until leaving nap mode. The 8b/10b encoder's running disparity will prevent the potentially long time repetition of this last valid sample from creating DC bias on the lane. In sleep mode the JESD204 lanes will be deactivated to conserve power. Thus, sometime after wake up code group alignment will be required to reestablish the link.

The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. The JESD204 link will only remain established during nap mode if the input clock continues to remain stable during the nap period.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 2. Please note that power on calibration occurs at power up time regardless of the state of the NAPSLP pin; immediately following this power on calibration routine the device will enter nap or sleep state if the NAPSLP pin voltage dictates it is to do so.

TABLE 2. NAPSLP PIN SETTINGS

NAPSLP PIN	MODE
AVSS	Normal
Float	Nap
AVDD	Sleep

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. However, if the ADC is powered-on with the NAPSLP pin in either Nap or Sleep modes, the pin must be first set to Normal before the SPI port will be enabled. Therefore, before the SPI port can be used to override the NAPSLP pin setting, the ADC must have been put into Normal mode at least once using the NAPSLP pin. Further details on the SPI port are contained in "Serial Peripheral Interface" on page 26.

Data Format

Output data can be presented in three formats: two's complement(default), Gray code and offset binary. The data format can be controlled through the SPI port by writing to address 0x73. Details on this are contained in "Serial Peripheral Interface" on page 26.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 39 shows this operation.

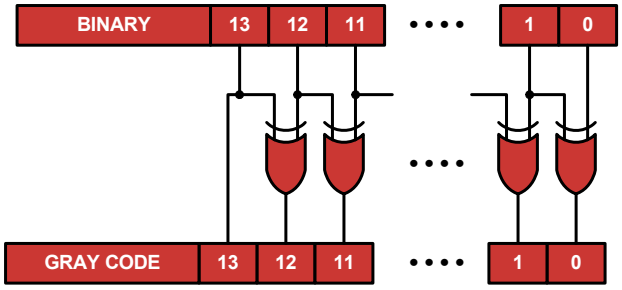


FIGURE 39. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 40.

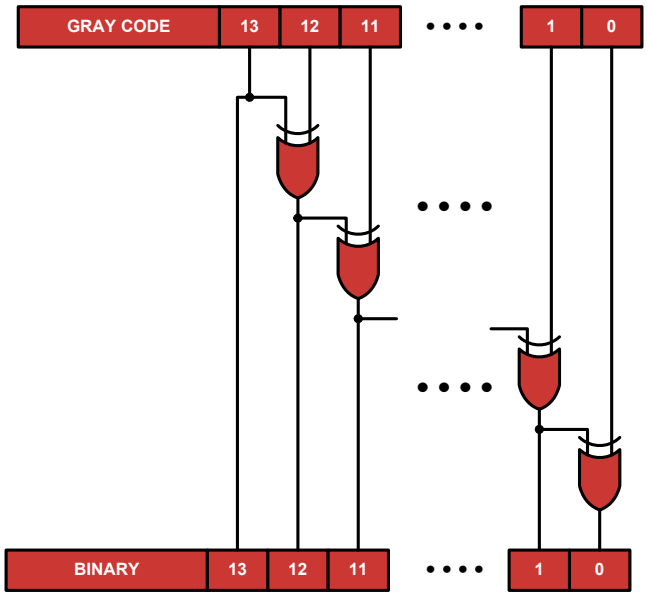


FIGURE 40. GRAY CODE TO BINARY CONVERSION

Mapping of the input voltage to the various data formats is shown in Table 3.

TABLE 3. INPUT VOLTAGE TO OUTPUT CODE MAPPING

INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT	GRAY CODE
–Full Scale	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000
–Full Scale + 1LSB	00 0000 0000 0001	10 0000 0000 0001	00 0000 0000 0001
Mid–Scale	10 0000 0000 0000	00 0000 0000 0000	11 0000 0000 0000
+Full Scale – 1LSB	11 1111 1111 1110	01 1111 1111 1110	10 0000 0000 0001
+Full Scale	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000

I2E Requirements and Restrictions

Overview

I2E is a blind and background capable algorithm, designed to transparently eliminate interleaving artifacts. This circuitry eliminates interleave artifacts due to offset, gain, and sample time mismatches between unit A/Ds, and across supply voltage and temperature variations in real-time.

Differences in the offset, gain, and sample times of time-interleaved A/Ds create artifacts in the digital outputs. Each of these artifacts creates a unique signature that may be detectable in the captured samples. The I2E algorithm optimizes performance by detecting error signatures and adjusting each unit A/D using minimal additional power.

I2E calibration is off by default at power-up. The I2E algorithm can be put in Active Run state via SPI. When the I2E algorithm is in Active Run state, it detects and corrects for offset, gain, and sample time mismatches in real time (see Track Mode description under "Active Run State" on page 20). However, certain analog input characteristics can obscure the estimation of these mismatches. The I2E algorithm is capable of detecting these obscuring analog input characteristics, and as long as they are present I2E will stop updating the correction in real time. Effectively, this freezes the current correction circuitry to the last known-good state (see Hold Mode description under "Active Run State" on page 20). Once the analog input signal stops obscuring the interleaved artifacts, the I2E algorithm will automatically start correcting for mismatch in real time again.

Active Run State

During the Active Run state the I2E algorithm actively suppresses artifacts due to interleaving based on statistics in the digitized data. I2E has two modes of operation in this state (described in the following), dynamically chosen in real-time by the algorithm based on the statistics of the analog input signal.

1. Track Mode refers to the default state of the algorithm, when all artifacts due to interleaving are actively being eliminated. To be in Track Mode the analog input signal to the device must adhere to the following requirements:

- Possess total power greater than -20dBFS, integrated from 1MHz to Nyquist but excluding signal energy in a 100kHz band centered at $f_S/4$

The criteria above assumes 500MSPS operation; the frequency bands should be scaled proportionally for lower sample rates. Note that the effect of excluding energy in the 100kHz band around of $f_S/4$ exists in every Nyquist zone. This band generalizes to the form ($N*f_S/4$ - 50kHz) to ($N*f_S/4$ + 50kHz), where N is any odd integer. An input signal that violates these criteria briefly (approximately 10µs), before and after which it meets this criteria, will not impact system performance.

The algorithm must be in Track Mode for approximately one second (defined in I2Epost_t specification) after power-up before the specifications apply. Once this requirement has been met, the specifications of the device will continue to be met while I2E remains in Track Mode, even in the presence of temperature and supply voltage changes.

2. Hold Mode refers to the state of the I2E algorithm when the analog input signal does not meet the requirements specified above. If the algorithm detects that the signal no longer meets the criteria, it automatically enters Hold Mode. In Hold Mode, the I2E circuitry freezes the adjustment values based on the most recent set of valid input conditions. However, in Hold Mode, the I2E circuitry will not correct for new changes in interleave artifacts induced by supply voltage and temperature changes. The I2E circuitry will remain in Hold Mode until such time as the analog input signal meets the requirements for Track Mode.

Power Meter

The power meter calculates the average power of the analog input, and determines if it's within range to allow operation in Track Mode. Both AC RMS and total RMS power are calculated, and there are separate SPI programmable thresholds and hysteresis values for each.

FS/4 Filter

A digital filter removes the signal energy in a 100kHz band around $f_S/4$ before the I2E circuitry uses these samples for estimating offset, gain, and sample time mismatches (data samples produced by the A/D are unaffected by this filtering). This allows the I2E algorithm to continue in Active Run state while in the presence of a large amount of input energy near the $f_S/4$ frequency. This filter can be powered down if it's known that the signal characteristics won't violate the restrictions. Powering down the FS/4 filter will reduce power consumption by approximately 30mW.

Nyquist Zones

The I2E circuitry allows the use of any one Nyquist zone without configuration, but requires the use of only one Nyquist zone. Inputs that switch dynamically between Nyquist zones will cause poor performance for the I2E circuitry. For example, I2E will function properly for a particular application that has f_S = 500MSPS and uses the 1st Nyquist zone (0MHz to 250MHz). I2E will also function properly for an application that uses f_S = 500MSPS and the 2nd Nyquist zone (250MHz to 500MHz). I2E will not function properly for an application that uses f_S = 500MSPS, and input frequency bands from 150MHz to 210MHz and 250MHz to 290MHz simultaneously. There is no need to configure the I2E algorithm to use a particular Nyquist zone, but no dynamic switching between Nyquist zones is permitted while I2E is running. If the analog input signal switches between multiple Nyquist zones, it may be necessary to reset I2E by turning if off and back on (via SPI register 0x31 bit 0) to properly calibrate in the new Nyquist zone.

Configurability and Communication

I2E can respond to status queries, be turned on and turned off, and generally configured via SPI programmable registers. Configuring of I2E is generally unnecessary unless the application cannot meet the requirements of Track Mode on or after power up. Parameters that can be adjusted and read back include FS/4 filter threshold and status, Power Meter threshold and status, and initial values for the offset, gain, and sample time values to use when I2E starts.

Clock Divider Synchronous Reset

The function of clock divider synchronous reset is available as a SPI-programmable overloaded function on the SYNCP and SYNCN pins. Given that the clock divider reset and SYNC features have the same electrical and timing requirements, this overloading allows the system to generate only a single well timed signal with respect to the ADC sample clock and select the ADC's interpretation of the signal as a SPI-programmable option (see SPI register 0x77 description for more information). By default the SYNCP and SYNCN pins will function as the JESD204 SYNC~.

The use of clock divider reset function is a requirement in a system that uses the ISLA214S50, ISLA214S35, or CLKDIV = 2, and also requires time alignment or deterministic latency of multiple devices. Please contact the factory for more details about this feature and its usage.

Soft Reset

Soft reset is a function intended to be used when the power on reset is to be re-run. An application may decide to issue a soft calibration command after significant temperature change or after a change in the sample rate frequency to optimize performance under the new condition.

Soft reset is issued by writing the Soft Reset bit at SPI address 0x00. Soft reset is a self-resetting bit in that will automatically return to 0 once the power on calibration has completed.

JESD204 Transmitter

Overview

The conversion data is presented by a JESD204B-compliant SERDES interface. The SERDES lane data rate supports typical speeds up to 4.375Gbps, exceeding the 3.125Gbps maximum specified by the JESD204 rev A standard. Two packing modes are supported: Efficient and Simple. A SYNC input is included, which is used for lane initialization as well as time alignment of multiple converter devices. AC coupling of the SERDES lane(s) on the board is required. A block diagram of this SERDES transmitter is shown in Figure 41.

For more information about the standardized characteristics and features of a JESD204 interface, please see JESD204 rev A and rev B standards. For application design support, including evaluation kit schematics and layout, reference FPGA project(s), and simulation models for functionality and signal integrity, please contact the factory and/or view application notes on the Intersil website.

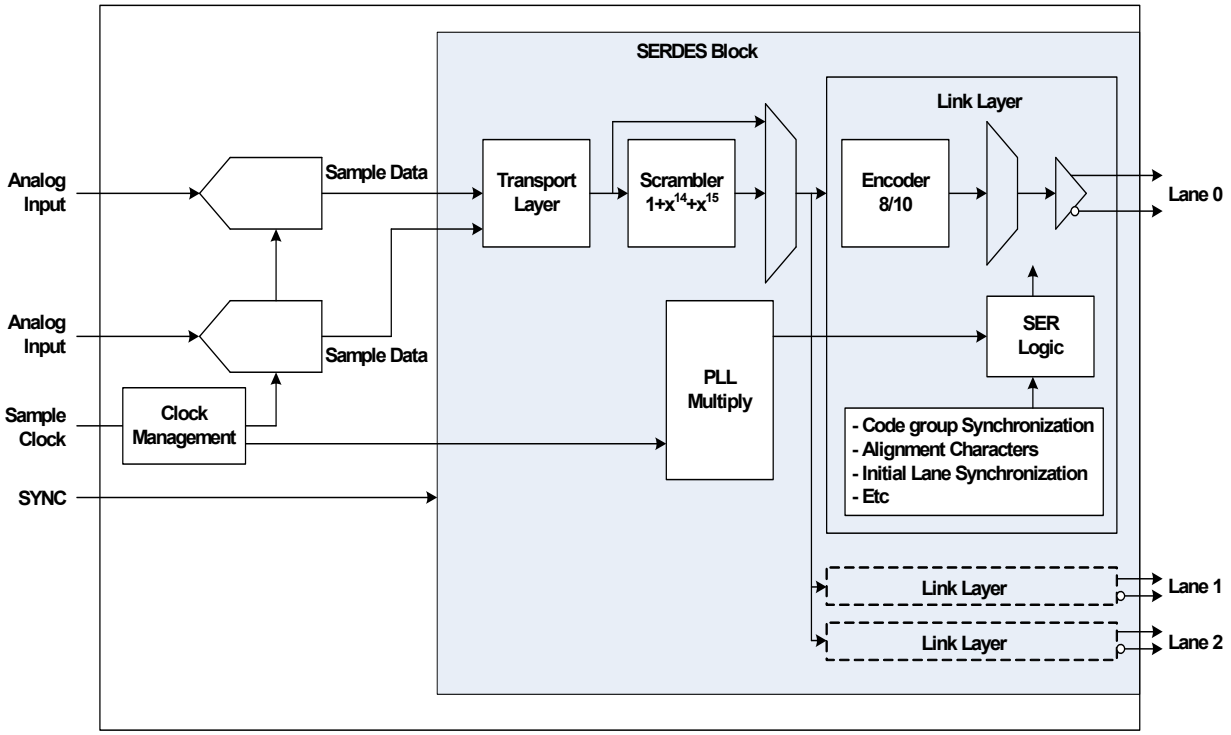


FIGURE 41. SERDES TRANSMITTER BLOCK DIAGRAM

To maximize flexibility at the system level, two transport layer packing modes are supported: simple and efficient. These two modes allow the system designer flexibility to trade off between the number of lanes to support a given throughput, the data rate of these lanes, and the complexity of the receiver. This translates directly into providing system level trade-offs between cost, power, and resource usage of the receiver and complexity of the solution.

Simple mode packs informationless bits onto each ADC sample to form full 16-bit data. In simple mode packing, the frame clock and ADC sample clock are the same frequency, easing frequency scaling requirements at the system level, but decreasing the payload efficiency of the lanes. Decreased payload efficiency of the lanes increases the lane data rate required to support a given throughput, and may require additional lanes to support a given configuration. The degree of payload efficiency loss is dependent on the ADC resolution.

Efficient mode packs sequential ADC samples into a contiguous block of an integer number of octets, and then slices the block into the octets for transport. This mode always achieves the theoretical maximum payload of the lanes (80%) regardless of the resolution of the ADC and the number of lanes used. This mode provides the minimum number of lanes at the minimum data rate that is theoretically possible given the 8b/10b encoding used in JESD204 systems. In efficient packing mode, frame clock and the ADC sample clock have an M/N relationship, where M and N are small integers and vary depending on the ADC resolution and number of lanes selected. Efficient mode packing may require additional frequency scaling elements (internal FPGA PLLs or discrete frequency scaling devices) to generate the frame clock for the receiving device.

The default configuration for this device is efficient packing mode. Reconfiguration into the simple packing mode is accomplished by programming the JESD204 parameters via the SPI bus. See Table 5 for the full list of parameters values for each mode and product. Via SPI, the JESD204 transmitter is highly configurable, supporting efficient to simple mode packing reconfiguration as well as "downgrading" a given product's JESD204 interface. For example, reconfiguring a 3-lane product into 2 lanes (with each running faster than with 3 lanes), or reducing the resolution of the ADC(s) to slow down the lane data rate in systems where the full ADC resolution is not required, are supported. Please contact the factory for a full list of downgradeable configurations that are supported.

Signal integrity plots, including data eye, BER bathtub curves, and edge histogram plots versus lane data rate can be found in the typical operating curves section.

Initial Lane Alignment

The link initialization process is started by asserting the SYNC~ signal to the ADC device. This assertion causes the JESD204 transmitter to generate comma characters, which are used by the receiver to accomplish code group synchronization (bit and octet alignment, respectively). Once code group synchronization is detected in the receiver, it de-asserts the SYNC~ signal, causing the JESD204 transmitter to generate the initial lane alignment sequence (ILA). The ILA is comprised of 4 multi-frames of data in a standard format, with the length of each multi-frame determined by the K parameter as programmed into the SPI JESD204 parameter table. The ILA includes standard control character markers that can be used to perform channel bonding in the receiving device if desired. The 2nd multi-frame includes the full JESD204 parameter data, allowing the receiver to auto-detect the lane configuration if desired.

After completion of the ILA the JESD204 transmitter begins transmitting ADC sample data. Continuous link and lane alignment monitoring is accomplished via an octet substitution scheme. The last octet in each frame, if identical to the last octet in the previous frame, is replaced with a specific control character. If both sides of the link support lane synchronization, the last octet in each multi-frame, if identical to the last octet in the previous frame, is replaced with a different specific control character. A more complete description of the link initialization sequence, including finite state machine implementation, can be found in the JESD204 rev A standard.

LANE DATA RATE

The lane data rate for this product family is constrained to be greater than or equal to 1Gbps and less than or equal to 3.125Gbps for guaranteed operation, so as to be consistent with the lane data rate limit of 3.125Gbps set by the JESD204 rev A standard. The lane data rate can typically exceed 4.2Gbps for this product family.

SCRAMBLER

The bypassable scrambler is compliant with the scrambler defined in the JESD204 rev A standard.

This implementation seeds the scrambler with the initial lane alignment sequence, such that the first two octets following the sequence can be properly descrambled if the receiver also passes the lane alignment sequence through its descrambler. Even if the receiver does not implement this detail, the 3rd and subsequent octets can be descrambled to yield ADC data due to the self-synchronizing nature of the scrambler used.

MULTI-CHIP TIME ALIGNMENT

The JESD204 standard (in various revisions) provides the capability to time align multiple JESD204 ADC devices to a single logic device (FPGA or ASIC). This feature is critical in many applications that cannot tolerate the variable latency of the JESD204 link, and that must process pipeline depth correct data from more than one ADC device.

Time alignment of multiple devices provides the capability to align samples from multiple JESD204 ADC devices in the system in a pipeline-depth correct manner, thus enabling the system to analyze the ADC data from multiple devices while eliminating the variable latency of the JESD204 link as a concern. This capability enables configurations of JESD204 ADCs as IQ, interleave, and/or simultaneously-sampled converters.

This ADC family uses the asserted to de-asserted SYNC~ transition as the absolute time event with which to generate a known sequence of characters at the JESD204 transmitter of equal pipeline depth between all ADC devices in the system to be time aligned. This is consistent with the JESD204 rev B subclass 2 device definition.

Test Patterns

The complexity of the JESD204 interface merits much more test pattern capability than less complex parallel interfaces. This device family consequently supports a much wider range of test patterns than previous ADC families.

Supported test patterns include both transport and link layer patterns. Transport layer patterns are passed through the transport layer of the JESD204 transmitter, following the same sequence of being packed and sliced into octets as the ADC sample data. Link layer test patterns bypass the transport layer and are injected directly into the 8b/10b encoder, serialized, and sent out of the physical media. Test pattern generation is controlled through SPI register 0xC0.

Link layer PRBS patterns are standard PRBS patterns that can be used with built-in standard PRBS checkers in, for example, FPGA SERDES-capable pins.

All transport layer test patterns re-initialize their phase when the SYNC~ de-assertion occurs; consequently, a system that provides a well-timed SYNC~ signal with respect to the ADC sample clock can expect transport layer test patterns to have consistent phase with respect to that de-assertion, which can be a significant aid when debugging the system.

TABLE 4. JESD204 CONFIGURATIONS AND CLOCK FREQUENCIES

PRODUCT	DESCRIPTION	PACKING MODE	NUMBER OF LANES	ADC SAMPLE CLOCK RANGE (MHz) (Note 16)	LANE DATA RATE MULTIPLIER FROM ADC SAMPLE CLOCK RATE	LANE DATA RATE (GBPS) (Note 16)
ISLA214S50	500MSPS, 14-bit	Efficient	3	200 to 500	(14-bits)*(1 ADC channel)*(10/8 encoder overhead)/(3 lanes) = (140/24) = 5.8333	1.16667 to 2.916675
ISLA214S35	350MSPS, 14-bit	Efficient	2	175 to 350	(14-bits)*(1 ADC channel)*(10/8 encoder overhead)/(2 lanes) = (140/16) = 8.75	1.53125 to 3.0625
		Simple	2	175 to 310	(14-bits+2-bit tail)*(1 ADC channel)*(10/8 encoder overhead)/(2 lanes) = (160/16) = 10	1.75 to 3.1

NOTE:

16. Maximum sample clock range calculated using the smaller of the maximum ADC core sample rate and the 3.125 Gbps maximum lane data rate dictated in the JESD204 rev A standard. Typically the maximum lane data rate achievable on these products far exceeds 3.125Gbps.

TABLE 5. JESD204 PARAMETERS

PRODUCT	PACKING MODE	NUMBER OF LANES	JESD204 PARAMETER	ENCODED	JESD204 PARAMETERS AND FRAME MAP (Notes 17, 18, 19)						
ISLA214S50	Efficient	3	CF = 0	0							
			CS = 0	0	C0S0[13:6]	C0S0[5:0]	C0S1[11:4]	C0S1[3:0]	C0S2[9:2]	C0S2[1:0]	C0S3[7:0]
			F = 7	6		C0S1[13:12]		C0S2[13:10]		C0S3[13:8]	
			HD = 0	0							
			L = 3	2	C0S4[13:6]	C0S4[5:0]	C0S5[11:4]	C0S5[3:0]	C0S6[9:2]	C0S6[1:0]	C0S7[7:0]
			M = 1	0		C0S5[13:12]		C0S6[13:10]		C0S7[13:8]	
			N = 14	13							
			N' = 14	13	C0S8[13:6]	C0S8[5:0]	C0S9[11:4]	C0S9[3:0]	C0S10[9:2]	C0S10[1:0]	C0S11[7:0]
			S = 12	11		C0S9[13:12]		C0S10[13:10]		C0S11[13:8]	
			K >= 3	>= 2							

TABLE 5. JESD204 PARAMETERS (Continued)

PRODUCT	PACKING MODE	NUMBER OF LANES	JESD204 PARAMETER	ENCODED	JESD204 PARAMETERS AND FRAME MAP (Notes 17, 18, 19)						
ISLA214S35	Efficient	2	CF = 0	0							
			CS = 0	0	C0S0[13:6]	C0S0[5:0]	C0S1[11:4]	C0S1[3:0]	C0S2[9:2]	C0S2[1:0]	C0S3[7:0]
			F = 7	6		C0S1[13:12]		C0S2[13:10]		C0S3[13:8]	
			HD = 0	0							
			L = 2	1	C0S4[13:6]	C0S4[5:0]	C0S5[11:4]	C0S5[3:0]	C0S6[9:2]	C0S6[1:0]	C0S7[7:0]
			M = 1	0		C0S5[13:12]		C0S6[13:10]		C0S7[13:8]	
			N = 14	13							
			N' = 14	13							
			S = 8	7							
			K >= 3	>= 2							
ISLA214S35	Simple	2	CF = 0	0							
			CS = 0	0	C0S0[13:6]	C0S0[5:0]					
			F = 2	1		TT					
			HD = 0	0							
			L = 2	1	C1S0[13:6]	C1S0[5:0]					
			M = 2	1		TT					
			N = 14	13							
			N' = 16	15							
			S = 1	0							
			K >= 9	>= 8							

NOTES:

17. The JESD204 parameters are shown as their actual values, with the JESD204 encoded values (i.e., the values that are programmed into the SPI registers) in the next column over. Typically values that must always be greater than 1 are encoded as value minus 1, and so on.
18. Frame map format decoder: "CxSy[a:b]" = Converter x, Sample y, bits a through b. For example, "C0S0[13:6]" = Converter 0, Sample 0, bits 13 through 6, etc. "T" = Tail bit (information-less bit packed in the transport layer mapping to form octets).
19. The topmost lane in the graphical frame map is Lane0, followed by Lane1 and Lane 2 (for 3-lane configurations).

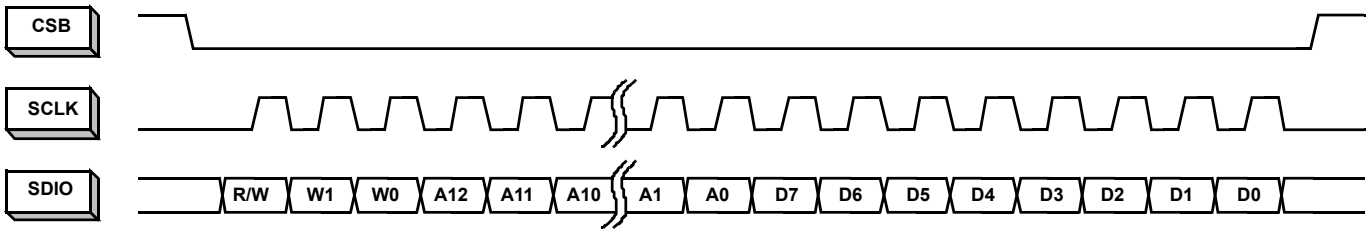


FIGURE 42. MSB-FIRST ADDRESSING

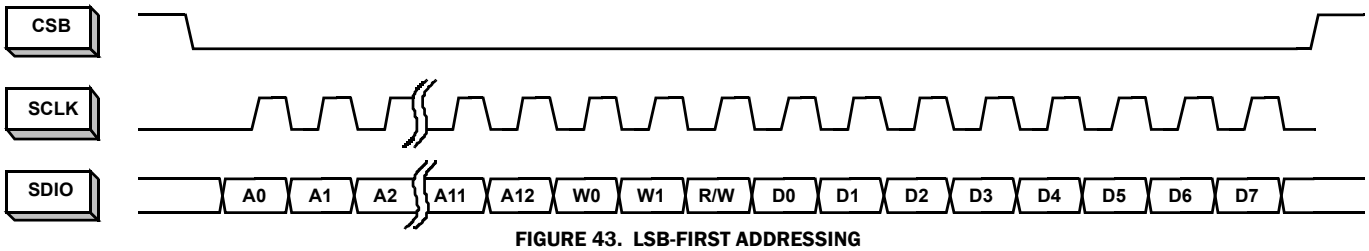
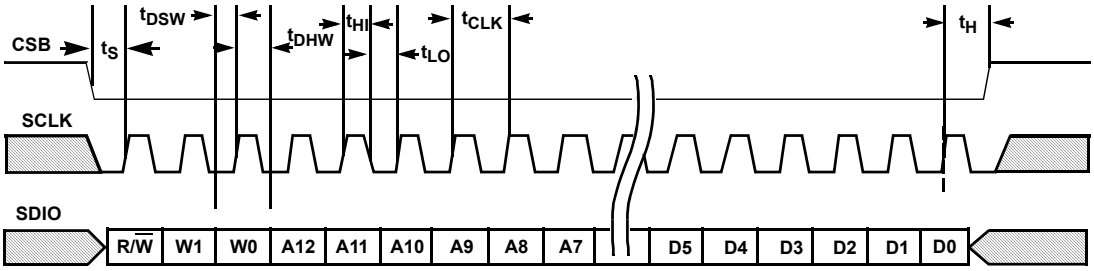
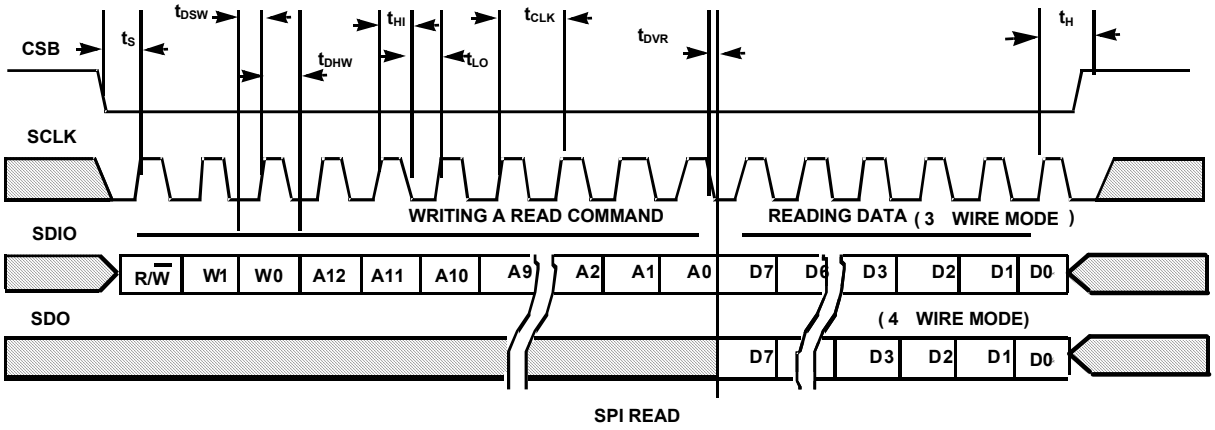


FIGURE 43. LSB-FIRST ADDRESSING



SPI WRITE

FIGURE 44. SPI WRITE



SPI READ

FIGURE 45. SPI READ

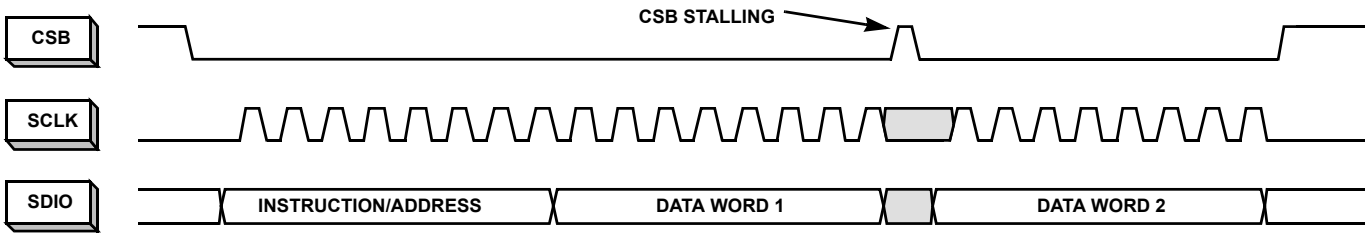


FIGURE 46. 2-BYTE TRANSFER

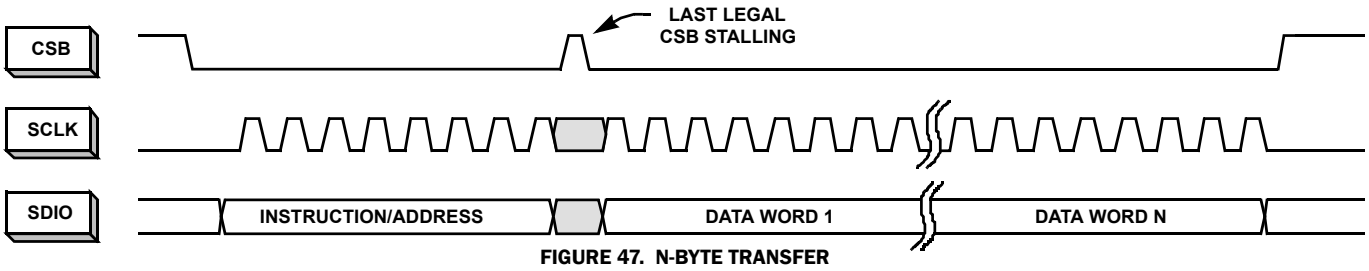


FIGURE 47. N-BYTE TRANSFER

Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data output (SDO), and serial data input/output (SDIO). The maximum SCLK rate is equal to the ADC sample rate (f_{SAMPLE}) divided by 14 for write operations and f_{SAMPLE} divided by 32 for reads. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ADC functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high-to-low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 42 and 43 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 6). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 44, and timing values are given in "Switching Specifications" on page 9.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the ADC (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

TABLE 6. BYTE TRANSFER SELECTION

[W1:W0]	BYTES TRANSFERRED
00	1
01	2
10	3
11	4 or more

Figures 46 and 47 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

SPI Configuration

ADDRESS 0X00: CHIP_PORT_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various micro controllers.

Bit 7 SDO Active

Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved

This bit should always be set high.

Bits 3:0 These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

ADDRESS 0X02: BURST_END

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. The burst is ended by pulling the CSB pin high. Setting the burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.

Device Information

ADDRESS 0X08: CHIP_ID

ADDRESS 0X09: CHIP_VERSION

The generic die identifier and a revision number, respectively, can be read from these two registers.

Device Configuration/Control

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Intersil ADC products.

ADDRESS 0X20: OFFSET_COARSE_ADC0

ADDRESS 0X21: OFFSET_FINE_ADC0

The input offset of the ADC core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in Table 7. The data format is twos complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 7. OFFSET ADJUSTMENTS

PARAMETER	0x20[7:0] COARSE OFFSET	0x21[7:0] FINE OFFSET
Steps	255	255
–Full Scale (0x00)	-133LSB (-47mV)	-5LSB (-1.75mV)
Mid–Scale (0x80)	0.0LSB (0.0mV)	0.0LSB
+Full Scale (0xFF)	+133LSB (+47mV)	+5LSB (+1.75mV)
Nominal Step Size	1.04LSB (0.37mV)	0.04LSB (0.014mV)

ADDRESS 0X22: GAIN_COARSE_ADC0

ADDRESS 0X23: GAIN_MEDIUM_ADC0

ADDRESS 0X24: GAIN_FINE_ADC0

Gain of the ADC core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2%. ('0011' ≅ -4.2% and '1100' ≅ +4.2%) It is recommended to use one of the coarse gain settings (-4.2%, -2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 0x0023 and 0x24.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 8. COARSE GAIN ADJUSTMENT

0x22[3:0] core 0 0x26[3:0] core 1	NOMINAL COARSE GAIN ADJUST (%)
Bit3	+2.8
Bit2	+1.4
Bit1	-2.8
Bit0	-1.4

TABLE 9. MEDIUM AND FINE GAIN ADJUSTMENTS

PARAMETER	0x23[7:0] MEDIUM GAIN	0x24[7:0] FINE GAIN
Steps	256	256
–Full Scale (0x00)	-2%	-0.20%
Mid–Scale (0x80)	0.00%	0.00%
+Full Scale (0xFF)	+2%	+0.2%
Nominal Step Size	0.016%	0.0016%

ADDRESS 0X25: MODES

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes (refer to "Nap/Sleep" on page 19). This functionality can be overridden and controlled through the SPI. However, if the ADC is powered-on with the NAPSLP pin in either Nap or Sleep modes, the pin must first be set to Normal before the SPI port will be enabled. Therefore, before the SPI port can be used to override the NAPSLP pin setting, the ADC must have been put into Normal mode at least once using the NAPSLP pin. This register is not changed by a Soft Reset.

TABLE 10. POWER-DOWN CONTROL

VALUE	0x25[2:0] POWER DOWN MODE
000	Pin Control
001	Normal Operation
010	Nap Mode
100	Sleep Mode

ADDRESS 0X26: OFFSET_COARSE_ADC1

ADDRESS 0X27: OFFSET_FINE_ADC1

The input offset of ADC core#1 can be adjusted in fine and coarse steps in the same way that offset for core#0 can be adjusted. Both adjustments are made via an 8-bit word as detailed in Table 7. The data format is two's complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

ADDRESS 0X28: GAIN_COARSE_ADC1

ADDRESS 0X29: GAIN_MEDIUM_ADC1

ADDRESS 0X2A: GAIN_FINE_ADC1

Gain of ADC core #1 can be adjusted in coarse, medium and fine steps in the same way that core #0 can be adjusted. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2.

ADDRESS 0X30: I2E STATUS

The I2E general status register.

Bits 0 and 1 indicate if the I2E circuitry is in Active Run or Hold state. The state of the I2E circuitry is dependent on the analog input signal itself. If the input signal obscures the interleave mismatched artifacts such that I2E cannot estimate the mismatch, the algorithm will dynamically enter the Hold state. For example, a DC mid-scale input to the A/D does not contain sufficient information to estimate the gain and sample time skew mismatches, and thus the I2E algorithm will enter the Hold state. In the Hold state, the analog adjustments for interleave correction will be frozen and mismatch estimate calculations will cease until such time as the analog input achieves sufficient quality to allow the I2E algorithm to make mismatch estimates again.

Bit 0: 0 = I2E has not detected a low power condition. 1 = I2E has detected a low power condition, and the analog adjustments for interleave correction are frozen.

Bit 1: 0 = I2E has not detected a low AC power condition. 1 = I2E has detected a low AC power condition, and I2E will continue to correct with best known information but will not update its interleave correction adjustments until the input signal achieves sufficient AC RMS power.

Bit 2: When first started, the I2E algorithm can take a significant amount of time to settle (~1s), dependent on the characteristics of the analog input signal. 0 = I2E is still settling, 1 = I2E has completed settling.

ADDRESS 0X31: I2E CONTROL

The I2E general control register. This register can be written while I2E is running to control various parameters.

Bit 0: 0 = turn I2E off, 1= turn I2E on

Bit 1: 0 = no action, 1 = freeze I2E, leaving all settings in the current state. Subsequently writing a 0 to this bit will allow I2E to continue from the state it was left in.

Bit 2-4: Disable any of the interleave adjustments of offset, gain, or sample time skew

Bit 5: 0 = bypass notch filter, 1 = use notch filter on incoming data before estimating interleave mismatch terms

ADDRESS 0X32: I2E STATIC CONTROL

The I2E general static control register. This register must be written prior to turning I2E on for the settings to take effect.

Bit 1-4: Reserved, always set to 0

Bit 5: 0 = normal operation, 1 = skip coarse adjustment of the offset, gain, and sample time skew analog controls when I2E is first turned on. This bit would typically be used if optimal analog adjustment values for offset, gain, and sample time skew have been preloaded in order to have the I2E algorithm converge more quickly.

The system gain of the pair of interleaved core A/Ds can be set by programming the medium and fine gain of the reference A/D before turning I2E on. In this case, I2E will adjust the non-reference A/D's gain to match the reference A/D's gain.

Bit 7: Reserved, always set to 0

ADDRESS 0X4A: I2E POWER DOWN

This register provides the capability to completely power down the I2E algorithm and the Notch filter. This would typically be done to conserve power.

BIT 0: Power down the I2E Algorithm

BIT 1: Power down the Notch Filter

ADDRESS 0X50-0X55: I2E FREEZE THRESHOLDS

This group of registers provides programming access to configure I2E's dynamic freeze control. As with any interleave mismatch correction algorithm making estimates of the interleave mismatch errors using the digitized application input signal, there are certain characteristics of the input signal that can obscure the mismatch estimates. For example, a DC input to the A/D contains no

information about the sample time skew mismatch between the core A/Ds, and thus should not be used by the I2E algorithm to update its sample time skew estimate. Under such circumstances, I2E enters Hold state. In the Hold state, the analog adjustments will be frozen and mismatch estimate calculations will cease until such time as the analog input achieves sufficient quality to allow the I2E algorithm to make mismatch estimates again.

These registers allow the programming of the thresholds of the meters used to determine the quality of the input signal. This can be used by the application to optimize I2E's behavior based on knowledge of the input signal. For example, if a specific application had an input signal that was typically 30dB down from full scale, and was primarily concerned about analog performance of the A/D at this input power, lowering the RMS power threshold would allow I2E to continue tracking with this input power level, thus allowing it to track over voltage and temperature changes.

0x50 (LSBs), 0x51 (MSBs) RMS Power Threshold

This 16-bit quantity is the RMS power threshold at which I2E will enter Hold state. The RMS power of the analog input is calculated continuously by I2E on incoming data.

Only the upper 12 bits of the ADC sample outputs are used in the averaging process for comparison to the power threshold registers. A 12-bit number squared produces a 24-bit result (for A/D resolutions under 12-bits, the A/D samples are MSB-aligned to 12-bit data). A dynamic number of these 24-bit results are averaged to compare with this threshold approximately every 1µs to decide whether or not to freeze I2E. The 24-bit threshold is constructed with bits 23 through 20 (MSBs) assigned to 0, bits 19 through 4 assigned to this 16-bit quantity, and bits 3 through 0 (LSBs) assigned to 0. As an example, if the application wanted to set this threshold to trigger near the RMS analog input of a -20dBFS sinusoidal input, the calculation to determine this register's value would be as shown by Equations 2 and 3:

$$RMS_{codes} = \frac{\sqrt{2}}{2} \times 10^{\left(\frac{-20}{20}\right)} \times 2^{12} \cong (290)\text{codes} \qquad \text{(EQ. 2)}$$

$$\text{hex}(((290))^2) = 0x14884_{TruncateMSBandLSBhexdigit} = \mathbf{0}x1488 \qquad \text{(EQ. 3)}$$

Therefore, programming 0x1488 into these two registers will cause I2E to freeze when the signal being digitized has less RMS power than a -20dBFS sinusoid.

The default value of this register is 0x1000, causing I2E to freeze when the input amplitude is less than -21.2 dBFS.

The freezing of I2E by the RMS power meter threshold affects the gain and sample time skew interleave mismatch estimates, but not the offset mismatch estimate.

0x52 RMS Power Hysteresis

In order to prevent I2E from constantly oscillating between the Hold and Track state, there is hysteresis in the comparison described above. After I2E enters a frozen state, the RMS input power must achieve ³ threshold value + hysteresis to again enter the Track state. The hysteresis quantity is a 24-bit value, constructed with bits 23 through 12 (MSBs) being assigned to 0, bits 11 through 4 assigned to this register's value, and bits 3 through 0 (LSBs) assigned to 0.

0X53(LSBS), 0X54(MSBS) AC RMS POWER THRESHOLD

Similar to RMS power threshold, there must be sufficient AC RMS power (or dV/dt) of the input signal to measure sample time skew mismatch for an arbitrary input. This is clear from observing the effect when a high voltage (and therefore large RMS value) DC input is applied to the A/D input. Without sufficient dV/dt in the input signal, no information about the sample time skew between the core A/Ds can be determined from the digitized samples. The AC RMS Power Meter is implemented as a high-passed (via DSP) RMS power meter.

The required algorithm is documented as follows.

1. Write the MSBs of the 16-bit quantity to SPI Address 0x54
2. Write the LSBs of the 16-bit quantity to SPI Address 0x53

Only the upper 12 bits of the ADC sample outputs are used in the averaging process for comparison to the power threshold registers. A 12-bit number squared produces a 24-bit result (for A/D resolutions under 12-bits, the A/D samples are MSB-aligned to 12-bit data). A dynamic number of these 24-bit results are averaged to compare with this threshold approximately every 1µs to decide whether or not to freeze I2E. The 24-bit threshold is constructed with bits 23 through 20 (MSBs) assigned to 0, bits 19 through 4 assigned to this 16-bit quantity, and bits 3 through 0 (LSBs) assigned to 0. The calculation methodology to set this register is identical to the description in the RMS power threshold description.

The freezing of I2E when the AC RMS power meter threshold is not met affects the sample time skew interleave mismatch estimate, but not the offset or gain mismatch estimates.

0x55 AC RMS Power Hysteresis

In order to prevent I2E from constantly oscillating between the Hold and Track state, there is hysteresis in the comparison described above. After I2E enters a frozen state, the AC RMS input power must achieve ³ threshold value + hysteresis to again enter the Track state. The hysteresis quantity is a 24-bit value, constructed with bits 23 through 12 (MSBs) being assigned to 0, bits 11 through 4 assigned to this register's value, and bits 3 through 0 (LSBs) assigned to 0.

Address 0x60-0x64: I2E initialization

These registers provide access to the initialization values for each of offset, gain, and sample time skew that I2E programs into the target core A/D before adjusting to minimize interleave mismatch. They can be used by the system to, for example, reduce the convergence time of the I2E algorithm by programming in the optimal values before turning I2E on. In this case, I2E only needs to adjust for temperature and voltage-induced changes since the optimal values were recorded.

Global Device Configuration/Control

ADDRESS 0X70: SKEW_DIFF

The value in the skew_diff register adjusts the timing skew between the two A/D cores. The nominal range and resolution of this adjustment are given in Table 11. The default value of this register after power-up is 80h.

TABLE 11. DIFFERENTIAL SKEW ADJUSTMENT

PARAMETER	0x70[7:0] DIFFERENTIAL SKEW
Steps	256
–Full Scale (0x00)	-6.5ps
Mid–Scale (0x80)	0.0ps
+Full Scale (0xFF)	+6.5ps
Nominal Step Size	51fs

ADDRESS 0X71: PHASE_SLIP

When using the clock_divide feature, the sample clock edge that the ADC uses to sample the analog input signal can be one of several different edges on the incoming higher frequency sample clock. For example, in clock_divide = 2 mode, every other incoming sample clock edge gets used by the ADC to sample the analog input. The phase_slip feature allows the system to control which edge of the incoming sample clock signals gets used to cause the sampling event, by “slipping” the sampling event by one input clock period each time phase_slip is asserted.

The clkdivrst feature can work in conjunction with phase_slip. After well-timed assertion of the clkdivrst signal (via overloading on the SYNC inputs), the sampling edge position with respect to the incoming clock rate will have been reset, allowing the system to “slip” whatever desired number of incoming clock periods from a known state.

ADDRESS 0X72: CLOCK_DIVIDE

The ADC has a selectable clock divider that can be set to divide by two or one (no division). By default, the tri-level CLKDIV pin selects the divisor This functionality can be overridden and controlled through the SPI, as shown in Table 12. This register is not changed by a Soft Reset.

TABLE 12. CLOCK DIVIDER SELECTION

VALUE	0x72[2:0] CLOCK DIVIDER
000	Pin Control
001	Divide by 1
010	Divide by 2
other	Not Allowed

ADDRESS 0X73: OUTPUT_MODE_A

The output_mode_A register controls the logical coding of the sample data. Data can be coded in three possible formats: two’s complement(default), Gray code or offset binary. See Table 13.

This register is not changed by a Soft Reset.

TABLE 13. OUTPUT FORMAT CONTROL

VALUE	0x73[2:0] OUTPUT FORMAT
000	Two’s Complement (Default)
010	Gray Code
100	Offset Binary

ADDRESS 0X74: OUTPUT_MODE_B

Bit 6 DLL Range

This bit sets the DLL operating range to fast (default) or slow.

Internal clock signals are generated by a delay-locked loop (DLL), which has a finite operating range. Table 14 shows the allowable sample rate ranges for the slow and fast settings.

TABLE 14. DLL RANGES

DLL RANGE	MIN	MAX	UNIT
Slow	80	200	MSPS
Fast	160	500	MSPS

ADDRESS 0X77: SYNC_FUNCTION

Bit 0 Clkdivrst

This bit controls the functionality of the SYNCP, SYNCN pins on this device. By default this bit equals ‘0’, which means that the functionality of the SYNCP, SYNCN pins is the JESD204 SYNC. Setting this bit equal to ‘1’ modifies the functionality of the SYNCP, SYNCN pins to be clkdivrst, which is a synchronous divider reset on all internal dividers in the device. Usage of this clkdivrst functionality is required to support multi-chip time alignment and deterministic latency for devices that use interleaved product configurations (ISLA214S50 and ISLA214S35), and for any other product configuration that uses clkdiv > 1. In both states, the setup and hold times with respect to the sample clock remain the same. Contact the factory for more details.

ADDRESS 0XB6: CALIBRATION STATUS

The LSB at address 0xB6 can be read to determine calibration status. The bit is ‘0’ during calibration and goes to a logic ‘1’ when calibration is complete.This register is unique in that it can be read after POR at calibration, unlike the other registers on chip, which can’t be read until calibration is complete.

DEVICE TEST

The device can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A user can pick from preset built-in patterns by writing to the output test mode field [7:4] at 0xC0 or user defined patterns by writing to the user test mode field [2:0] at 0xC0. The user defined patterns should be loaded at address space 0xC1 through 0xD0, see the “SPI Memory Map” on page 33 for more detail. The test mode is enabled asynchronously to the sample clock, therefore several sample clock cycles may elapse before the data is present on the output bus.

ADDRESS 0XC0: TEST_IO

Bits 7:4 Output Test Mode

These bits set the test mode according to the description in “SPI Memory Map” on page 33.

Bits 2:0 User Test Mode

The three LSBs in this register determine the test pattern in combination with registers 0xC1 through 0xD0. Refer to the “SPI Memory Map” on page 33.

ADDRESS 0XC1: USER_PATT1_LSB

ADDRESS 0XC2: USER_PATT1_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 1.

ADDRESS 0XC3: USER_PATT2_LSB

ADDRESS 0XC4: USER_PATT2_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 2.

ADDRESS 0XC5: USER_PATT3_LSB

ADDRESS 0XC6: USER_PATT3_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 3.

ADDRESS 0XC7: USER_PATT4_LSB

ADDRESS 0XC8: USER_PATT4_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 4.

ADDRESS 0XC9: USER_PATT5_LSB

ADDRESS 0XCA: USER_PATT5_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 5.

ADDRESS 0XCB: USER_PATT6_LSB

ADDRESS 0XCC: USER_PATT6_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 6.

ADDRESS 0XCD: USER_PATT7_LSB

ADDRESS 0XCE: USER_PATT7_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 7.

ADDRESS 0XCF: USER_PATT8_LSB

ADDRESS 0XD0: USER_PATT8_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 8.

ADDRESS 0xDF - 0xF3: JESD204 REGISTERS

Address 0xDF-0xEE: JESD204 Parameter Interface

This set of registers controls the JESD204 transmitter configuration. By programming these parameters, the system can select between efficient and simple packing, select the number of powered up SERDES lanes, choose the ADC resolution transmitted, and so on. Contact the factory for details.

0xE0 through 0xED are the JESD204 parameter registers. These parameters are written to set the transport layer mapping of the JESD204 transmitter in this product family. These registers can be written to shift between efficient and simple packing, to enable or bypass scrambling, and to reduce the number of powered up lanes used in the link. Each speed graded product allows downgrading of the JESD204 link (such as reducing the number of lanes, reducing the converter resolution, etc), but not upgrading. These parameters are communicated on every lane of the link during the 2nd multi-frame of the initial lane alignment sequence, and therefore can be used by a generic JESD204A or JESD204B receiver that supports the given configuration. See the JESD204A or JESD204B specification for additional information on how these registers are used in a JESD204 system, including encoding rules.

ADDRESS 0XDF: JESD204_UPDATE_CONFIG_START

Bit 0 update_start

This self-resetting bit is used to indicate that some or all the JESD204 parameters (addresses 0xE0 through 0xED) are going to be written. Writing a '1' to this bit will hold the JESD204 PLL and transmitter in a reset state while these parameters are written, because these parameters can affect the transmitter's dynamic behavior (such as modifying the PLL's frequency multiplication). The bit will automatically reset to a '0' once a '1' is written to address 0xEE Bit[0] "update_complete". The recommended sequence for modifying the JESD204 transmitter is:

1. Write a '1' to 0xDF Bit[0]
2. Write some or all modified values to 0xE0 through 0xEC
3. Write a '1' to 0xEE Bit[0]. Note: 0xDF Bit[0] and 0xEE Bit[0] will automatically be reset to a '0' once configuration has been applied to the circuitry.

ADDRESS 0XE0: JESD204_CONFIG_0

Bits 7:0 “DID”, JESD204 Device Identification Number.

ADDRESS 0XE1: JESD204_CONFIG_1

Bits 3:0 “BID”, JESD204 Bank ID.

ADDRESS 0XE2: JESD204_CONFIG_2

Bits 4:0 “LID” JESD204 Lane Identification Number.

ADDRESS 0XE3: JESD204_CONFIG_3

Bit 7 "SCR", JESD204 SCR controls if scrambling across the SERDES lane(s) is enabled ('1' means enabled).

Bits 4:0 "L", JESD204 number of SERDES lanes in the link.

ADDRESS 0XE4: JESD204_CONFIG_4

Bits 7:0 “F”, JESD204 number of octets per frame.

ADDRESS 0XE5: JESD204_CONFIG_5

Bits 4:0 "K", JESD204 Number of frame periods per multi-frame period. This product family supports the full programmable range of K (decimal 0 through 31), although note that the JESD204 standard dictates a minimum number for this parameter that is configuration dependent. There must be at least 17 and no more than 1024 octets per multiframe. K must be set to meet this constraint.

ADDRESS 0XE6: JESD204_CONFIG_6

Bits 7:0 “M” JESD204 number of converters per device.

ADDRESS 0XE7: JESD204_CONFIG_7

Bits 7:6 "CS", JESD204 number of control bits per sample (Always '0' for this product family).

Bits 4:0 "N", JESD204 converter resolution.

ADDRESS 0XE8: JESD204_CONFIG_8

Bits 7:5 "SUBCLASSV", JESD204 Device Subclass Version
000 - Subclass 0
001 - Subclass 1 (not supported in this product family)
010 - Subclass 2

Bits 4:0 "N'", JESD204 total number of bits per sample.

ADDRESS 0XE9: JESD204_CONFIG_9

Bits 7:5 "JESDV" JESD204 Version
000 - JESD204A
001 - JESD204B

Bits 4:0 "S", JESD204 number of samples per converter per frame.

ADDRESS 0XEA: JESD204_CONFIG_10

Bit 7 "HD", JESD204 HD indicates if a converter's sample can be split across multiple lanes in the link (always '0' for this product family).

Bits 4:0 "CF", JESD204 number of control frames per frame clock (always '0' for this product family).

ADDRESS 0XEB: JESD204_CONFIG_11

Bits 7:0 “RES1”, JESD204 reserved for future use.

ADDRESS 0XEC: JESD204_CONFIG_12

Bits 7:0 “RES2”, JESD204 reserved for future use.

ADDRESS 0XED: JESD204_CONFIG_13

Bits 7:0 "FCHK", JESD204 checksum (unsigned sum MOD 256) of the other JESD204 parameter register values (0xE0 - 0xED). This is a read-only register, as the checksum is calculated by the device.

ADDRESS 0XEE: JESD204_UPDATE_CONFIG_COMPLETE

Bit 0 update_complete

This self-resetting bit is used to indicate that all the modifications to the JESD204 parameters are complete.

ADDRESS 0XEF: JESD204_PLL_MONITOR_RESET

Bit 0 “pll_lock_mon_rst”, This self resetting register resets the state of the 0xF0 Bit[0] "latched_pll_lockn" bit. The purpose of this pair of bits is as a debugging feature to the system designer. The "latched_pll_lockn" bit indicates if the JESD204 transmitter PLL inside the device has at any time lost lock since the last '1' was written to the pll_lock_mon_rst" bit. This can be used to help identify the source of intermittent link lost errors in the system.

ADDRESS 0XF0: JESD204_STATUS

Bit 2 "op_cfg_wrong" indicates if the JESD204 parameters (registers 0xE0 through 0xED) are supported by the JESD204 transmitter (a '1' indicates they are not supported, a '0' indicates they are supported).

Bit 1 "pll_lockn" indicates if the JESD204 transmitter PLL is currently locked (a '1' indicates it is not locked, a '0' indicates it is locked).

Bit 0 "latched_pll_lockn" indicates if the JESD204 transmitter PLL has lost lock since the last assertion of the "pll_lock_mon_rst" (see register 0xEF description for more information).

ADDRESS 0XF1: JESD204_SYNC

Bit 0 “sync_req” this register provides a SPI-programmable interface that can be used to assert and de-assert the JESD204 SYNC~ functionality. Certain systems may benefit from the elimination of SYNC~ as a separate board-level LVDS signal (and the power, PCB space, and pins it consumes), and these systems can use this register to functionally assert and de-assert SYNC~. For this bit to have any effect, a ‘1’ must have previously been written to the SYNC_FUNCTION (Address 0x77, bit 0).

A ‘1’ written to this bit will result in behavior identical to the assertion of SYNC~ (comma character generation), and ‘0’ will result in the behavior identical to the de-assertion of SYNC~ (initial lane alignment sequence followed by converter data). Usage of this SPI SYNC~ capability may compromise the system’s ability to perform multi-chip time alignment, as the SYNC~ asserted to de-asserted transition using this register is not well timed with respect to sample clock.

ADDRESS 0XF2: JESD204_TRANS_PAT_CONFIG

Bit 0 "no_mf_lane_sync", By default, this device family assumes that both sides of the link support lane synchronization. As per the JESD204 rev A and B standards, in this case continuous frame alignment monitoring via character substitution (section 5.3.3.4) is modified such that a different control character is substituted when the octet reoccurrence happens at the end of a multiframe. This behavior occurs when bit 0 is '0' (the power on default). writing a '1' to bit 0 will inform the JESD204 transmitter than the receiving device does not support lane synchronization, and therefore the transmitter will no longer substitute this different control character when reoccurrence of octets occurs at the end of a multi-frame.

Bit 1 "trans_pat_max_len" There is some ambiguity of the proper length of the JESD204 rev A section 5.1.6.2 required transport layer test pattern. Specifically, that the description perhaps should have "max()" in place of "min()" for the equation defining the length of the pattern. Setting bit 1 in this register to a '0' (also the power-on default) and issuing this test pattern by writing to 0xC0 will cause the pattern to assume a "min()" interpretation of the pattern described in section 5.1.6.2. Setting the bit to a '1' will assume a "max()" interpretation of the described pattern.

ADDRESS 0XF3: JESD204_CML_POLARITY

0xF3 Bit[2:0]: “TX polarity flip lane x” This register allows the system designer to invert the sense of the SERDES pins on a per lane basis. For example, writing a ‘1’ to Bit[0] causes LANE0N to functionally become LANE0P and LANE0P to become LANE0N.

This feature allows the system designer to avoid having to crossover P and N sides of the CML pair on the board to match pin out and layout of the transmitter and receiver. Typically, a trace crossover would require vias, which can degrade the signal integrity of the high-speed SERDES lanes.

SPI Memory Map

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
SPI Config/Control	00	port_config	SDO Active	LSB First	Soft Reset			Mirror (bit5)	Mirror (bit6)	Mirror (bit7)	00h
	01	Reserved	Reserved								
	02	burst_end	Burst end address [7:0]								00h
	03-07	Reserved	Reserved								
DUT Info	08	chip_id	Chip ID #								Read only
	09	chip_version	Chip Version #								Read only
	0A-0F	Reserved	Reserved								
Device Config/Control	10-1F	Reserved	Reserved								
	20	offset_coarse_adc0	Coarse Offset								cal. value
	21	offset_fine_adc0	Fine Offset								cal. value
	22	gain_coarse_adc0	Reserved				Coarse Gain				cal. value
	23	gain_medium_adc0	Medium Gain								cal. value
	24	gain_fine_adc0	Fine Gain								cal. value
	25	modes_adc0	Reserved					Power Down Mode ADC0 [2:0] 000 = Pin Control 001 = Normal Operation 010 = Nap 100 = Sleep Other codes = Reserved			00h NOT reset by Soft Reset
	26	offset_coarse_adc1	Coarse Offset								cal. value
	27	offset_fine_adc1	Fine Offset								cal. value
	28	gain_coarse_adc1	Reserved				Coarse Gain				cal. value
	29	gain_medium_adc1	Medium Gain								cal. value
	2A	gain_fine_adc1	Fine Gain								cal. value
	2B	modes_adc1	Reserved					Power Down Mode ADC1 [2:0] 000 = Pin Control 001 = Normal Operation 010 = Nap 100 = Sleep Other codes = Reserved			00h NOT reset by Soft Reset
	2C-2F	Reserved	Reserved								

SPI Memory Map (Continued)

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
I2E Control and Status	30	I2E_status				Reserved		I2E Settled	Low AC RMS Power	Low RMS Power	Read only
	31	I2E_control			Enable Notch Filter	Disable Offset	Disable Gain	Disable Skew	Freeze	Run	20h
	32	I2E_static_control	Reserved must be set to 0		Skip coarse adj.	Reserved, must be set to 0				Should be set to 1	01h
	33-49	Reserved	Reserved								
	4A	I2E_power_down							Notch Filter Power Down	I2E Power Down	03h
	4B	temp_counter_high						Temp Counter [10:8]			Read only
	4C	temp_counter_low	Temp Counter [7:0]								Read only
	4D	temp_counter_control		Enable	PD	Reset	Divider [2:0]			Select	00h
	4E-4F	Reserved	Reserved								
	50	I2E_rms_power_threshold_lsb	RMS Power Threshold, LSBs [7:0]								00h
	51	I2E_rms_power_threshold_msb	RMS Power Threshold, MSBs [15:8]								10h
	52	I2E_rms_hysteresis	RMS Power Hysteresis								FFh
	53	I2E_ac_rms_power_threshold_lsb	AC Power Threshold, LSBs, [7:0]								50h
	54	I2E_ac_rms_power_threshold_msb	AC Power Threshold, MSBs, [15:8]								00h
	55	I2E_ac_rms_hysteresis	AC RMS Power Hysteresis								10h
	56-5F	Reserved	Reserved								
	60	coarse_offset_init	Coarse Offset Initialization value								80h
	61	fine_offset_init	Fine Offset Initialization value								80h
	62	medium_gain_init	Medium Gain Initialization value								80h
	63	fine_gain_init	Fine Gain Initialization value								80h
	64	sample_time_skew_init	Sample Time Skew Initialization value								80h
	65-6F	Reserved	Reserved								
	70	skew_diff	Differential Skew								80h
	71	phase_slip	Reserved							Next Clock Edge	00h
	72	clock_divide						Clock Divide [2:0] 000 = Pin Control 001 = divide by 1 010 = divide by 2 Other codes = Reserved			00h NOT reset by Soft Reset

SPI Memory Map (Continued)

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
Device Config/Control	73	output_mode_A						Output Format [2:0] 000 = Two's Complement (Default) 010 = Gray Code 100 = Offset Binary Other codes = Reserved			00h NOT reset by Soft Reset
	74	output_mode_B		DLL Range 0 = Fast 1 = Slow Default='0'							00h NOT reset by Soft Reset
	75-76	Reserved	Reserved								
	77	SYNC_function								Clkdivrst	
	78-B5	Reserved	Reserved								
	B6	cal_status	Reserved							Calibration Done	Read Only
	B7-BF	Reserved									

SPI Memory Map (Continued)

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
Device Test	C0	test_io	Output Test Mode [7:4]				JESD Test	User Test Mode [2:0]			00h
			<7:4>=Output Test, <3> = JESD Test JESD Test=0 Output Test = 0x0= Output Test Mode Off. During calibration MSB justified constant output 0xCCCC 0x1 = Midscale adjusted by numeric format 0x2 = Plus full scale, adjusted by numeric format 0x3 = Minus full scale adjusted by numeric format 0x4 = Checkboard output - 0xAAAA, 0x5555 0x5 = reserved 0x6 = reserved 0x7 = 0xFFFF, 0x0000 all on pattern 0x8 = User pattern 8 deep, MSB justified with output 0x9 = reserved 0xA, Count-up ramp 0xB, PRBS-9 0xC, PRBS-15 0xD, PRBS-23 0xE, PRBS-31 0xF = reserved JESD Test=1 Output Test = 0x0 =Link Layer Repeat K28.5+Lane Alignment Sequence 0x1, Link Layer Repeat K28.5 0x2, Link Layer Repeat D21.5 0x3, Link Layer Repeat K28.7 0x4, Link Layer PRBS-7 0x5, Link Layer PRBS-23 0x6, Link Layer All Zeros 0x7, Link Layer All Ones 0x8-0xE, reserved 0xF, JESD204A section 5.1.6.2 Transport Layer Test Pattern					User Test Mode (Single ADC products only) 0 = user pattern 1 only 1 = cycle pattern 1 through 2 2 = cycle pattern 1 through 3 3 = cycle pattern 1 through 4 4 = cycle pattern 1 through 5 5 = cycle pattern 1 through 6 6 = cycle pattern 1 through 7 7 = cycle pattern 1 through 8 User Test Mode (Dual and interleaved ADC products only) 0 = cycle pattern 1 through 2 1 = cycle pattern 1 through 4 2 = cycle pattern 1 through 6 3 = cycle pattern 1 through 8 4 -7 = NA			
	C1	user_patt1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C2	user_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C3	user_patt2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C4	user_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C5	user_patt3_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C6	user_patt3_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C7	user_patt4_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C8	user_patt4_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C9	user_patt5_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CA	user_patt5_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CB	user_patt6_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CC	user_patt6_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CD	user_patt7_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CE	user_patt7_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CF	user_patt8_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	D0	user_patt8_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	D1-DE	Reserved	Reserved								

SPI Memory Map (Continued)

	ADDR. (Hex)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
JESD204 Interface	DF	JESD204_update_config_start								update_ start	00h
	E0	JESD204_config_0	*DID* (Device ID Number)								00h
	E1	JESD204_config_1					*BID* (Bank ID Number)				00h
	E2	JESD204_config_2				*LID* (Lane ID Number)					00h
	E3	JESD204_config_3	*SCR*			*L* (Number of Lanes per Device)					82h
	E4	JESD204_config_4	*F* (Number of Octets per Frame)								06h
	E5	JESD204_config_5				*K* (Number of octets per multi-frame)					02h
	E6	JESD204_config_6	*M* (Number of Converters per Device)								00h
	E7	JESD204_config_7	*CS* (Number of Control bits per Sample)			*N* (Converter Resolution in bits)					0Dh
	E8	JESD204_config_8	SUBCLASSV			*N'* (Total number of bits per Sample)					0Dh
	E9	JESD204_config_9	JESDV			*S* (Number of Samples per Converter per Frame)					0Bh
	EA	JESD204_config_10	*HD*			*CF* (Number of Control Words per Frame per Link)					00h
	EB	JESD204_config_11	*RES1*								00h
	EC	JESD204_config_12	*RES2*								00h
	ED	JESD204_config_13	*FCHK* (Checksum)								AFh
	EE	JESD204_update_config_complete								update_ complete	00h
	EF	JESD204_PLL_monitor_reset								pll_lock_ mon_rst	00h
	F0	JESD204_status						op_confg_ wrong	pll_lockn	latched_ pll_lockn	00h
	F1	JESD204_sync								sync_req	
	F2	JESD204_trans_pat_config							trans_pat_ max_len	no_mf_ lane_sync	
	F3	JESD204_CML_polarity						lane_2_ polarity	lane_1_ polarity	lane_0_ polarity	00h
	F4-FF	Reserved	Reserved								

Equivalent Circuits

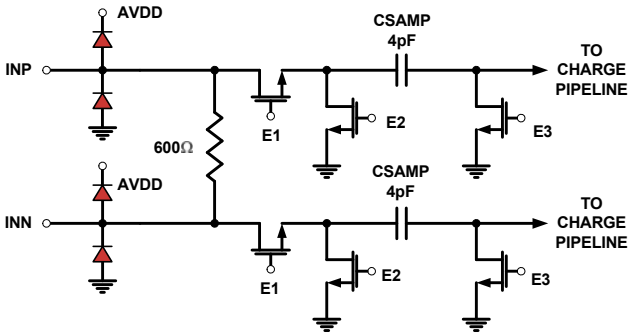


FIGURE 48. ANALOG INPUTS

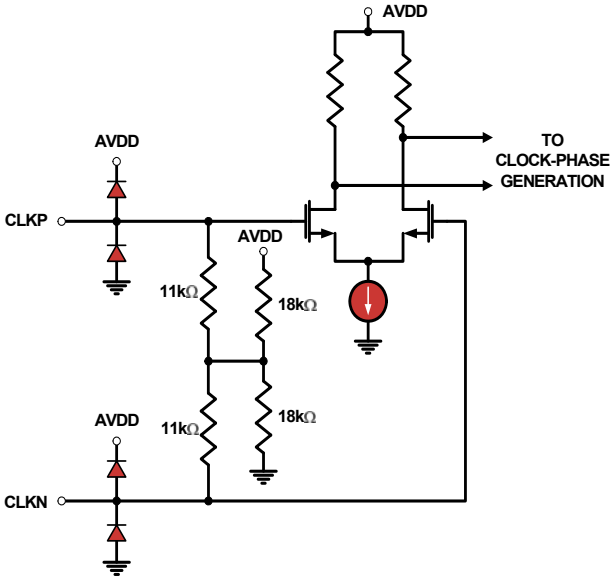


FIGURE 49. CLOCK INPUTS

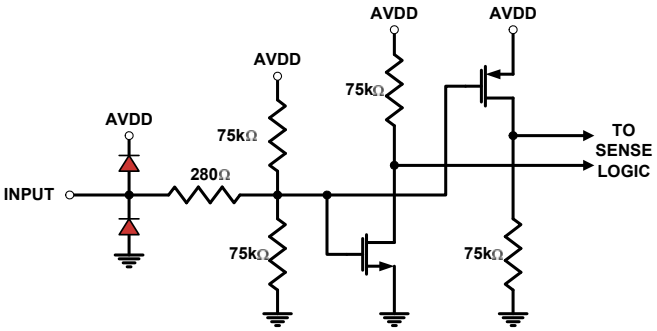


FIGURE 50. TRI-LEVEL DIGITAL INPUTS

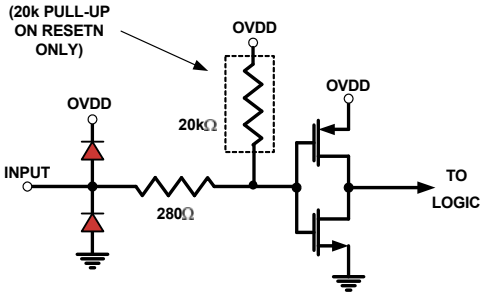


FIGURE 51. DIGITAL INPUTS

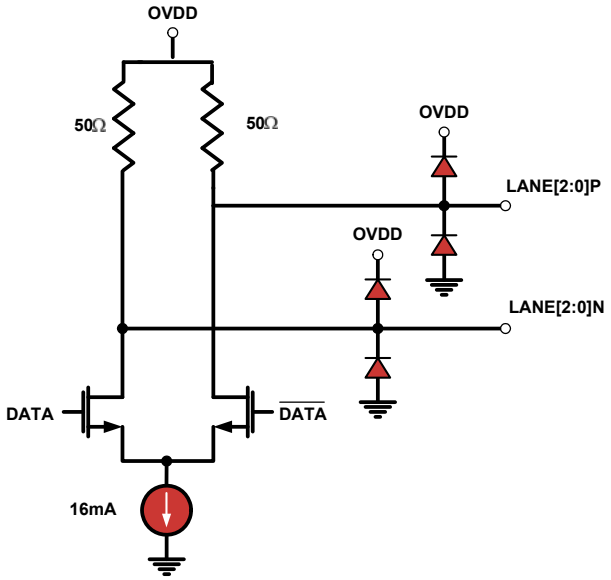


FIGURE 52. CML OUTPUTS

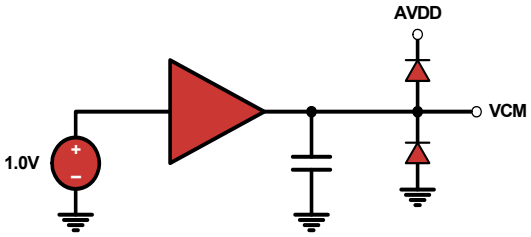


FIGURE 53. VCM_OUT OUTPUT

ADC Evaluation Platform

Intersil offers ADC Evaluation platforms which can be used to evaluate any of Intersil's high speed ADC products. Each platform consists of a FPGA based data capture motherboard and a family of ADC daughtercards. The USB interface and evaluation platform control software allow a user to quickly evaluate the ADC's performance at a user's specific application frequency requirements. More information is available at http://www.intersil.com/converters/adc_eval_platform/

Layout Considerations

Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins, as longer traces between the ceramic bypass capacitors and the device pins will increase inductance, which can result in diminished dynamic performance. Best practices bypassing is especially important on the AVDD and OVDD(PLL) power supply pins. Whenever possible, each supply pin should have its own 0.1uF bypass capacitor. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

CML Outputs

Output traces and connections must be designed for 50Ω (100Ω differential) characteristic impedance. Keep traces direct and short, and minimize bends and vias where possible. Avoid crossing ground and power-plane breaks with signal traces. Keep good clearance (at least 5 trace widths) between the SERDES traces and other signals. Given the speed of these outputs and importance of maintaining an open eye to achieve low BER, signal integrity simulations are recommended, especially when the data lane rate exceeds 3Gbps and/or the trace or cable length between the ADC and the reciever gets larger than 20cm.

Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which will not be operated do not require connection to ensure optimal ADC performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP) accept a floating input as a valid state, and therefore should be biased according to the desired functionality.

Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.

Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD - 1.76)/6.02

Gain Error is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage less than 2 LSB. It is typically expressed in percent.

I2E The Intersil Interleave Engine. This highly configurable circuitry performs estimates of offset, gain, and sample time skew mismatches between the core converters, and updates analog adjustments for each to minimize interleave spurs.

Integral Non-Linearity (INL) is the maximum deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N - 1)$ where N is the resolution in bits.

Missing Codes are output codes that are skipped and will never appear at the ADC output. These codes cannot be reached with any input value.

Most Significant Bit (MSB) is the bit that has the largest value or weight.

Pipeline Delay is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

Power Supply Rejection Ratio (PSRR) is the ratio of the observed magnitude of a spur in the ADC FFT, caused by an AC signal superimposed on the power supply voltage.

Signal to Noise-and-Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

Signal-to-Noise Ratio (without Harmonics) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

SNR and SINAD are either given in units of dB when the power of the fundamental is used as the reference, or dBFS (dB to full scale) when the converter's full-scale input power is used as the reference.

Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the largest spurious spectral component. The largest spurious spectral component may or may not be a harmonic.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
April 15, 2013	FN7973.2	Pages 26, 30: Updated JESD204_config register definitions for E8, E9 Page 30: Added default values for JESD204_config registers
December 21, 2011	FN7973.1	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

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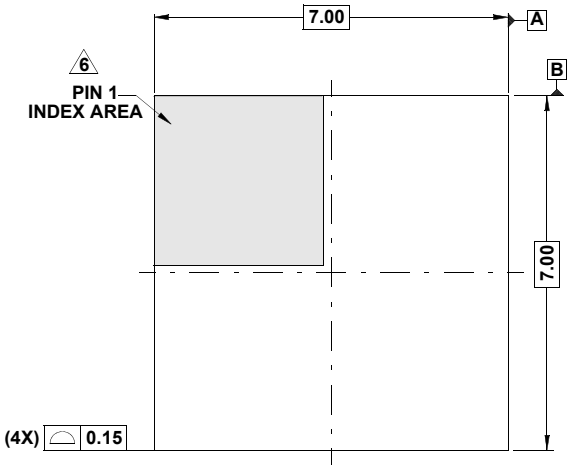
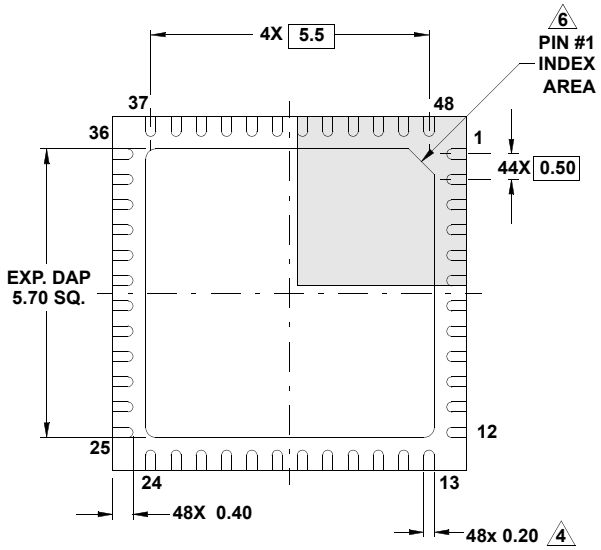
Package Outline Drawing

L48.7x7G

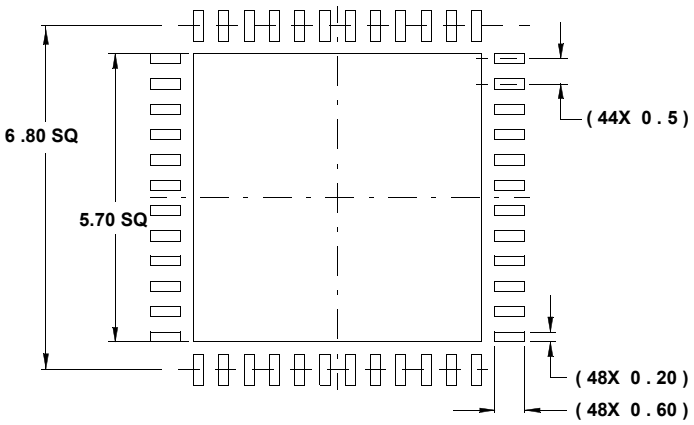
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 1/10



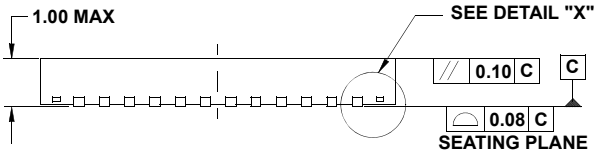
TOP VIEW



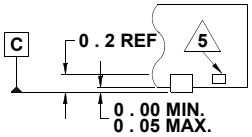
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.