19-3759; Rev 0; 8/05

EVALUATION KIT AVAILABLE

1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

General Description

The MAX1217 dual, monolithic, 12-bit, 125Msps analog-to-digital converter (ADC) provides outstanding dynamic performance up to a 250MHz input frequency. The device operates with conversion rates up to 125Msps while consuming only 650mW per channel.

At 125Msps and an input frequency of 200MHz, the MAX1217 achieves an 80dBc spurious-free dynamic range (SFDR) with excellent 65.3dB signal-to-noise ratio (SNR) at 200MHz. The SNR remains flat (within 3dB) for input tones up to 200MHz. This makes the MAX1217 ideal for wideband applications such as communications receivers, cable head-end receivers, and power-amplifier predistortion in cellular base-station transceivers.

The MAX1217 operates from a single 1.8V power supply. The analog inputs of each channel are designed for AC-coupled, differential or single-ended operation. The ADC also features a selectable on-chip divide-by-2 clock circuit that accepts clock frequencies as high as 250MHz and reduces the phase noise of the input clock source. A low-voltage differential signal (LVDS) sampling clock is recommended for best performance. The converter's digital outputs are LVDS compatible and the data format can be selected to be either two's complement or offset binary.

The MAX1217 is available in a 100-pin TQFP package with exposed paddle and is specified over the extended (-40°C to +85°C) temperature range. Refer to the MAX1218 (170Msps) and the MAX1219 (210Msps) data sheets for higher speed, pin-compatible devices.

Applications

Cable Modem Termination Systems (CMTS)

Cable Digital Return Path Transmitters

Cellular Base-Station Power-Amplifier Linearization

IF and Baseband Digitization

ATE and Instrumentation

Radar Systems

Pin Configuration appears at end of data sheet.

Features

- **125Msps Conversion Rate**
- **Excellent Low-Noise Characteristics**
  SNR = 67dB at f_{IN} = 100MHz
  SNR = 65.3dB at f_{IN} = 200MHz
- **Excellent Dynamic Range**
  SFDR = 85dBc at f_{IN} = 100MHz
  SFDR = 80dBc at f_{IN} = 200MHz
- **Single 1.8V Supply**
- **1.3W Power Dissipation at f_{SAMPLE} = 125Msps and f_{IN} = 10MHz**
- **On-Chip Track-and-Hold Amplifier**
- **Internal 1.24V Bandgap Reference**
- **On-Chip Selectable Divide-by-2 Clock Input**
- **LVDS Digital Outputs with Data Clock Output**
- **EV Kit Available (Order MAX1217EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX1217ECQ	-40°C to +85°C	100 TQFP-EP*	C100E-6

**EP = Exposed paddle.*

Pin-Compatible Versions

PART	RESOLUTION (BITS)	SPEED GRADE (Msps)
MAX1219	12	210
MAX1218	12	170
MAX1217	12	125

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

ABSOLUTE MAXIMUM RATINGS

AV_{CC} to AGND .....-0.3V to +2.1V
OV_{CC} to OGND .....-0.3V to +2.1V
OV_{CC} to AV_{CC} .....-0.3V to +0.3V
OGND to AGND .....-0.3V to +0.3V
CLKP, CLKN, INAP, INAN, INBP, INBN to AGND .....-0.3V to (AV_{CC} + 0.3V)
CLKDIV, $\overline{T}$/BA, $\overline{T}$/BB to AGND .....-0.3V to (AV_{CC} + 0.3V)
REFA, REFADJA, REFB, REFADJB to AGND.....-0.3V to (AV_{CC} + 0.3V)
DCOP, DCON, DA0P–DA11P, DA0N–DA11N, DB0P–DB11P, DB0N–DB11N, ORAP, ORAN, ORBP, ORBN to OGND.....-0.3V to (OV_{CC} + 0.3V)
Current into any Pin.....50mA
ESD Voltage on INAP, INAN, INBP, INBN (Human Body Model).....±750V
ESD Voltage on All Other Pins (Human Body Model).....±2000V
Continuous Power Dissipation (T_A = +70°C)
100-Pin TQFP (derate 37mW/°C above +70°C).....2963mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(AV_{CC} = OV_{CC} = +1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, differential input and differential sine-wave clock signal, 0.1µF capacitors on REFA and REFB, internal reference, digital output differential R_L = 100Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	N		12			Bits
Integral Nonlinearity (Note 2)	INL	f_{IN} = 10MHz	-2	±0.6	+2	LSB
Differential Nonlinearity (Note 2)	DNL	No missing codes	-1	±0.3	+1	LSB
Transfer Curve Offset	V_{OS}	T_A = +25°C (Note 2)	-3		+3	mV
Offset Temperature Drift				10		µV/°C
ANALOG INPUTS (INAP, INAN, INBP, INBN)						
Full-Scale Input Voltage Range	V_{FSR}	T_A = +25°C (Note 2)	1375	1475	1625	mV_{P-P}
Full-Scale Range Temperature Drift				150		ppm/°C
Common-Mode Input Range	V_{CM}			0.8		V
Differential Input Capacitance	C_{IN}			3		pF
Differential Input Resistance	R_{IN}			1.8		kΩ
Full-Power Analog Bandwidth	FPBW			800		MHz
REFERENCE (REFA, REFB, REFADJA, REFADJB)						
Reference Output Voltage	$V_{REF_}$	T_A = +25°C, REFADJ_ = AGND	1.18	1.24	1.30	V
Reference Temperature Drift				65		ppm/°C
REFADJ_ Input High Voltage	$V_{REFADJ_}$	Used to disable the internal reference	AV_{CC} - 0.1			V
SAMPLING CHARACTERISTICS						
Maximum Sampling Rate	f_{SAMPLE}		125			MHz
Minimum Sampling Rate	f_{SAMPLE}			40		MHz

DC ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = +1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, differential input and differential sine-wave clock signal, 0.1µF capacitors on REFA and REFB, internal reference, digital output differential R_L = 100Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Pulse-Width Low	t_{CL}	Figure 5 (Note 3)	2		20	ns
Clock Pulse-Width High	t_{CH}	Figure 5 (Note 3)	2		20	ns
Clock Duty Cycle		Set by clock-management circuit		40 to 60		%
Aperture Delay	t_{AD}	Figures 5, 11		340		ps
Aperture Jitter	t_{AJ}	Figure 11		0.15		ps_{RMS}
CLOCK INPUTS (CLKP, CLKN)						
Differential Clock Input Amplitude		(Note 3)	200	500		mV_{P-P}
Clock Input Common-Mode Voltage	V_{CLKCM}			1.15 ± 0.25		V
Clock Differential Input Resistance	R_{CLK}	T_A = +25°C (Note 3)		10 ±25%		kΩ
Clock Differential Input Capacitance	C_{CLK}			3		pF
DYNAMIC CHARACTERISTICS (at -1dBFS) (Note 4)						
Signal-to-Noise Ratio	SNR	f_{IN} = 10MHz	65.2	67.7		dB
		f_{IN} = 65MHz	65.2	67.5		
		f_{IN} = 100MHz		67		
		f_{IN} = 200MHz		65.3		
Effective Number of Bits	ENOB	f_{IN} = 10MHz	10.5	11		Bits
		f_{IN} = 65MHz	10.5	10.9		
		f_{IN} = 100MHz		10.8		
		f_{IN} = 200MHz		10.6		
Signal-to-Noise Plus Distortion	SINAD	f_{IN} = 10MHz	65	67.6		dB
		f_{IN} = 65MHz	65	67.4		
		f_{IN} = 100MHz		66.8		
		f_{IN} = 200MHz		65.1		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10MHz	72	88		dBc
		f_{IN} = 65MHz	72	86		
		f_{IN} = 100MHz		85		
		f_{IN} = 200MHz		80		
Worst Harmonic (HD2 or HD3)		f_{IN} = 10MHz		-88	-72	dBc
		f_{IN} = 65MHz		-86	-72	
		f_{IN} = 100MHz		-85		
		f_{IN} = 200MHz		-80		
Two-Tone Intermodulation Distortion	TTIMD	f_{IN1} = 29MHz at -7dBFS f_{IN2} = 31MHz at -7dBFS		-92		dBc
		f_{IN1} = 97MHz at -7dBFS f_{IN2} = 100MHz at -7dBFS		-90		

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DC ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = +1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, differential input and differential sine-wave clock signal, 0.1µF capacitors on REFA and REFB, internal reference, digital output differential R_L = 100Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHANNEL CROSSTALK AND CHANNEL MATCHING SPECIFICATIONS						
Channel Isolation		f_{IN} = 200MHz, A_{IN} = -1dBFS		90		dB
LVCMOS LOGIC INPUTS (CLKDIV, $\overline{T}$/BA, $\overline{T}$/BB)						
Input High Voltage	V_{IH}		0.8 x OV_{CC}			V
Input Low Voltage	V_{IL}				0.2 x OV_{CC}	V
Input Capacitance				2		pF
LVDS DIGITAL OUTPUTS (DA0P/N–DA11P/N, DB0P/N–DB11P/N, ORAP/N, ORBP/N, DCOP/N)						
Differential Output Voltage	$\lvert V_{OD} \rvert$		225		490	mV
Output Offset Voltage	V_{OS}		1.125		1.310	V
OUTPUT TIMING CHARACTERISTICS						
CLK to Data Propagation Delay	t_{PDL}	Figure 5 (Note 3)		1.7		ns
CLK to DCO Propagation Delay	t_{CPDL}	Figure 5 (Note 3)		5.2		ns
DCO to Data Propagation Delay	t_{PDL} - t_{CPDL}	(Note 3)	3.7	4.4	5.2	ns
LVDS Output Rise Time	t_{RL}	20% to 80%, C_L = 5pF		350		ps
LVDS Output Fall Time	t_{FL}	20% to 80%, C_L = 5pF		350		ps
Output Data Pipeline Delay	$t_{LATENCY}$	Figure 5		11		Clock Cycles
POWER REQUIREMENTS						
Analog Supply Voltage Range	AV_{CC}		1.71	1.8	1.89	V
Output Supply Voltage Range	OV_{CC}		1.71	1.8	1.89	V
Analog Supply Current	I_{AVCC}	f_{IN} = 10MHz		600	725	mA
Output Supply Current	I_{OVCC}	f_{IN} = 10MHz		120	160	mA
Analog Power Dissipation	P_{DISS}	f_{IN} = 10MHz		1.3	1.6	W
Power-Supply Rejection Ratio	PSRR	(Note 5)		1		mV/V

Note 1: Values at T_A = +25°C to +85°C are guaranteed by production test. Values at T_A < +25°C are guaranteed by design and characterization.

Note 2: Static linearity and offset parameters are computed from a best-fit straight line through the code transition points. The full-scale range (FSR) is defined as 4095 x slope of the line.

Note 3: Parameter guaranteed by design and characterization; T_A = -40°C to +85°C.

Note 4: ENOB and SINAD are computed from a curve fit.

Note 5: PSRR is measured with the analog and output supplies connected to the same potential.

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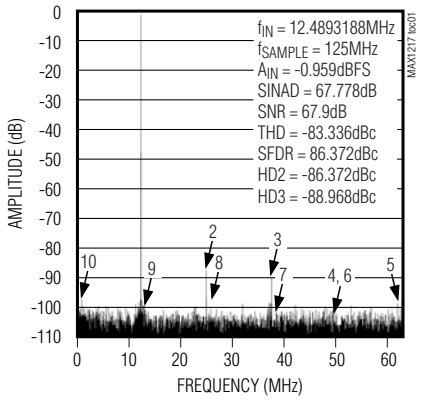
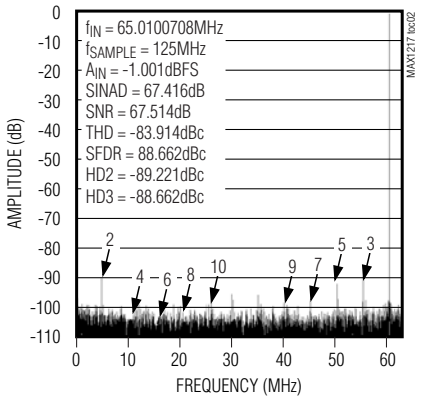
Typical Operating Characteristics

(AV_{CC} = OV_{CC} = +1.8V, f_{SAMPLE} = 125MHz, differential input and differential sine-wave clock, 0.1µF capacitors on REFA and REFB, digital output differential R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

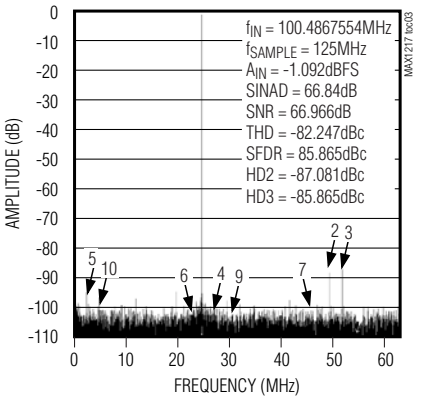
FFT PLOT (16,384 SAMPLES)



FFT PLOT (16,384 SAMPLES)



FFT PLOT (16,384 SAMPLES)



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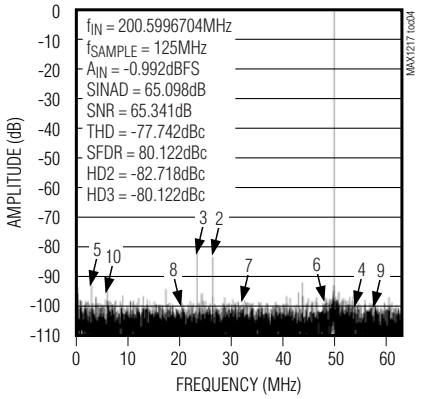

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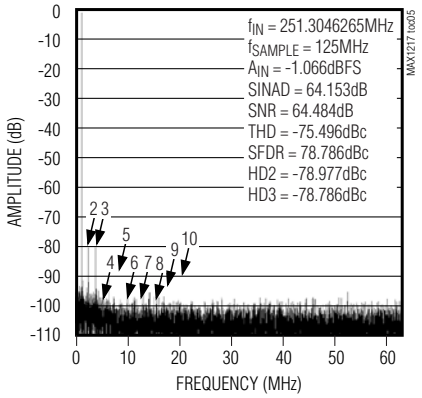
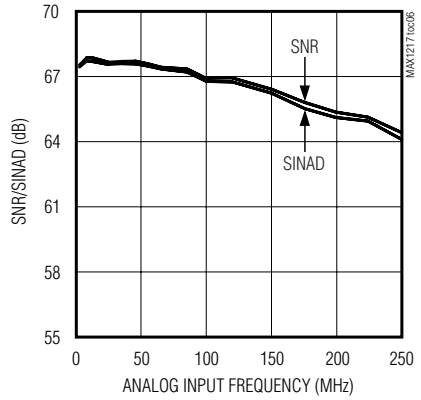
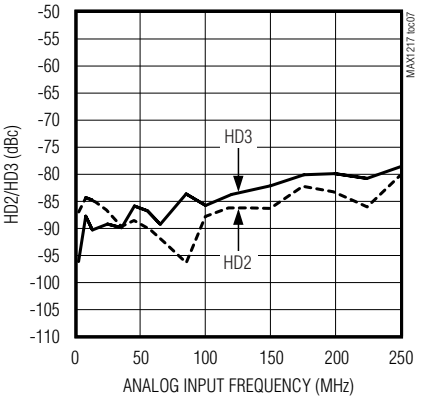


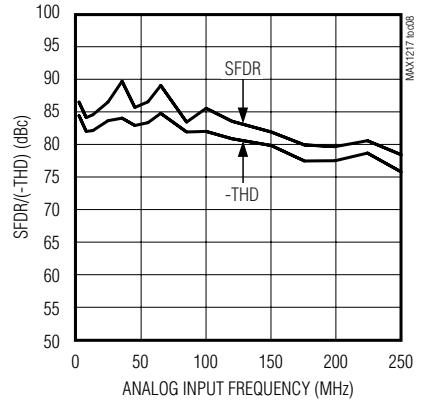
SNR/SINAD vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 125MHz, A_{IN} = -1dBFS)



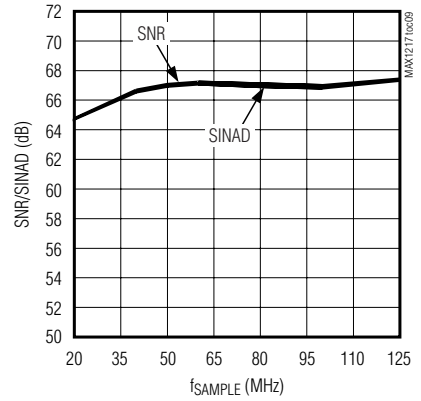
HD2/HD3 vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 125MHz, A_{IN} = -1dBFS)



SFDR/(-THD) vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 125MHz, A_{IN} = -1dBFS)



SNR/SINAD vs. f_{SAMPLE} (f_{IN} = 65.010071MHz, A_{IN} = -1dBFS)

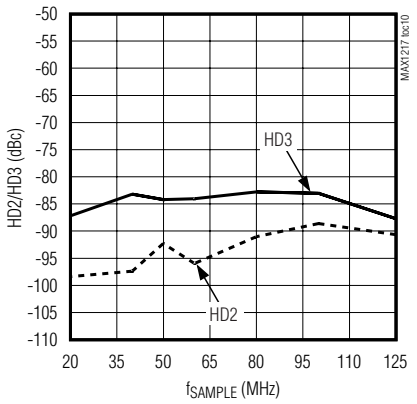


1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

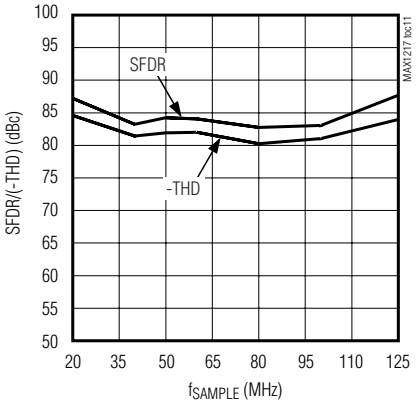
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = +1.8V, f_{SAMPLE} = 125MHz, differential input and differential sine-wave clock, 0.1µF capacitors on REFA and REFB, digital output differential R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

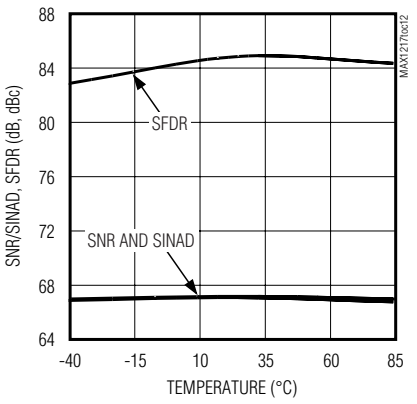
HD2/HD3 vs. f_{SAMPLE} (f_{IN} = 65.010071MHz, A_{IN} = -1dBFS)



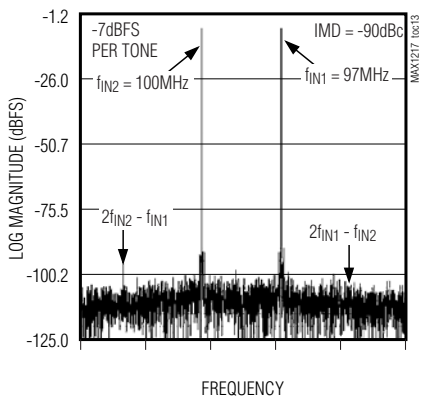
SFDR/(-THD) vs. f_{SAMPLE} (f_{IN} = 65.010071MHz, A_{IN} = -1dBFS)



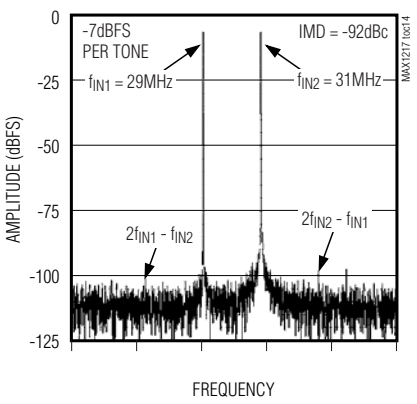
SNR/SINAD, SFDR vs. TEMPERATURE (f_{IN} = 10MHz, A_{IN} = -1dBFS)



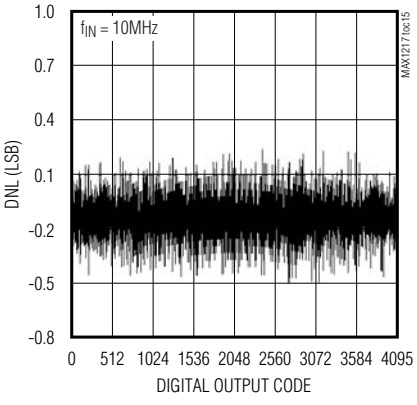
IMD FFT PLOT



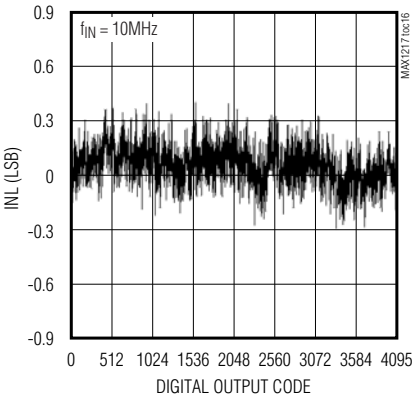
FFT PLOT



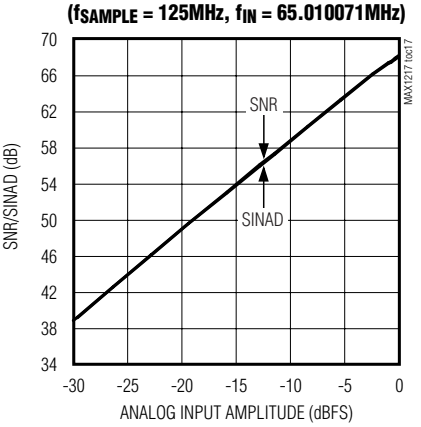
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



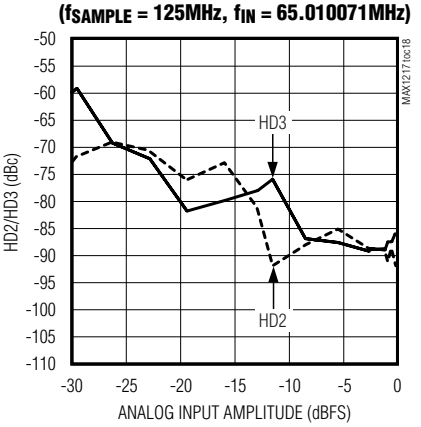
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



SNR/SINAD vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 125MHz, f_{IN} = 65.010071MHz)



HD2/HD3 vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 125MHz, f_{IN} = 65.010071MHz)

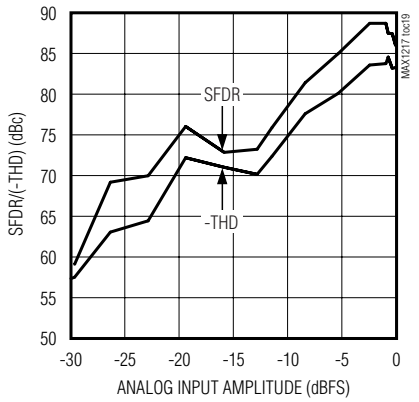


1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

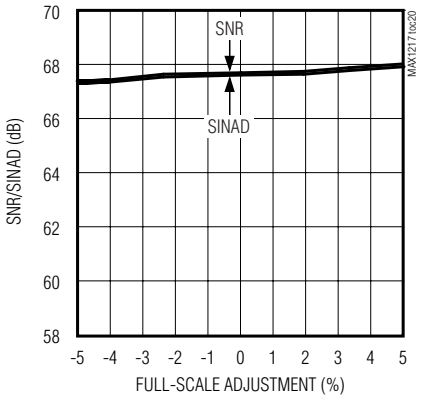
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = +1.8V, f_{SAMPLE} = 125MHz, differential input and differential sine-wave clock, 0.1µF capacitors on REFA and REFB, digital output differential R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

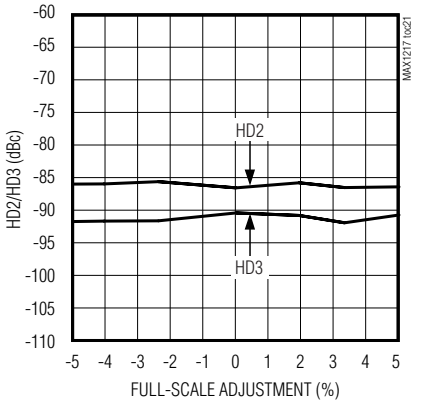
SFDR/(-THD) vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 125MHz, f_{IN} = 65.010071MHz)



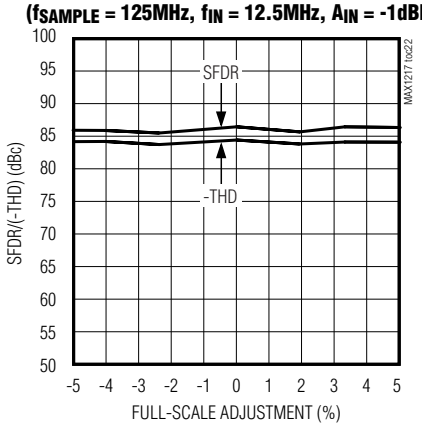
SNR/SINAD vs. % FS ADJUSTMENT (f_{SAMPLE} = 125MHz, f_{IN} = 12.5MHz, A_{IN} = -1dBFS)



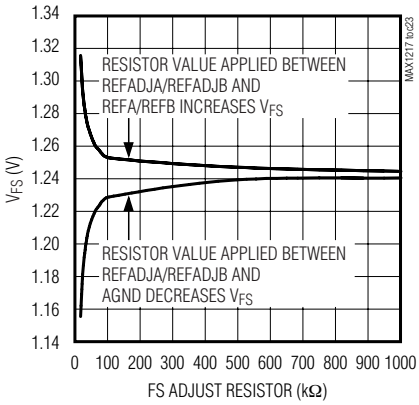
HD2/HD3 vs. % FS ADJUSTMENT (f_{SAMPLE} = 125MHz, f_{IN} = 12.5MHz, A_{IN} = -1dBFS)



SFDR/(-THD) vs. % FS ADJUSTMENT (f_{SAMPLE} = 125MHz, f_{IN} = 12.5MHz, A_{IN} = -1dBFS)



FS VOLTAGE vs. ADJUST RESISTOR



1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

Pin Description

PIN	NAME	FUNCTION
1	REFA	Channel A Reference Input/Output. Channel A 1.24V reference output when REFADJA is driven low. Channel A external reference input when REFADJA is driven high. Connect a 0.1µF capacitor from REFA to AGND with both external and internal references.
2	REFADJA	Channel A Reference Adjust Input. REFADJA allows for full-scale range adjustments by placing a resistor or trim potentiometer between REFADJA and AGND (decreases FS range) or REFADJA and REFA (increases FS range). Connect REFADJA to AV_{CC} to overdrive the internal reference with an external reference. Connect REFADJA to AGND to allow the internal reference to determine the full-scale range of the data converter. See the *FSR Adjustments Using the Internal Bandgap Reference* section.
3, 5, 8, 11, 14, 18, 21, 23, 26, 28, 30, 33, 93, 96, 99, 100	AGND	Analog Converter Ground
4, 9, 10, 15, 16, 17, 22, 27, 29, 31, 94, 95	AV_{CC}	Analog Supply Voltage. Bypass AV_{CC} to AGND with a 0.1µF capacitor for best decoupling results. Use additional board decoupling. See the *Grounding, Bypassing, and Layout Considerations* section.
6	INAP	Positive Analog Input A. Positive analog input to channel A.
7	INAN	Negative Analog Input A. Negative analog input to channel A.
12	CLKP	True Clock Input. Apply an LVDS-compatible input level to CLKP.
13	CLKN	Complementary Clock Input. Apply an LVDS-compatible input level to CLKN.
19	INBN	Negative Analog Input B. Negative analog input to channel B.
20	INBP	Positive Analog Input B. Positive analog input to channel B.
24	REFADJB	Channel B Reference Adjust Input. REFADJB allows for full-scale range adjustments by placing a resistor or trim potentiometer between REFADJB and AGND (decreases FS range) or REFADJB and REFA (increases FS range). Connect REFADJB to AV_{CC} to overdrive the internal reference with an external reference. Connect REFADJB to AGND to allow the internal reference to determine the full-scale range of the data converter. See the *FSR Adjustments Using the Internal Bandgap Reference* section.
25	REFB	Channel B Reference Input/Output. Channel B 1.24V reference output when REFADJB is driven low. Channel B external reference input when REFADJB is driven high. Connect a 0.1µF capacitor from REFB to AGND with both external and internal references.
32	CLKDIV	Clock-Divider Input. CLKDIV controls the sampling frequency relative to the input clock frequency. CLKDIV has an internal pulldown resistor. CLKDIV = 0: Sampling frequency is one-half the input clock frequency. CLKDIV = 1: Sampling frequency is equal to the input clock frequency.
34, 62, 92	OV_{CC}	Output Stage Supply Voltage. Bypass OV_{CC} with a 0.1µF capacitor to AGND. Use additional board decoupling. See the *Grounding, Bypassing, and Layout Considerations* section.
35	ORBP	Channel B True Differential Over-Range Output
36	ORBN	Channel B Complementary Differential Over-Range Output
37	DB11P	Channel B True Differential Digital Output Bit 11 (MSB)
38	DB11N	Channel B Complementary Differential Digital Output Bit 11 (MSB)
39	DB10P	Channel B True Differential Digital Output Bit 10
40	DB10N	Channel B Complementary Differential Digital Output Bit 10
41	DB9P	Channel B True Differential Digital Output Bit 9
42	DB9N	Channel B Complementary Differential Digital Output Bit 9

Pin Description (continued)

PIN	NAME	FUNCTION
43	DB8P	Channel B True Differential Digital Output Bit 8
44	DB8N	Channel B Complementary Differential Digital Output Bit 8
45	DB7P	Channel B True Differential Digital Output Bit 7
46	DB7N	Channel B Complementary Differential Digital Output Bit 7
47	DB6P	Channel B True Differential Digital Output Bit 6
48	DB6N	Channel B Complementary Differential Digital Output Bit 6
49	DB5P	Channel B True Differential Digital Output Bit 5
50	DB5N	Channel B Complementary Differential Digital Output Bit 5
51	DB4P	Channel B True Differential Digital Output Bit 4
52	DB4N	Channel B Complementary Differential Digital Output Bit 4
53	DB3P	Channel B True Differential Digital Output Bit 3
54	DB3N	Channel B Complementary Differential Digital Output Bit 3
55	DB2P	Channel B True Differential Digital Output Bit 2
56	DB2N	Channel B Complementary Differential Digital Output Bit 2
57	DB1P	Channel B True Differential Digital Output Bit 1
58	DB1N	Channel B Complementary Differential Digital Output Bit 1
59	DB0P	Channel B True Differential Digital Output Bit 0 (LSB)
60	DB0N	Channel B Complementary Differential Digital Output Bit 0 (LSB)
61, 63	OGND	Output Stage Ground. Ground connection for output circuitry.
64	DCON	Complementary LVDS Digital Clock Output. Outputs same frequency as ADC sampling frequency.
65	DCOP	True LVDS Digital Clock Output. Outputs same frequency as ADC sampling frequency.
66	DA0N	Channel A Complementary Differential Digital Output Bit 0 (LSB)
67	DA0P	Channel A True Differential Digital Output Bit 0 (LSB)
68	DA1N	Channel A Complementary Differential Digital Output Bit 1
69	DA1P	Channel A True Differential Digital Output Bit 1
70	DA2N	Channel A Complementary Differential Digital Output Bit 2
71	DA2P	Channel A True Differential Digital Output Bit 2
72	DA3N	Channel A Complementary Differential Digital Output Bit 3
73	DA3P	Channel A True Differential Digital Output Bit 3
74	DA4N	Channel A Complementary Differential Digital Output Bit 4
75	DA4P	Channel A True Differential Digital Output Bit 4
76	DA5N	Channel A Complementary Differential Digital Output Bit 5
77	DA5P	Channel A True Differential Digital Output Bit 5
78	DA6N	Channel A Complementary Differential Digital Output Bit 6
79	DA6P	Channel A True Differential Digital Output Bit 6
80	DA7N	Channel A Complementary Differential Digital Output Bit 7
81	DA7P	Channel A True Differential Digital Output Bit 7
82	DA8N	Channel A Complementary Differential Digital Output Bit 8
83	DA8P	Channel A True Differential Digital Output Bit 8
84	DA9N	Channel A Complementary Differential Digital Output Bit 9

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Pin Description (continued)

PIN	NAME	FUNCTION
85	DA9P	Channel A True Differential Digital Output Bit 9
86	DA10N	Channel A Complementary Differential Digital Output Bit 10
87	DA10P	Channel A True Differential Digital Output Bit 10
88	DA11N	Channel A Complementary Differential Digital Output Bit 11 (MSB)
89	DA11P	Channel A True Differential Digital Output Bit 11 (MSB)
90	ORAN	Channel B Complementary Differential Over-Range Output
91	ORAP	Channel B True Differential Over-Range Output
97	$\overline{T}$/BB	Output Format Select Input for Channel B. $\overline{T}$/BB controls the digital output format of channel B of the MAX1217. $\overline{T}$/BB has an internal pulldown resistor. $\overline{T}$/BB = 1: Binary output format. $\overline{T}$/BB = 0: Two's-complement output format.
98	$\overline{T}$/BA	Output Format Select Input for Channel A. $\overline{T}$/BA controls the digital output format of channel A of the MAX1217. $\overline{T}$/BA has an internal pulldown resistor. $\overline{T}$/BA = 1: Binary output format. $\overline{T}$/BA = 0: Two's-complement output format.
—	EP	Exposed Paddle. The exposed paddle is located on the backside of the device and must be connected to AGND.

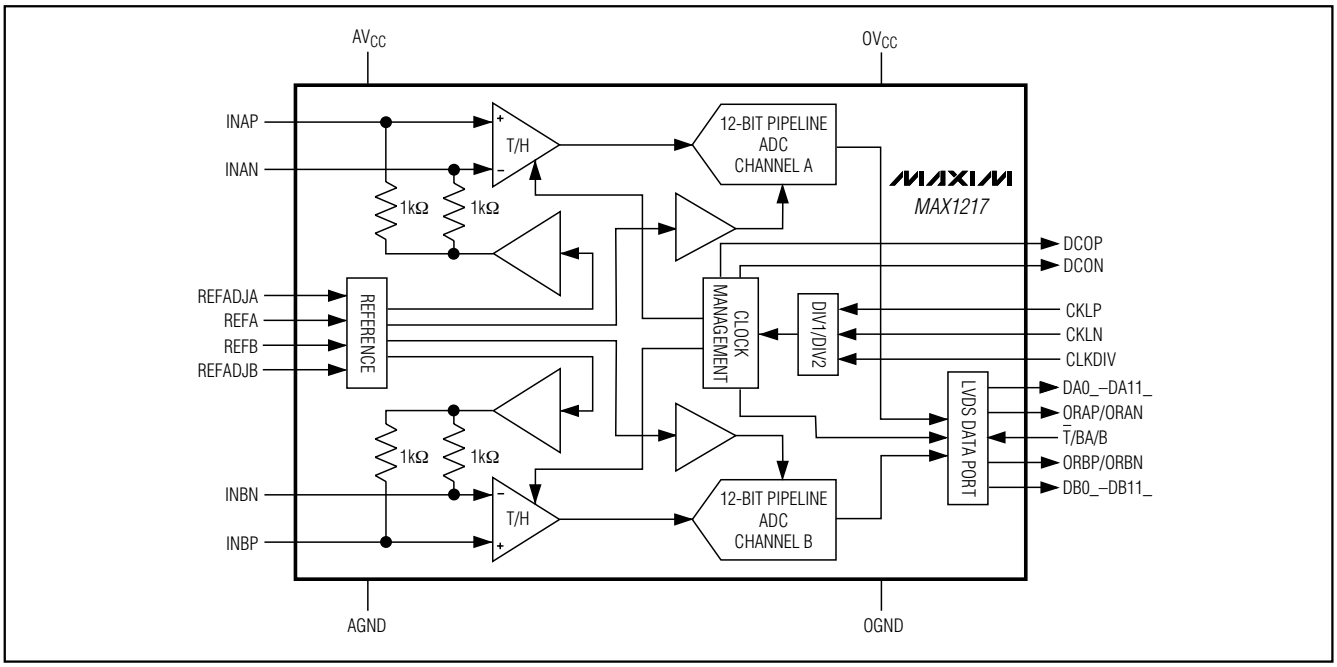

Figure 1. Functional Diagram

Detailed Description

Theory of Operation

The MAX1217 uses a fully differential pipelined architecture that allows for high-speed conversion, optimized accuracy, and linearity while minimizing power consumption.

Both positive inputs (INAP, INBP) and negative/complementary analog inputs (INAN, INBN) are centered around a 0.8V common-mode voltage, and each accept a $\pm V_{FS}$ / 4 differential analog input voltage swing, providing a $1.475V_{P-P}$ typical differential full-scale signal swing. Each set of inputs (INAP, INAN and INBP, INBN) is sampled when the differential sampling clock signal transitions high. When using the clock-divide mode, the analog inputs are sampled at every other high transition of the differential sampling clock.

Each pipeline converter stage converts its input voltage to a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed along to the next pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. The result is a 12-bit parallel digital output word in selectable two's-complement or offset binary output formats with LVDS-compatible output levels (Figure 1).

Analog Inputs

The MAX1217 features two sets of fully differential inputs (INAP, INAN and INBP, INBN) for each input channel. Differential inputs feature good rejection of even-order harmonics, which allows for enhanced AC performance as the signals are progressing through the analog stages. The MAX1217 analog inputs are self-biased at a 0.8V common-mode voltage and allow a $1.475V_{P-P}$ differential input voltage swing (Figure 2). Both sets of inputs are self-biased through 1kΩ resistors, resulting in a typical 2kΩ differential input resistance. Drive the analog inputs of the MAX1217 in AC-coupled configuration to achieve best dynamic performance. See the *Transformer-Coupled, Differential Analog Input Drive* section.

On-Chip Reference Circuit

The MAX1217 features an internal 1.24V bandgap reference circuit (Figure 3), which, in combination with two internal reference-scaling amplifiers, determines the FSR of each channel. Bypass REFA and REFB with a 0.1µF capacitor to AGND. Adjust the voltage of the bandgap reference for each channel independently by adding an external resistor (e.g., 100kΩ trim potentiometer) between REFADJA/REFADJB and AGND or REFADJA/REFADJB and REFA/REFB to compensate for gain errors or increase the FSR of each channel. See the *Applications Information* section for a detailed description of this process.

To disable the internal reference for each channel, connect the reference adjust input (REFADJA, REFADJB) to AV_{CC}. Apply an external, stable reference to the channel's reference input/output (REFA, REFB) to set the converter's full scale. To enable the internal reference for a channel, connect the appropriate reference adjust input (REFADJA, REFADJB) to AGND.

Clock Inputs (CLKP, CLKN)

Drive the clock inputs of the MAX1217 with an LVDS-compatible clock to achieve the best dynamic performance. The clock signal source must be a high-quality, low phase noise to avoid any degradation in the noise performance of the ADC. The clock inputs (CLKP, CLKN) are internally biased to 1.15V to accept a typical $0.5V_{P-P}$ differential signal swing (Figure 4). See the *Differential, AC-Coupled LVPECL-Compatible Clock Input* section for more circuit details on how to drive CLKP and CLKN appropriately. Although not recommended, the clock inputs also accept a single-ended input signal.

The MAX1217 also features an internal clock-management circuit (duty-cycle equalizer) to ensure that the clock signal applied to inputs CLKP and CLKN is processed to provide a 50% duty-cycle clock signal that desensitizes the performance of the converter to variations in the duty cycle of the input clock source. The clock duty-cycle equalizer cannot be turned off externally and requires a minimum 40MHz clock frequency to allow the device to meet data sheet specifications.

If the MAX1217 is not clocked, the digital outputs begin to change state randomly, resulting in a supply current increase of up to 40mA.

Clock Outputs (DCON, DCOP)

The MAX1217 features a differential clock output, which can be used to latch the digital output data with an external latch or receiver. Additionally, the clock output can be used to synchronize external devices (e.g., FPGAs) to the ADC. DCOP and DCON are differential outputs with LVDS-compatible voltage levels. There is a 5.2ns (typ) delay between the rising (falling) edge of CLKP (CLKN) and the rising (falling) edge of DCOP (DCON). See Figure 5 for timing details.

Divide-by-2 Clock Control

The MAX1217 offers a clock control line (CLKDIV) that supports the reduction of clock jitter in a system. Connect CLKDIV to OGND to enable the ADC's internal

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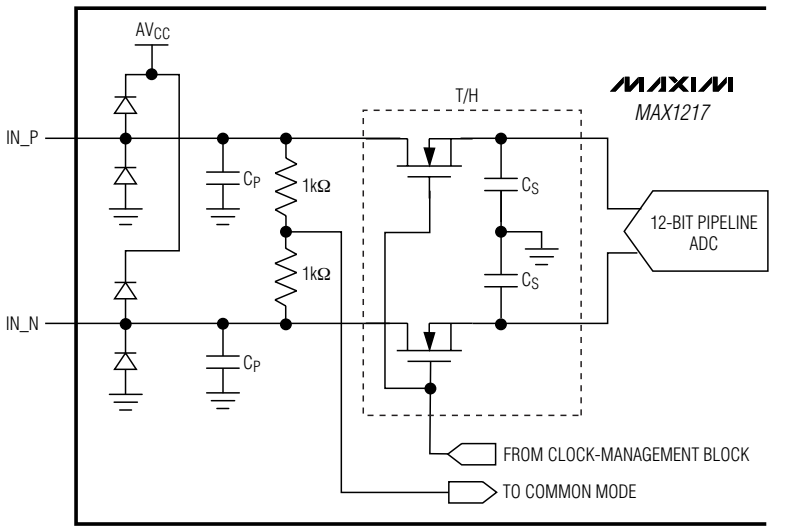

C_S IS THE SAMPLING CAPACITANCE
C_P IS THE PARASITIC CAPACITANCE ~ 1pF

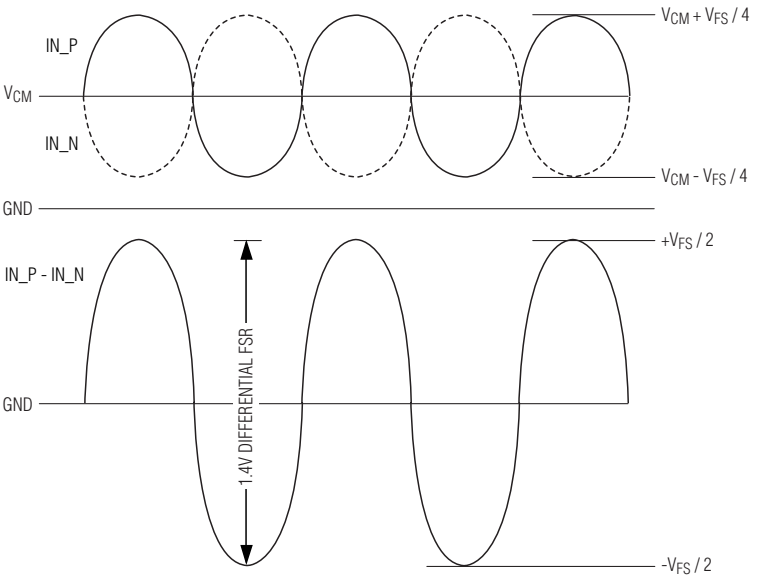

Figure 2. Simplified Analog Input Architecture and Allowable Input Voltage Range

divide-by-2 clock divider. Data is now updated at one-half the ADC's input clock rate. CLKDIV has an internal pulldown resistor and can be left open for applications that require this divide-by-2 mode. Connecting CLKDIV to OV_{CC} disables the divide-by-2 mode.

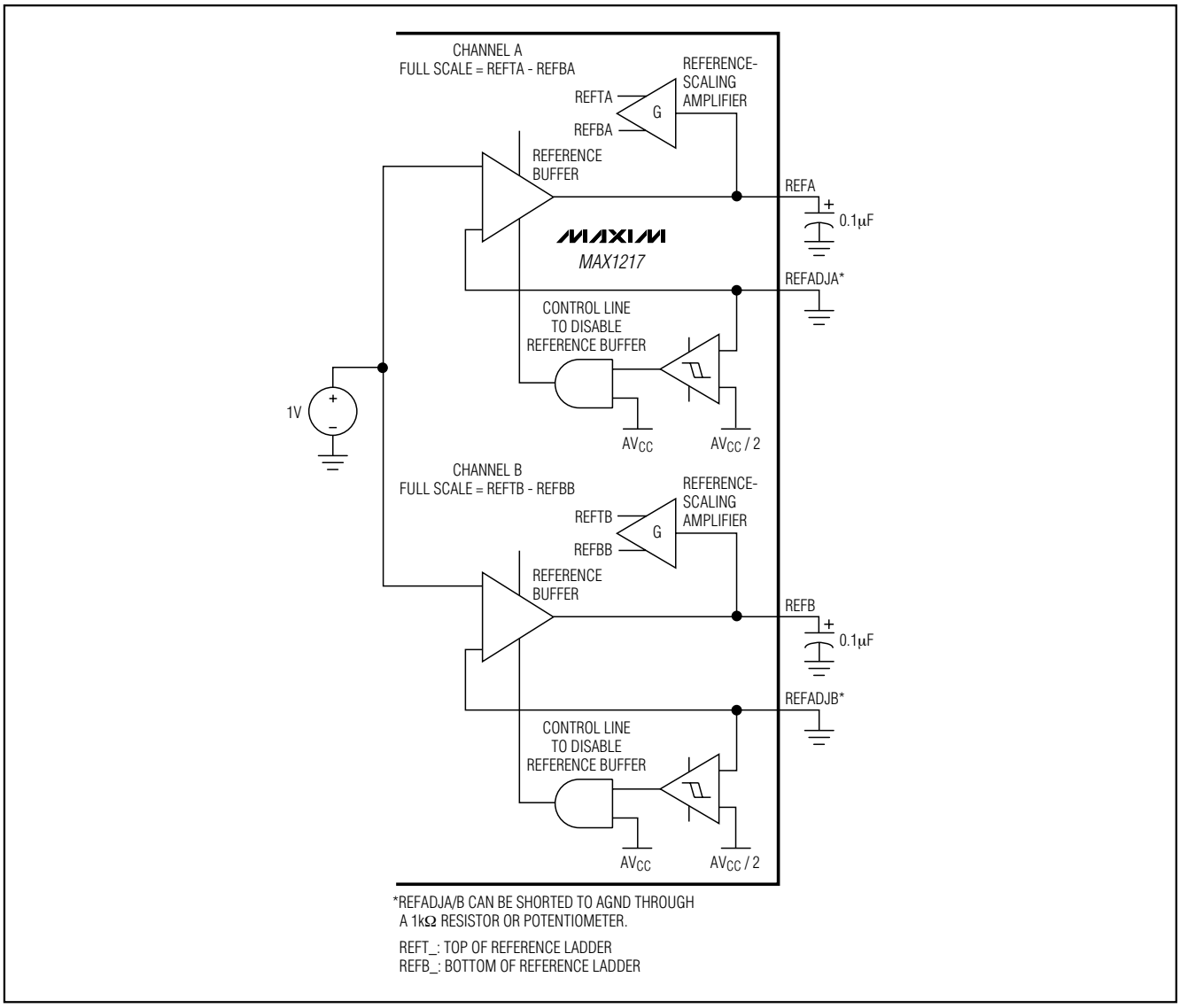

Figure 3. Simplified Reference Architecture

System Timing Requirements

Figure 5 depicts the relationship between the clock input and output, analog input, sampling event, and data output. The MAX1217 samples on the rising (falling) edge of CLKP (CLKN). Output data is valid on the next rising (falling) edge of DCOP (DCON), with an internal latency of 11 clock cycles.

Digital Outputs (DA0P/N–DA11P/N, DB0P/N–DB11P/N, ORAP/N, ORBP/N, DCOP/N) and Control Inputs $\overline{T}$/BA, $\overline{T}$/BB

Digital outputs DA0P/N–DA11P/N, DB0P/N–DB11P/N, ORAP/N, ORBP/N, and DCOP/N are LVDS compatible, and data on DA0P/N–DA11P/N and DB0P/N–DB11P/N are presented in either binary or two's-complement format (Table 1). The $\overline{T}$/BA, $\overline{T}$/BB control lines are LVCMOS-compatible inputs that allow a selectable output format for each channel. Pulling $\overline{T}$/BA, $\overline{T}$/BB low outputs data in two's complement and pulling it high presents data in offset binary format on each of the channels' 12-bit parallel buses. $\overline{T}$/BA, $\overline{T}$/BB have an internal pulldown resistor and can be left unconnected in applications using

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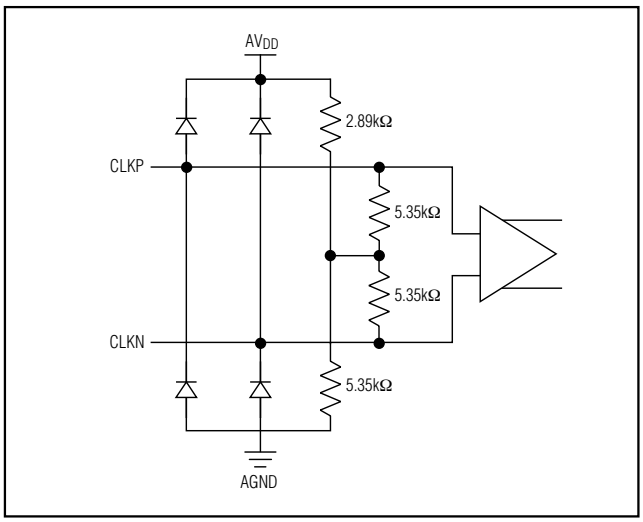

Figure 4. Simplified Clock Input Architecture

only two's-complement output format. All LVDS outputs provide a typical 0.371V voltage swing around roughly a 1.2V common-mode voltage, and must be terminated at the far end of each transmission line pair (true and complementary) with 100Ω. Apply a 1.71V to 1.89V voltage supply at OV_{CC} to power the LVDS outputs.

The MAX1217 offers an additional set of differential output pairs (ORAP/N and ORBP/N) to flag out-of-range conditions for each channel, where out-of-range is above positive or below negative full scale. An out-of-range condition on each channel is identified with ORAP or ORBP (ORAN or ORBN) transitioning high (low).

Note: Although a differential LVDS output architecture reduces single-ended transients to the supply and ground planes, capacitive loading on the digital outputs should still be kept as low as possible. Using LVDS buffers on the digital outputs of the ADC when driving larger loads improves overall performance and reduces system-timing constraints.

Applications Information

FSR Adjustments Using the Internal Bandgap Reference

The MAX1217 supports a 10% (±5%) full-scale adjustment range on each channel. Add an external resistor ranging from 13kΩ to 1MΩ between the reference adjust input of the channel (REFADJA, REFADJB) and AGND to decrease the full-scale range of the channel. Adding a variable resistor, potentiometer, or predetermined resistor value between the reference adjust input of a channel (REFADJA, REFADJB) and its respective reference input/output (REFA, REFB) increases the FSR of the channel. Figure 6a shows the two possible configurations and their impact on the overall full-scale range adjustment of the MAX1217. The FSR for each channel can be set to any value in the allowed range independent of the FSR of the other channel. Do not use resistor values of less than 13kΩ to avoid instability of the internal gain regulation loop for the bandgap reference. See Figure 6b for the resulting FSR for a series of resistor values.

Differential, AC-Coupled, LVPECL-Compatible Clock Input

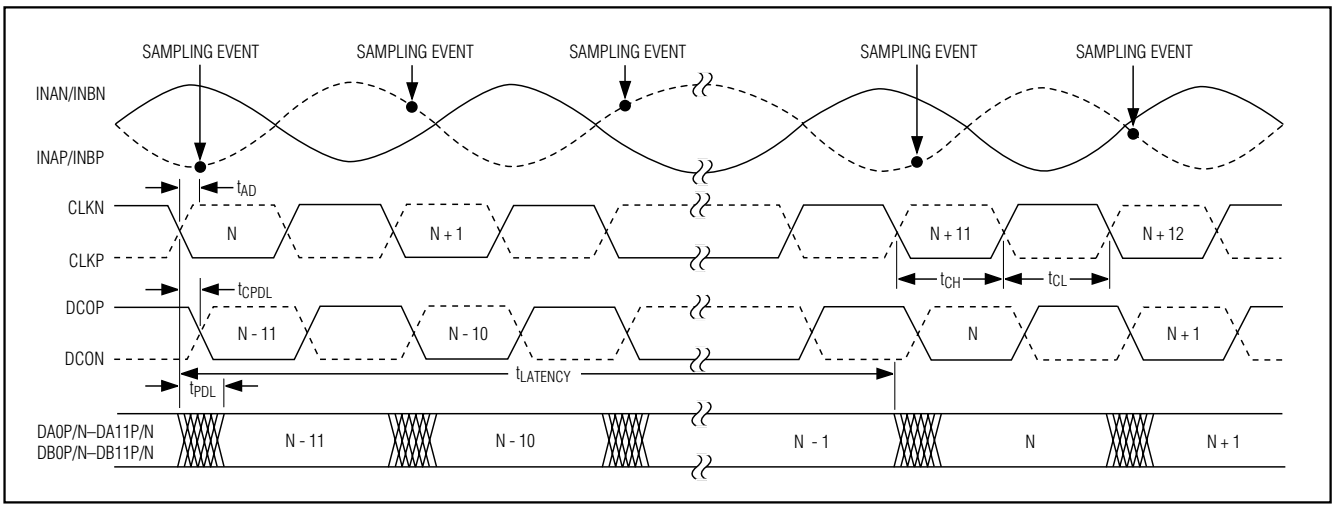

Figure 5. System and Output Timing Diagram

Table 1. MAX1217 Digital Output Coding

INAP/INBP ANALOG INPUT VOLTAGE LEVEL	INAN/INBN ANALOG INPUT VOLTAGE LEVEL	OUT-OF-RANGE ORAP/ORBP (ORAN/ORBN)	BINARY DIGITAL OUTPUT CODE (DA11P/N–DA0P/N; DB11P/N–DB0P/N)	TWO'S-COMPLEMENT DIGITAL OUTPUT CODE (DA11P/N–DA0P/N; DB11P/N–DB0P/N)
> V_{CM} + V_{FS} /4	< V_{CM} - V_{FS} /4	1 (0)	1111 1111 1111 (exceeds +FS, OR set)	0111 1111 1111 (exceeds +FS, OR set)
V_{CM} + V_{FS} /4	V_{CM} - V_{FS} /4	0 (1)	1111 1111 1111 (+FS)	0111 1111 1111 (+FS)
V_{CM}	V_{CM}	0 (1)	1000 0000 0000 or 0111 1111 1111 (FS / 2)	0000 0000 0000 or 1111 1111 1111 (FS / 2)
V_{CM} - V_{FS} /4	V_{CM} + V_{FS} /4	0 (1)	0000 0000 0000 (-FS)	1000 0000 0000 (-FS)
< V_{CM} + V_{FS} /4	> V_{CM} - V_{FS} /4	1 (0)	0000 0000 0000 (exceeds -FS, OR set)	1000 0000 0000 (exceeds -FS, OR set)

The MAX1217 dynamic performance depends on the use of a very clean clock source. The phase noise floor of the clock source has a negative impact on the SNR performance. Spurious signals on the clock signal source also affect the ADC's dynamic range. The preferred method of clocking the MAX1217 is differentially with LVDS- or LVPECL-compatible input levels. The fast data transition rates of these logic families minimize the clock input circuitry's transition uncertainty, thus improving the SNR performance. To accomplish this, AC-couple a 50Ω reverse-terminated clock signal source with low phase noise into a fast differential receiver, such as the MAX9388 (Figure 7). The receiver produces the necessary LVPECL output levels to drive the clock inputs of the data converter.

Transformer-Coupled, Differential Analog Input Drive

The MAX1217 provides the best SFDR and THD performance with fully differential input signals. In differential input mode, even-order harmonics are lower since the inputs to each channel (INAP/N and INBP/N) are balanced, and each of the channel's inputs only requires half the signal swing compared to a single-ended configuration.

Wideband RF transformers provide an excellent solution to convert a single-ended signal to a fully differential signal. Apply a secondary-side termination to a 1:1 transformer (e.g., Mini-Circuit's ADT1-1WT) by two separate 24.9Ω resistors. Higher source impedance values can be used at the expense of a degradation in dynamic performance. Use resistors with tight tolerance (0.5%) to minimize effects of imbalance, maximizing the ADC's dynamic range. This configuration optimizes THD and SFDR performance of the ADC by reducing the effects of transformer parasitics. However, the source impedance combined with the shunt capacitance provided by a PC board and the ADC's parasitic capacitance limit the ADC's full-power input bandwidth.

To further enhance THD and SFDR performance at high input frequencies (> 100MHz) place a second transformer (Figure 8) in series with the single-ended-to-differential conversion transformer. The second transformer reduces the increase of even-order harmonics at high frequencies.

Single-Ended, AC-Coupled Analog Inputs

Although not recommended, the MAX1217 can be used in single-ended mode (Figure 9). AC-couple the analog signals to the positive input of each channel (INAP, INBP) through a 0.1µF capacitor terminated with a 49.9Ω resistor to AGND. Terminate the negative input of each channel (INAN, INBN) with a 24.9Ω resistor in series with a 0.1µF capacitor to AGND. In single-ended mode the input range is limited to approximately half of the FSR of the device, and dynamic performance usually degrades.

Grounding, Bypassing, and Board Layout

The MAX1217 requires board layout design techniques suitable for high-speed data converters. This ADC accepts separate analog and output power supplies. The analog and output power-supply inputs accept 1.71V to 1.89V input voltage ranges. Although both AV_{CC} and OV_{CC} can be supplied from one source, use separate sources to reduce performance degradation caused

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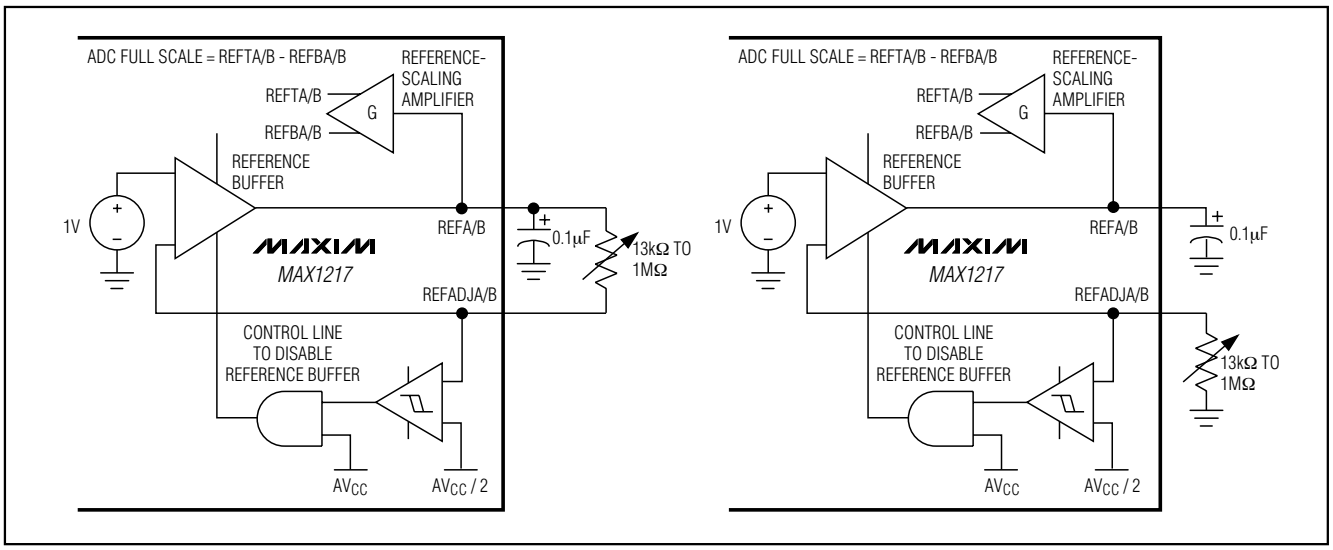

Figure 6a. Circuit Suggestions to Adjust the ADC's Full-Scale Range

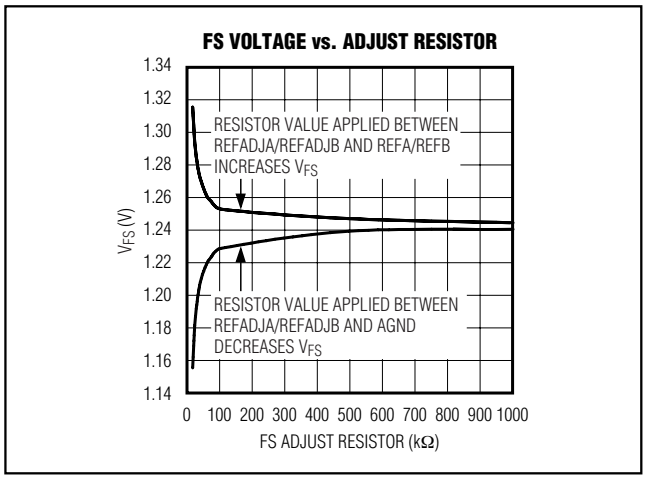

Figure 6b. FS Adjustment Range vs. FS Adjustment Resistor

by output switching currents, which can couple into the analog supply network. Isolate analog and output supplies (AV_{CC} and OV_{CC}) where they enter the PC board with separate networks of ferrite beads and capacitors to their corresponding grounds (AGND, OGND).

To achieve optimum performance, provide each supply with a separate network of 47µF tantalum capacitor and parallel combination of 10µF and 1µF ceramic capacitors. Additionally, the ADC requires each supply input to be bypassed with a separate 0.1µF ceramic capacitor (Figure 10). Locate these capacitors directly at the ADC supply inputs or as close as possible to the MAX1217. Choose surface-mount capacitors, whose preferred location is on the same side as the converter to save space and minimize inductance. If close placement on the same side is not possible, route these bypassing capacitors through vias to the bottom side of the PC board.

Multilayer boards with separate ground and power planes produce the highest level of signal integrity. Use a split ground plane arranged to match the physical location of the analog and output grounds on the ADC's package. Join the two ground planes at a single point so the noisy output ground currents do not interfere with the analog ground plane. Dynamic currents traveling long distances before reaching ground cause large and undesirable ground loops. Ground loops can degrade the input noise by coupling back to the analog front-end of the converter, resulting in increased spurious activity, leading to decreased noise performance.

All AGND connections could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, output systems ground. To minimize the coupling of the output signals from the analog input, segregate the output bus carefully from the analog input circuitry. To further minimize the effects of output noise coupling, position ground return vias throughout the layout to divert output switching currents away from the sensitive analog sections of the ADC. This approach does not require split ground planes, but can be accom-

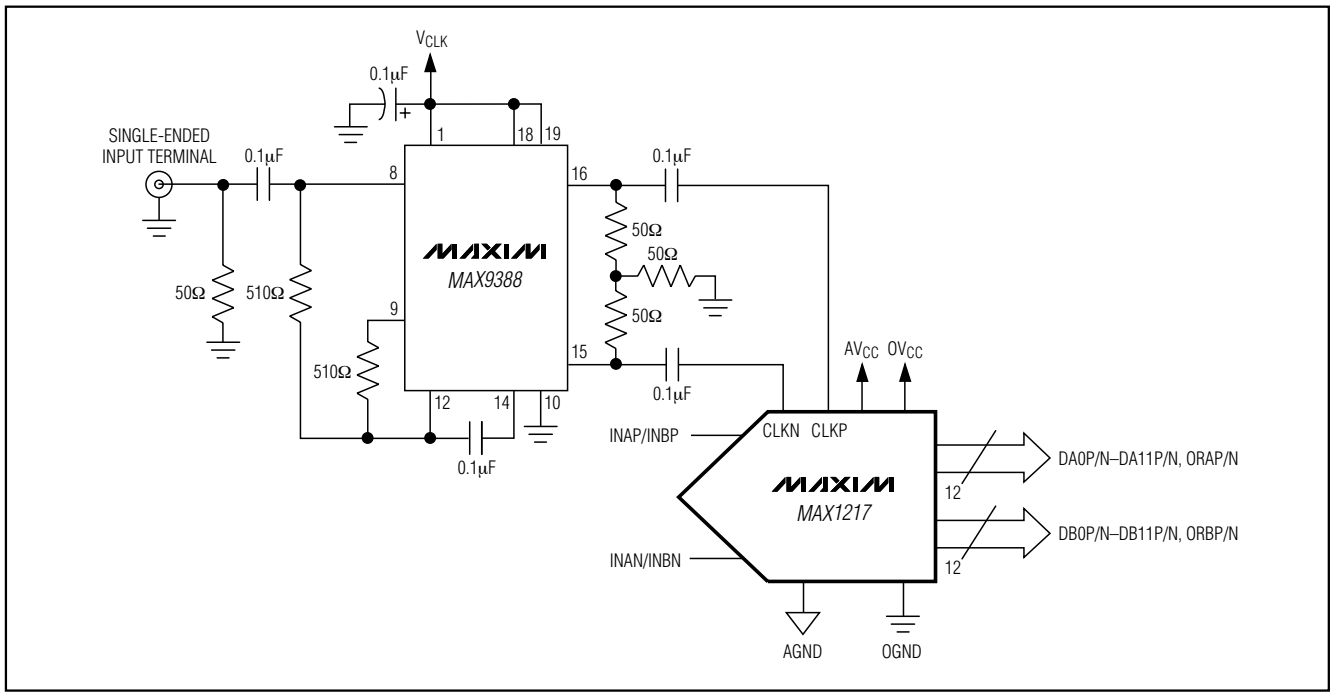

Figure 7. Differential, AC-Coupled, LVPECL-Compatible Clock Input Configuration

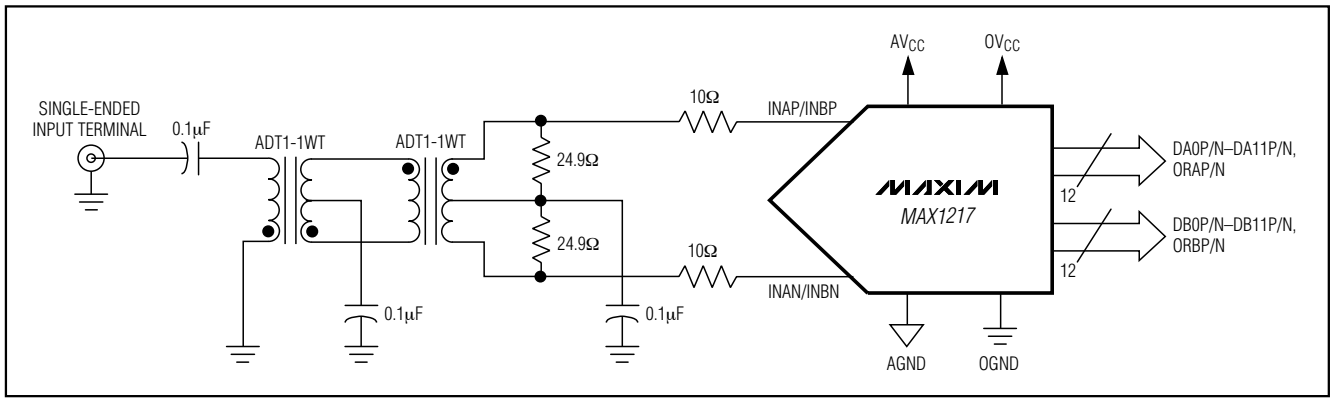

Figure 8. Analog Input Configuration with Back-to-Back Transformers and Secondary-Side Termination

plished by placing substantial ground connections between the analog front-end and the digital outputs.

The MAX1217 is packaged in a 100-pin TQFP-EP package (**package code: C100E-6**), providing greater design flexibility, increased thermal dissipation, and optimized AC performance of the ADC. The exposed paddle (EP) must be soldered to AGND.

The data converter die is attached to an EP lead frame with the back of this frame exposed to the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the board with standard infrared (IR) flow soldering techniques.

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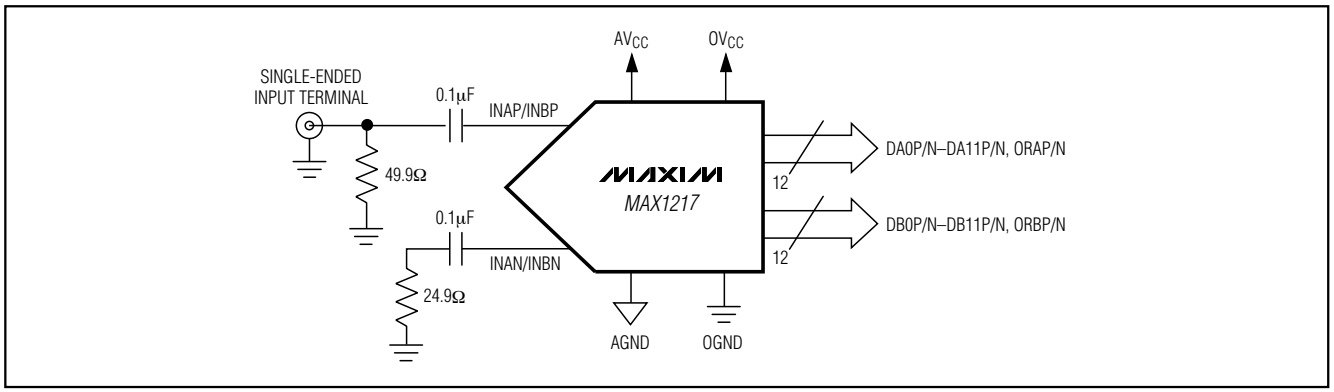


Figure 9. Single-Ended AC-Coupled Analog Input Configuration

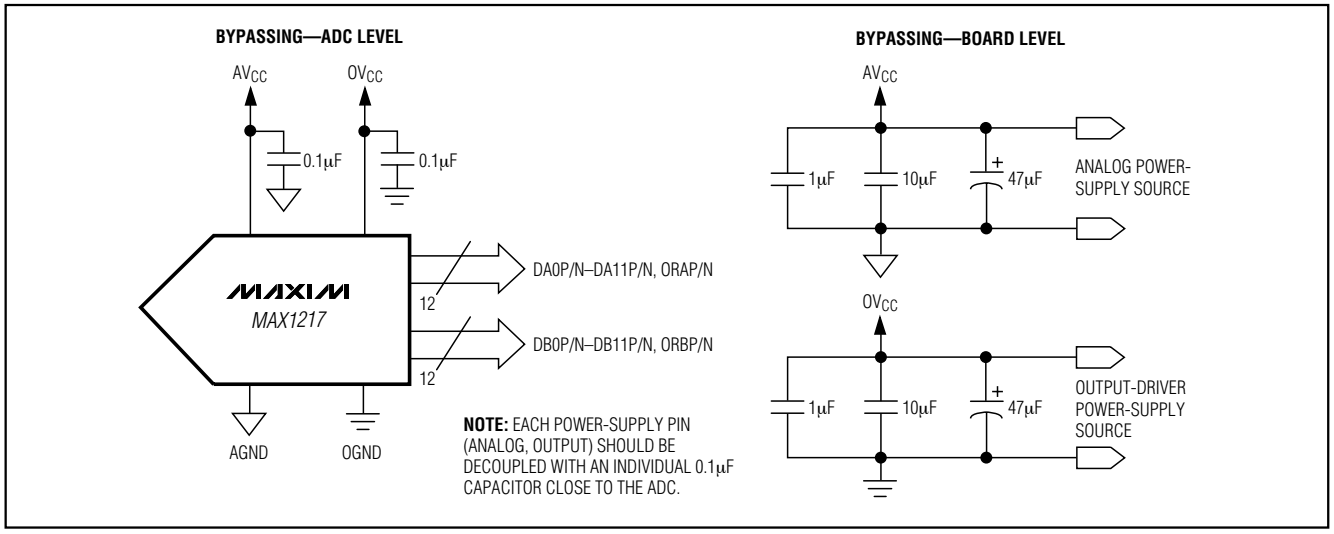


Figure 10. Grounding, Bypassing, and Decoupling Recommendations for the MAX1217

Thermal efficiency is one of the factors for selecting a package with an exposed paddle for the MAX1217. The exposed paddle improves thermal efficiency and ensures a solid ground connection between the ADC and the PC board's analog ground layer.

Route the digital output traces for a high-speed, high-resolution data converter with care. Keep trace lengths at a minimum and place minimal capacitive loading, less than 5pF, on any digital trace to prevent coupling to sensitive analog sections of the ADC. Run the LVDS output traces as differential lines with 100Ω characteristic impedance from the ADC to the LVDS load device.

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. However, the static linearity parameters for the MAX1217 are measured using the histogram method with a 10MHz input frequency.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL

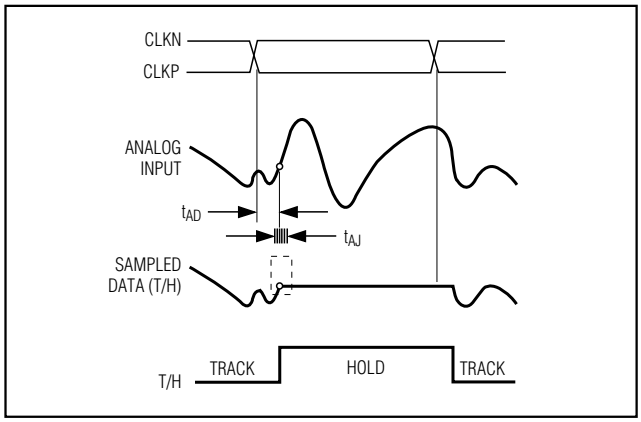


Figure 11. Aperture Jitter/Delay Specifications

error specification that is -1 LSB or better, guarantees no missing codes and a monotonic transfer function. The MAX1217's DNL specification is measured with the histogram method based on a 10MHz input tone.

Dynamic Parameter Definitions

Aperture Jitter

Figure 11 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 11).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB}[max] = 6.02dB \times N + 1.76dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components excluding the fundamental and the DC offset. In the case of the MAX1217, SINAD is computed from a curve fit.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest noise or harmonic distortion component, excluding DC offset. SFDR is usually measured in dBc with respect to the fundamental (carrier) frequency amplitude or in dBFS with respect to the ADC's full-scale range.

Intermodulation Distortion (IMD)

IMD is the ratio of the RMS sum of the intermodulation products to the RMS sum of the two fundamental input tones. This is expressed as:

$$IMD = 20 \times \log\left(\frac{\sqrt{V^2_{IM1} + V^2_{IM2} + \ldots + V^2_{IMn}}}{\sqrt{V_1^2 + V_2^2}}\right)$$

The fundamental input tone amplitudes (V_1 and V_2) are at -7dBFS. The intermodulation products are the amplitudes of the output spectrum at the following frequencies:

- 2nd-order intermodulation products (IM2): $f_{IN1} + f_{IN2}$, $f_{IN2} - f_{IN1}$
- 3rd-order intermodulation products (IM3): $2f_{IN1} - f_{IN2}$, $2f_{IN2} - f_{IN1}$, $2f_{IN1} + f_{IN2}$, $2f_{IN2} + f_{IN1}$
- 4th-order intermodulation products (IM4): $3f_{IN1} - f_{IN2}$, $3f_{IN2} - f_{IN1}$, $3f_{IN1} + f_{IN2}$, $3f_{IN2} + f_{IN1}$
- 5th-order intermodulation products (IM5): $3f_{IN1} - 2f_{IN2}$, $3f_{IN2} - 2f_{IN1}$, $3f_{IN1} + 2f_{IN2}$, $3f_{IN2} + 2f_{IN1}$

Full-Power Bandwidth

A large -1dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. The -3dB point is defined as the full-power input bandwidth frequency of the ADC.

Offset Error

Ideally, the midscale MAX1217 transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured transition point and the ideal transition point.

Gain Error

Ideally, the positive full-scale MAX1217 transition occurs at 1.5 LSB below positive full scale, and the negative full-scale transition occurs at 0.5 LSB above negative full scale. The gain error is the difference of the measured transition points minus the difference of the ideal transition points.

1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02}\right)$$

Total Harmonic Distortion (THD)

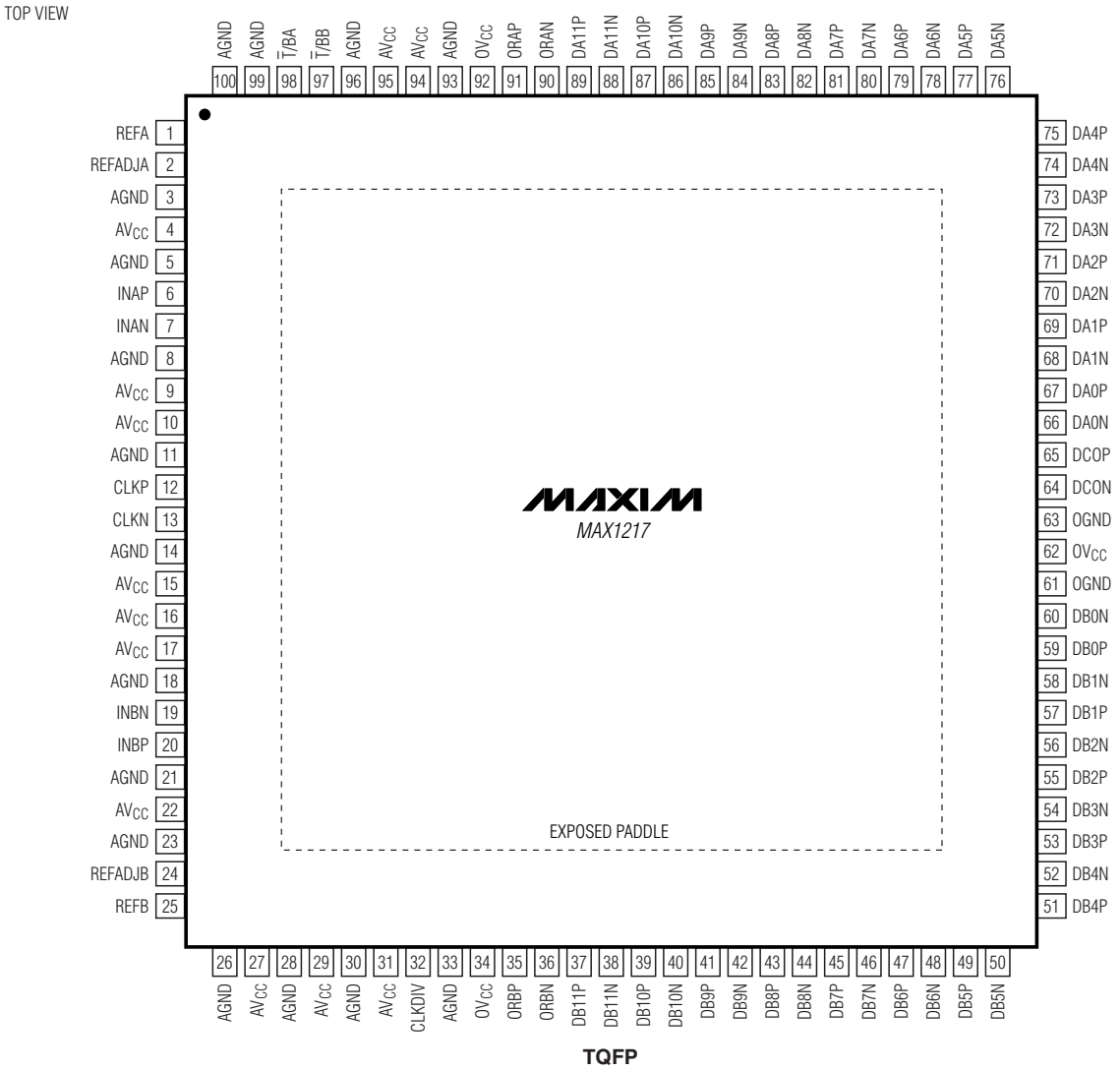
THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2)}}{V_1}\right]$$

where V_1 is the fundamental amplitude, and V_2 through V_7 are the amplitudes of the 2nd- through 7th-order harmonics (HD2–HD7).

1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

Pin Configuration



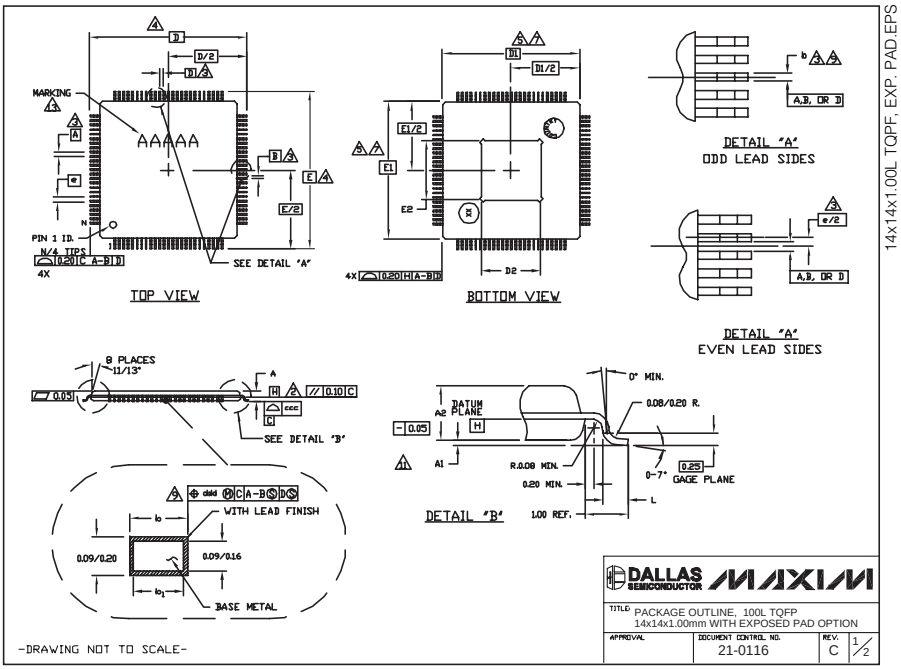
TQFP

1.8V, Dual, 12-Bit, 125Msps ADC for Broadband Applications

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

14x14x1.00L TQPF, EXP. PAD.EPS



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. DATUM PLANE [H] LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUM [A–B] AND [D] TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXITS PLASTIC BODY AT DATUM PLANE H .
4. TO BE DETERMINED AT SEATING PLANE [C] .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254mm ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [H] .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
9. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. THIS OUTLINE CONFROMS TO JEDEC MS-026.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
12. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05mm.
13. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	ALL DIMENSIONS ARE IN MILLIMETERS			
	MIN.	NOM.	MAX.	NOTES
A	—	—	1.20	
A1	0.05	—	0.15	11
A2	0.95	1.00	1.05	
D		16.00 BSC.		4
D1		14.00 BSC.		7,8
E		16.00 BSC.		4
E1		14.00 BSC.		7,8
L	0.45	0.60	0.75	
N		100		
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	—	—	0.08	
ddd	—	—	0.08	

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG. CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C100E-2	7.7	8.0	8.3	7.7	8.0	8.3
C100E-3	6.2	6.5	6.8	6.2	6.5	6.8
C100E-6	4.7	5.0	5.3	4.7	5.0	5.3

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 100L TQFP
14x14x1.00mm WITH EXPOSED PAD OPTION
APPROVAL
DOCUMENT CONTROL NO. 21-0116
REV. C
2/2

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