ADC1005S060

Single 10 bits ADC, up to 60 MHz

Rev. 03 — 2 July 2012 Product data sheet

1. General description

The ADC1005S060 is a 10-bit high-speed low-power Analog-to-Digital Converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary or gray coded digital words at a maximum sampling rate of 60 MHz. All digital inputs and outputs are Transistor-Transistor Logic (TTL) and CMOS compatible, although a low-level sine wave clock input signal is allowed.

The device requires an external source to drive its reference ladder.

2. Features

- 10-bit resolution (binary or gray code)
- Sampling rate up to 60 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 5 MHz full-scale input at f_{clk} = 60 MHz)
- No missing codes guaranteed
- In-Range (IR) CMOS output
- TTL and CMOS levels compatible digital inputs
- 2.7 V to 3.6 V CMOS digital outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 312 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required

3. Applications

- Video data digitizing
- Radar
- Barcode scanners
- Digital instrumentation
- Transient signal analysis
- ΣΔ modulators
- Medical imaging

4. Quick reference data

Table 1. Quick reference data

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3.3 V; V_{RB} = 1.3 V; V_{RT} = 3.7 V; C_L = 10 pF and T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		2.7	3.3	3.6	V
I_{CCA}	analog supply current		-	29	37	mA
I_{CCD}	digital supply current		-	33	40	mA
I_{CCO}	output supply current	f_{clk} = 60 MHz; ramp input	-	0.5	2.0	mA
INL	integral non-linearity		-	±0.8	±2.0	LSB
DNL	differential non-linearity		-	±0.35	±0.9	LSB
$f_{clk(max)}$	maximum clock frequency		60	-	-	MHz
P_{tot}	total power dissipation	f_{clk} =60 MHz; ramp input	-	312	411	mW

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
ADC1005S060TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

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6. Block diagram

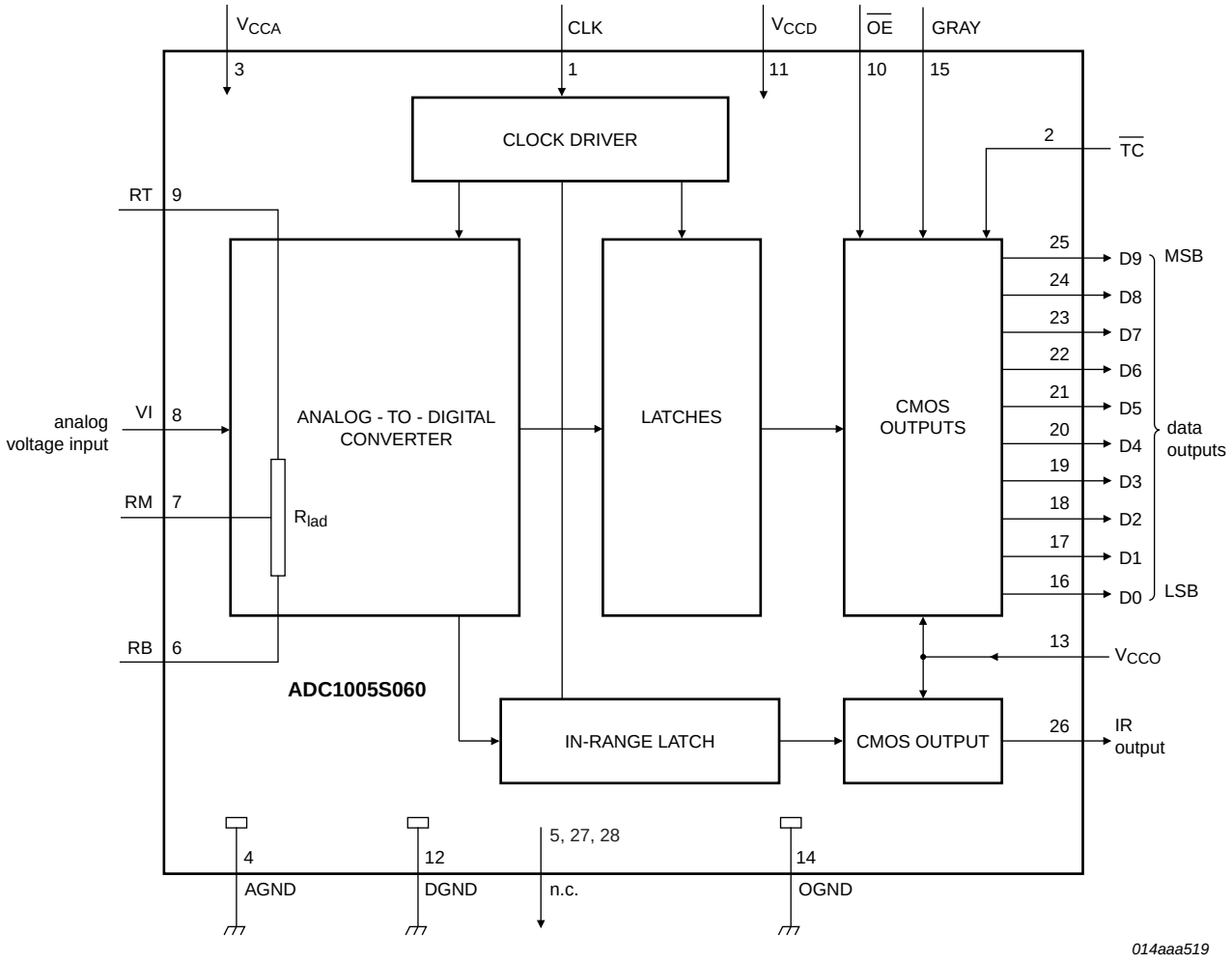

Fig 1. Block diagram

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7. Pinning information

7.1 Pinning

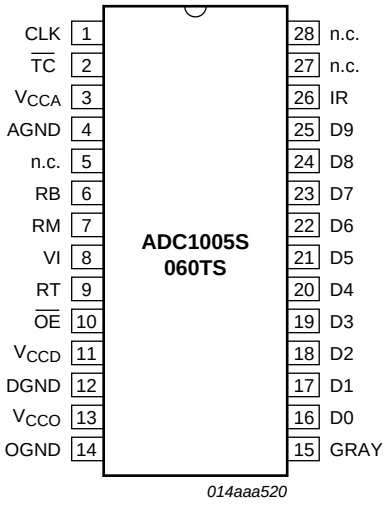

Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CLK	1	clock input
$\overline{TC}$	2	twos complement input (active LOW)
V_{CCA}	3	analog supply voltage (5 V)
AGND	4	analog ground
n.c.	5	not connected
RB	6	reference voltage BOTTOM input
RM	7	reference voltage MIDDLE input
VI	8	analog voltage input
RT	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (active LOW)
V_{CCD}	11	digital supply voltage (2.7 V to 3.6 V)
DGND	12	digital ground
V_{CCO}	13	supply voltage for output stages (2.7 V to 3.6 V)
OGND	14	output ground
GRAY	15	gray code input (active HIGH)
D0	16	data output; bit 0 (Least Significant Bit (LSB))
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3

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Table 3. Pin description *...continued*

Symbol	Pin	Description
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (Most Significant Bit (MSB))
IR	26	in-range data output
n.c.	27	not connected
n.c.	28	not connected

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	−0.3	+7.0	V
V_{CCD}	digital supply voltage		[1]	−0.3	+7.0	V
V_{CCO}	output supply voltage		[1]	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$		−0.1	+1.0	V
		$V_{CCD} - V_{CCO}$; $V_{CCA} - V_{CCO}$		−0.1	+4.0	V
V_I	input voltage	referenced to AGND		−0.3	+7.0	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage	for switching; referenced to DGND		-	V_{CCD}	V
I_O	output current			-	10	mA
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
T_j	junction temperature			-	150	°C

[1] The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between −0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	110	K/W

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10. Characteristics

Table 6. Characteristics

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3.3 V; V_{RB} = 1.3 V; V_{RT} = 3.7 V; C_L = 10 pF and T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		2.7	3.3	3.6	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$	−0.2	-	+0.2	V
		$V_{CCA} - V_{CCO}$; $V_{CCD} - V_{CCO}$	−0.2		+2.55	V
I_{CCA}	analog supply current		-	29	37	mA
I_{CCD}	digital supply current		-	33	40	mA
I_{CCO}	output supply current	f_{clk} = 60 MHz; ramp input	-	0.5	2.0	mA
P_{tot}	total power dissipation	f_{clk} = 60 MHz; ramp input	-	312	411	mW
Inputs						
Clock input CLK (Referenced to DGND)[1]						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{clk} = 0.8 V	−1	0	+1	µA
I_{IH}	HIGH-level input current	V_{clk} = 2 V	-	2	10	µA
C_i	input capacitance		-	2	-	pF
Inputs $\overline{OE}$ $\overline{TC}$ and GRAY (Referenced to DGND); see Table 3 and 4						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	−1	-	-	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	-	-	1	µA
Analog input VI (Referenced to AGND)						
I_{IL}	LOW-level input current	$V_I = V_{RB}$ = 1.3 V	-	0	-	µA

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Table 6. Characteristics *...continued*

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3.3 V; V_{RB} = 1.3 V; V_{RT} = 3.7 V; C_L = 10 pF and T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{RT}$ = 3.7 V		-	55	-	μA
Y_i	input admittance	f_i = 5 MHz	[2]				
		R_i, input resistance		-	45	-	kΩ
		C_i, input capacitance		3	5	7	pF
Reference voltages for the resistor ladder; see Table 7							
V_{RB}	voltage on pin RB			1.2	1.3	2.2	V
V_{RT}	voltage on pin RT			3.4	3.7	V_{CCA} − 0.8	V
$V_{ref(dif)}$	differential reference voltage	$V_{RT} - V_{RB}$		2.2	2.4	3.2	V
I_{ref}	reference current	$V_{ref(dif)}$ = 2.4 V		-	17.6	-	mA
R_{lad}	ladder resistance			-	136	-	Ω
TC_{Rlad}	ladder resistor temperature coefficient			-	253	-	mΩ/K
V_{offset}	offset voltage	$V_{ref(dif)}$ = 2.4 V					
		BOTTOM	[3]	-	200	-	mV
		TOP	[3]	-	190	-	mV
$V_{i(a)(p-p)}$	peak-to-peak analog input voltage	$V_{ref(dif)}$ = 2.4 V	[4]	1.95	2.01	2.10	V
Outputs							
Digital outputs D9 to D0 and IR (Referenced to OGND)							
V_{OL}	LOW-level output voltage	I_O = 1 mA		0	-	0.5	V
V_{OH}	HIGH-level output voltage	I_O = −1 mA		V_{CCO} − 0.5	-	V_{CCO}	V
I_{OZ}	OFF-state output current	0.5 V < V_O < V_{CCO}		−20	-	+20	μA
Switching characteristics; Clock input CLK; see Figure 4[1]							
$f_{clk(max)}$	maximum clock frequency			60	-	-	MHz
$t_{w(clk)H}$	HIGH clock pulse width	T_{amb} = 25 °C		7.0	-	-	ns
$t_{w(clk)L}$	LOW clock pulse width	T_{amb} = 25 °C		3.5	-	-	ns
Analog signal processing; f_{clk} = 60 MHz							
Linearity							
INL	integral non-linearity	ramp input		-	±0.8	±2.0	LSB
DNL	differential non-linearity	ramp input		-	±0.35	±0.9	LSB

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Table 6. Characteristics *...continued*

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3.3 V; V_{RB} = 1.3 V; V_{RT} = 3.7 V; C_L = 10 pF and T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_{offset}	offset error	middle code		-	±1	-	LSB
E_G	gain error	from device to device	[5]	-	±0.5	-	%
Bandwidth							
B	bandwidth	full-scale sine wave	[6]	-	30	-	MHz
		75 % full-scale sine wave		-	45	-	MHz
		small signal at mid-scale; V_I = ±10 LSB at code 512		-	700	-	MHz
$t_{s(LH)}$	LOW to HIGH settling time	full-scale square wave; see Figure 6	[7]	-	5	-	ns
$t_{s(HL)}$	HIGH to LOW settling time	full-scale square wave; see Figure 6	[7]	-	5	-	ns
Harmonics							
α_{2H}	second harmonic level	f_i = 5 MHz		-	−68	-	dB
α_{3H}	third harmonic level	f_i = 5 MHz		-	−67	-	dB
THD	total harmonic distortion	f_i = 5 MHz		-	−64	-	dB
		f_i = 15 MHz		-	−57	-	dB
SFDR	spurious free dynamic range	f_i = 5 MHz		-	72		dB
Signal-to-Noise ratio[8]							
S/N	signal-to-noise ratio	without harmonics; f_i = 5 MHz		-	58	-	dB
		without harmonics; f_i = 15 MHz		53	57	-	dB
Effective bits[8]							
ENOB	effective number of bits	f_i = 5 MHz		-	9.3	-	bits
		f_i = 10 MHz		-	8.9	-	bits
		f_i = 15 MHz		-	8.8	-	bits
		f_i = 20 MHz		-	8.6	-	bits
Two-tone intermodulation[9]							
α_{IM}	intermodulation suppression	f_{clk} = 60 MHz		-	−67	-	dB
Bit error rate							
BER	bit error rate	f_i = 5 MHz; V_I = ±16 LSB at code 512		-	10^{-13}	-	times/samples
Timing (f_{clk} = 60 MHz; C_L = 10 pF); see Figure 4[10]							
$t_{d(s)}$	sampling delay time			-	0.7	2	ns
$t_{h(o)}$	output hold time			4	-	-	ns
$t_{d(o)}$	output delay time	V_{CCO} = 2.7 V		-	10	14	ns
		V_{CCO} = 3.3 V		-	9	13	ns

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Table 6. Characteristics *…continued*

V_{CCA} = 4.75 V to 5.25 V; V_{CCD} = 4.75 V to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 °C to 70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V; V_{CCO} = 3.3 V; V_{RB} = 1.3 V; V_{RT} = 3.7 V; C_L = 10 pF and T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_L	load capacitance		-	-	10	pF
SR	slew rate	V_{CCO} = 2.7 V	0.2	0.3	-	V/ns
3-state output delay times (f_{clk} = 60 MHz; V_{CCO} = 3.3 V); see Figure 5						
t_{dZH}	float to active HIGH delay time		-	16	20	ns
t_{dZL}	float to active LOW delay time		-	30	34	ns
t_{dHZ}	active HIGH to float delay time		-	25	30	ns
t_{dLZ}	active LOW to float delay time		-	23	27	ns

[1] The rise and fall times of the clock signal must not be less than 0.5 ns.

[2] The input admittance is $Y_i + \frac{1}{R_i} + j\omega C_i$

[3] Analog input voltages producing code 0 up to and including code 1023:

a) V_{offset} BOTTOM is the difference between the analog input which produces data equal to 00 and the reference voltage on pin RB (V_{RB}) at T_{amb} = 25 °C.

b) V_{offset} TOP is the difference between the reference voltage on pin RT (V_{RT}) and the analog input which produces data outputs equal to code 1023 at T_{amb} = 25 °C.

[4] To ensure the optimum linearity performance of such a converter architecture the lower and upper extremities of the converter reference resistor ladder are connected to pins RB and RT via offset resistors R_{OB} and R_{OT} as shown in Figure 3.

a) The current flowing into the resistor ladder is $I = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to 1023 is $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} + V_{RB}) = 0.8375 \times (V_{RT} - V_{RB})$

b) Since R_L, R_{OB} and R_{OT} have similar behavior with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from device to device. Consequently, variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is optimized.

[5] $E_G = \frac{(V_{1023} - V_0) - V_{i(p-p)}}{V_{i(p-p)}} \times 100$

[6] The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSB, neither any significant attenuation are observed in the reconstructed signal.

[7] The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data.

[8] Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half the clock frequency (Nyquist frequency). Conversion to signal-to-noise ratio: S/N = ENOB × 6.02 + 1.76 dB.

[9] Intermodulation measured relative to either tone with analog input frequencies of 4.3 MHz and 4.5 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter.

[10] Output data acquisition: the output data is available after the maximum delay time of $t_{d(o)}$. IDT recommends the lowest possible output load. These parameters are guaranteed by characterization and not by production test.

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11. Additional information relating to Table 6

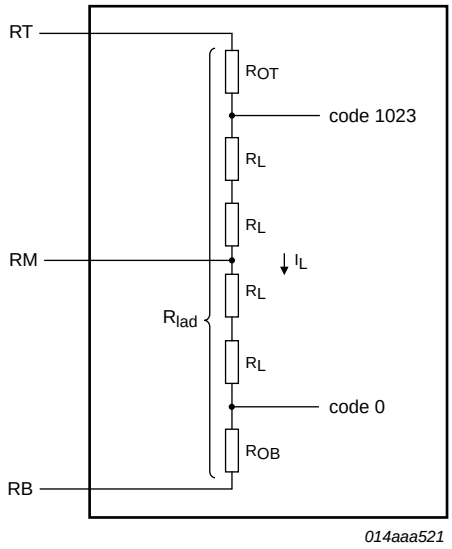

Fig 3. Converter reference resistor ladder

Table 7. Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.3 V, V_{RT} = 3.7 V; binary/gray codes)

Code	$V_{i(a)(p-p)}$ (V)	IR	Binary outputs D9 to D0	Gray outputs D9 to D0
Underflow	< 1.5	0	00 0000 0000	00 0000 0000
0	1.5	1	00 0000 0000	00 0000 0000
1	-	1	00 0000 0001	00 0000 0001
↓	-	↓	↓	↓
1022	-	1	11 1111 1110	10 0000 0001
1023	3.51	1	11 1111 1111	10 0000 0000
Overflow	> 3.51	0	11 1111 1111	10 0000 0000

Table 8. Output coding and input voltage (typical values; referenced to AGND; binary/twos complement codes)

Code	$V_{i(a)(p-p)}$ (V)	IR	Binary outputs D9 to D0	twos complement outputs D9 to D0
Underflow	< 1.5	0	00 0000 0000	10 0000 0000
0	1.5	1	00 0000 0000	10 0000 0000
1	-	1	00 0000 0001	10 0000 0001
↓	-	↓	↓	↓
1022	-	1	11 1111 1110	01 1111 1110
1023	3.51	1	11 1111 1111	01 1111 1111
Overflow	> 3.51	0	11 1111 1111	01 1111 1111

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Table 9. $\overline{TC}$ mode selection

$\overline{TC}$	$\overline{OE}$	D9 to D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Table 10. Gray mode selection

Gray	$\overline{OE}$	D9 to D0	IR
X	1	high impedance	high impedance
0	0	active; binary	active
1	0	active; gray	active

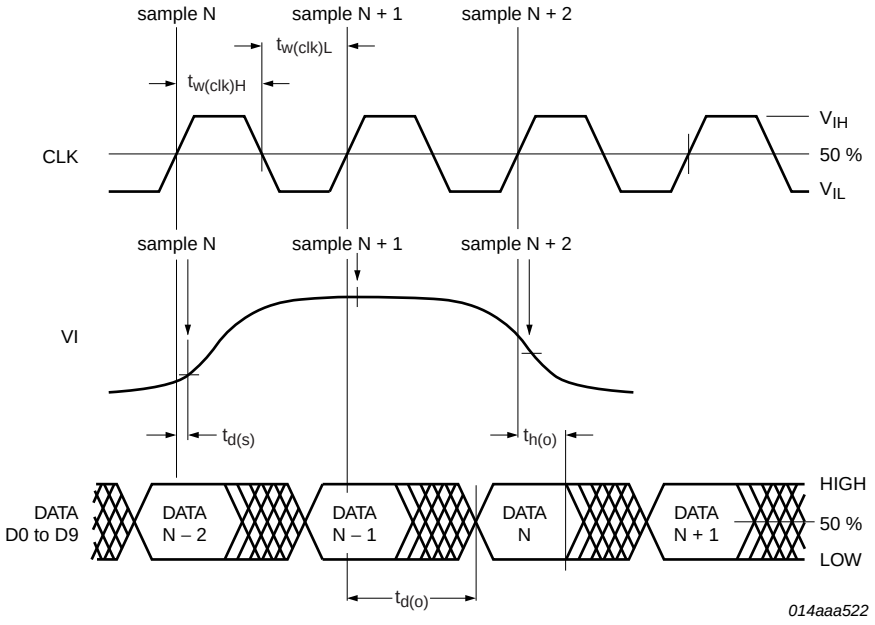

Fig 4. Timing diagram

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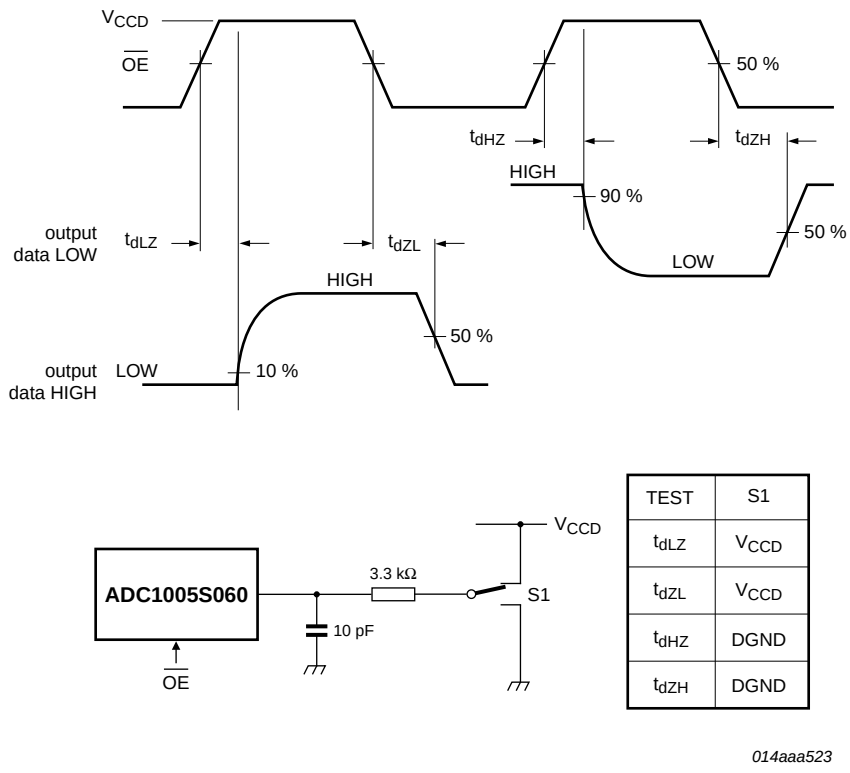

frequency on pin $\overline{OE}$ = 100 kHz.

Fig 5. Timing diagram and test conditions of 3-state output delay time

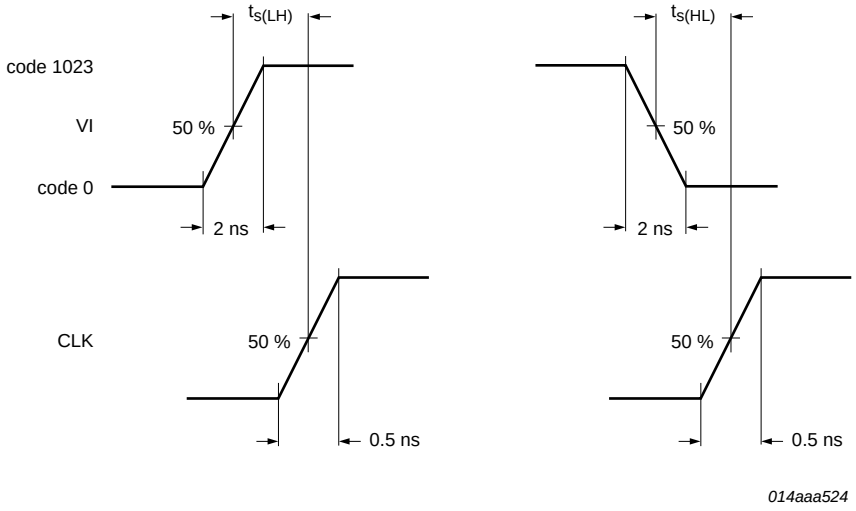

Fig 6. Analog input settling time diagram

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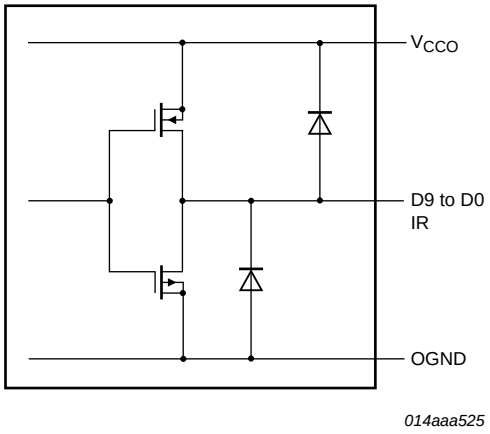

Fig 7. D9 to D0 and IR outputs

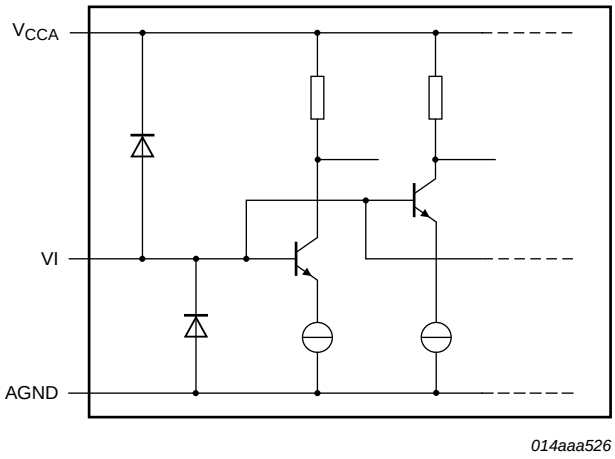

Fig 8. VI analog input

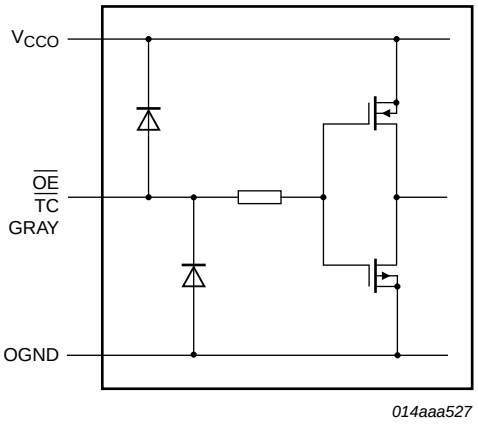

Fig 9. $\overline{OE}$ GRAY and $\overline{TC}$ inputs

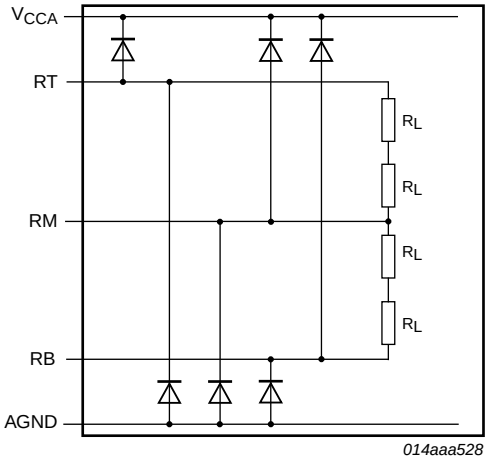

Fig 10. RB, RM and RT inputs

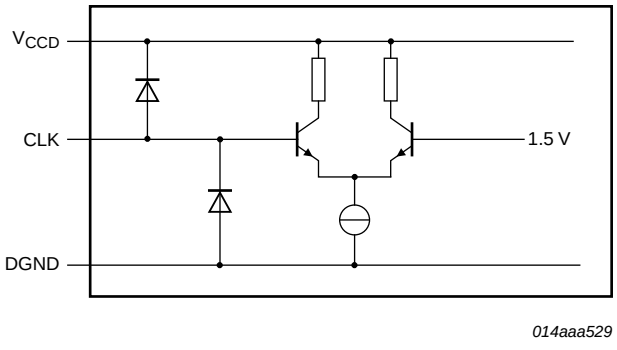

Fig 11. CLK input

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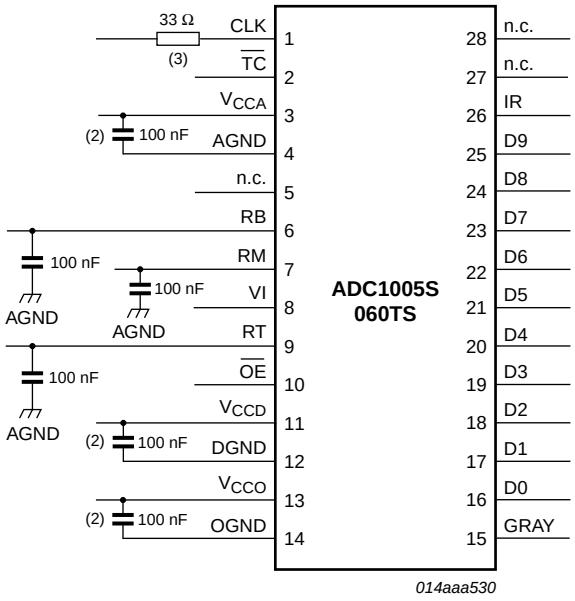
12. Application information

12.1 Application diagrams



The analog and digital supplies should be separated and decoupled.

A user manual is available that describes the demonstration board that uses the version ADC1004S030/040/050 family with an application environment.

(1) RB, RM and RT are decoupled to AGND

(2) Decoupling capacitor for supplies must be placed close to the device.

(3) This resistor is mandatory (33 Ω is its minimum value) and must be near the clock source.

Fig 12. Application diagram

12.2 Alternative parts

The following alternative parts are also available:

Table 11. Alternative parts

Type number	Description		Sampling frequency
ADC0804S030	Single 8 bits ADC	[1]	30 MHz
ADC0804S040	Single 8 bits ADC	[1]	40 MHz
ADC0804S050	Single 8 bits ADC	[1]	50 MHz
ADC1003S030	Single 10 bits ADC, with internal reference regulator	[1]	30 MHz
ADC1003S040	Single 10 bits ADC, with internal reference regulator	[1]	40 MHz
ADC1003S050	Single 10 bits ADC, with internal reference regulator	[1]	50 MHz

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Table 11. Alternative parts

Type number	Description		Sampling frequency
ADC1004S030	Single 10 bits ADC	[1]	30 MHz
ADC1004S040	Single 10 bits ADC	[1]	40 MHz
ADC1004S050	Single 10 bits ADC	[1]	50 MHz

[1] Pin to pin compatible

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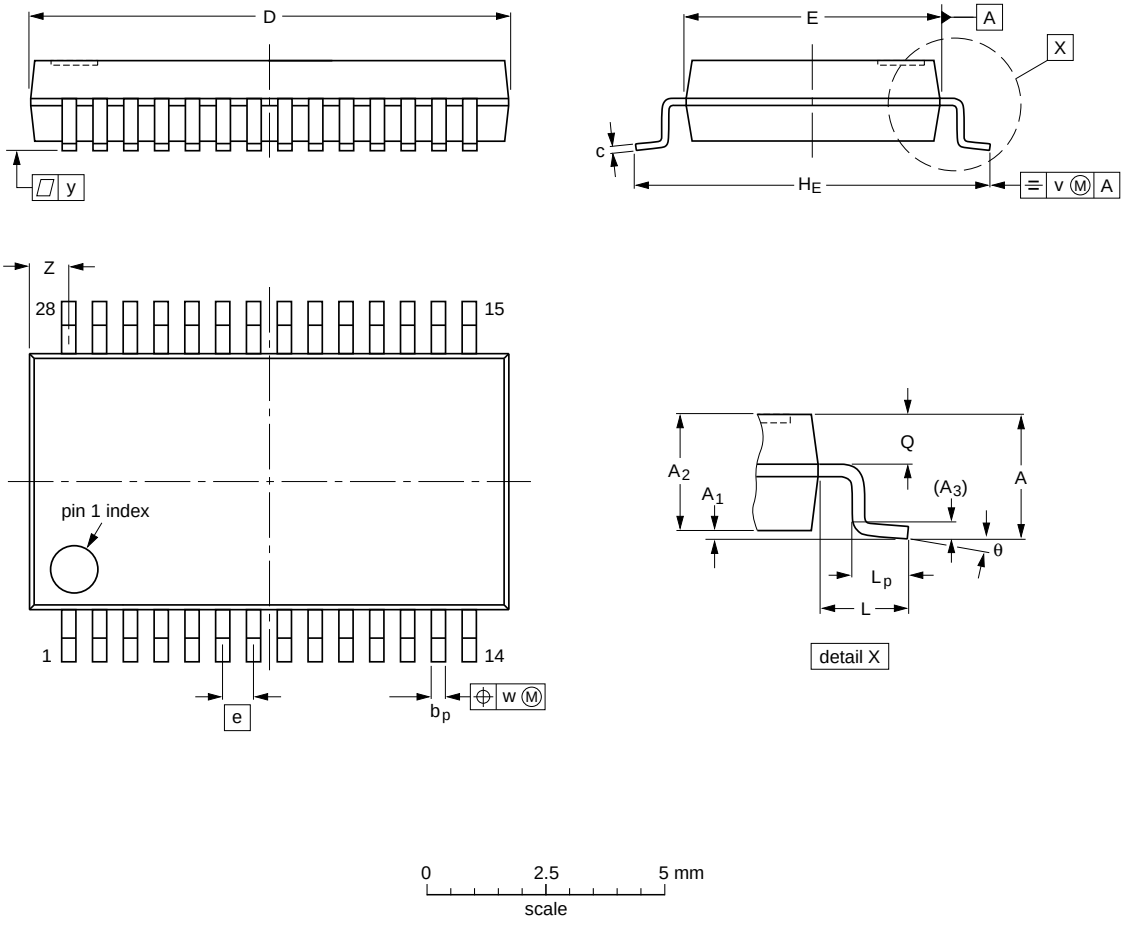
13. Package outline

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT341-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT341-1 (SSOP28)

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14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1005S060_3	20120702	Product data sheet	-	ADC1005S060_2
ADC1005S060_2	20080813	Product data sheet	-	ADC1005S060_1
Modifications:	• Corrections made to INL and DNL conditions in Table 1. • Corrections made to several entries and notes in Table 6. • Correction made to table description in Table 7. • Correction made to column D9 to D0 in Table 10. • Correction made to Figure 8. • Correction made to Figure 10.			
ADC1005S060_1	20080616	Product data sheet	-	-

15. Contact information

For more information or sales office addresses, please visit: http://www.idt.com

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