MAX11261

24-Bit, 6-Channel, 16ksps, 6.2nV/√Hz PGA, Delta-Sigma ADC with I²C Interface

General Description

The MAX11261 is a 6-channel, 24-bit delta-sigma ADC that achieves exceptional performance while consuming very low power. Sample rates up to 16ksps allow precision DC measurements. The device also features a 64-entry, on-chip FIFO to offload the host processor. The MAX11261 communicates through an I²C-compatible serial interface and is available in a small, wafer-level package (WLP).

The MAX11261 offers a 6.2nV/√Hz noise programmable gain amplifier (PGA) with gain settings from 1x to 128x. The integrated PGA provides isolation of the signal inputs from the switched capacitor sampling network. The PGA also enables the MAX11261 to interface directly with high-impedance sources without compromising the available dynamic range.

The MAX11261 operates from a single 2.7V to 3.6V analog supply. The digital supply range is 1.7V to 2.0V (internal LDO off) and 2.0V to 3.6V (internal LDO on) enabling communication with 1.8V, 2.5V, 3V, or 3.3V logic.

Applications

- Wearable Electronics
- Medical Equipment
- Weigh Scales
- Pressure Sensors
- Battery-Powered Instrumentation

Benefits and Features

- Analog Supply
  - 2.7V to 3.6V
- Digital Supply
  - Internal LDO Disabled—1.7V to 2.0V
  - Internal LDO Enabled—2.0V to 3.6V
- 3ppm INL (typ)
- PGA
  - Gains of 1, 2, 4, 8, 16, 32, 64, 128
  - Low-Noise Mode, 6.2nV/√Hz Noise
  - Low-Power Mode, 10nV/√Hz Noise
- Input-Referred Noise
  - PGA Low-Noise Mode, Gain of 64 at 1ksps Continuous, 0.15μV_{RMS}
- Fully Differential Signal and Reference Inputs
- Internal System Clock of 8.192MHz
- I²C-Compatible Serial Interface
- Supports Standard, Fast-Mode, and Fast-Mode Plus I²C Specifications
- 64-Entry, On-Chip FIFO
- Hardware Interrupt for Input Monitoring and FIFO Usage
- On-Demand Self and System Gain and Offset Calibration
- User-Programmable Offset and Gain Registers
- Two Power-Down Modes (SLEEP and STANDBY)
- Low Power Dissipation
- ESD Rating: ±2.5kV (HBM), 750V (CDM)
- -40°C to +85°C Operating Temperature Range
- 6 x 6 Bump, 0.4mm Pitch, 2.838mm x 2.838mm x 0.5mm WLP

***Ordering Information* appears at end of data sheet.**

19-100250; Rev 1; 11/20

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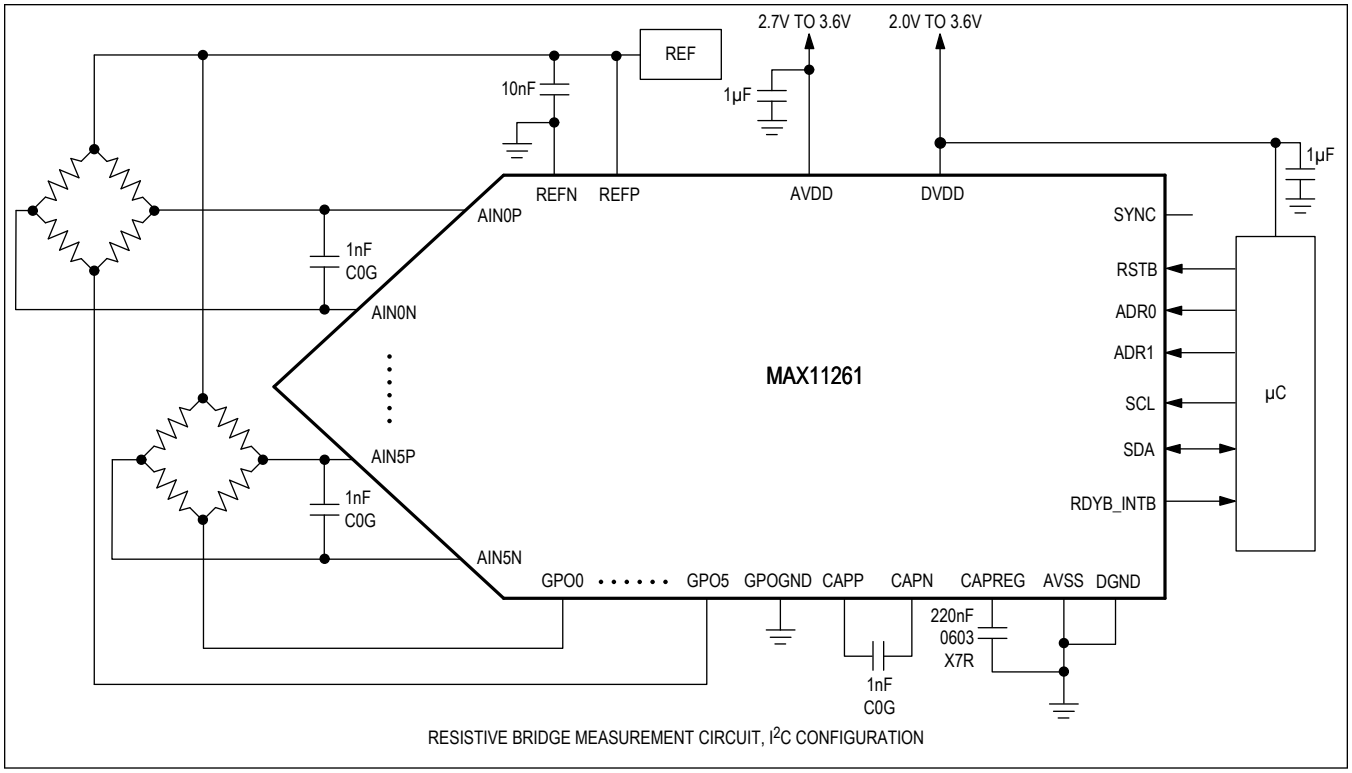
Typical Application Circuit



RESISTIVE BRIDGE MEASUREMENT CIRCUIT, I2C CONFIGURATION

Absolute Maximum Ratings

AVDD to AVSS ..... -0.3V to +3.9V
DVDD to DGND ..... -0.3V to +3.9V
AVSS to DGND ..... -0.3V to +0.3V
Analog Inputs: .....
GPOGND to AVSS or DGND ..... -0.3V to +0.3V
(AIN_P, AIN_N, CAPP, CAPN, REFP, REFN) to AVSS ..-0.3V to the lower of +3.9V or (V_{AVDD} + 0.3V)
GPO_ to GPOGND or AVSS or DGND .... -0.3V to to the lower of +3.9V or (V_{AVDD} + 0.3V)
Digital Inputs: .....
(RSTB, SYNC, SCL, SDA, ADR0, ADR1) to DGND ... 0.3V to the lower of +3.9V or (V_{DVDD} + 0.3V)
Digital Outputs: .....
(RDYB_INTB, SDA, SYNC) to DGND ... -0.3V to (V_{DVDD} + 0.3V)
CAPREG to DGND ..... -0.3V to +2.1V
Maximum Continuous Current into Any Pins Except GPO_ and GPOGND Pins ..... ±50mA
Maximum Continuous Current into GPO_ and GPOGND Pins 150mA
Continuous Power Dissipation (T_A = +70°C; WLP; derate 21.7mW/°C above +70°C) 1736mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -55°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

36 WLP

Package Code	**N362B2+2**
Outline Number	21-0742
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	46°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (SINGLE-CYCLE CONVERSION MODE)							
Noise Voltage (Referred to Input)	Vn	PGA gain of 128, single-cycle mode at 1ksps data rate	PGA low-noise mode		0.19		μV_{RMS}
			PGA low-power mode		0.26		
		PGA gain of 128, single-cycle mode at 12.8ksps data rate	PGA low-noise mode		0.83		
			PGA low-power mode		1.16		
		PGA gain of 128, continuous mode at 64ksps data rate	PGA low-noise mode		0.83		
			PGA low-power mode		1.16		
Integral Nonlinearity	INL				3	15	ppm
Zero Error	Z_{ERR}	After system zero-scale calibration			1		µV
Zero Drift	Z_{Drift}				50		nV/°C
Full-Scale Error (*Note 2* and *Note 3*)	FSE	After system full-scale calibration			2		ppmFSR
Full-Scale Error Drift	FSE_{Drift}				0.05		ppm FSR/°C
Common-Mode Rejection	CMR	DC rejection		110	130		dB
		50Hz/60Hz rejection (*Note 4*)		110	130		
		DC rejection with PGA gain 128		80	95		
AVDD, AVSS DC Supply Rejection Ratio	PSRRA	DC rejection		75	95		dB
AVDD, AVSS DC SupplyRejection Ratio	PSRRA	50Hz/60Hz rejection (*Note 4*)		75	95		dB
AVDD, AVSS DC Supply Rejection Ratio	PSRRA	DC rejection with PGA gain 128		65	75		dB
DVDD DC Supply Rejection Ratio	PSRRD	DC rejection		103	115		dB
		50Hz/60Hz rejection (*Note 4*)		103	115		
		DC rejection with PGA gain 128		86	110		
PGA							
Gain Setting				1		128	V/V
Noise-Spectral Density	NSD	Low-noise mode			6.2		nV/√Hz
		Low-power mode			10		

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Error, Not Calibrated	G_{ERR}	Gain = 1		0.75		%
		Gain = 2		1.2		
		Gain = 4		2		
		Gain = 8		3		
		Gain = 16		4.5		
		Gain = 32		6		
		Gain = 64		5.5		
		Gain = 128		2		
Output Voltage Range	V_{OUTRNG}		V_{AVSS} + 0.3		V_{AVDD} - 0.3	V
MUX						
Channel-to-Channel Isolation	ISO_{CH-CH}	DC		140		dB
GENERAL-PURPOSE OUTPUTS						
Resistance (On)	R_{ON}	Voltage between GPO_ and GPOGND < 200mV, GPOGND connected to AVSS		3.5	10	Ω
Maximum Current (On)	I_{MAX}	Per output		30		mA
		Total from all outputs into GPOGND bump (*Note 4*)			90	
Leakage Current (Off)	I_{LEAK1}	Current into the GPOGND pin with one individual GPO_ pin connected to 3V		0.4		nA
	I_{LEAK6}	Current into the GPOGND pin with all GPO_ pins connected to 3V		13	100	
AUTOSCAN TIMER						
Timer Resolution	AST_{RES}			4		ms
Accuracy	AST_{ACC}	Over voltage and temperature (*Note 4*)		5	10	%
POWER-UP DELAYS (*Note 4*)						
Power-Up Time	T_{PUPSLP}	SLEEP state (full power-down) to LDO wake-up, V_{AVDD} = 2.7V, V_{DVDD} = 2.0V, CAPREG = 220nF		23	45	µs
	T_{PUPSBY}	STANDBY state (analog blocks powered down, LDO on) to Active		4	8	
RSTB Fall to RDYB '1'	t_{R2}	RDYB transition from '0' to '1' on falling edge of RSTB (*Note 4*)			300	ns
ANALOG INPUTS/REFERENCE INPUTS						
Common-Mode Input Voltage Range, V_{CM} = (V_{AIN_P} + V_{AIN_N})/2	CMI_{RNG}	Direct (PGA bypassed)	V_{AVSS}		V_{AVDD}	V
Common-Mode Input Voltage Range, V_{CM} = (V_{AIN_P} + V_{AIN_N})/3	CMI_{RNG}	PGA	V_{AVSS} + 0.3		V_{AVDD} -1.3	V

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Input Voltage Range	VABSRNG	Direct (PGA bypassed)	VAVSS		VAVDD	V
	$VABS_{RNG}$	PGA	V_{AVSS} + 0.3		V_{AVDD} -1.3	
DC Input Leakage	IIN_{LEAK}	SLEEP state enabled		±0.1		nA
Differential Input Conductance	G_{DIFF}	Direct (PGA bypassed)		±11.6		µA/V
Differential Input Current	I_{DIFF}	PGA enabled		±1.0		nA
Common-Mode Input Conductance	G_{CM}	Direct (PGA bypassed)		±1.0		µA/V
Common-Mode Input Current	I_{CM}	PGA enabled		±10		nA
Reference Differential Input Resistance	R_{REF}	Active state		26		kΩ
Reference Differential Input Current	I_{REF_PD}	STANDBY and SLEEP state		±1		nA
Input Capacitance	C_{IN}	Direct (PGA bypassed)		2.5		pF
	CP_{GAIN}	PGA		0.25		
Voltage Range (AINP - AINN)	$V_{IN(DIFF)}$	Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}$		$+V_{REF}$	
AINP, AINN Sampling Rate	f_S			4.096		MHz
REFP, REFN Voltage Range	$VRABS_{RNG}$	(*Note 5*)			V_{AVDD}	V
REFP – REFN Differential Voltage Range	V_{REF}		1.5		V_{AVDD}	V
REFP, REFN Sampling Rate				4.096		MHz
SENSOR FAULT DETECT CURRENTS						
Current				1.1		µA
Initial Tolerance				±10		%
Drift				0.3		%/°C
DIGITAL SINC FILTER RESPONSE						
Bandwidth (-3dB)				0.203 x DATA RATE		Hz
Settling Time (Latency)				5/DATA RATE		s
LOGIC INPUTS						
VIMAX_I²C		Maximum input voltage of SDA and SCL			V_{DVDD}	V
Input Current	$IDIGI_{LEAK}$	Leakage current			±1	µA

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
LOGIC OUTPUTS						
VOMAX_I²C		Maximum output voltage of SDA			V_{DVDD}	V
Output Low Level	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Level (RDYB, DOUT)	V_{OH}	I_{OH} = 1mA	0.9 x V_{DVDD}			V
Floating State Leakage Current	$IDIGO_{LEAK}$				±10	µA
Floating State Output Capacitance	C_{DIGO}			9		pF
POWER REQUIREMENTS						
Negative Analog Supply Voltage	V_{AVSS}		0			V
Positive Analog Supply Voltage	V_{AVDD}		2.7		3.6	V
I/O Supply Voltage	V_{DVDD}	CAPREG is not being driven by external supply	2.0		3.6	V
		DVDD and CAPREG bumps connected together on the circuit board	1.7		2.0	
CAPREG Supply Voltage	V_{CAPREG}	Voltage developed internally from DVDD using a subregulator; When CAPREG pin is driven externally, ensure that it is connected directly to DVDD pin.	1.7		2.0	V
Analog Supply Current	I_{AVDD}	Direct		2.2	3	mA
		PGA low-power mode		3.5	4.6	
		PGA low-noise mode		4.2	5.65	
DVDD Operating Current	$I_{DVDD(CNV)}$	V_{DVDD} = 2.0V, LDO enabled		0.65	1.1	mA
		V_{DVDD} = V_{CAPREG} = 2.0V, LDO disabled		0.58		
AVDD Sleep Current	$I_{AVDD(SLP)}$	V_{AVDD} = 3.466V, V_{AVSS} = 0V, V_{DVDD} = 2.0V		1		µA
DVDD Sleep Current	$I_{DVDD(SLP)}$	V_{DVDD} = 2.0V		0.3	1	µA
AVDD Standby Current	$I_{AVDD(SBY)}$	V_{AVDD} = 3.465V, V_{AVSS} = 0V, V_{DVDD} = 2.0V		1.5		µA
DVDD Standby Current	$I_{DVDD(SBY)}$	V_{DVDD} = 2.0V, LDO enabled		50	175	µA
		V_{DVDD} = V_{CAPREG} = 2.0V, LDO disabled		2.5		

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Threshold Low-to-High	V_{LH}	AVDD, DVDD supply undervoltage lockout	0.8	1.2	1.65	V
		CAPREG supply undervoltage lockout	0.7	1.0	1.35	
UVLO Threshold High-to-Low	V_{HL}	AVDD, DVDD supply undervoltage lockout	0.6	1.1	1.5	V
		CAPREG supply undervoltage lockout	0.5	0.95	1.3	
UVLO Hysteresis	V_{HYS}	AVDD, DVDD supply undervoltage lockout		4		%
		CAPREG supply undervoltage lockout		5		
UVLO Delay Low-to-High or High-to-Low	T_{DEL}	AVDD, DVDD supply undervoltage lockout		10		µs
		CAPREG supply undervoltage lockout		3.5		
UVLO Glitch Suppression	T_P	AVDD, DVDD supply undervoltage lockout		10		ns
		CAPREG supply undervoltage lockout		10		
Serial Clock Frequency	f_{SCL}	Note 4 applies to minimum value	0.1		1	MHz
Bus Free Time Between STOP and START Condition	t_{BUF}		0.5			µs
Hold Time (Repeated) START Condition (After This Period, First Clock Pulse Is Generated)	$t_{HD;STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for Repeated START Condition	$t_{SU;STA}$		0.26			µs
Data Hold Time	$t_{HD;DAT}$		0			µs
Data Setup Time	$t_{SU;DAT}$		50			ns
SDA and SCL Receiving Rise Time	tr	(Note 4)			120	ns
SDA and SCL Receiving Fall Time	tf	(Note 4)	20 x V_{DVDD}/5.5		120	ns
SDA Transmitting Fall Time	tf		20 x V_{DVDD}/5.5		120	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus Capacitance Allowed	C_b	(Note 4)			550	pF

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width of Suppressed Spike	t_{SP}			50		ns

Note 1: Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Full-scale error includes errors from gain and offset or zero-scale error.

Note 3: ppmFSR is parts per million of full-scale range.

Note 4: These specifications are guaranteed by design, characterization, or I²C protocol.

Note 5: Reference common mode (V_{REFP} + V_{REFN})/2 ≤ (V_{AVDD} + V_{AVSS})/2 + 0.1V.

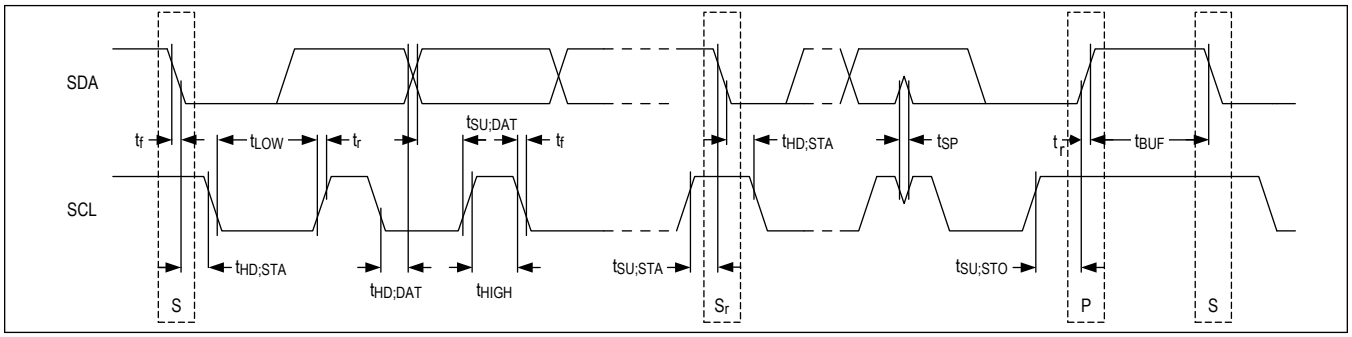
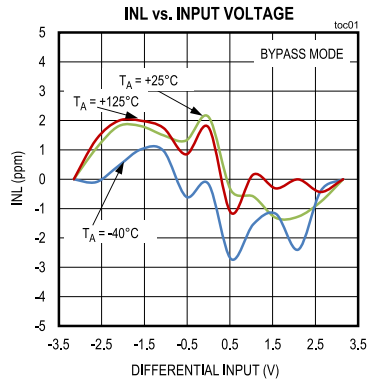
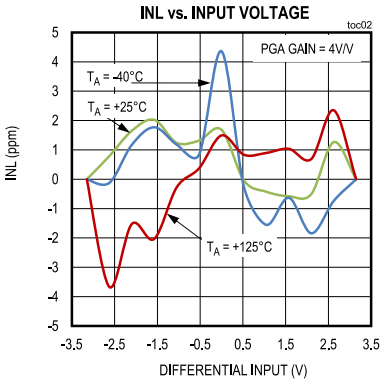


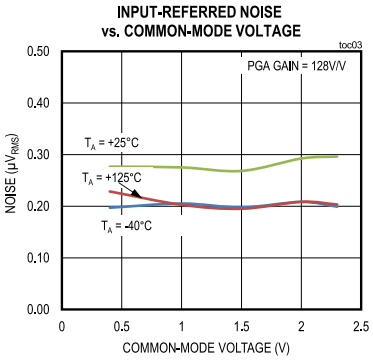
Figure 1. I²C Timing Diagram

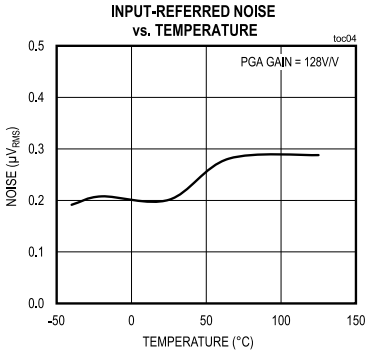
Typical Operating Characteristics

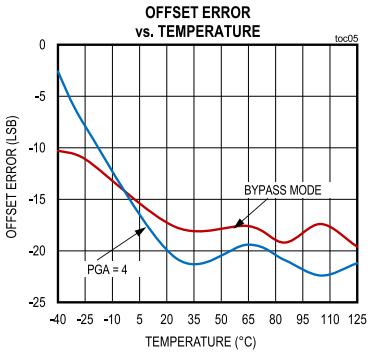
(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Typical values are at T_A = +25°C.)

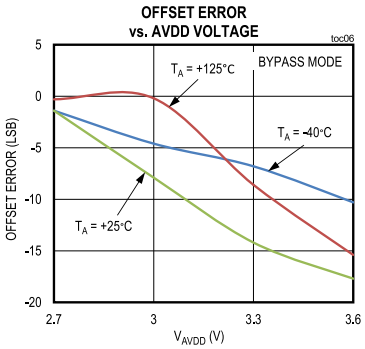


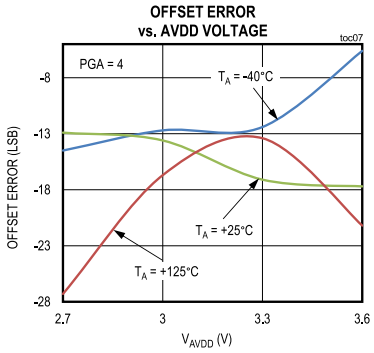


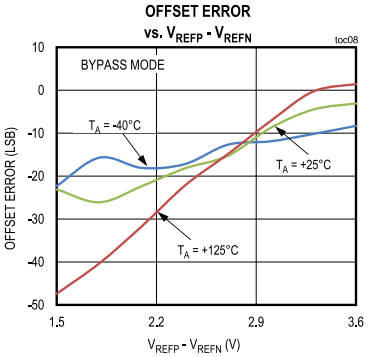


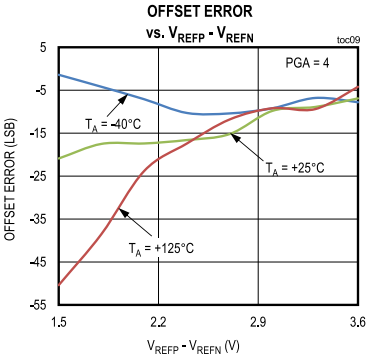






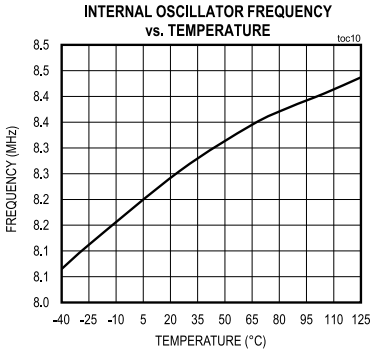


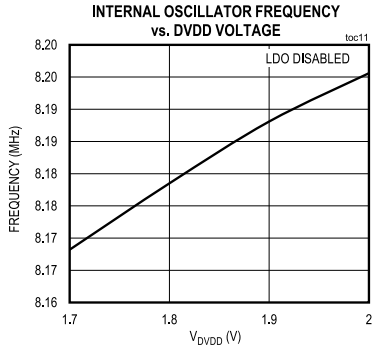


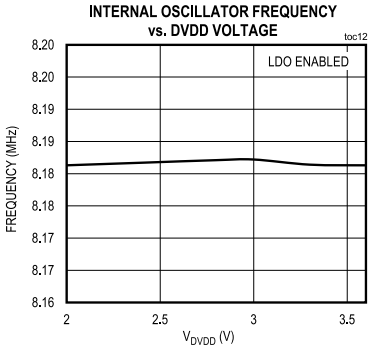


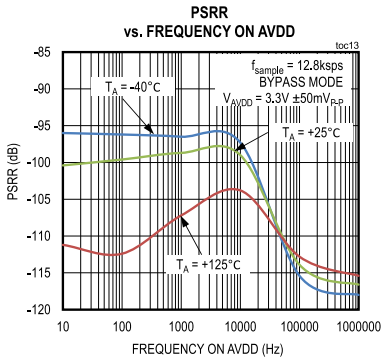
Typical Operating Characteristics (continued)

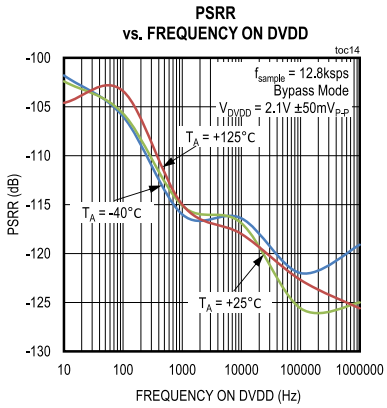
(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Typical values are at T_A = +25°C.)

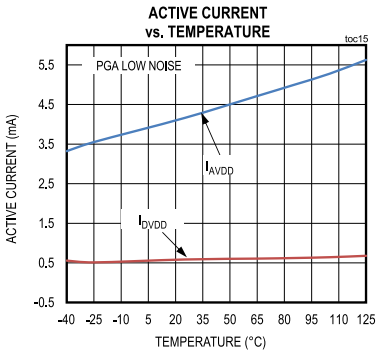


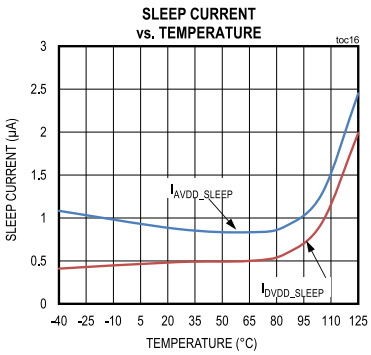


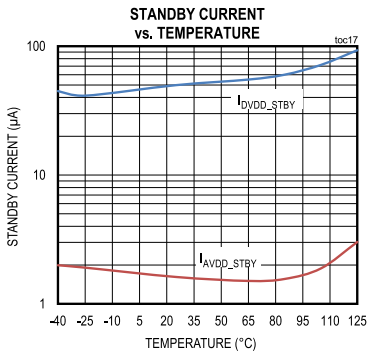


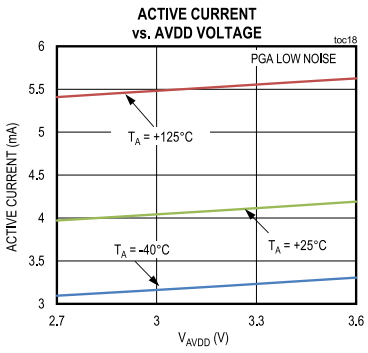






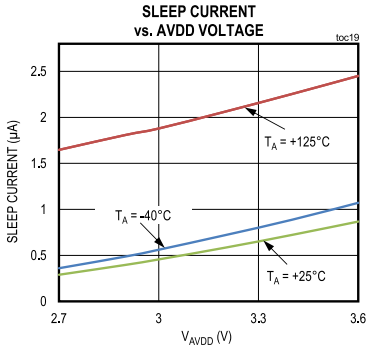


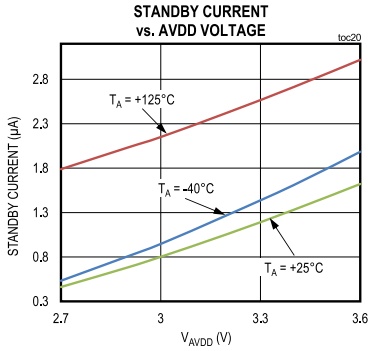


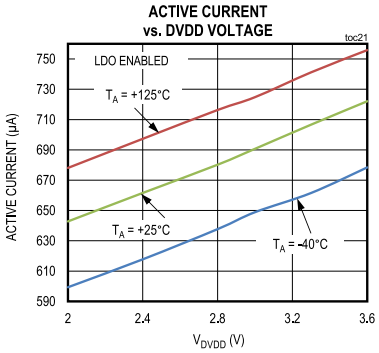


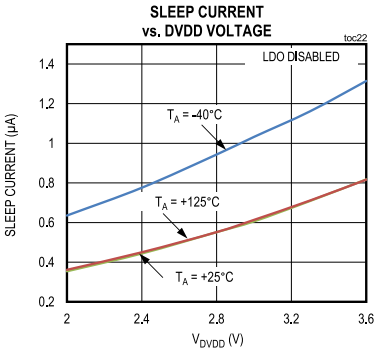
Typical Operating Characteristics (continued)

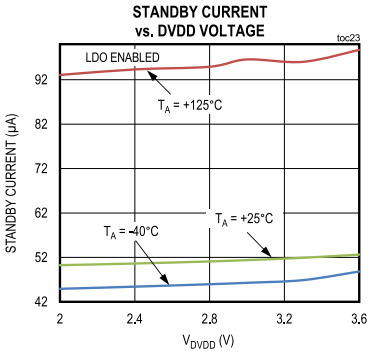
(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Typical values are at T_A = +25°C.)



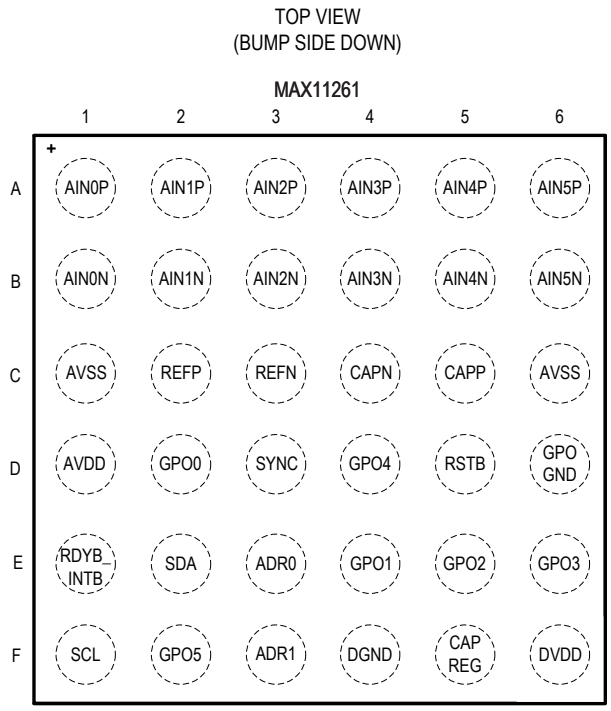








Bump Configuration



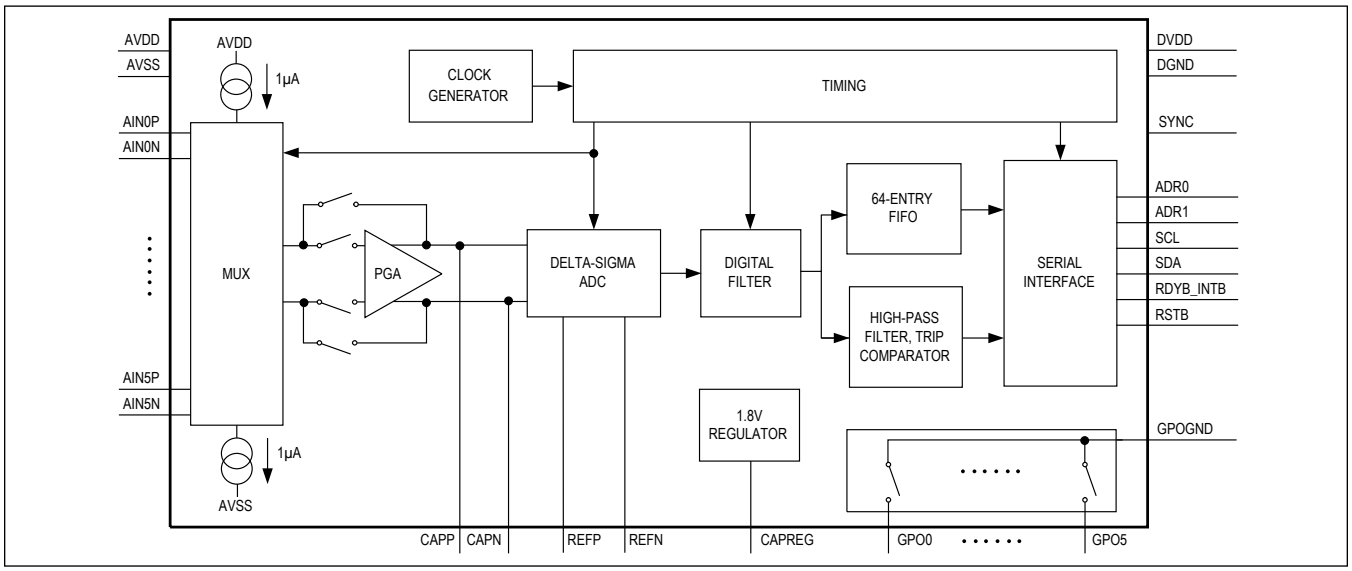
Bump Descriptions

PIN	NAME	FUNCTION	TYPE
A1	AIN0P	Positive Analog Input 0. A 1nF C0G capacitor should be added between differential input pin pairs.	IN/Analog
A2	AIN1P	Positive Analog Input 1. A 1nF C0G capacitor should be added between differential input pin pairs	IN/Analog
A3	AIN2P	Positive Analog Input 2. A 1nF C0G capacitor should be added between differential input pin pairs.	IN/Analog
A4	AIN3P	Positive Analog Input 3. A 1nF C0G capacitor should be added between differential input pin pairs.	IN/Analog
A5	AIN4P	Positive Analog Input 4. A 1nF C0G capacitor should be added between differential input pin pairs.	IN/Analog
A6	AIN5P	Positive Analog Input 5. A 1nF C0G capacitor should be added between differential input pin pairs.	IN/Analog
B1	AIN0N	Negative Analog Input 0	IN/Analog
B2	AIN1N	Negative Analog Input 1	IN/Analog
B3	AIN2N	Negative Analog Input 2	IN/Analog
B4	AIN3N	Negative Analog Input 3	IN/Analog
B5	AIN4N	Negative Analog Input 4	IN/Analog
B6	AIN5N	Negative Analog Input 5	IN/Analog

Bump Descriptions (continued)

PIN	NAME	FUNCTION	TYPE
C1, C6	AVSS	Analog Ground	AGND
C2	REFP	Positive Reference Input	IN/Analog
C3	REFN	Negative Reference Input	IN/Analog
C4	CAPN	PGA Filter Input. Connect 1nF C0G capacitor between CAPP and CAPN.	IN/Analog
C5	CAPP	PGA Filter Input. Connect 1nF C0G capacitor between CAPP and CAPN.	IN/Analog
D1	AVDD	Positive Analog Supply	PWR
D2	GPO0	Analog Switch Normally Open Terminal/General-Purpose Output 0. Register controlled, close position connects GPO0 to GPOGND. Current sink only.	OUT/Analog
D3	SYNC	Synchronization Pin for Multiple Devices. At power-up, the device defaults to a master (CTRL3:SYNC = 1) and the SYNC pin output is in high impedance state (CTRL3:SYNCZ = 1). When the device is configured as a master and the register CTRL3:SYNCZ is set to 0, the SYNC pin is changed to an active-low, open-drain output pin. Set CTRL:SYNC to 0 puts the device in slave mode and the SYNC pin is an input. An external pullup resistor is required if the SYNC function is used.	IN/OUT/ Digital
D4	GPO4	Analog Switch Normally Open Terminal/General-Purpose Output 4. Register controlled, close position connects GPO4 to GPOGND. Current sink only.	OUT/Analog
D5	RSTB	Active-Low Power-On-Reset Input	IN/Digital
D6	GPOGND	Analog Switch/General-Purpose Output, GND Terminal	OUT/Analog
E1	RDYB_INTB	Active-Low Open-Drain Output. A pullup resistor to DVDD is required. The typical resistor value is 10kΩ. In sequencer modes 1, 2, and 3: RDYB_INTB goes low when a new conversion result is available in the FIFO. When the FIFO entries are completely read out, RDYB_INTB returns high if no FIFO usage interrupt is asserted. The RDYB_INTB also goes low when there is at least one FIFO usage interrupt. In sequencer mode 4: RDYB_INTB indicates the input comparison result and FIFO usage interrupt.	OUT/Digital
E2	SDA	I²C Serial Data	IN/OUT/I²C
E3	ADR0	I²C Address Select Line 0	IN/Digital
E4	GPO1	Analog Switch Normally Open Terminal/General-Purpose Output 1. Register controlled, close position connects GPO1 to GPOGND. Current sink only.	OUT/Analog
E5	GPO2	Analog Switch Normally Open Terminal/General-Purpose Output 2. Register controlled, close position connects GPO2 to GPOGND. Current sink only.	OUT/Analog
E6	GPO3	Analog Switch Normally Open Terminal/General-Purpose Output 3. Register controlled, close position connects GPO3 to GPOGND. Current sink only.	OUT/Analog
F1	SCL	I²C Serial Clock Input	IN/Digital/I²C
F2	GPO5	Analog Switch Normally Open Terminal/General-Purpose Output 5. Register controlled, close position connects GPO5 to GPOGND. Current sink only.	OUT/Digital
F3	ADR1	I²C Address Select Line 1	INDigital
F4	DGND	Digital Ground	DGND
F5	CAPREG	1.8V Subregulator Output. Connects to DVDD when driven externally by a 1.8V supply. Connect a 220nF to DGND.	PWR
F6	DVDD	Digital Power Supply	PWR

Functional Diagrams



Detailed Description

The MAX11261 is a 24-bit, delta-sigma ADC that achieves exceptional performance consuming minimal power. Sample rates up to 16ksps support precision DC measurements. The built-in sequencer supports scanning of selected analog channels, auto wake-up, programmable conversion delay, and math operations to automate sensor monitoring.

The fourth-order, delta-sigma modulator is unconditionally stable and measures the six differential input voltages. To prevent overdriving, the modulator is monitored for overrange conditions and is reported in the status register. The digital filter is a variable decimation-rate SINC filter with overflow monitoring reported in the status register.

The programmable gain differential amplifier (PGA) is low noise and is programmable from 1 to 128. The PGA buffers the modulator and provides a high-impedance input to the analog channels.

The device stores the conversion results in a 64-entry FIFO. The FIFO interrupts wake up the host processor less frequently to reduce the system power consumption. The device also features an autonomous scan mode to monitor the input activity. The device only interrupts the host when the input is out of a configured range.

System Clock

The MAX11261 incorporates a highly stable internal oscillator that provides the system clock. The system clock is trimmed to 8.192MHz, providing digital and analog timing.

Voltage Reference Inputs

The MAX11261 provides differential inputs REFP and REFN for an external reference voltage. Connect the external reference directly across the REFP and REFN bumps to obtain the differential reference voltage. The V_{REFP} voltage should always be greater than the V_{REFN} voltage, and the common-mode voltage range is between 0.75V and V_{AVDD} - 0.75V.

Analog Inputs

The MAX11261 measures six pairs of differential analog inputs (AIN_P, AIN_N) in direct connection or buffered through the PGA. See the CTRL2: Control Register 2 (Read/Write) table for programming and enabling the PGA or direct connect mode. The default configuration is direct connect with the PGA powered down.

Bypass/Direct Connect

The MAX11261 offers the option to bypass the PGA and route the analog inputs directly to the modulator. This option lowers the power of the device since the PGA is powered down.

Programmable Gain Amplifier (PGA)

The integrated PGA provides gain settings from 1x to 128x (Figure 2). Direct connection is available to bypass the PGA and directly connect to the modulator. The PGA's absolute input voltage range is CMIRNG and the PGA output voltage range is V_{OUTRNG}, as specified in the *Electrical Characteristics*.

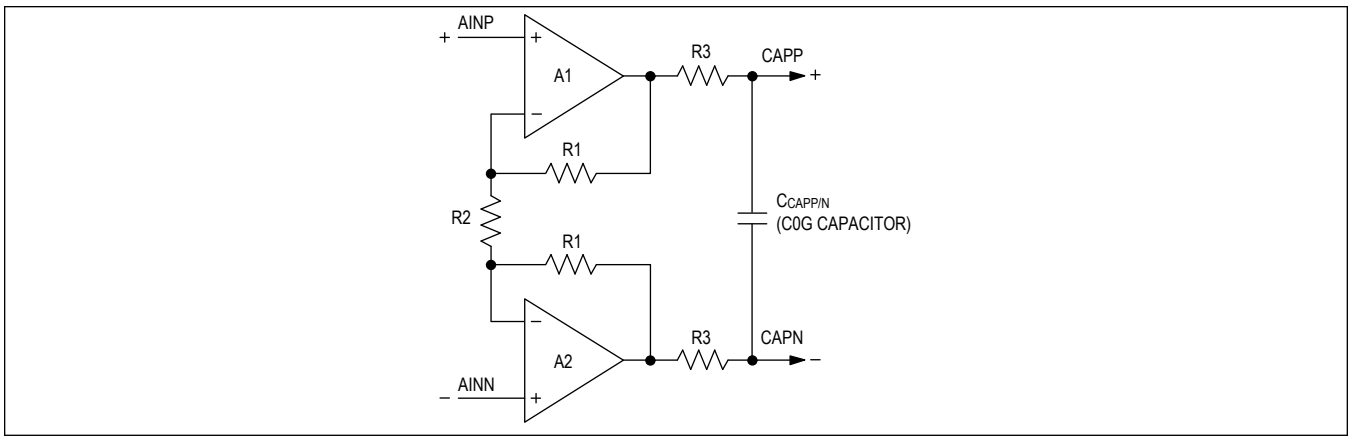


Figure 2. Simplified Equivalent Diagram of the PGA

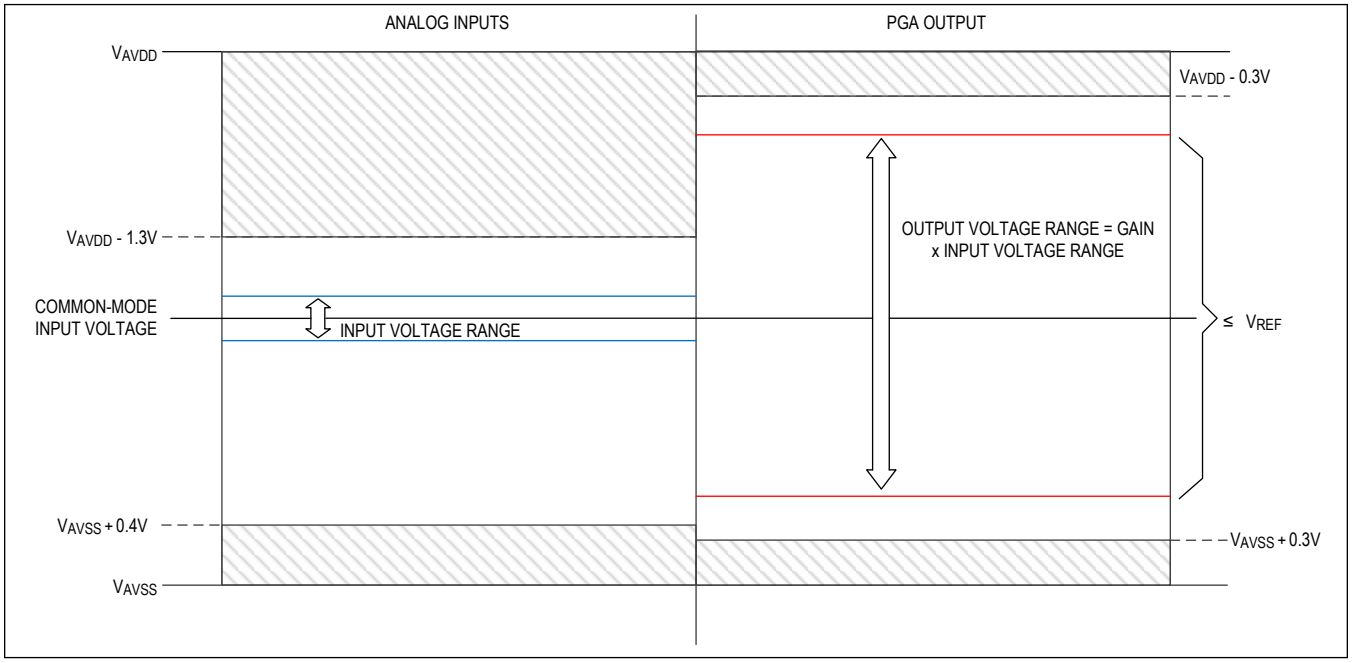


Figure 3. Analog Input Voltage Range Compared to PGA Output Range

Note that linearity and performance degrade when the specified input common-mode voltage of the PGA is exceeded. The input common-mode range and output common-mode range are shown in Figure 3. The following equations describe the relationship between the analog inputs and PGA output.

AINP = Positive input to the PGA

AINN = Negative input to the PGA

CAPP = Positive output of PGA

CAPN = Negative output of PGA

V_{CM} = Input common mode

GAIN = PGA gain

V_{REF} = ADC reference input voltage

$V_{IN} = V_{AINP} - V_{AINN}$

Note: Input voltage range is limited by the reference voltage, as described by $V_{IN} \leq \pm V_{REF}/GAIN$:

$$V_{CM} = \frac{(V_{ANP} + V_{AINN})}{2}$$

$$V_{CAPP} = V_{CM} + GAIN \times (V_{AINP} - V_{CM})$$

$$V_{CAPN} = V_{CM} - GAIN \times (V_{CM} - V_{AINN})$$

PGA High Current

When V_{AVDD} voltage is above 2.9V and PGA is enabled, high I_{AVDD} current could be observed on the MAX11261 if the PGA outputs are driven out of normal operating range and then rapidly driven back within the range during continuous conversion. The current can be as high as 30mA, depending on the AV_{DD} supply voltage and PGA output voltage.

To trigger the PGA high-current state, drive the PGA output from normal low-side compliance range (> V_{AVSS} + 0.3V) to less than (V_{AVSS} + 40mV), and then drive back into compliance range (> V_{AVSS} + 0.3V) with a slew rate greater than 0.7V/µs while the device is performing continuous conversion.

The high-current state can also be triggered when interrupting a self-calibration in progress by starting a new conversion command when the PGA is enabled, which internally creates the trigger condition.

The PGA high-current state cannot be triggered with V_{AVDD} supply voltage below 2.9V.

When PGA high-current state is triggered, I_{AVDD} current could be 4.5 times as high as the normal I_{AVDD} current.

Exit Condition

PGA high-current state can always be exited by changing the MAX11261 to STANDBY or SLEEP state.

It will be automatically recovered when the MAX11261 is configured in mode 1 single-cycle conversion mode, mode 2, mode 3, or mode 4 if AutoScan Delay > 0. In these modes, the device automatically goes to STANDBY or SLEEP mode after the conversion.

When PGA high current state is triggered in mode 1 continuous conversion mode or mode 4 AutoScan Delay = 0, it can be recovered by issuing firmware command to cycle STANDBY or SLEEP state. To force the MAX11261 into STANDBY or SLEEP state, either issue a power-down command or write to one of the CTRL registers.

Input Voltage Range

The ADC input range is programmable for bipolar ($-V_{REF}$ to $+V_{REF}$) or unipolar (0 to V_{REF}) ranges. The U/B bit in the CTRL1 register configures the MAX11261 for unipolar or bipolar transfer functions.

Data Rates

Table 1 lists the available data rates for the MAX11261, RATE[3:0] setting of the conversion command (see the *Modes and Registers* section). The single-cycle mode has an overhead of 48 digital master clocks that is approximately 5.86µs from a typical digital master clock frequency of 8.192MHz. The single-cycle effective column contains the data rate values including the 48 clock startup delays. The 48 clocks are to stabilize the modulator startup. In continuous conversion mode, the output data rate is five times the single-cycle rate up to a maximum of 16ksps. During continuous conversions, the output sample data requires five 24-bit cycles to settle to a valid conversion from an input step, PGA gain changes, or a change of input channel through the multiplexer.

If self-calibration operation is used, 48 additional master clocks are required to process the data per conversion. Likewise, system calibration takes an additional 48 master clocks to complete.

If both self and system-calibration are used, it takes an additional 80 master clocks to complete. If self and/or system calibration are used, the effective data rate will be reduced by these additional clock cycles per conversion.

Table 1. Available Programmable Data Rates

	DATA RATE (sps)

Table 1. Available Programmable Data Rates (continued)

RATE[3:0]	CONTINUOUS	SINGLE CYCLE	CONVERSION ONLY	CONVERSION PLUS SELF-CALIBRATION*	CONVERSION PLUS SELF-CALIBRATION PLUS SYSTEM CALIBRATION*
0000	1.9	50	50.01	49.99	49.98
0001	3.9	62.5	62.51	62.48	62.47
0010	7.8	100	99.98	99.92	99.88
0011	15.6	125	124.95	124.86	124.80
0100	31.2	200	199.80	199.57	199.41
0101	62.5	250	249.66	249.29	249.05
0110	125	400	398.98	398.05	397.44
0111	250	500	498.34	496.89	495.93
1000	500	800	796.11	792.41	789.97
1001	1000	1000	991.86	986.13	982.35
1010	2000	1600	1578.72	1564.26	1554.77
1011	4000	2000	1974.16	1951.60	1936.84
1100	8000	3200	3114.26	3058.48	3022.39
1101	16000**	4000	3895.78	3808.89	3753.08
1110	Not available	6400	6135.27	5922.49	5788.64
1111	Not available	12800	11776.90	11017.10	10562.79

*The effective data rate is lower when the calibration is enabled due to additional MAC (multiply/accumulate) operations required after the conversion is complete to perform the calibration adjustment.

**Only supported in Fast-Mode Plus.

Noise Performance

The MAX11261 provides exceptional noise performance. SNR is dependent on data rate, PGA gain, and power mode. Bandwidth is reduced at low data rates; both noise and SNR are improved proportionally. Table 2 and Table 3 summarize the noise performance for both single cycle and continuous operation versus data rate, PGA gain, and power mode.

Table 2. Noise vs. PGA Mode and Gain (Single-Cycle Conversion)

DATA RATE (sps)	SINGLE-CYCLE CONVERSION MODE INPUT-REFERRED NOISE VOLTAGE (mV_{RMS}) vs. PGA GAIN SETTING															
	1		2		4		8		16		32		64		128	
	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN
50	0.81	0.58	0.38	0.27	0.18	0.13	0.10	0.07	0.09	0.07	0.08	0.06	0.08	0.06	0.08	0.06
62.5	0.88	0.63	0.48	0.34	0.21	0.15	0.12	0.09	0.09	0.07	0.08	0.06	0.08	0.05	0.08	0.05
100	1.18	0.84	0.61	0.44	0.30	0.21	0.17	0.12	0.12	0.08	0.09	0.07	0.09	0.07	0.10	0.07
125	1.24	0.89	0.59	0.42	0.31	0.22	0.18	0.13	0.12	0.08	0.10	0.07	0.10	0.07	0.10	0.07
200	1.38	0.99	0.68	0.49	0.35	0.25	0.21	0.15	0.15	0.10	0.12	0.08	0.11	0.08	0.11	0.08
250	1.38	0.99	0.72	0.52	0.39	0.28	0.23	0.16	0.16	0.11	0.13	0.09	0.12	0.09	0.12	0.09
400	1.63	1.16	0.85	0.61	0.45	0.32	0.27	0.19	0.19	0.14	0.16	0.12	0.15	0.11	0.16	0.11
500	1.79	1.28	0.93	0.66	0.48	0.34	0.29	0.21	0.21	0.15	0.18	0.13	0.17	0.12	0.18	0.13
800	2.12	1.51	1.10	0.79	0.61	0.43	0.36	0.26	0.27	0.20	0.24	0.17	0.23	0.16	0.23	0.16
1,000	2.38	1.70	1.25	0.89	0.69	0.49	0.41	0.29	0.31	0.22	0.27	0.19	0.26	0.18	0.26	0.19

Table 2. Noise vs. PGA Mode and Gain (Single-Cycle Conversion) (continued)

1,600	3.21	2.29	1.67	1.19	0.89	0.64	0.56	0.40	0.41	0.29	0.36	0.26	0.35	0.25	0.35	0.25
2,000	3.76	2.69	1.95	1.39	1.04	0.74	0.65	0.47	0.48	0.34	0.43	0.30	0.41	0.29	0.42	0.30
3,200	4.41	3.15	2.28	1.63	1.25	0.89	0.78	0.55	0.58	0.41	0.51	0.36	0.49	0.35	0.49	0.35
4,000	5.18	3.70	2.68	1.91	1.48	1.06	0.91	0.65	0.69	0.49	0.60	0.43	0.58	0.41	0.59	0.42
6,400	7.34	5.24	3.83	2.73	2.08	1.48	1.29	0.92	0.98	0.70	0.86	0.61	0.81	0.58	0.83	0.59
12,800	10.84	7.74	5.59	3.99	3.01	2.15	1.85	1.32	1.37	0.98	1.23	0.88	1.17	0.83	1.16	0.83

LP = low power, LN = low noise

Table 3. Noise vs. PGA Mode and Gain (Continuous Conversion)

	CONTINUOUS CONVERSION MODE INPUT-REFERRED NOISE VOLTAGE (mV_{RMS}) vs. PGA GAIN SETTING															
DATA RATE (sps)	1		2		4		8		16		32		64		128	
	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN
15.6	0.45	0.32	0.20	0.14	0.11	0.08	0.06	0.04	0.04	0.03	0.03	0.02	0.03	0.02	0.03	0.02
31.2	0.58	0.41	0.26	0.18	0.13	0.10	0.08	0.06	0.05	0.04	0.04	0.03	0.04	0.03	0.04	0.03
62.5	0.68	0.48	0.34	0.25	0.18	0.13	0.10	0.07	0.07	0.05	0.06	0.04	0.06	0.04	0.06	0.04
125	0.86	0.61	0.44	0.32	0.23	0.16	0.14	0.10	0.10	0.07	0.08	0.06	0.08	0.06	0.08	0.06
250	1.14	0.82	0.56	0.40	0.30	0.22	0.18	0.13	0.14	0.10	0.11	0.08	0.11	0.08	0.11	0.08
500	1.47	1.05	0.76	0.54	0.41	0.29	0.25	0.18	0.19	0.13	0.16	0.11	0.16	0.11	0.16	0.11
1,000	1.99	1.42	1.03	0.73	0.56	0.40	0.35	0.25	0.26	0.19	0.23	0.16	0.21	0.15	0.22	0.16
2,000	2.73	1.95	1.40	1.00	0.76	0.54	0.47	0.34	0.36	0.26	0.31	0.22	0.30	0.21	0.30	0.21
4,000	3.68	2.63	1.86	1.33	1.03	0.73	0.64	0.45	0.49	0.35	0.42	0.30	0.40	0.28	0.41	0.29
8,000	4.57	3.26	2.36	1.69	1.30	0.93	0.81	0.58	0.61	0.43	0.53	0.38	0.52	0.37	0.52	0.37
16,000	5.22	3.73	2.66	1.90	1.48	1.06	0.93	0.67	0.68	0.49	0.61	0.44	0.58	0.41	0.60	0.43

LP = low power, LN = low noise

I²C Protocol

The I²C-compatible serial interface consists of the standard I²C signals: SCL and SDA. The SCL and the SDA pins are bidirectional lines, connected to a positive supply voltage through a current source or a pullup resistor. The data is clocked into the MAX11261 from the SDA pin on the rising edge of SCL. Data is clocked out of the MAX11261 on the SDA pin on the falling edge of SCL. The SCL/SDA have an open-drain pad for wired-AND connection on the bus. Fast Mode Plus protocol is supported at maximum SCL clock rate of 1MHz. Each device on the I²C bus is recognized by a unique device address and can operate as a transmitter and a receiver. The interface is backward compatible with Standard mode and Fast mode.

Due to the variety of different devices (bipolar, CMOS, nMOS) that can be connected to the I²C bus, the input reference levels are set as 30% and 70% of V_{DVDD}. The data on the SDA line must be stable during the high period of SCL. The HIGH or LOW state of SDA can only change when SCL is LOW for a normal byte transfer except for START and STOP conditions.

All transactions begin with a START (S) and are terminated by a STOP (P). A high-to-low transaction on the SDA line while SCL is high defines a START condition. A low-to-high transition on the SDA line while SCL is high defines a STOP condition. The START and STOP are always generated by the I²C master. Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted is unrestricted. Each byte must be followed by an acknowledge (ACK). Data is transferred with MSB first. The MAX11261 always sends out an ACK in response to the master's request for reading or writing data. If the MAX11261 receives a not acknowledge (NACK) from the master it will reset the I²C interface and wait for another START condition.

SCL (Serial Clock)

The SCL pin synchronizes data communication between the host device and the MAX11261. Data is latched into the MAX11261 on the rising edge of SCL and data is shifted out of the MAX11261 on the falling edge of SCL. The MAX11261 does not support SCL clock stretching.

SDA (Serial Data Input/Output)

The SDA line is considered an input when the master is transmitting the data to the MAX11261. The SDA line will be used as an output when the MAX11261 has data to be sent onto the I2C bus during a register read by the host master. The slave in the MAX11261 implements mandatory requirements as specified in the I2C standard, which are detections of START and STOP conditions and support for ACK/NACK. This slave only supports 7-bit addressing and does not support general call address.

RDYB_INTB (Data Ready and Interrupt)

In sequencer modes 1, 2, and 3, RDYB_INTB indicates the ADC conversion status and the availability of the conversion result. When RDYB_INTB is low, a conversion result is available. When RDYB_INTB is high, a conversion is in progress and the data for the current conversion is not available. RDYB_INTB is driven high after a complete FIFO read. RDYB_INTB resets to high four master clock cycles prior to the next FIFO register update.

If data was read, then RDYB_INTB transitions from high to low at the output data rate. If the previous data was not read, the RDYB_INTB transitions from low to high for four master clock cycles and then transitions from high to low. In continuous mode, RDYB_INTB remains high for the first four conversion results and on the 5th result, RDYB_INTB goes low.

For sequencer mode 2 and sequencer mode 3 the RDYB_INTB behavior for a multichannel conversion can be controlled by the SEQ:RDYBEN bit. The default value of SEQ:RDYBEN is ‘0’. When set to ‘0’, RDYB_INTB for a multichannel conversion behaves the same as a single-channel operation. The RDYB_INTB toggles high to low after each channel is ready to update its corresponding data register. After the channel data is read, the RDYB_ INTB will reset back to ‘1’. If the channel data is not read and the next channel is ready to update its data, the RDYB_INTB will toggle low to high four cycles before the data update (similar to a single-channel case), and then toggle high to low indicating the new channel’s conversion data is available. If ‘N’ channels are enabled, RDYB_INTB will toggle high to low ‘N’ times. If SEQ:RDYBEN is set to ‘1’, the RDYB_INTB event for each channel is suppressed. The RDYB_INTB toggles high to low when the last channel is ready to update its corresponding data register and a single high-to-low transition happens.

In sequencer modes 1, 2, and 3, RDYB_INTB is also ORing the FIFO usage interrupt outputs.

RDYB_INTB is used as an interrupt in sequencer mode 4, so it has no significance in terms of indicating data availability when operating in sequencer mode 4.

The STAT:SRDY[5:0] bits get set to ‘1’ when their corresponding channel finishes converting irrespective of the RDYBEN setting for sequencer modes 2, 3, and 4. The conversion status is available by reading STAT:MSTAT bit. This stays high as long as the modulator is converting.

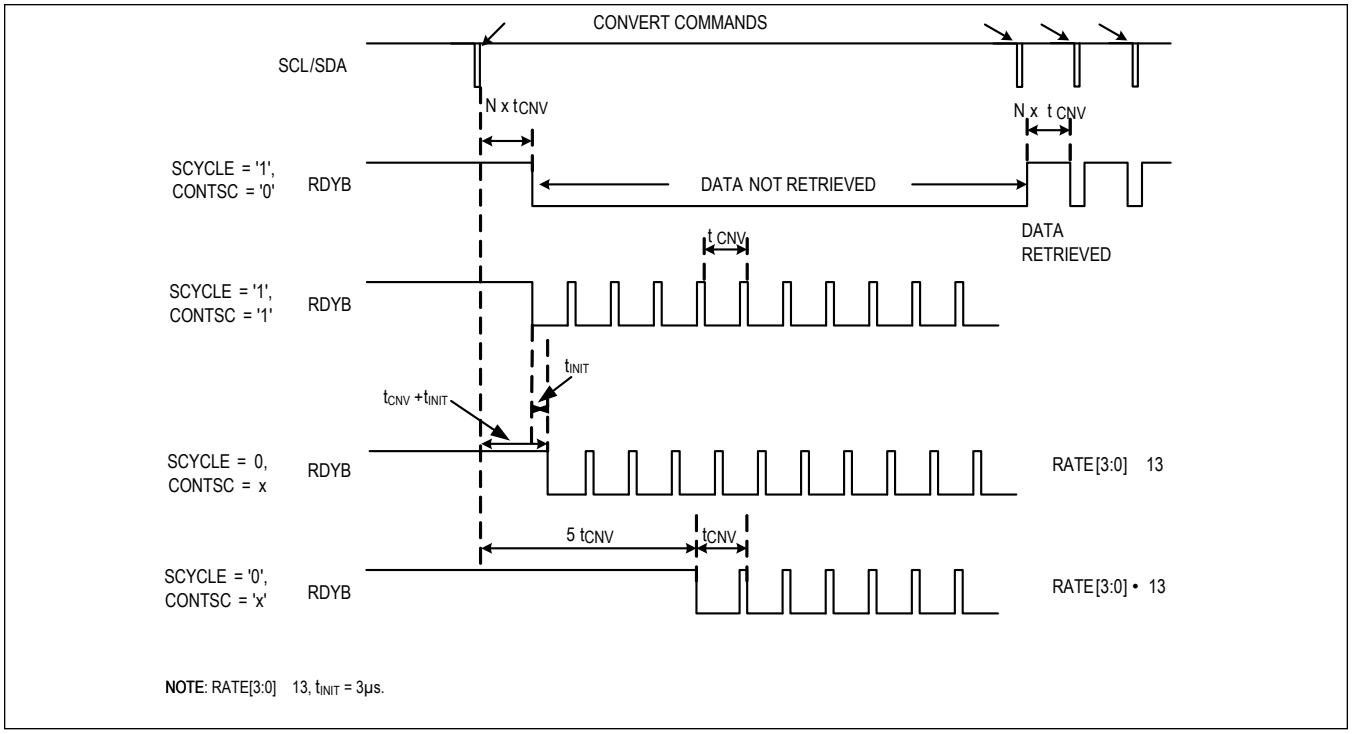


Figure 4. RDYB

I2C Sequence

The master needs to send out the first byte with a valid device address. The last bit of the first byte is a R/$\overline{W}$ bit and the master needs to send a '0' in this bit. The device will ignore a '1' sent in this bit. This is followed by a COMMAND byte for the MAX11261 as described in the command structure. The MAX11261 then responds to the command request depending on the MODE bit in the command.

Writing a Command to the MAX11261 for Conversion/Calibration/Power-Down

1. I2C START.
2. I2C WRITE.
   a. Send Device Address with a '0' in bit 8 indicating that the master will send a command byte followed by the device address. (8'b011xxxx_0)
   b. Check ACK.
   c. Send a command byte to convert/power down/calibrate. (8'b10_01_xxxx)
   d. Check ACK.
3. I2C STOP.

Sequence to Execute I2C Write Operation

1. I2C START.
2. I2C WRITE.
   a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address. (8'b011xxxx_0)
   b. Check ACK.
   c. Send a command byte to the Write registers. (8'b11_reg_addr[4:0]_0)
   d. Check ACK.

   e. Send the 8-bit register data MSB first.
   f. Check ACK.
   g. Check ACK.
3. I2C STOP.

Sequence to Execute I2C Read Operation

1. I2C START.
2. I2C WRITE.
   a. Send Device Address with a '0' in bit 8 indicating that the master will send a command byte followed by the device address. (8'b011xxxx_0)
   b. Check ACK.
   c. Send a command byte to the Read registers (8'b11_reg_addr[4:0]_1)
   d. Check ACK.
3. I2C Repeat START.
4. I2C WRITE.
   a. Send Device Address with a '1' in bit 8 indicating that the master will read the register data out.
   b. Check ACK.
5. I2C READa. Receive 8 bits of data.
   a. Send ACK.
   b. Receive 8 bits of data.
   c. Send NACK.
6. I2C STOP.

I2C Timing Characteristics

The I2C timing diagram is shown in Figure 1. The bus timing requirements are specified in I2C Timing Requirements table. The data is sampled on the positive edge of SCL and launched on negative edge of SCL for ACK and DATA reads. This gives a sufficient hold time for the master to sample the data.

I2C Device Addressing Scheme

The I2C slave has a 7-bit long device address. The device address is followed by a R/$\overline{W}$ bit which is low for a write command and high for a read command.

The first three most significant bits of the device address are always 011. Slave address bits A[4:1] correspond by the matrix in Table 4 to the states of the device address bumps AD0 and AD1.

The AD0 and AD1 bumps can be connected to any of the three signals: DGND, DVDD, and SDA giving three possible addresses for each bump allowing up to nine devices connected to the bus (see Figure 5).

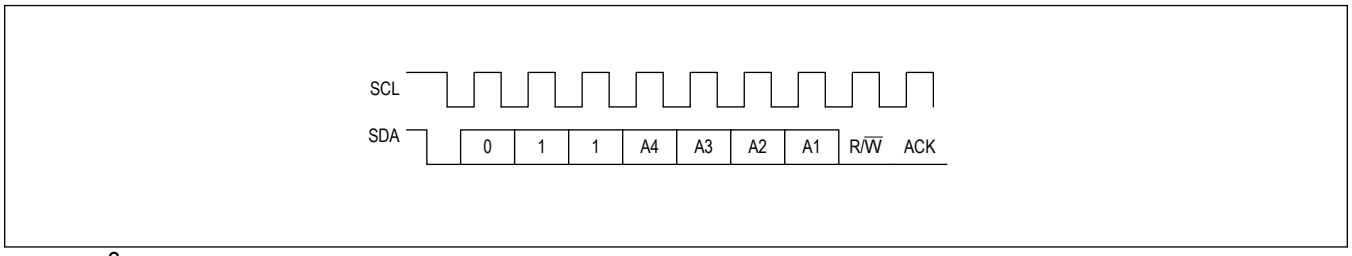


Figure 5. I2C Slave Address

Table 4. I²C Device Address Mapping (up to 9 Devices Selected on the I²C Bus Using the Following Addressing Scheme; I²C Addresses Are Not Contiguous)

ADDRESS PINS		DEVICE ADDRESS							
ADR1	ADR0	A7	A6	A5	A4	A3	A2	A1	A0
DGND	DGND	0	1	1	0	0	0	0	R/$\overline{W}$
DGND	DVDD				0	0	0	1	R/$\overline{W}$
DGND	SDA				0	0	1	1	R/$\overline{W}$
DVDD	DGND				0	1	0	0	R/$\overline{W}$
DVDD	DVDD				0	1	0	1	R/$\overline{W}$
DVDD	SDA				0	1	1	1	R/$\overline{W}$
SDA	DGND				1	1	0	0	R/$\overline{W}$
SDA	DVDD				1	1	0	1	R/$\overline{W}$
SDA	SDA				1	1	1	1	R/$\overline{W}$

Modes and Registers

The MAX11261 interface operates in two fundamental modes, either to issue a conversion command or to access registers. The mode of operation is selected by a command byte. Every I²C transaction to the MAX11261 starts with a command byte. The command byte begins with the MSB (B7) set to '1'. The next bit (B6) determines whether a conversion command is sent or register read/write access is requested.

Command Byte

The conversion command sets the mode of operation (conversion, calibration, or power-down), as well as the conversion speed of the MAX11261. The register read/write command specifies the register address, as well as the direction of the access (read or write).

Table 5. Command Byte Definition

	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
Conversion Command	1	0	MODE1	MODE0	RATE3	RATE2	RATE1	RATE0
Register Read/Write	1	1	RS4	RS3	RS2	RS1	RS0	R/$\overline{W}$

Table 6. Command Byte Decoding

BIT NAME	DESCRIPTION		
MODE[1:0]	The MODE bits are used to set the functional operation of the MAX11261 according to the following decoding.		
	MODE1	MODE0	DESCRIPTION
	0	0	Unused
	0	1	Power-down performed based on the CTRL1:PD[1:0] setting.
	1	0	Calibration performed based on the CTRL1:CAL[1:0] setting.
	1	1	Sequencer mode. The operation is based on the configuration of the SEQ register.
RATE[3:0]	These bits determine the conversion speed of the MAX11261. The decoding is shown in Table 1.		
RS[4:0]	Register address as shown in Table 9.		
R/$\overline{W}$	The R/$\overline{W}$ bit enables either a read or a write access to the address specified in RS[4:0]. If R/$\overline{W}$ is set to '0', then data is written to the register. If the bit is set to '1', then data is read from the register.		

Channel Sequencing

Changing SEQUENCER Modes

Mode Exit

(See Table 9.)

To exit any of the four sequencer modes, program the following sequence:

1. Issue a power-down command to exit the conversion process to STANDBY or SLEEP, as defined in CTRL1:PD[1:0]:a. Write a conversion command byte see Table 5.) and set MODE[1:0] of the command byte to '01'2) Wait for STAT:PDSTAT[1:0] = '01' (SLEEP) or STAT:PDSTAT[1:0]= '10' (STANDBY).

Note: In all sequencer modes, the default exit state is SLEEP with the following exceptions where the exit state is defined by CTRL1:PD[1:0]:

- Sequencer mode 1 continuous conversion (CTRL1:SCYCLE = '0')
- Sequencer mode 1 continuous single-cycle conversion (CTRL1:SCYCLE = '1' and CTRL1:CONTSC = '1')

Mode Change

To change sequencer modes or to update the SEQ register program the following sequence:

1. Perform Sequencer Mode Exit (see the *Mode Exit* section).
2. Set up the following registers: SEQ, CTRL1.
   a. Set SEQ:MODE[1:0] to select the new sequencer mode.
   b. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion.
3. Write the command byte (see Table 5).
   a. Set MODE[1:0] of command byte to "11" (sequencer mode).
4. Wait for STAT:PDSTAT[1:0] = "00" to confirm conversion mode.

SEQUENCER Mode 1—Single-Channel Conversion with GPO Control and MUX Delays

This mode is used for single-channel conversions where the sequencer is disabled. [[Sequence Mode 1 Timing Diagram]] illustrates the timing. To support high-impedance source networks, the conversion delay (SEQ:MDREN) feature must be enabled. The states of the GPO bumps are configured using the GPO_DIR registers and can be modified anytime during mode 1 operation. The values of the CHMAP0/CHMAP1 registers and DELAY:GPO[7:0] bits are ignored in this mode.

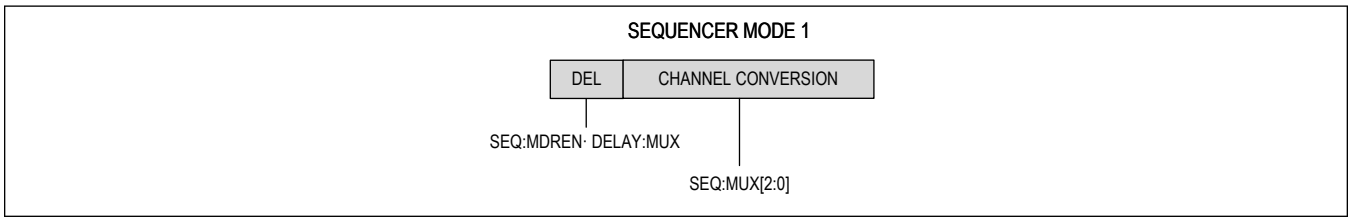


Figure 6. Sequencer Mode 1 Timing Diagram

Programming Sequence

Mode Entry

1. Set up the following registers: SEQ, DELAY, CTRL1, GPO_DIR.
   a. SEQ:MODE[1:0] = '00' for sequencer mode 1.
   b. SEQ:MUX[2:0] to select the channel for conversion.
   c. Enable SEQ:MDREN to delay conversion start to allow for input settling. Set DELAY:MUX[7:0] to the desired

conversion delay.

d. Set CTRL1:SCYCLE for either single-cycle (no latency) or continuous conversion.
e. If single-cycle conversion is selected, set CTRL1:CONTSC to ‘1’ if continuous single-cycle conversion is desired.
f. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to ‘01’ is issued during the conversion.
g. Set register GPO_DIR to enable or disable the desired GPO bumps.

2. Write a conversion command (see Table 5).
   a. Set the data rate using bits RATE[3:0] of the command byte.
   b. Set MODE[1:0] of the command byte to ‘11’ for sequencer mode.
3. Monitor RDYB_INTB for availability of conversion results in the FIFO register (see Figure 4 for RDYB timing).

Mode Exit

1. In single-cycle conversion mode (CTRL1:SCYCLE = ’1’) the sequencer exits into SLEEP state.
2. In continuous conversion mode (CTRL1: SCYCLE = ’0’ or (CTRL:SCYCLE = ’1’ and CTRL1:CONTSC = ’1’)), conversions continue nonstop until the mode is exited. To interrupt and exit continuous conversion or continuous single-cycle conversion, follow the *Changing SEQUENCER Modes - Mode Exit* section to put the part into STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1f of the *Mode Entry* section.

Changing Input Channel During Continuous Single-Cycle Conversion in Mode 1

1. Issue a conversion command with MODE[1:0] set to ‘01’ to exit the conversion process to STANDBY or SLEEP state (see the *Changing SEQUENCER Modes - Mode Exit* section).
2. Monitor STAT:PDSTAT = ‘10’ or ‘01’ to confirm exit to STANDBY or SLEEP state.
3. Set SEQ:MUX[2:0] to select the new channel for conversion.
4. Write a conversion command (see Table 5) and set MODE[1:0] of the command byte to ‘11’.

SEQUENCER Mode 2 – Multichannel Scan with GPO Control and MUX Delays

This mode is used to sequentially convert a programmed set of channels in a preset order. Figure 7 illustrates the timing.

The states of the GPO bumps are configured using the GPO_DIR register and can be modified anytime during mode 2 operation. In mode 2, register bits CHMAP0:CHn_ ORD[2:0], CHMAP1:CHn_ORD[2:0], CHMAP0:CHn_EN, and CHMAP1:CHn_EN are used to select channels and conversion order. Bits DELAY:GPO[7:0], CHMAP0:CHn_ GPO[2:0], CHMAP0:CHn_GPOEN, CHMAP1:CHn_ GPO[2:0], and CHMAP1:CHn_GPOEN are ignored in this mode. The bit CTRL1:CONTSC is ignored and bit CTRL1:SCYCLE = ‘0’ is invalid in this mode.

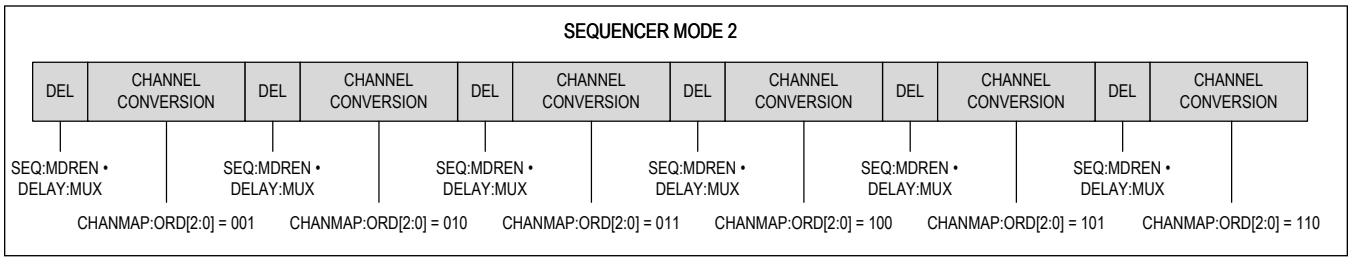


Figure 7. Sequencer Mode 2 Timing Diagram

Programming Sequence

Mode Entry

1. Set up the following registers: SEQ, CHMAP0, CHMAP1, DELAY, GPO_DIR, CTRL1.
   a. SEQ:MODE[1:0] = ‘01’ for sequencer mode 2.
   b. If desired, set SEQ:RDYBEN to ‘1’ to signal data ready only when all channel conversions are completed.
   c. Enable SEQ:MDREN to delay conversion start to allow for input settling. Set DELAY:MUX[7:0] to the desired

conversion delay.

d. Set CHMAP0 and CHMAP1 to select the channels and channel order for conversion.
e. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion.
f. Set register GPO_DIR to enable or disable the desired GPO bumps.
g. Set CTRL1:SCYCLE = '1' for single-cycle conversion mode.

2. Write a conversion command (see Table 5).
   a. Set the data rate using bits RATE[3:0] of the command byte.
   b. Set MODE[1:0] of the command byte to '11'.
3. Monitor RDYB_INTB (if SEQ:RDYBEN = '0') and bits STAT:SRDY[5:0] for availability of per channel conversion results in FIFO registers.

Mode Exit

1. This mode exits to SLEEP state upon completion of sequencing all channels.
2. To interrupt current sequencing perform mode exit, see the *Changing SEQUENCER Modes—Mode Exit* section. This device is put in STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1e of the *Mode Entry* section.

SEQUENCER Mode 3 – Scan, with Sequenced GPO Controls

This mode is used to sequentially convert a programmed set of channels in a preset order and sequence the GPO bumps concurrently. The GPO bumps are used to bias external circuitry such as bridge sensors; the common reference (GPOGND) is typically ground. After all channel conversions have completed, the MAX11261 automatically powers down into SLEEP mode. Figure 8 illustrates the sequencer mode 3 timing diagram for a 3-channel scan. Register GPO_DIR is ignored in this mode, as the output controls are controlled by the sequencer.

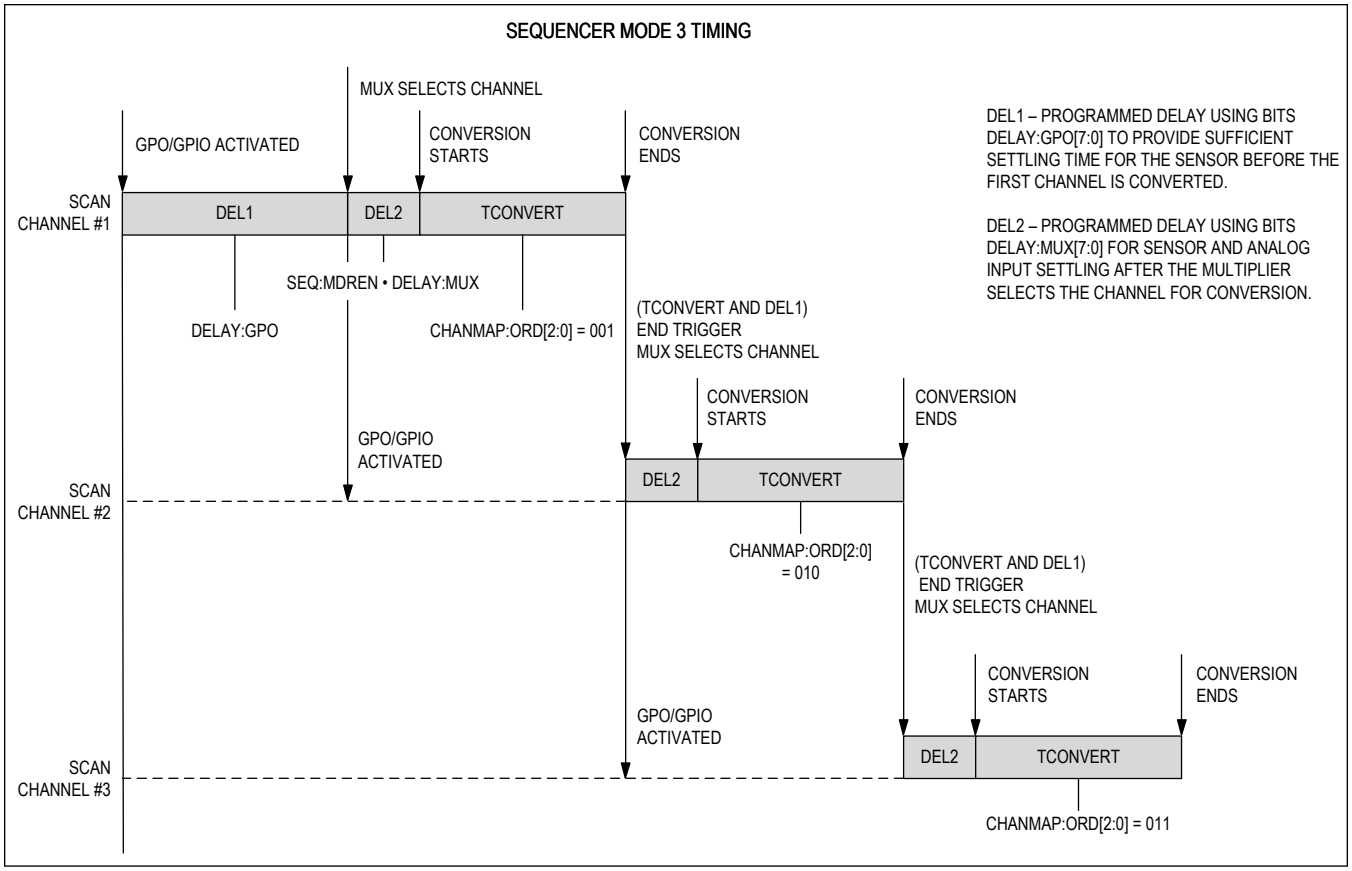


Figure 8. Sequencer Mode 3 Timing Diagram for a 3-Channel Scan

Programming Sequence

Mode Entry

1. Set up the following registers: SEQ, CHMAP0, CHMAP1, DELAY, CTRL1, CTRL3.
   a. SEQ:MODE[1:0] = ”10” for sequencer mode 3.
   b. If desired, set SEQ:RDYBEN to ‘1’ to signal data ready only when all channel conversions are completed.
   c. Enable SEQ:MDREN if conversion start is to be delayed to allow for input settling. Set DELAY:MUX[7:0] to the desired conversion delay.
   d. Set CHMAP0 and CHMAP1 to enable the channels for conversion and the channel conversion order. Map the corresponding GPO bumps to a channel.
   e. Enable SEQ:OCDREN for adding a delay before the multiplexer selects this channel for conversion. Set DELAY:GPO to a delay value sufficient for the bias to settle.
   f. Set CTRL1:PD[1:0] to STANDBY or SLEEP state (desired exit state if an IMPD command is issued during the conversion).
   g. Set CTRL1:SCYCLE = ‘1’ for single conversion mode.
2. Write the command byte (see Table 5).
   a. Set the data rate using bits RATE[3:0] of the command byte.
   b. Set MODE[1:0] of command byte to “11”.
3. Monitor RDYB_INTB (if SEQ:RDYBEN = ‘0’) and bits STAT:SRDY[5:0] for availability of per-channel conversion results in FIFO registers.

Mode Exit

1. This mode exits to SLEEP state upon completion of sequencing all channels and output controls.
2. To interrupt current sequencing, perform mode exit. See the *Changing SEQUENCER Modes - Mode Exit* section. The device is put in STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1) of the *Mode Entry* section.

The bit CTRL1:CONTSC is ignored and bit CTRL1:SCYCLE = ‘0’ is invalid in this mode.

SEQUENCER Mode 4 – Autoscan with GPO Controls (CHMAP) and Interrupt

This mode features a programmable timer to wake the MAX11261 from SLEEP and power down the MAX11261 between operations.

The MAX11261 automatically cycles through a sequence of delay, power-up, operate the GPO, scan selected channels, perform math operations, and power-down into SLEEP state. See Figure 9.

The duty cycle is programmed by DELAY:AUTOSCAN[7:0]. The programmed value must be greater than “0x00”, otherwise power-down is skipped and followed immediately by another scan cycle. This sequence continues until the conversion is halted. The autoscan delay is from 4ms to 1024ms.

To generate SYNC signals for other slave devices, the master must configure AUTOSCAN[7:0] greater than “0x00”, otherwise the SYNC signal cannot be generated.

In this mode, a register INT_STAT read will clear RDYB_ INTB if the FIFO usage interrupts are not triggered. If any of the FIFO usage interrupts is triggered, RDYB_INTB will keep asserted. The user can disable the FIFO usage interrupts to allow only the input comparison to generate interrupts.

The behavior of the RDYB_INTB pin ignores the SEQ:RDYBEN bit.

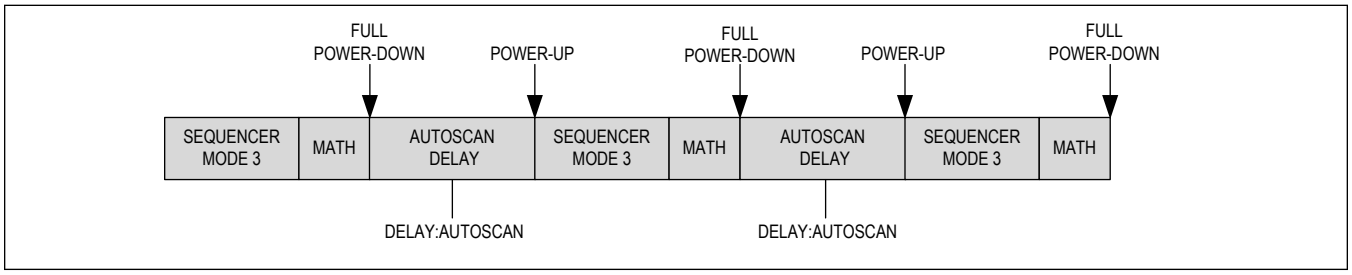


Figure 9. Sequencer Mode 4 Timing Diagram

The GPOs are operated by the sequencer and programmed by CHMAPx registers. GPO_DIR register is ignored in this mode. A DELAY:GPO[7:0] value of ‘0x00’ represents no delay. This mode also utilizes the channel MUX delay if enabled by setting the SEQ:MDREN bit to ‘1’. The value programmed into the DELAY:MUX[7:0] register will be used to delay the start of the conversion after selecting the channel. If the CTRL1:CONTSC bit is ‘1’, it is ignored in this mode. CTRL1:SCYCLE bit of ‘0’ is invalid in this mode.

Math Operation: Conversion Result Processing and Out-Of-Range (OOR) Bit Generation

There are three options to process the conversion results to detect if a channel input signal is changing. They are controlled by the HPF:CMP_MODE[1:0] register. The conversion result processing is shown in Figure 10.

In the following section, n indicates the channel number, N indicates a specific sample, and N-1 indicates the previous sample of the same channel.

1. CMP_MODE[1:0] = 0b00. Compare the current result DATAn(N) with the user-programmable low limit (LIMIT_LOWn) and the high limit (LIMIT_HIGHn). If the conversion result is within LIMIT_LOWn and LIMIT_HIGHn, there is no OOR generated. Otherwise, an OOR is generated.
2. CMP_MODE[1:0] = 0b01. Subtract the current result DATAn(N) by the previous result DATAn(N-1). Then compare the resultant with the user-programmable low limit (LIMIT_LOWn) and the high limit (LIMIT_ HIGHn). If the resultant is within LIMIT_LOWn and LIMIT_HIGHn, there is no OOR generated. Otherwise an OOR is generated. After writing

HPF register with HPF:CMP_MODE[1:0] = 0b01, the comparator is initialized and the first conversion does not detect the OOR condition.

3. CMP_MODE[1:0] = 0b10. This option enables the highpass digital filter, generating a highpass filter output based on the user-programmable cutoff frequency register HPF:FREQUENCY[2:0]. Compare the HPF output with the user-programmable low limit (LIMIT_LOWn) and the high limit (LIMIT_HIGHn). If the HPF output is within LIMIT_LOWn and LIMIT_HIGHn, there is no OOR generated. Otherwise an OOR is generated. Writing to the HPF register with HPF:CMP_MODE[1:0] = 0b10 resets the highpass filter. The highpass filter cutoff frequency is calculated as shown in Table 7.
4. CMP_MODE[1:0] = 0b11 is reserved.

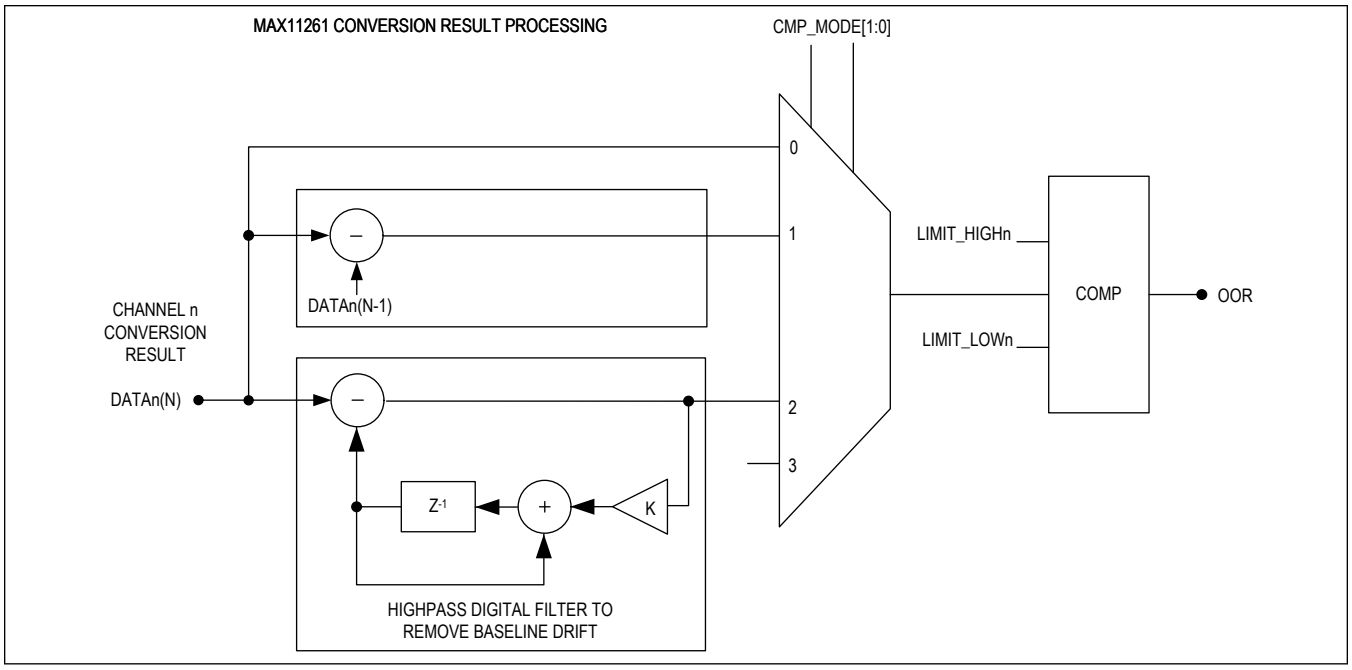


Figure 10. Conversion Result Math Operation

Table 7. HPF Cutoff Frequency vs. HPF:FREQUENCY[2:0] Register Values

HPF:FREQUENCY[2:0]	CUTOFF FREQUENCY (Hz)
0	Scan Rate/39.0625
1	Scan Rate/78.125
2	Scan Rate/156.25
3	Scan Rate/312.5
4	Scan Rate/625
5	Scan Rate/1250
6	Scan Rate/2500
7	Scan Rate/5000

Unipolar Mode Not Supported

The math operations performed in this mode prevent using unipolar ranges. Only bipolar ranges and two's complement numbers are used. The LIMIT_LOWn, LIMIT_HIGHn registers are bipolar two's complement values.

Programming Sequence

Mode Entry

1. Set up the following registers: SEQ, CHMAP0, CHMAP1, DELAY.
   a. SEQ:MODE[1:0] = ”11” for sequencer mode 4.
   b. Enable SEQ:MDREN if conversion start is to be delayed to allow for input settling. Write to DELAY:MUX[7:0] to set conversion delay.
   c. Set HPF:MODE[1:0], LIMIT_LOWn, and LIMIT_ HIGHn registers to desired values.
   d. Set CHMAP0 and CHMAP1 to enable the channels for conversion and the channel conversion order. Map the GPO bump to a channel and enable it for the conversion process.
   e. Enable SEQ:GPODREN for adding a delay (DEL1) before the multiplexer selects the first channel for conversion. See [[Sequencer Mode 3 Timing Diagram for a Three-Channel Scan]] for timing. Set DELAY:GPO to a delay value sufficient for the bias to settle.
   f. Set CTRL1:PD[1:0] to STANDBY or SLEEP state (desired exit state if an IMPD command is issued during the conversion).
   g. Set CTRL1:SCYCLE = ‘1’ for single-conversion mode.
2. Write the command byte (see Table 5).
   a. Set the data rate using bits RATE[3:0] of the command byte.
   b. Set MODE[1:0] of the command byte to “11”.
3. This mode is perpetual; monitor interrupt signal RDYB_INTB for different interrupt requests.
   a. Per-channel conversion data ready is available by reading bits STAT:SRDY[5:0] for analog input channel 5 to channel 0.
   b. Do not overwrite SEQ:MODE[1:0] during mode 4 operation. Write new SEQ:MODE[1:0] during mode exit; see *Mode Exit* steps 1a and 1b.

Mode Exit

1. To exit to another sequencer mode:
   a. Write SEQ:MODE[1:0] to the desired sequencer mode.
   b. Issue a conversion command.
2. To exit to STANDBY or SLEEP state:
   a. Follow the *Changing SEQUENCER Modes—Mode Exit* section to STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1f of the *Mode Entry* section.

AUTOSCAN Delay

Program delay using bits DELAY:AUTOSCAN[7:0] for selecting the scan rate. This is a power-saving feature for throttling system power consumption. During the autoscan delay period, the MAX11261 is powered down and woken up automatically.

Supplies and Power-On Sequence

The MAX11261 requires two power supplies, AVDD and DVDD. These power supplies can be sequenced in any order. The analog supply (AVDD) powers the analog inputs and the modulator. The DVDD supply powers the I2C interface. The low-voltage core logic can either be powered by the integrated LDO (default) or through DVDD. Figure 11 shows the two possible schemes. CAPREG denotes the internally generated supply voltage. If the LDO is used, the DVDD operating voltage range is from 2.0V to 3.6V. If the core logic is directly powered by DVDD (DVDD and CAPREG connected together), the DVDD operating voltage range is from 1.7V to 2.0V.

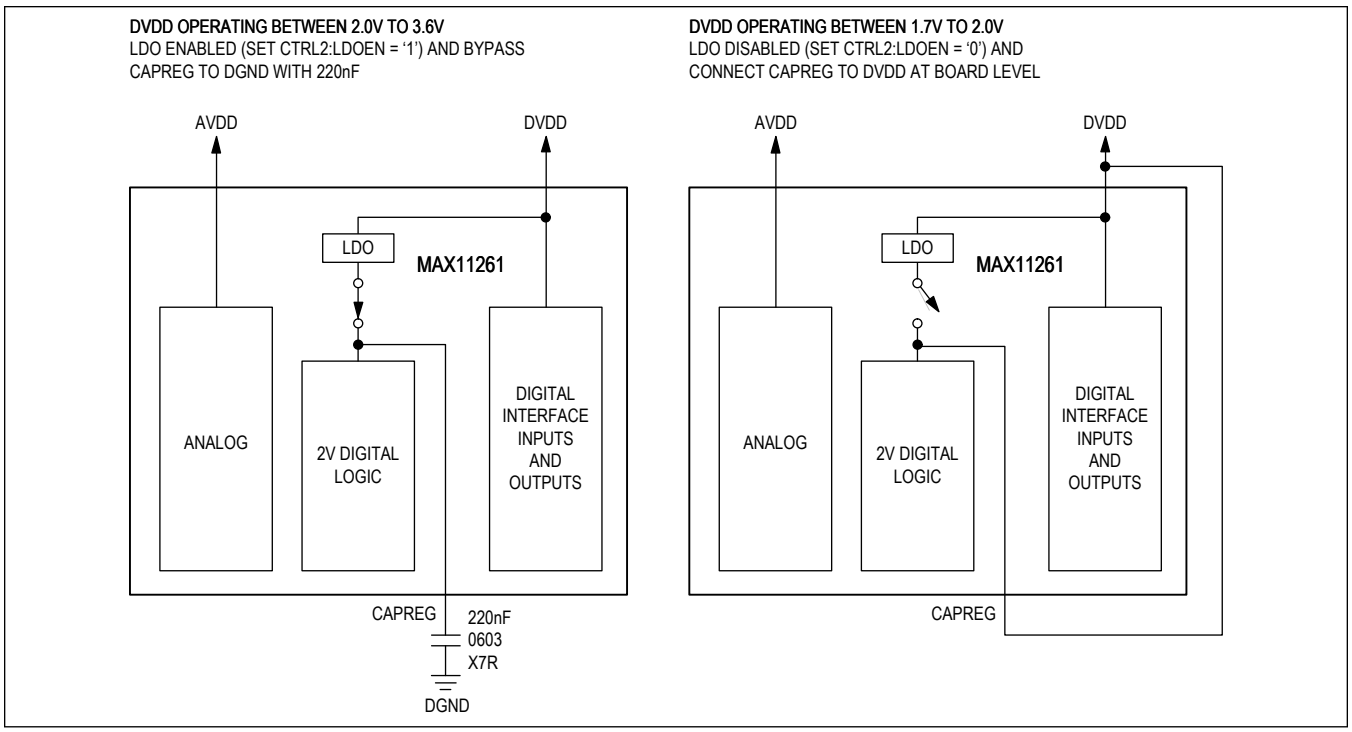


Figure 11. Digital Power Architecture

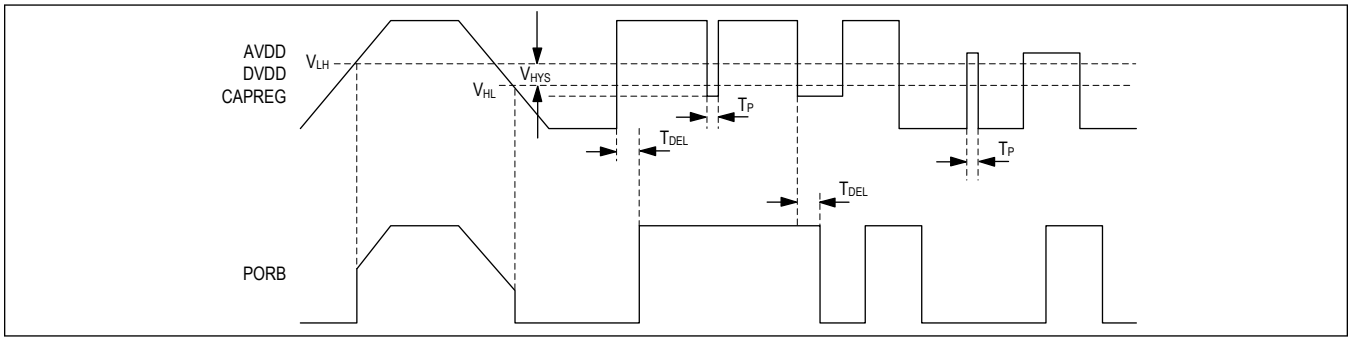


Figure 12. Undervoltage Lockout Characteristic Voltage Levels and Timing

Power-On Reset and Undervoltage Lockout

A global power-on reset (POR) is triggered until AVDD, DVDD, and CAPREG cross a minimum threshold voltage (V_{LH}), as shown in Figure 12.

To prevent ambiguous power-supply conditions from causing erratic behavior, voltage detectors monitor AVDD, DVDD, and CAPREG and hold the MAX11261 in reset when supplies fall below V_{HL} (see Figure 12). The analog undervoltage lockout (AVDD UVLO) prevents the ADC from converting when AVDD falls below V_{HL}. The CAPREG UVLO resets and prevents the low-voltage digital logic from operating at voltages below V_{HL}. DVDD UVLO thresholds supersede CAPREG thresholds when CAPREG is externally driven. Figure 13 shows a flow diagram of the POR sequence. Glitches on supplies AVDD, DVDD, and CAPREG for durations shorter than T_P are suppressed without triggering POR or UVLO. For glitch durations longer than T_P, POR is triggered within T_{DEL} seconds. See the *Electrical Characteristics* table for values of V_{LH}, V_{HL}, T_P, and T_{DEL}.

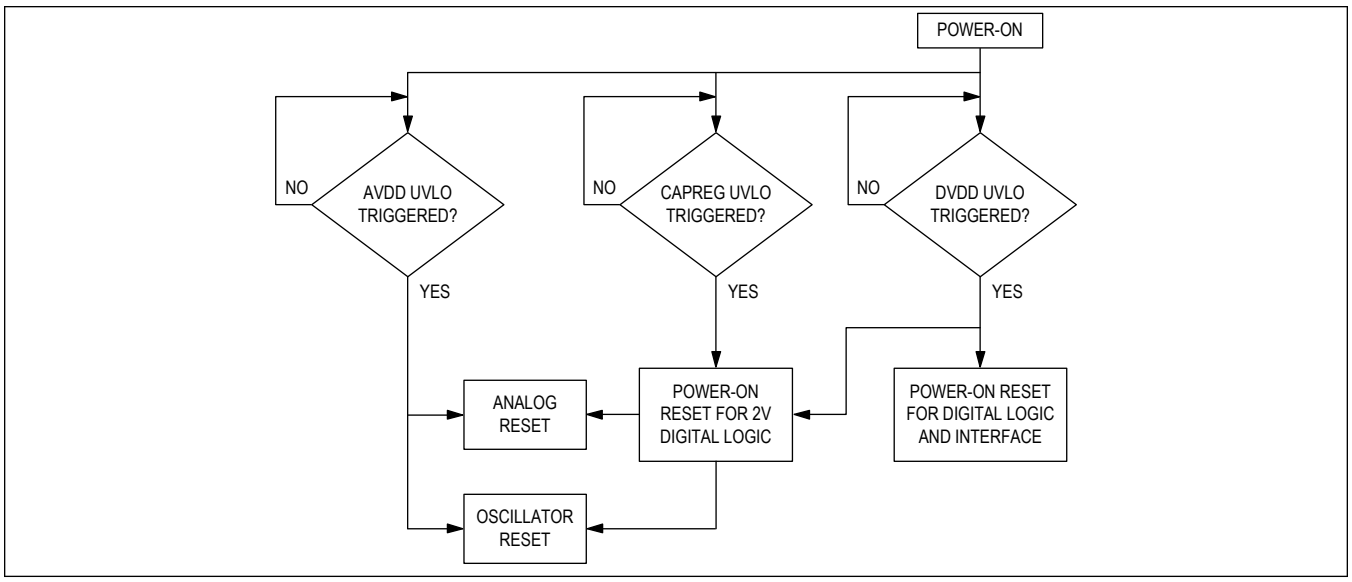


Figure 13. MAX11261 UVLO and POR Flow Diagram

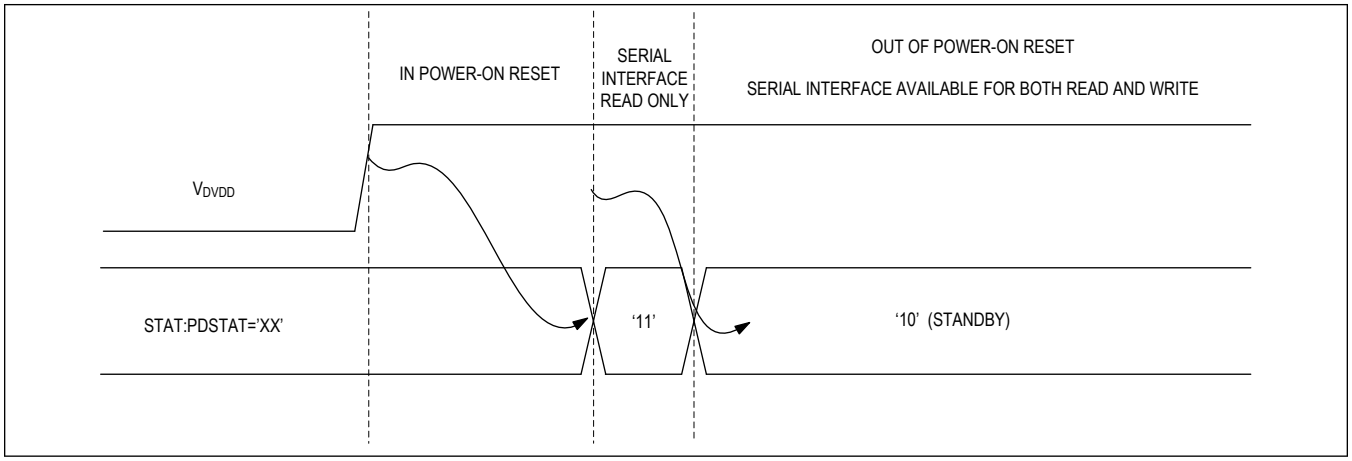


Figure 14. Power-On Reset and PDSTAT Timing

Power-On-Reset Timing

Power-on reset is triggered during power-up and undervoltage conditions as described above. Completion of the POR process is monitored by polling STAT:PDSTAT[1:0] = '10' for STANDBY state (see Figure 14).

Reset

Hardware Reset Using RSTB

The MAX11261 features an active-low RSTB bump to perform a hardware reset. Pulling the RSTB bump low stops any conversion in progress, reconfigures the internal registers to the power-on reset state and resets all digital filter states to zero. After the reset cycle is completed, the MAX11261 remains in STANDBY state and awaits further commands.

Software Reset

The host can issue a software reset to restore the default state of the MAX11261. A software reset sets the interface registers back into their default states and resets the internal state machines. However, a software reset does not emulate

the complete POR or hardware reset sequence.

Two I2C transactions are required to issue a software reset: First set CTRL1:PD[1:0] to '11' (RESET). Then issue a conversion command with MODE[1:0] set to '01'. To confirm the completion of the reset operation, STAT:PDSTAT and STAT:INRESET must be monitored.

Table 8. Maximum Delay Time for Mode Transitions

COMMAND ISSUED	CHIP STATE BEFORE COMMAND	COMMAND INTERPRETATION	MAXIMUM DELAY TIME TO NEXT STATE†	CHIP STATE AFTER COMMAND
SLEEP	RESET	Command ignored	0	RESET
	SLEEP	Command ignored	0	SLEEP
	STANDBY	Chip powers down into a leakage-only state	20ms	SLEEP
	STANDBY (fast)***	Issue a conversion command and then monitor STAT:PDSTAT[1:0] for change of mode then send IMPD command	15µs	SLEEP
	Calibration	Calibration stops, chip powers down into a leakage-only state	3µs	SLEEP
	Conversion	Conversion stops, chip powers down into a leakage-only state	3µs	SLEEP
	Mode 4 convert**	LDO wake-up and overhead	$T_{PUPSLP*}$ + 3µs	SLEEP
CONVERT	SLEEP	Mode change from SLEEP to conversion From conversion command to PDSTAT="00"	$T_{PUPSLP*}$ + 3µs	CONVERT
	STANDBY	STANDBY to conversion	$T_{PUPSBY*}$ + 3µs	CONVERT
STANDBY	RESET	Command ignored	0	RESET
	SLEEP	SLEEP to STANDBY	20ms	STANDBY
	SLEEP (fast)***	Mode change from SLEEP to STANDBY through conversion operation. The delay includes SLEEP state power-up time (TPUPSLP*) and switching time from slow standby clock to high-speed MCLK.	85µs	STANDBY
	STANDBY	Command ignored	0	STANDBY
	Calibration	Calibration stops	3µs	STANDBY
	Conversion	Conversion stops	3µs	STANDBY
	Mode 4 SLEEP**	LDO wake-up and overhead	$T_{PUPSLP*}$ + 3µs	STANDBY
RESET	RESET	Command ignored	0	RESET
	SLEEP	Command ignored	0	SLEEP
	STANDBY	Register values reset to default	28ms	STANDBY
	Calibration	Calibration stops, register values reset to default	6µs	STANDBY
	Conversion	Conversion stops, register values reset to default	6µs	STANDBY
POR	OFF	From complete power-down to STANDBY state	10ms	STANDBY
RSTB	Any	From any state to STANDBY mode	10ms	STANDBY

†Guaranteed by design.

*See the *Electrical Characteristics* table.

**During wake-up transition switching between SLEEP and CONVERT states.

***Assume full active power during these state transitions.

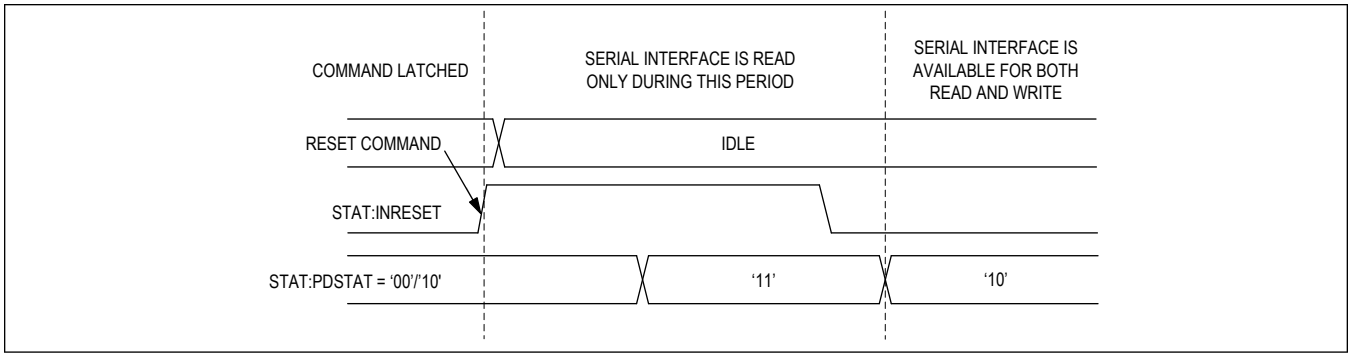


Figure 15. STAT:INRESET and STAT:PDSTAT Timing

Figure 15 shows the state transition for the RESET command and the relative timing of STAT register update. During reset, INRESET = '1' and PDSTAT= '11'. The I2C interface cannot be written until MAX11261 enters STANDBY state where PDSTAT = '10'. To confirm completion of the RESET command, monitor for INRESET = '0' and PDSTAT = '10'. Table 8 summarizes the maximum delay for reset operation.

The commands are defined as follows:

- SLEEP: Set CTRL1:PD[1:0] to '01'; issue a conversion command with MODE[1:0] set to '01'
- STANDBY: Set CTRL1:PD[1:0] to '10'; issue a conversion command with MODE[1:0] set to '01'
- RESET: Set CTRL1:PD[1:0] to '11'; issue a conversion command with MODE[1:0] set to '01'
- CONVERT: Any conversion command with MODE[1:0] set to '11'
- POR: Power-on reset during initial power-up or UVLO
- RSTB: Hardware reset with RSTB bump

Power-Down States

To reduce overall power consumption, the MAX11261 features two power-down states: STANDBY and SLEEP. In SLEEP mode all circuitry is powered down, and the supply currents are reduced to leakage currents. In STANDBY mode, the internal LDO and a low-frequency oscillator are powered up to enable fast startup. After POR or a hardware reset, the MAX11261 is in STANDBY mode until a command is issued.

Changing Power-Down States

Mode transition times are dependent on the current mode of operation. STAT:PDSTAT is updated at the end of all mode changes and is a confirmation of a completed transaction. The MAX11261 does not use a command FIFO or queue. The user must confirm the completed transaction by polling STAT:PDSTAT after the expected delay, as described in Table 8. Once the transition is complete, it is safe to send the next command. Verify that STAT:PDSTAT indicates the desired state before issuing a conversion command. Writes to any CTRL register during a conversion aborts the conversion and returns the MAX11261 to STANDBY state.

SLEEP STATE TO STANDBY STATE (FAST)

1. Set CTRL1:PD[1:0] = '10' for STANDBY state.
2. Set SEQ:MODE[1:0] = '00' for sequencer mode 1.
3. Issue a conversion command with MODE[1:0] set to '11'.
4. Monitor STAT:PDSTAT[1:0] = '00' for active state.
5. Write the conversion command with MODE[1:0] set to '01'.
6. Monitor STAT:PDSTAT = '10' for completion.

STANDBY STATE TO SLEEP STATE (FAST)

1. Set CTRL1:PD[1:0] = '01' for STANDBY state.
2. Set SEQ:MODE[1:0] = '00' for sequencer mode 1.
3. Issue a conversion command with MODE[1:0] set to 11'.

4. Monitor STAT:PDSTAT[1:0] = ‘00’ for active state.
5. Write the conversion command with MODE[1:0] set to 01’.
6. Monitor STAT:PDSTAT = ‘01’ for completion.

Calibration

Two types of calibration are available: self calibration and system calibration. Self calibration is used to reduce the MAX11261’s gain and offset errors during changing operating conditions such as supply voltages, ambient temperature, and time. System calibration is used to reduce the gain and offset error of the entire signal path. This enables calibration of board level components and the integrated PGA. System calibration requires the MAX11261’s inputs to be reconfigured for zero scale and full scale during calibration. The GPO bumps can be used for this purpose. See Figure 16 for details of the calibration signal flow.

The calibration coefficients are stored in the registers SCOC, SCGC, SOC, and SGC. Data written to these registers is stored within the I2C domain and copied to internal registers before a conversion starts to process the raw data (see Figure 16). An internal or system calibration only updates the internal register values and does not alter the contents stored in the I2C domain. The bit CTRL3:CALREGSEL decides whether the internal contents or the contents stored in the I2C domain are read back during a read access of these registers.

Bits NOSCO, NOSCG, NOSYSO, NOSYSG enable or disable the use of the individual calibration coefficients during data processing. See Figure 16.

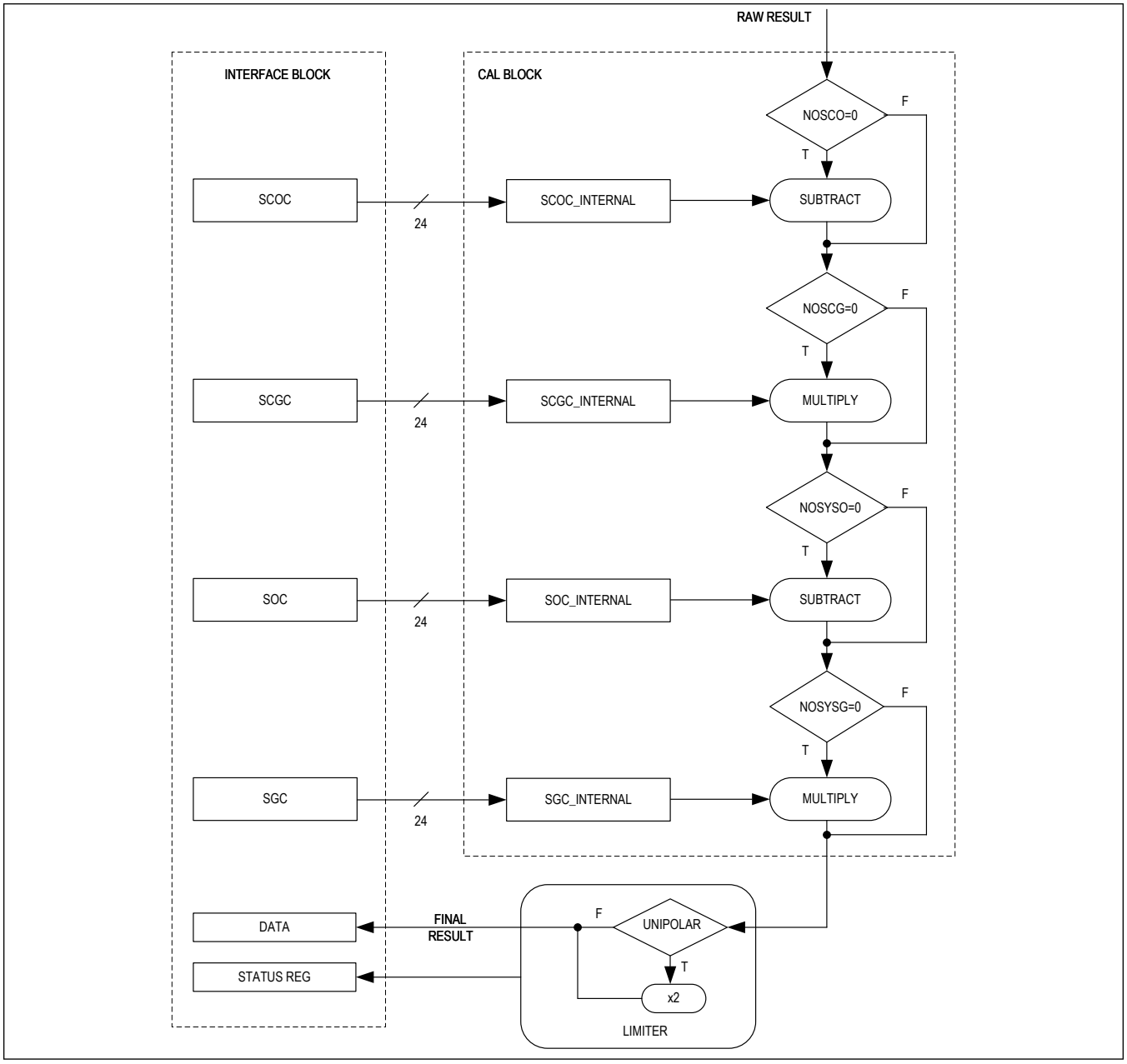


Figure 16. Calibration Flow Diagram

Self-Calibration

The self-calibration is an internal operation and does not disturb the analog inputs. The self-calibration command can only be issued with the sequencer in mode 1 (SEQ:MODE[1:0] = “00”). Self-calibration is accomplished in two independent phases, offset, and gain. The first phase disconnects the inputs to the modulator and shorts them together internally to develop a zero-scale signal. A conversion is then completed and the results are post-processed to generate an offset coefficient which cancels all internally generated offsets. The second phase connects the inputs to the reference to develop a full-scale signal. A conversion is then completed and the results are post-processed to generate a full-scale coefficient, which scales the converters full-scale analog range to the full-scale digital range.

The entire self-calibration sequence requires two independent conversions, one for offset and one for full scale. The conversion rate is 50sps in the single-cycle mode. This rate provides the lowest noise and most accurate calibrations.

The self-calibration operation excludes the PGA. A system-level calibration is available in order to calibrate the PGA signal path.

System Calibration

This mode is used when calibration of board level components and the integrated PGA is required. The system calibration command is only available in sequencer mode 1. A system calibration requires the input to be configured to the proper level for calibration. The offset and full-scale system calibrations are, therefore, performed using separate commands. The channel selected in the SEQ:MUX bits is used for system calibrations.

To perform a system offset calibration, the inputs must be configured for zero scale. The inputs do not necessarily need to be shorted to 0V as any voltage within the range of the calibration registers can be nulled in this calibration.

A system offset calibration is started as follows: Set CTRL1:CAL[1:0] to '01' (system offset calibration). Then issue a conversion command with the MODE[1:0] bits set to '10' (calibration). The system offset calibration requires 100ms to complete.

To perform a system full-scale calibration, the inputs must be configured for full scale. The input full-scale value does not necessarily need to be equal to V_{REF} since the input voltage range of the calibration registers can scale up or down appropriately within the range of the calibration registers.

A system full-scale calibration is started as follows: Set CTRL1:CAL[1:0] to '10' (system full-scale calibration). Then issue a conversion command with the MODE[1:0] bits set to '10' (calibration). The system full-scale calibration requires 100ms to complete. The GPO bumps can be used during a system calibration.

All four calibration registers (SOC, SGC, SCOC, and SCGC) can be written by the host to store special calibration values. The new values will be copied to the internal registers at the beginning of a new conversion.

Components of the ADC

Modulator

MODULATOR DIGITAL OVERRANGE

The output of the SINC filter is monitored for overflow. When SINC filter overflow is detected, the STAT:DOR bit is set to '1' and a default value is loaded into the FIFO register depending on the polarity of the overload. A positive overrange causes 0x7FFFFF to be written to the FIFO register. A negative overrange causes 0x800000 to be written to the FIFO register. See Table 9.

MODULATOR ANALOG OVERRANGE

The modulator analog overrange is used to signal the user that the input analog voltage has exceeded preset limits defined by the modulator operating range. These limits are approximately 120% of the applied reference voltage. When analog overrange is detected, the STAT:AOR bit is set to '1' after FIFO is updated. The AOR bit will always correspond to the current value in the FIFO register. See Table 9.

The DATA values shown are for bipolar ranges with two's complement number format. V_{OVRRNG} is the overrange voltage value typically > 120% of V_{REF}.

Table 9. Analog Overrange Behavior for Different Operating Conditions and Modes

	STAT REGISTER		
INPUT VOLTAGE	**AOR**	**DOR**	**DATA**
$-V_{REF} < V_{IN} < V_{REF}$	0	0	RESULT
$V_{REF} < V_{IN} < V_{OVRRNG}$	1	0	RESULT
$-V_{OVRRNG} < V_{IN} < -V_{REF}$	1	0	RESULT
$V_{IN} > V_{OVRRNG}$	1	1	0x7FFFFF

Table 9. Analog Overrange Behavior for Different Operating Conditions and Modes (continued)

	STAT REGISTER		
$V_{IN} < -V_{OVRRNG}$	1	1	0x800000

SINC Filter

The digital filter is a mode-configurable digital filter and decimator that processes the data stream from the fourth-order delta-sigma modulator and implements a fifth-order SINC function with an averaging function to produce a 24-bit wide data stream.

The SINC filter allows the MAX11261 to achieve very high SNR. The bandwidth of the fifth-order SINC filter is approximately twenty percent of the data rate. See Figure 17 and Figure 18 for the filter response of 12.8ksps and 4ksps, respectively. See Figure 19 for the bandwidth of the individual signal stages.

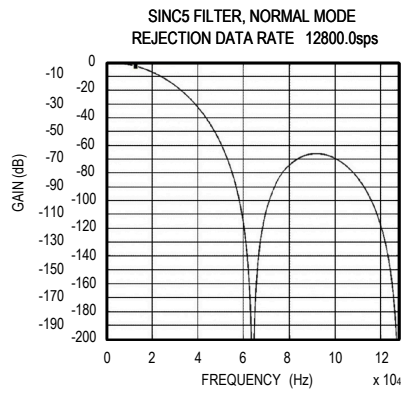


Figure 17. Digital Filter Frequency Response for 12.8ksps Single-Cycle Data Rate

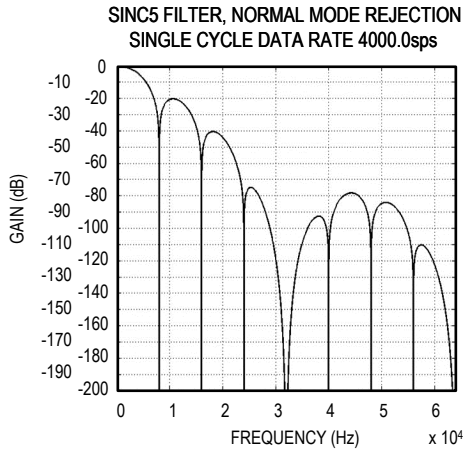


Figure 18. Digital Filter Frequency Response for 4ksps Single-Cycle Data Rate

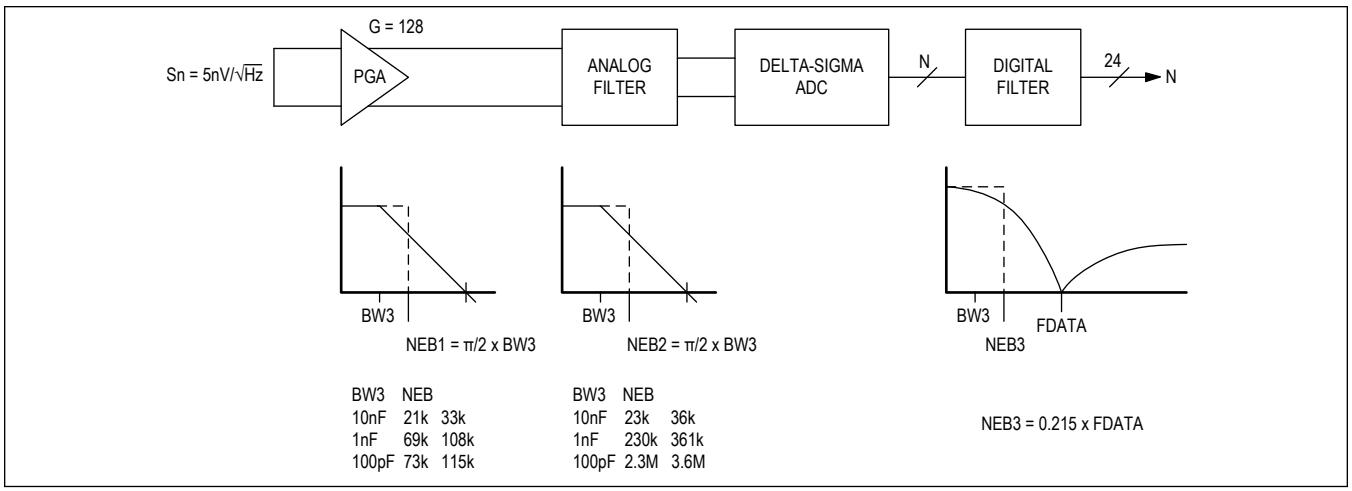


Figure 19. Signal Path Block Diagram Including Bandwidth of Each Stage

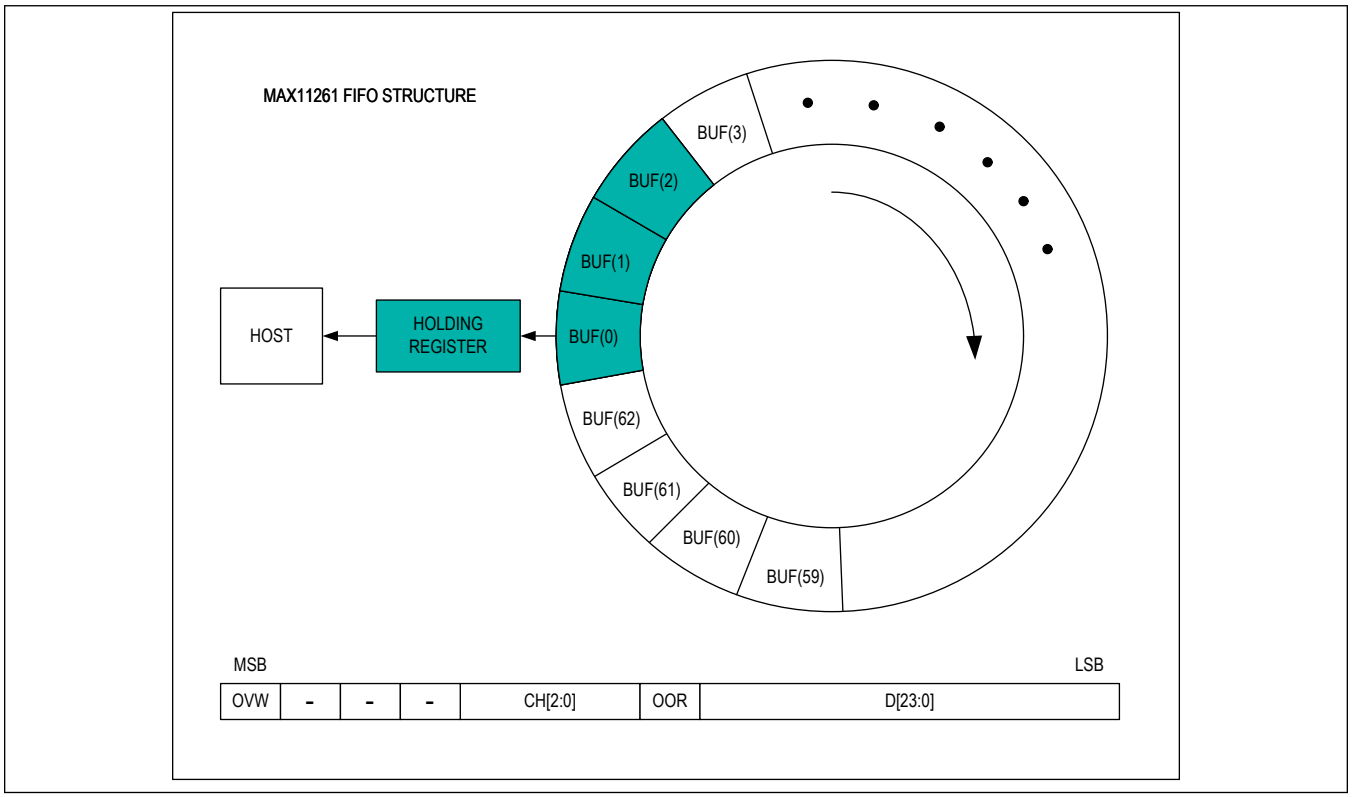


Figure 20. MAX11261 FIFO Structure

FIFO Operation

The MAX11261 stores conversion results in a 64-entry FIFO, which includes a holding register and 63 circular buffers.

Each FIFO entry consists of 32 bits of data. From the MSB, they are the OVW bit (indicating the previous entry is overwritten), 3 bits reserved, the channel ID CH[2:0], the OOR bit (indicating the channel's input is out-of-range by using the math operation), and the conversion result D[23:0].

The register FIFO_LEVEL stores the number of conversion results currently held in the FIFO. In Figure 20, FIFO_LEVEL = 4.

The first conversion result is stored in the holding register. And the next conversion results are stored in the 63 buffers sequentially. If there are more than 64 conversion results (e.g., 65) the first conversion result is kept in the holding register, the second conversion result is overwritten (lost), the third conversion result is stored in BUF[1], and the OVW bit is set in BUF[1], indicating that the previous conversion result is overwritten. The fourth conversion result is stored in BUF[2], and so on. The 65th conversion result is stored in BUF[0]. Only the results in the circular buffers will be overwritten.

The FIFO read always starts from the oldest conversion result, which is held in the holding register. After all conversion results are read, the FIFO_LEVEL register is cleared to 0. When the FIFO is empty, a FIFO read returns 0xFFFF_FFFF.

When reading the FIFO while the ADC is running it is important to first read the FIFO_LEVEL and then read the FIFO by the number of entries indicated by the FIFO_LEVEL. Reading more entries than are available in the FIFO (underflow) when the ADC is running can (albeit unlikely) result in data loss.

To the user, the FIFO is a single addressable register. After one conversion result is transferred from the holding register to the user, the MAX11261 automatically moves the next conversion result to the holding register. The user can burst read the FIFO to reduce power consumption.

The following example shows how a microcontroller reads N FIFO entries; N can be smaller or larger than FIFO_LEVEL.

1. I2C START.
2. I2C WRITE.
   a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address (8’b011xxxx_0).
   b. Check ACK.
   c. Send a command byte to the Read FIFO register (8’b11_FIFO_reg_addr[4:0]_1).
   d. Check ACK.
3. I2C Repeat START.
4. I2C WRITE.
   a. Send Device Address with a '1' in bit 8 indicating the master will read the register data out.
   b. Check ACK.
5. I2C READ.
   - (Transfer the first FIFO entry, 32 bits, MSB first.)

   a. Receive 8 bits of data (OVW, 3 bits reserved, CH[2:0], OOR).
   b. Send ACK.
   c. Receive 8 bits of data (D[23:16]).
   d. Send ACK.
   e. Receive 8 bits of data (D[15:8]).
   f. Send ACK.
   g. Receive 8 bits of data (D[7:0]).
   h. Send ACK.

   - (Transfer the second FIFO entry, 32 bits.)

   i. Receive 8 bits of data (OVW, 3 bits reserved, CH[2:0], OOR).
   j. Send ACK.
   k. ...

   - (Transfer the Nth entry, 32 bits).

   l. Receive 8 bits of data (OVW, 3 bits reserved, CH[2:0], OOR).
   m. Send ACK.
   n. Receive 8 bits of data (D[23:16]).
   o. Send ACK.

p. Receive 8 bits of data (D[15:8]).
q. Send ACK.
r. Receive 8 bits of data (D[7:0]).
s. Send NACK.

6. I2C STOP.

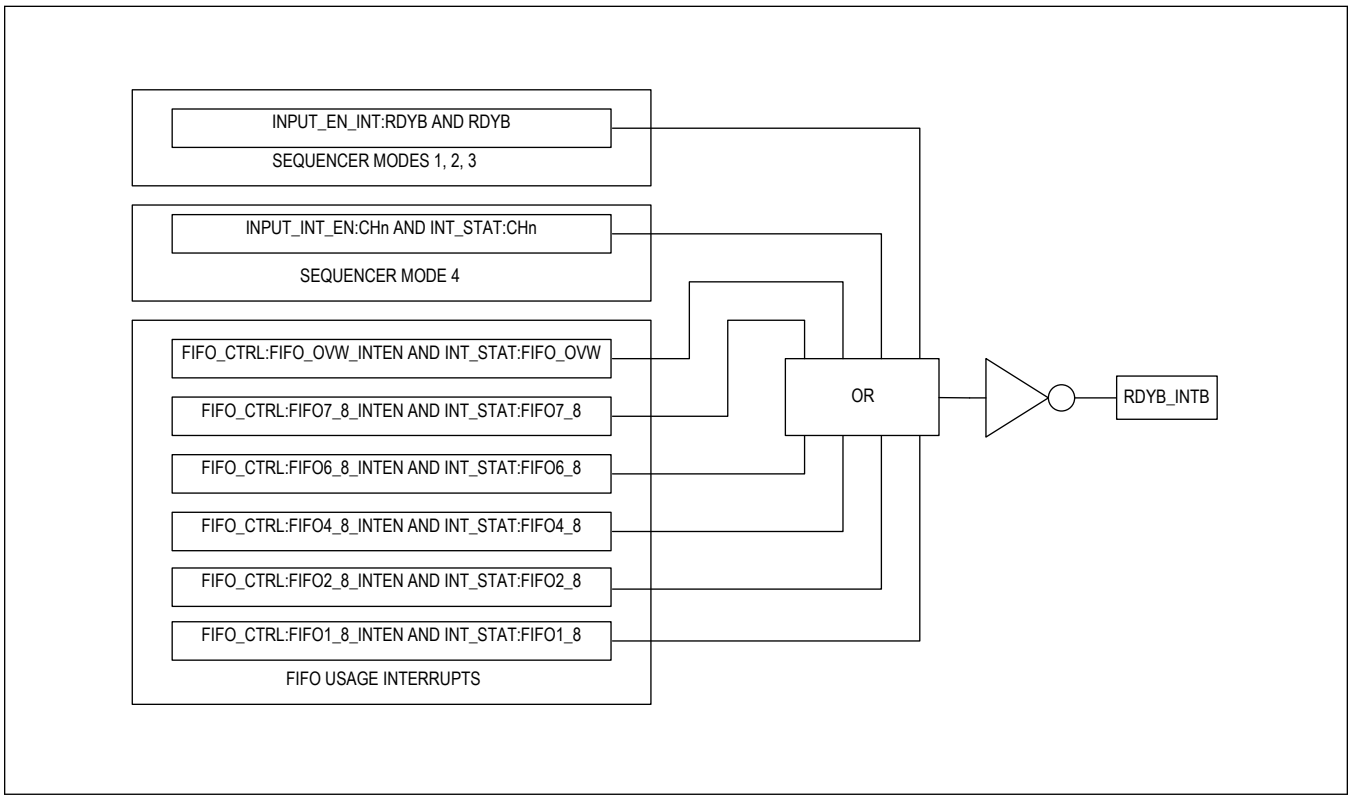


Figure 21. MAX11261 Interrupt Sources

Hardware Interrupts

The MAX11261 hardware interrupt output RDYB_INTB is generated from data availability (RDYB) in modes 1, 2, and 3; the math operation in mode 4, and the FIFO usage.

The math operation interrupts are generated based on the calculations (dependent on the setting of CMP_ MODE[1:0] register) of:

- DATAn > LIMIT_HIGHn or DATAn < LIMIT_LOWn, or
- (DATAn(N) – DATAn(N-1) > LIMIT_HIGHn) or (DATAn(N) – DATAn(N-1) < LIMIT_LOWn), or
- HPF output > LIMIT_HIGHn or HPF output < LIMIT_ LOWn.

INT_STAT:CHn: 1 = Channel n input math operation is out-of-range.
INT_STAT:FIFO_OVW: 1 = The FIFO is overwritten. INT_STAT:FIFO7/8: 1 = The FIFO is 7/8 full (at least 56 conversion results are stored in the FIFO).
INT_STAT:FIFO6/8: 1 = The FIFO is 6/8 full (at least 48 conversion results are stored in the FIFO).
INT_STAT:FIFO4/8: 1 = The FIFO is 4/8 full (at least 32 conversion results are stored in the FIFO).
INT_STAT:FIFO2/8: 1 = The FIFO is 2/8 full (at least 16 conversion results are stored in the FIFO).
INT_STAT:FIFO1/8: 1 = The FIFO is 1/8 full (at least 8 conversion results are stored in the FIFO).

INT_STAT:CHn is cleared by a register INT_STAT read. The FIFO interrupt status register bits reflect the real-time FIFO

usage. These register bits are automatically cleared when the FIFO usage is reduced below the corresponding levels.

Synchronization Between Multiple MAX11261 Devices

The SYNC pin synchronizes multiple MAX11261's when multiple devices work together to monitor more than 6 input channels. At power up, the device is default to a master (CTRL3:SYNC = 1) and the SYNC pin output is in high impedance state (CTRL3:SYNCZ = 1). When the device is configured as a master and the register CTRL3:SYNCZ is set to 0, the SYNC pin is changed to an active-low, open-drain output pin. Set CTRL3:SYNC to 0 puts the device in slave mode and the SYNC pin is an input. An external pullup resistor is required if the SYNC function is used. When the master starts a scan cycle, it pulls SYNC pin from high to low. All of the MAX11261 slave devices start their own scan cycles on detection of a high-to-low transition on the SYNC pin.

This feature is only valid in sequencer mode 4. The AUTOSCAN[7:0] register is ignored in slave devices.

Table 10. SYNC Pin Configuration

CTRL3:SYNC	CTRL3:SYNCZ	DEVICE MODE AND SYNC PIN STATE
0	x	Slave, SYNC pin is high impedance input
1	0	Master, SYNC pin is active-low output (needs external pullup)
1	1	Standalone, SYNC pin is high impedance output

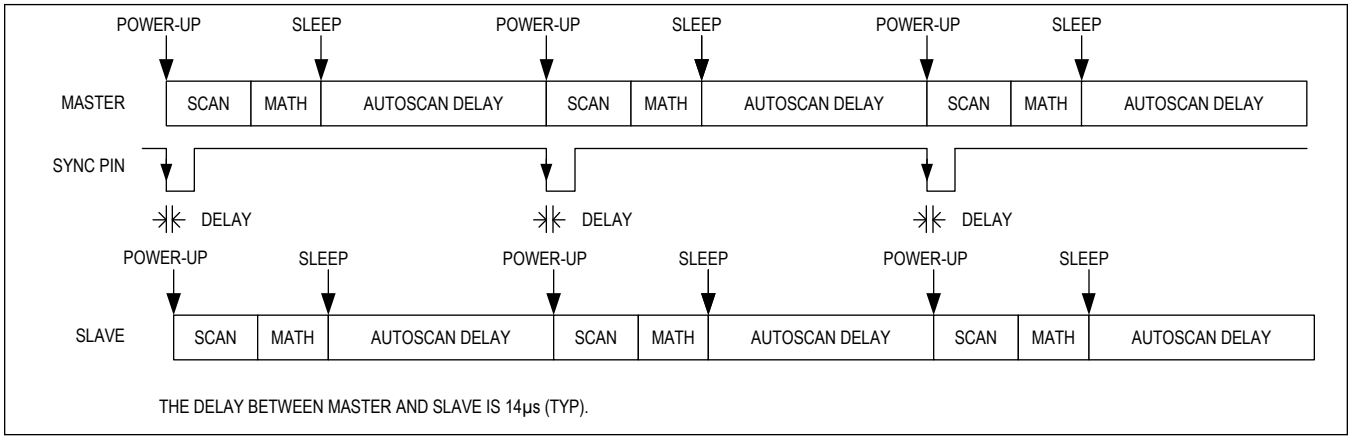


Figure 22. SYNC Timing Diagram

Register Map

MAX11261 Register Map

ADDRESS	NAME	MSB							LSB
REGISTERS									
0x00	STAT[23:16]	RESERVED	INRESET	SRDY[5:0]					
	STAT[15:8]	SCANER R	REFDET	ORDER R	GPOER R	ERROR	SYSGO R	DOR	AOR
	STAT[7:0]	RATE[3:0]				PDSTAT[1:0]		MSAT	RDY
0x01	CTRL1[7:0]	CAL[1:0]		PD[1:0]		U_B	FORMAT	SCYCLE	CONTSC
0x02	CTRL2[7:0]	RST	CSSEN	LDOEN	LPMODE	PGAEN	PGA[2:0]		
0x03	CTRL3[7:0]	RESERVED	SYNCZ	SYNC	CALREGSEL	NOSYSG	NOSYSO	NOSCG	NOSCO
0x04	SEQ[15:8]	MUX[2:0]			MODE[1:0]		GPODREN	MDREN	RDYBEN
	SEQ[7:0]	RESERVED[5:0]						SIF_FREQ[1:0]	
0x05	CHMAP1[23:16]	CH5_GPO[2:0]			CH5_ORD[2:0]			CH5_EN	CH5_GPOEN
	CHMAP1[15:8]	CH4_GPO[2:0]			CH4_ORD[2:0]			CH4_EN	CH4_GPOEN
	CHMAP1[7:0]	CH3_GPO[2:0]			CH3_ORD[2:0]			CH3_EN	CH3_GPOEN
0x06	CHMAP0[23:16]	CH2_GPO[2:0]			CH2_ORD[2:0]			CH2_EN	CH2_GPOEN
	CHMAP0[15:8]	CH1_GPO[2:0]			CH1_ORD[2:0]			CH1_EN	CH1_GPOEN
	CHMAP0[7:0]	CH0_GPO[2:0]			CH0_ORD[2:0]			CH0_EN	CH0_GPOEN
0x07	DELAY[23:16]	AUTOSCAN[7:0]							
	DELAY[15:8]	MUX[7:0]							
	DELAY[7:0]	GPO[7:0]							
0x08	LIMIT_LOW0[23:16]	D[23:16]							
	LIMIT_LOW0[15:8]	D[15:8]							
	LIMIT_LOW0[7:0]	D[7:0]							
0x09	LIMIT_LOW1[23:16]	D[23:16]							
	LIMIT_LOW1[15:8]	D[15:8]							
	LIMIT_LOW1[7:0]	D[7:0]							
0x0A	LIMIT_LOW2[23:16]	D[23:16]							
	LIMIT_LOW2[15:8]	D[15:8]							
	LIMIT_LOW2[7:0]	D[7:0]							
0x0B	LIMIT_LOW3[23:16]	D[23:16]							
	LIMIT_LOW3[15:8]	D[15:8]							

ADDRESS	NAME	MSB							LSB
	LIMIT_LOW3[7:0]	D[7:0]							
0x0C	LIMIT_LOW4[23:16]	D[23:16]							
	LIMIT_LOW4[15:8]	D[15:8]							
	LIMIT_LOW4[7:0]	D[7:0]							
0x0D	LIMIT_LOW5[23:16]	D[23:16]							
	LIMIT_LOW5[15:8]	D[15:8]							
	LIMIT_LOW5[7:0]	D[7:0]							
0x0E	SOC[23:16]	D[23:16]							
	SOC[15:8]	D[15:8]							
	SOC[7:0]	D[7:0]							
0x0F	SGC[23:16]	D[23:16]							
	SGC[15:8]	D[15:8]							
	SGC[7:0]	D[7:0]							
0x10	SCOC[23:16]	D[23:16]							
	SCOC[15:8]	D[15:8]							
	SCOC[7:0]	D[7:0]							
0x11	SCGC[23:16]	D[23:16]							
	SCGC[15:8]	D[15:8]							
	SCGC[7:0]	D[7:0]							
0x12	GPO_DIR[7:0]	RESERVED[1:0]		GPO[5:0]					
0x13	FIFO[31:24]	OVW	RESERVED[2:0]			CH[2:0]			OOR
	FIFO[23:16]	D[23:16]							
	FIFO[15:8]	D[15:8]							
	FIFO[7:0]	D[7:0]							
0x14	FIFO_LEVEL[7:0]	RESERVED	FIFO_LEVEL[6:0]						
0x15	FIFO_CTRL[7:0]	RESERVED	FIFO_OVW_INTEN	FIFO7_8_INTEN	FIFO6_8_INTEN	FIFO4_8_INTEN	FIFO2_8_INTEN	FIFO1_8_INTEN	RST
0x16	INPUT_INT_EN[7:0]	RDYB	RESERVED	CH[5:0]					
0x17	INT_STAT[15:8]	RESERVED2	FIFO_OVW	FIFO7_8	FIFO6_8	FIFO4_8	FIFO2_8	FIFO1_8	RESERVED1
	INT_STAT[7:0]	RESERVED[1:0]		CH[5:0]					
0x18	HPF[7:0]	RESERVED[2:0]			CMP_MODE[1:0]		FREQUENCY[2:0]		
0x19	LIMIT_HIGH0[23:16]	D[23:16]							
	LIMIT_HIGH0[15:8]	D[15:8]							
	LIMIT_HIGH0[7:0]	D[7:0]							
0x1A	LIMIT_HIGH1[23:16]	D[23:16]							
	LIMIT_HIGH1[15:8]	D[15:8]							
	LIMIT_HIGH1[7:0]	D[7:0]							
0x1B	LIMIT_HIGH2[23:16]	D[23:16]							

ADDRESS	NAME	MSB							LSB
	LIMIT_HIGH2[15:8]	D[15:8]							
	LIMIT_HIGH2[7:0]	D[7:0]							
0x1C	LIMIT_HIGH3[23:16]	D[23:16]							
	LIMIT_HIGH3[15:8]	D[15:8]							
	LIMIT_HIGH3[7:0]	D[7:0]							
0x1D	LIMIT_HIGH4[23:16]	D[23:16]							
	LIMIT_HIGH4[15:8]	D[15:8]							
	LIMIT_HIGH4[7:0]	D[7:0]							
0x1E	LIMIT_HIGH5[23:16]	D[23:16]							
	LIMIT_HIGH5[15:8]	D[15:8]							
	LIMIT_HIGH5[7:0]	D[7:0]							

Register Details

STAT (0x0)

Status Register (Read)

BIT	23	22	21	20	19	18	17	16
Field	RESERVED	INRESET	SRDY[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Read Only	Read Only	Read Only					

BIT	15	14	13	12	11	10	9	8
Field	SCANERR	REFDET	ORDERR	GPOERR	ERROR	SYSGOR	DOR	AOR
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	RATE[3:0]				PDSTAT[1:0]		MSAT	RDY
Reset	0x0				0b00		0b0	0b0
Access Type	Read Only				Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RESERVED	23	Reserved
INRESET	22	This bit indicates the status of a reset command.
SRDY	21:16	For sequencer modes 2, 3, and 4, this bit when set to ‘1’ indicates that a new conversion result is available from the channel indicated by the SRDY bit position. A complete read of the FIFO register associated with the SRDY bit will reset the bit to ‘0’. At the start of a scan mode these bits are reset to ‘0’.
SCANERR	15	Flag is set if the sequencer scan mode is enabled (mode 2, 3, or 4) and no channels or invalid channel numbers (3’b110, 3’b111) are enabled in the CHMAP1 or CHMAP2 register. Until SCANERR is cleared, CONVERSION commands are aborted.

BITFIELD	BITS	DESCRIPTION
REFDET	14	This bit is a ‘1’ if a proper reference voltage is detected and ‘0’ if a proper reference voltage is missing. In SLEEP or STANDBY the value of this bit is ‘0’. The trigger level for this bit is V_{REF} < 0.35V. This error does not inhibit normal operation and is intended for status only. This flag is only valid during a conversion in progress and if the user needs to verify valid reference level they should read this status bit. The value of this status bit is valid within 30µs after a conversion start command and is invalid when not in conversion.
ORDERR	13	This bit is not valid in sequencer mode 1. The flag is set if two or more CHX_ORD bits decode to the same scan sequence order and are also enabled. This bit is also set for the case when a channel is enabled for scan with CHX_EN=’1’ and CHX_ORD[2:0] = ‘000’ or ‘111’. The CHX_ORD[2:0] values of ‘000’ and ‘111’ are not allowed for the order of an enabled channel. The allowable orders are 1, 2, 3, 4, 5, 6. The MAX11261 remains in STANDBY state until this error is removed. The channel order must be strictly sequential and no missing numbers are allowed. For instance, if 4 channels are enabled, then the order must be 1, 2, 3, 4. Any other order is flagged as ORDERR and the MAX11261 remains in STANDBY mode.
GPOERR	12	This bit is not valid in sequencer mode 1. This bit is set to ‘1’ if more than one input channel is mapped to the same GPO bump, and CHX_GPOEN is enabled for more than one channel. The MAX11261 remains in STANDBY state until this error is removed.
ERROR	11	Flag for invalid configuration states. The flag is set if CAL[1:0] programmed to ‘11’ which is an invalid state. The flag is set if CTRL1:SCYCLE = ‘0’ for scan modes 2, 3, and 4. This error puts the MAX11261 into STANDBY mode.
SYSGOR	10	This bit when set to ‘1’ indicates that a system gain calibration was overrange. The SCGC calibration coefficient is the maximum value of 1.9999999. This bit when set to ‘1’ indicates that full-scale value out of the converter is likely not available.
DOR	9	This bit when set to ‘1’ indicates that the conversion result has exceeded the maximum or minimum value of the converter and that the result has been clipped or limited to the maximum value. When ‘0’ the conversion result is within the full-scale range of the inputs.
AOR	8	This bit indicates if the modulator detected an analog overrange condition from having the input signal level greater than the reference voltage. This check for overrange includes the PGA.
RATE	7:4	These bits indicate the conversion rate that corresponds to the result in the FIFO register or the rate that was used for calibration coefficient calculation. The corresponding RATE[3:0] is only valid until the FIFO register is read.
PDSTAT	3:2	These bits indicate the power-down state of the chip. See Table 5 for transition times. ‘00’ = CONVERSION ‘01’ = SLEEP ‘10’ = STANDBY (default) ‘11’ = RESET
MSAT	1	This bit is set to ‘1’ when a signal measurement is in progress. This indicates that a conversion, self-calibration, or system calibration is in progress and that the modulator is busy. When the modulator is not converting, this bit will be set to ‘0’.
RDY	0	For sequencer mode 1, this bit when set to ‘1’ indicates that a new conversion result is available. A complete read of the FIFO Register will reset this bit to ‘0’. This bit is invalid in sequencer mode 2, 3, or 4. The function of this bit is redundant and is duplicated by the RDYB_INTB pin.

CTRL1 (0x1)

Control Register 1 (Read/Write)

This register controls the selection of operational modes and configurations.

BIT	7	6	5	4	3	2	1	0
Field	CAL[1:0]		PD[1:0]		U_B	FORMAT	SCYCLE	CONTSC
Reset	0b00		0b00		0b0	0b0	0b1	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CAL	7:6	Calibration bits control the type of calibration performed when the calibration command byte is issued. Selects the type of calibration to perform. ‘00’ = Performs a self-calibration. ‘01’ = Performs a system-level offset calibration. ‘10’ = Performs a system-level full-scale calibration. ‘11’ = Not used, reserved state.
PD	5:4	Selects the power-down state to be executed. The MAX11261 enters the selected power-down state after the IMPD is written. These bits are decoded below: ‘00’ = NOP (default) ‘01’ = SLEEP ‘10’ = STANDBY ‘11’ = RESET
U_B	3	The ‘unipolar/bipolar’ bit controls the input range. A ‘1’ selects unipolar input range and a ‘0’ selects bipolar input range.
FORMAT	2	The ‘format’ bit controls the digital format of the bipolar range data. A ‘0’ selects two’s complement and a ‘1’ selects offset binary format of the bipolar range. The data from unipolar range is always formatted in offset binary format. The value of the format must be ‘0’ when operating sequencer mode 4, incorrect results are obtained when ‘1’.
SCYCLE	1	The ‘single-cycle’ bit selects either no-latency single conversion mode or latent continuous conversion in sequencer mode 1. A ‘1’ selects single-cycle mode where a no-latency conversion is followed by a power-down to SLEEP state. A ‘0’ selects continuous conversion mode with a latency of 5 conversion cycles for filtering and the RDYB pin goes low when valid/settled data is available. Only SCYCLE = ‘1’ is valid in sequencer mode 2, 3, and 4. Set SCYCLE to 0 in mode 2, 3, and 4 will flag ERROR and put the device in STANDBY mode.
CONTSC	0	The ‘continuous single-cycle’ bit selects between single or continuous conversions while operating in single-cycle mode in sequencer mode 1. A ‘1’ selects continuous conversions and a ‘0’ selects single conversion. CONTSC is ignored in mode 2, 3, and 4.

CTRL2 (0x2)

Control Register 2 (Read/Write)

This register controls the selection and configuration of optional functions.

BIT	7	6	5	4	3	2	1	0
Field	RST	CSSEN	LDOEN	LPMODE	PGAEN	PGA[2:0]		
Reset	0b0	0b0	0b1	0b0	0b0	0b000		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
RST	7	Write 1 to reset the device.
CSSEN	6	Setting this bit to ‘1’ enables the current source and current sink on the analog inputs to detect sensor opens or shorts.
LDOEN	5	Integrated LDO enable. Set this bit to ‘0’ when driving the CAPREG pin externally with a 1.8V supply. When driving with external supply the user must ensure that the CAPREG pin is connected to the DVDD pin.
LPMODE	4	PGA low-power mode is enabled by setting this bit to ‘1’. The PGA operates with reduced power consumption and reduced performance. The LPMODE does not affect power or performance when the PGA is not enabled.
PGAEN	3	The ‘PGA enable’ bit controls the operation of the PGA. A ‘1’ enables and a ‘0’ disables the PGA.
PGA	2:0	The ‘PGA’ bits control the PGA gain. The PGA gain is determined by: ‘000’ = 1 ‘001’ = 2 ‘010’ = 4 ‘011’ = 8 ‘100’ = 16 ‘101’ = 32 ‘110’ = 64 ‘111’ = 128

CTRL3 (0x3)

Control Register 3 (Read/Write)

This register is used to control the operation and calibration of the MAX11261.

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	SYNCZ	SYNC	CALREGSEL	NOSYSG	NOSYSO	NOSCG	NOSCO
Reset	0b0	0b1	0b1	0b1	0b1	0b1	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RESERVED	7	Reserved
SYNCZ	6	In sequencer mode 4, when CTRL3:SYNC is set high (the device is a master), set CTRL3:SYNCZ high to put SYNC pin in high impedance state. Set CTRL3:SYNCZ low to put SYNC pin in active-low, open-drain output state.
SYNC	5	Set this bit to 1 to configure the device as a master device.

BITFIELD	BITS	DESCRIPTION
CALREGSEL	4	The value of this bit controls which calibration value is read during a calibration register inquiry. When the user writes into one of the calibration registers, the value is stored within the interface domain. Once a command to convert is received, the new calibration value is transferred to a MATH module in a separate digital domain to be used in any valid calibration sequence. The user has access to both registers; i.e., the register value that was used to produce the current conversion result in the FIFO register or the value that was just written and is meant to be used for following conversions. It is common for a user to immediately read back the value written to insure that communication was not flawed. To accomplish this, set the CTRL3:CALREGSEL bit to ‘1’ in order to read back the interface value of the register. Set this bit to ‘0’ to read the MATH module value; i.e., the value used to generate the result in the FIFO register. Note that when CTRL3:CALREGSEL is ‘0’ only read operations are valid.
NOSYSG	3	The ‘no system gain’ bit controls the use of the system gain calibration coefficient. A ‘1’ in this location disables the use of the system gain value when computing the final offset and gain corrected data value. A ‘0’ in this location enables the use of the system gain value when computing the final offset and gain corrected data value.
NOSYSO	2	The ‘no system offset’ bit controls the use of the system offset calibration coefficient. A ‘‘1’ in this location disables the use of the system offset value when computing the final offset and gain corrected data value. A ‘‘0’ in this location enables the use of the system offset value when computing the final offset and gain corrected data value.
NOSCG	1	The ‘no self-calibration gain’ bit controls the use of the self-calibration gain calibration coefficient. A ‘1’ in this location disables the use of the self-calibration gain value when computing the final offset and gain corrected data value. A ‘0’ in this location enables the use of the self-calibration gain value when computing the final offset and gain corrected data value.
NOSCO	0	The ‘no self-calibration offset’ bit controls the use of the self-calibration offset calibration coefficient. A ‘1’ in this location disables the use of the self-calibration offset value when computing the final offset and gain corrected data value. A ‘0’ in this location enables the use of the self-calibration offset value when computing the final offset and gain corrected data value.

SEQ (0x4)

Sequencer Register (Read/Write)

This register is used to control the operation of the sequencer when enabled.

BIT	15	14	13	12	11	10	9	8
Field	MUX[2:0]			MODE[1:0]		GPODREN	MDREN	RDYBEN
Reset	0b000			0b00		0b0	0b0	0b0
Access Type	Write, Read			Write, Read		Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[5:0]						SIF_FREQ[1:0]	
Reset	0x00						0b01	
Access Type	Write, Read						Write, Read	

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>MUX</td><td>15:13</td><td>Binary channel selection for sequencer mode 1. Valid channels are from 3’b000 (channel 0) to 3’b101 (channel 5).</td></tr>
<tr><td>MODE</td><td>12:11</td><td>Sequencer mode is decoded as shown in the following table:
<table>
<tr><th>MODE1</th><th>MODE0</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0</td><td>Sequencer Mode 1</td></tr>
<tr><td>0</td><td>1</td><td>Sequencer Mode 2</td></tr>
<tr><td>1</td><td>0</td><td>Sequencer Mode 3</td></tr>
<tr><td>1</td><td>1</td><td>Sequencer Mode 4</td></tr>
</table></td></tr>
<tr><td>GPODREN</td><td>10</td><td>GPO delay enable. Enables operation of the GPO switch delay. When enabled, the channel selection is delayed. The value of the delay is set by the DELAY:GPO bits.</td></tr>
<tr><td>MDREN</td><td>9</td><td>MUX delay enable. Enables the timer setting in DELAY:MUX register to delay the conversion start of the selected channel.</td></tr>
<tr><td>RDYBEN</td><td>8</td><td>Ready Bar enable. When this bit is ‘1’, the RDYB is inhibited from asserting in sequencer mode 2 and 3 until all channels are converted.</td></tr>
<tr><td>RESERVED</td><td>7:2</td><td>Reserved</td></tr>
<tr><td>SIF_FREQ</td><td>1:0</td><td>The register SIF_FREQ[1:0] configures the internal FIFO clock according to the serial interface clock speed at which the FIFO register is being read.

Before reading the FIFO register at a different serial clock speed range, set SIF_FREQ[1:0] accordingly.
<table>
<tr><th>SIF_FREQ1</th><th>SIF_FREQ0</th><th>SERIAL CLOCK SPEED</th></tr>
<tr><td>0</td><td>0</td><td>100kHz ≤ speed ≤ 400kHz</td></tr>
<tr><td>0</td><td>1</td><td>400kHz < speed ≤ 1MHz</td></tr>
<tr><td>1</td><td>0</td><td>1MHz < speed ≤ 3MHz</td></tr>
<tr><td>1</td><td>1</td><td>3MHz < speed ≤ 5MHz</td></tr>
</table></td></tr>
</table>

CHMAP1 (0x5)

Channel Map Register (Read/Write)

These registers are used to enable channels for scan, enable output controls for scan, program the channel scan order, and pair the GPO bumps with its associated channel. These registers cannot be written during an active conversion.

BIT NAME	DESCRIPTION
CHX_GPO[2:0]	Used to map which GPO bump is activated when this channel is selected. The STAT:GPOERR flag is set if two or more output controls are mapped to the same channel.
CHX_ORD[2:0]	Used to define the order during scan when the channel is enabled. The CHX_ORD[2:0] values of ‘000’ and ‘111’ are not allowed for the order of an enabled channel. The allowable orders are 1, 2, 3, 4, 5, and 6 representing first, second, third, and so on. The value of ‘000’ is a default value and the value of ‘111’ is greater than the number of scannable channels. A value greater than the number of scannable channels is invalid and will set an error condition at STAT:ORDERR. Setting a channels order to ‘000’ or ‘111’ and enabling it will set the STAT:ORDERR flag in the STAT register.
CHX_EN	Used to enable this channel for scan.
CHX_GPOEN	Used to enable activation of the GPO bump when this channel is selected during scan.

BIT	23	22	21	20	19	18	17	16
Field	CH5_GPO[2:0]			CH5_ORD[2:0]			CH5_EN	CH5_GPOEN
Reset	0b000			0b000			0b0	0b0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BIT	15	14	13	12	11	10	9	8
Field	CH4_GPO[2:0]			CH4_ORD[2:0]			CH4_EN	CH4_GPOEN
Reset	0b000			0b000			0b0	0b0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	CH3_GPO[2:0]			CH3_ORD[2:0]			CH3_EN	CH3_GPOEN
Reset	0b000			0b000			0b0	0b0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CH5_GPO	23:21	
CH5_ORD	20:18	
CH5_EN	17	
CH5_GPOEN	16	
CH4_GPO	15:13	
CH4_ORD	12:10	
CH4_EN	9	
CH4_GPOEN	8	
CH3_GPO	7:5	
CH3_ORD	4:2	
CH3_EN	1	
CH3_GPOEN	0	

CHMAP0 (0x6)

Channel Map Register (Read/Write)

BIT	23	22	21	20	19	18	17	16
Field	CH2_GPO[2:0]			CH2_ORD[2:0]			CH2_EN	CH2_GPOEN
Reset	0b000			0b000			0b0	0b0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BIT	15	14	13	12	11	10	9	8
Field	CH1_GPO[2:0]			CH1_ORD[2:0]			CH1_EN	CH1_GPOEN
Reset	0b000			0b000			0b0	0b0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	CH0_GPO[2:0]			CH0_ORD[2:0]			CH0_EN	CH0_GPOEN
Reset	0b000			0b000			0b0	0b0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CH2_GPO	23:21	
CH2_ORD	20:18	
CH2_EN	17	
CH2_GPOEN	16	
CH1_GPO	15:13	
CH1_ORD	12:10	
CH1_EN	9	
CH1_GPOEN	8	
CH0_GPO	7:5	
CH0_ORD	4:2	
CH0_EN	1	
CH0_GPOEN	0	

DELAY (0x7)

Delay Register (Read/Write)

BIT	23	22	21	20	19	18	17	16
Field	AUTOSCAN[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	MUX[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	GPO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AUTOSCAN	23:16	Used to program the autoscan delay. The autoscan delay ranges from 4ms to 1.024s. The default value of 0x00 corresponds to no delay. The timer resolution is 4ms.
MUX	15:8	Used to program the mux delay. The mux delay ranges from 4µs to 1.024ms. The default value of 0x00 corresponds to no delay. The timer resolution is 4µs.
GPO	7:0	Used to program the GPO delay. The GPO delay ranges from 20µs to 5.1ms. The default value of 0x00 corresponds to no delay. 1 LSB = 20µs of delay.

LIMIT_LOW0 (0x8)

This register stores the lower limit value for channel 0. It sets the lower bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_LOW1 (0x9)

This register stores the lower limit value for channel 1. It sets the lower bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_LOW2 (0xA)

This register stores the lower limit value for channel 2. It sets the lower bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_LOW3 (0xB)

This register stores the lower limit value for channel 3. It sets the lower bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	Reserved

LIMIT_LOW4 (0xC)

This register stores the lower limit value for channel 4. It sets the lower bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_LOW5 (0xD)

This register stores the lower limit value for channel 5. It sets the lower bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

SOC (0xE)

System Offset Calibration Register (Read/Write)

The System Offset Calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the system offset calibration value. The format is in two's complement binary format. An internal system calibration does not overwrite the SOC register.

The readback value of this register depends on CTRL3:CALREGSEL. A '1' reads back the user programmed value. A '0' reads back the results of an internal register as described in CTRL3 for bit CALREGSEL. The internal register can only be read during conversion.

The system offset calibration value is subtracted from each conversion result—provided the NOSYSO bit in the CTRL3 register is set to 0. The system offset calibration value is subtracted from the conversion result after self-calibration, but before system gain correction. It is also applied prior to the 1x or 2x scale factor associated with bipolar and unipolar modes. When a system offset calibration is in progress, this register is not writable by the user.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

SGC (0xF)

System Gain Calibration Register (Read/Write)

The System Gain Calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the system gain calibration value. The format is unsigned 24-bit binary. An internal system calibration does not overwrite the SGC register.

The readback value of this register depends on CTRL3:CALREGSEL. A '1' reads back the user programmed value. A

‘0’ reads back the results of an internal register as described in CTRL3 for bit CALREGSEL. The internal register can only be read during conversion.

The system gain calibration value is used to scale the offset corrected conversion result, provided the NOSYSG bit in the CTRL3 register is set to 0. The system gain calibration value scales the offset corrected result by up to 2x or can correct a gain error of approximately -50%. The amount of positive gain error that can be corrected is determined by modulator overload characteristics, which may be as much as +25%. When a system gain calibration is in progress, this register is not writable by the user.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x7FFFFF							
Access Type	Write, Read							
BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x7FFFFF							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x7FFFFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

SCOC (0x10)

Self-Calibration Offset Calibration Register (Read/Write)

The Self-Calibration Offset register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the self-calibration offset value. The format is always in two’s complement binary format. An internal self-calibration does not overwrite the SCOC register.

The readback value of this register depends on CTRL3:CALREGSEL. A ‘1’ reads back the user programmed value. A ‘0’ reads back the results of an internal register as described in CTRL3 for bit CALREGSEL. The internal register can only be read during conversion.

The self-calibration offset value is subtracted from each conversion result, provided the NOSCO bit in the CTRL3 register is set to 0. The self-calibration offset value is subtracted from the conversion result before the self-calibration gain correction and before the system offset and gain correction. It is also applied prior to the 2x scale factor associated with unipolar mode. When a self-calibration is in progress, this register is not writable by the user.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

SCGC (0x11)

Self-Calibration Gain Calibration Register (Read/Write)

The Self-Calibration Offset register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the self-calibration offset value. The format is always in two's complement binary format. An internal self-calibration does not overwrite the SCGC register.

The readback value of this register depends on CTRL3:CALREGSEL. A '1' reads back the user programmed value. A '0' reads back the results of an internal register as described in CTRL3 for bit CALREGSEL. The internal register can only be read during conversion.

The self-calibration gain calibration value is used to scale the self-calibration offset corrected conversion result before the system offset and gain calibration values have been applied, provided the NOSCG bit in the CTRL3 register is set to 0. The self-calibration gain calibration value scales the self-calibration offset corrected conversion result by up to 2x or can correct a gain error of approximately -50%. The gain will be corrected to within 2 LSB. When a self-calibration is in progress, this register is not writable by the user.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0xBF851B							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0xBF851B							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0xBF851B							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

GPO_DIR (0x12)

GPO Direct Access Register (Read/Write)

This register is used to turn on and off the GPO directly except when operating in mode 3 or mode 4. When operating in sequencer mode 1 or 2, the activation of the GPO is immediate upon setting a bit to a ‘1’ and the deactivation of the GPO is immediate upon setting the bit to a ‘0’. In SLEEP state, the values in this register do not control the state of the GPO as they all are deactivated. When in STANDBY state and programmed for sequencer mode 1 or mode 2, register writes immediately update the GPOs. Writes to this register are ignored when operating in sequencer mode 3 or mode 4. This register is used during system offset calibration, system gain calibration, and self-calibration modes.

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		GPO[5:0]					
Reset	0b00		0b000000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION
RESERVED	7:6	Reserved
GPO	5:0	

FIFO (0x13)

FIFO Register (Read Only)

The FIFO holds the most recent conversion results (up to a maximum of 64). If more than 64 conversions are captured and the user does not transfer the oldest FIFO entry, the oldest entry will be overwritten by the newest conversion result.

The FIFO are read-only registers. Any attempt to write data to this location will have no effect. The data read from these registers is clocked out MSB first. The result D[23:0] is stored in a format according to the FORMAT bit in the CTRL1 register. The data format while in unipolar mode is always offset binary. In offset binary format the most negative value is 0x000000, the midscale value is 0x800000 and the most positive value is 0xFFFFFF. In bipolar mode, if the FORMAT bit = ‘1’, then the data format is offset binary. If the FORMAT bit = ‘0’, then the data format is two’s complement. In two’s complement, the negative full-scale value is 0x800000, the midscale is 0x000000, and the positive full scale is 0x7FFFFF. Any input exceeding the available input range is limited to the minimum or maximum data value.

BIT	31	30	29	28	27	26	25	24
Field	OVW	RESERVED[2:0]			CH[2:0]			OOR
Reset	0b0	0b000			0b000			0b0
Access Type	Read Only	Read Only			Read Only			Read Only

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Read Only							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x000000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OVW	31	If this bit is set to 1, it indicates the previous FIFO entry overwrites the original data.
RESERVED	30:28	Reserved
CH	27:25	Channel ID. This register represents the FIFO entry and contains the result of the channel CH[2:0].
OOR	24	Out-of-range indication. If the channel's comparison result is out of the range set by LIMIT_LOWn and LIMIT_HIGHn registers, the OOR bit is set to 1.
D	23:0	The channel's conversion result.

FIFO_LEVEL (0x14)

FIFO Usage Level Register (Read Only)

The number of conversion results stored in the FIFO.

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	FIFO_LEVEL[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Read Only						

BITFIELD	BITS	DESCRIPTION
RESERVED	7	Reserved
FIFO_LEVEL	6:0	

FIFO_CTRL (0x15)

FIFO Control Register (Write/Read)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	FIFO_OVW_INTEN	FIFO7_8_INTEN	FIFO6_8_INTEN	FIFO4_8_INTEN	FIFO2_8_INTEN	FIFO1_8_INTEN	RST
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RESERVED	7	Reserved
FIFO_OVW_INTEN	6	Set to 1 to enable the hardware interrupt output when the FIFO overwrite happens.
FIFO7_8_INTEN	5	Set to 1 to enable the hardware interrupt output pin when the FIFO is 7/8 full.
FIFO6_8_INTEN	4	Set to 1 to enable the hardware interrupt output pin when the FIFO is 6/8 full.
FIFO4_8_INTEN	3	Set to 1 to enable the hardware interrupt output pin when the FIFO is 4/8 full.
FIFO2_8_INTEN	2	Set to 1 to enable the hardware interrupt output pin when the FIFO is 2/8 full.
FIFO1_8_INTEN	1	Set to 1 to enable the hardware interrupt output pin when the FIFO is 1/8 full.

BITFIELD	BITS	DESCRIPTION
RST	0	Write 1 to clear the FIFO.

INPUT_INT_EN (0x16)

Input Interupt Enable Register (Write/Read)

BIT	7	6	5	4	3	2	1	0
Field	RDYB	RESERVED	CH[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RDYB	7	In modes 1, 2, and 3, set RDYB to 1 to generate an interrupt when conversion data is available. Set RDYB to 0 disable the interrupts even when conversion data is available. This bit is ignored in mode 4.
RESERVED	6	Reserved
CH	5:0	CHn set to 1 to enable the channel to generate an interrupt when the channel's input is out of range.

INT_STAT (0x17)

Interrupt Status Register (Read only)

A register INT_STAT read clears CHn bits, but the FIFO interrupt status register bits reflect the real-time FIFO usage. These register bits are automatically cleared when the FIFO usage is reduced below the corresponding levels.

BIT	15	14	13	12	11	10	9	8
Field	RESERVED 2	FIFO_OVW	FIFO7_8	FIFO6_8	FIFO4_8	FIFO2_8	FIFO1_8	RESERVED 1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		CH[5:0]					
Reset	0b00		0b000000					
Access Type	Read Only		Read Only					

BITFIELD	BITS	DESCRIPTION
RESERVED2	15	Reserved
FIFO_OVW	14	When a FIFO overwrite happens, FIFO_OVW is set to 1.
FIFO7_8	13	When the FIFO is 7/8 full, FIFO7_8 is set to 1.
FIFO6_8	12	When the FIFO is 6/8 full, FIFO6_8 is set to 1.
FIFO4_8	11	When the FIFO is 4/8 full, FIFO4_8 is set to 1.
FIFO2_8	10	When the FIFO is 2/8 full, FIFO2_8 is set to 1.
FIFO1_8	9	When the FIFO is 1/8 full, FIFO1_8 is set to 1.
RESERVED1	8	Reserved
RESERVED	7:6	Reserved
CH	5:0	When a channel input is out of range, the corresponding CHn is set to 1.

HPF (0x18)

High-Pass Digital Filter Control Register (Write/Read)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			CMP_MODE[1:0]		FREQUENCY[2:0]		
Reset	0b000			0b00		0b000		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:5	Reserved	
CMP_MODE	4:3	Sets how input conversion results are used to generate the input activity indication and out-of-range bit.	0x0: use DATAn to compare with LIMIT_LOWn and LIMIT_HIGHn 0x1: use DATAn - previous DATAn to compare with LIMIT_LOWn and LIMIT_HIGHn 0x2: use high-pass filter output to compare with LIMIT_LOWn and LIMIT_HIGHn 0x3: RESERVED
FREQUENCY	2:0	The HPF Cutoff Frequency (Hz)	0x0: Scan rate/39.0625 0x1: Scan rate/78.125 0x2: Scan rate/156.25 0x3: scan rate/312.5 0x4: scan rate/625 0x5: scan rate/1250 0x6: scan rate/2500 0x7: scan rate/5000

LIMIT_HIGH0 (0x19)

This register stores the higher limit value for channel 0. It sets the upper bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_HIGH1 (0x1A)

This register stores the higher limit value for channel 1. It sets the upper bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_HIGH2 (0x1B)

This register stores the higher limit value for channel 2. It sets the upper bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_HIGH3 (0x1C)

This register stores the higher limit value for channel 3. It sets the upper bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_HIGH4 (0x1D)

This register stores the higher limit value for channel 4. It sets the upper bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

LIMIT_HIGH5 (0x1E)

This register stores the higher limit value for channel 5. It sets the upper bound for the comparator.

BIT	23	22	21	20	19	18	17	16
Field	D[23:16]							
Reset	0x000000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	D[15:8]							
Reset	0x000000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
D	23:0	

Applications Information

Connecting an External 1.8V Supply to DVDD for Digital I/O and Digital Core

The voltage range of the DVDD I/O supply is specified from 2.0V to 3.6V if the internal LDO is used to power the digital core. If a lower I/O supply voltage is desired, the internal LDO can be disabled, and DVDD and CAPREG can be connected together as shown in Figure 23. In this mode of operation, DVDD can vary from 1.7V to 2.0V. The internal LDO must be disabled by setting CTRL2:LDOEN to '0'.

Sensor Fault Detection

The MAX11261 includes a 1µA current source and a 1µA current sink. The source pulls current from AVDD to AIN_P and sink from AIN_N to AVSS. The currents are enabled by register bit CTRL2:CSSEN. These currents are used to detect damaged sensors in either open or shorted state. The current sources and sinks are functional over the normal input operating voltage range, as specified.

These currents are used to test sensors for functional operation before taking measurements on that input channel. With the source and sink enabled, the currents flow into the external sensor circuit and measurement of the input voltage is used to diagnose sensor faults. A full-scale reading could indicate a sensor is open-circuit or overloaded or that the ADC's reference is absent. If a zero scale is read back, this may indicate the sensor is short-circuited.

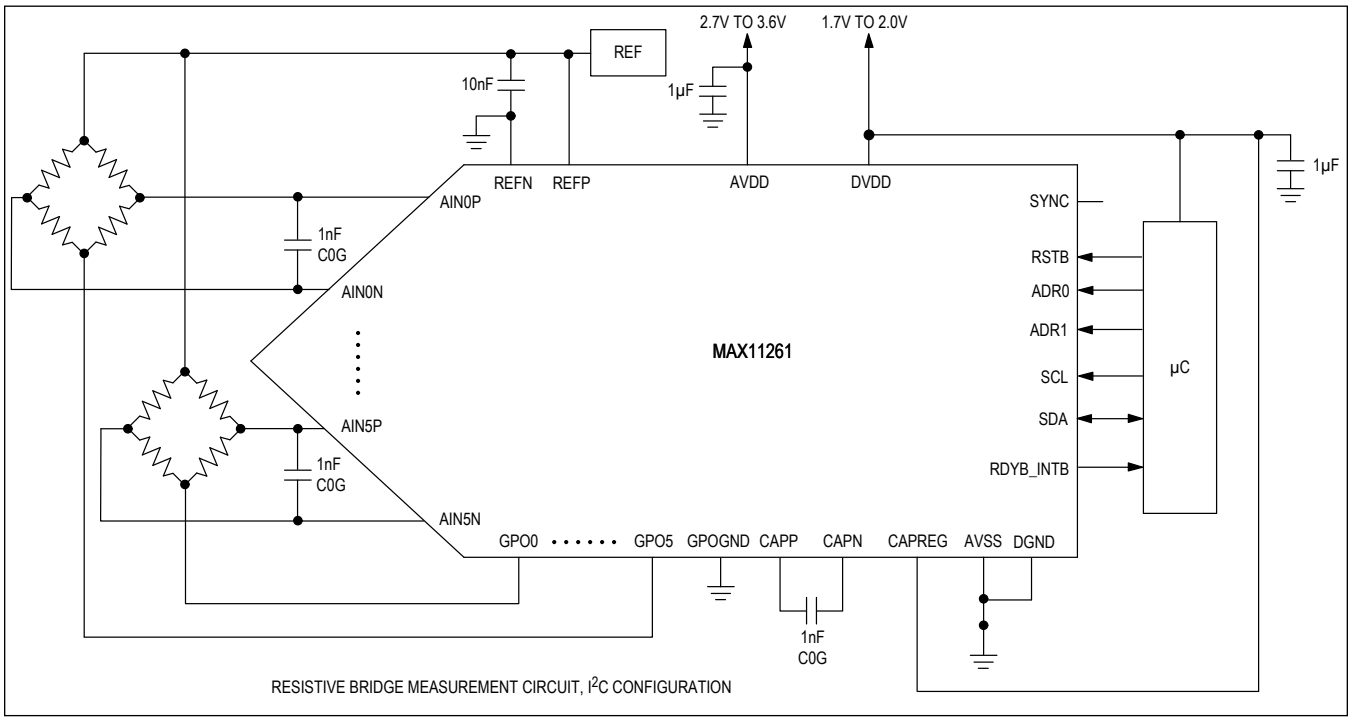


Figure 23. Application Diagram for 1.8V DVDD

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	MAX HEIGHT
MAX11261ENX+	-40°C to +85°C	36 WLP	0.5mm

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/18	Initial release	—
1	11/20	Updated *Detailed Description*	18, 39

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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