ADC1115S125

Single 11-bit ADC; 125 Msps with input buffer; CMOS or LVDS DDR digital outputs

Rev. 03 — 2 July 2012 Product data sheet

1. General description

The ADC1115S125 is a single channel 11-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performance and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1115S125 is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in CMOS mode, because of a separate digital output supply.

The ADC1115S125 supports the Low Voltage Differential Signalling (LVDS) Double Data Rate (DDR) output standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC.

The device also includes a SPI programmable full-scale to allow flexible input voltage range from 1 V to 2 V (peak-to-peak). With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1115S125 is ideal for use in communications, imaging and medical applications - especially in high Intermediate Frequency (IF) applications because of the integrated input buffer. The input buffer ensures that the input impedance remains constant and low and the performance consistent over a wide frequency range.

2. Features and benefits

- SNR, 66.5 dBFS; SFDR, 86 dBc
- Sample rate up to 125 Msps
- 11-bit pipelined ADC core
- Clock input divided by 2 for less jitter contribution
- Integrated input buffer
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- CMOS or LVDS DDR digital outputs
- Pin compatible with the ADC1415S series, the ADC1215S series and the ADC1015S series
- Input bandwidth, 600 MHz
- Power dissipation, 840 mW including analog input buffer
- Serial Peripheral Interface (SPI)
- Duty cycle stabilizer
- Fast OuT-of-Range (OTR) detection
- Offset binary, two’s complement, gray code
- Power-down mode and Sleep mode
- HVQFN40 package

3. Applications

- Wireless and wired broadband communications
- Portable instrumentation
- Imaging systems
- Digital predistortion loop, power amplifier linearization
- Spectral analysis
- Ultrasound equipment
- Software defined radio

4. Ordering information

Table 1. Ordering information

Type number	f_s (Msps)	Package		
		Name	Description	Version
ADC1115S125HN-C1	125	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-6

5. Block diagram

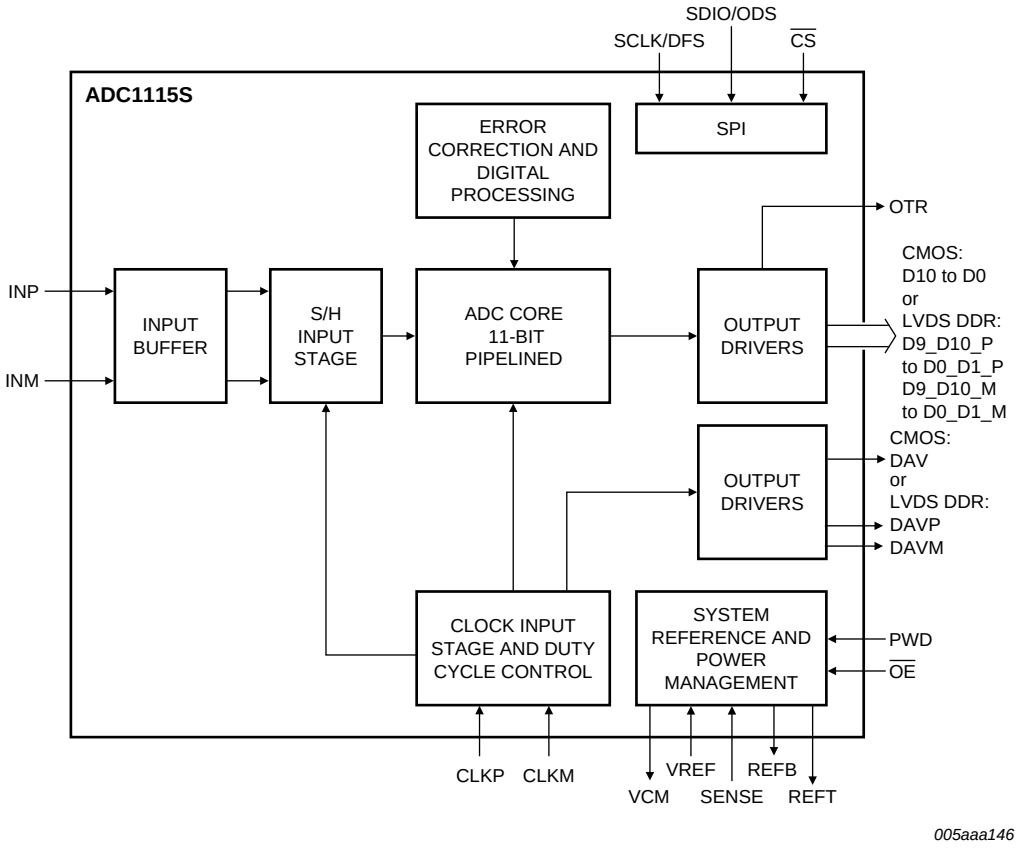


Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

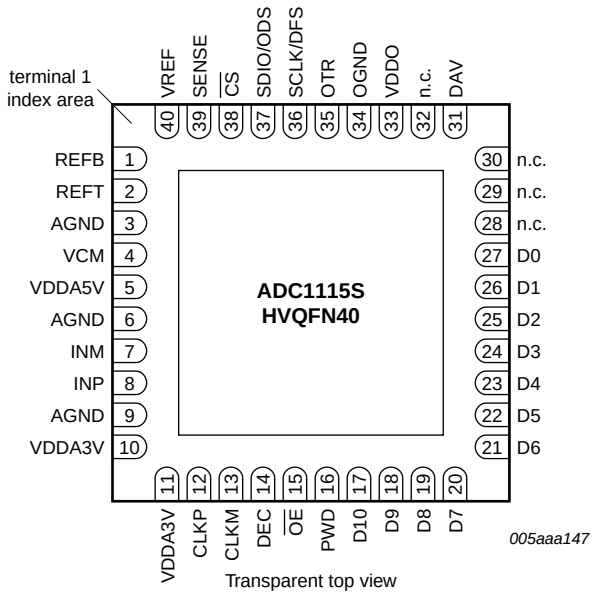


Fig 2. Pin configuration with CMOS digital outputs selected

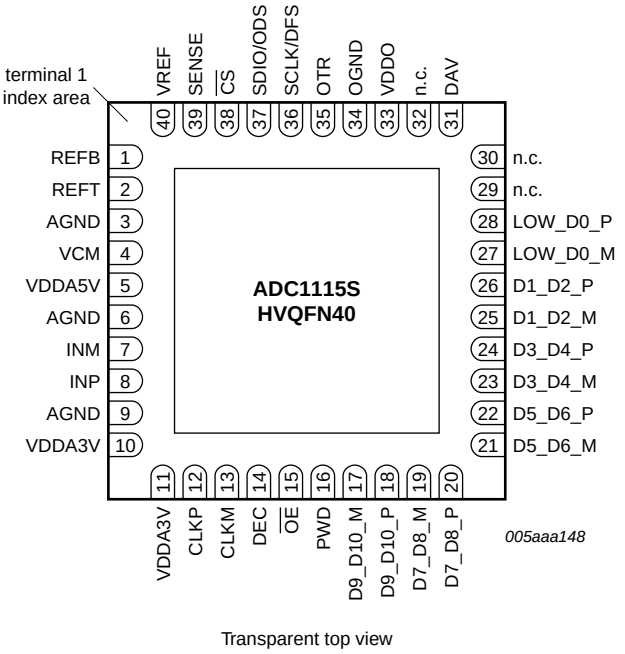


Fig 3. Pin configuration with LVDS/DDR digital outputs selected

6.2 Pin description

Table 2. Pin description (CMOS digital outputs)

Symbol	Pin	Type [1]	Description
REFB	1	O	bottom reference
REFT	2	O	top reference
AGND	3	G	analog ground
VCM	4	O	common-mode output voltage
VDDA5V	5	P	analog power supply 5 V
AGND	6	G	analog ground
INM	7	I	complementary analog input
INP	8	I	analog input
AGND	9	G	analog ground
VDDA3V	10	P	analog power supply 3 V
VDDA3V	11	P	analog power supply 3 V
CLKP	12	I	clock input
CLKM	13	I	complementary clock input
DEC	14	O	regulator decoupling node
$\overline{OE}$	15	I	output enable, active LOW
PWD	16	I	power down, active HIGH

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Table 2. Pin description (CMOS digital outputs) *...continued*

Symbol	Pin	Type [1]	Description
D10	17	O	data output bit 10 (Most Significant Bit (MSB))
D9	18	O	data output bit 9
D8	19	O	data output bit 8
D7	20	O	data output bit 7
D6	21	O	data output bit 6
D5	22	O	data output bit 5
D4	23	O	data output bit 4
D3	24	O	data output bit 3
D2	25	O	data output bit 2
D1	26	O	data output bit 1
D0	27	O	data output bit 0 (Least Significant Bit (LSB))
n.c.	28	-	not connected
n.c.	29	-	not connected
n.c.	30	-	not connected
DAV	31	O	data valid output clock
n.c.	32	-	not connected
VDDO	33	P	output power supply
OGND	34	G	output ground
OTR	35	O	out of range
SCLK/DFS	36	I	SPI clock / data format select
SDIO/ODS	37	I/O	SPI data IO / output data standard
$\overline{CS}$	38	I	SPI chip select
SENSE	39	I	reference programming pin
VREF	40	I/O	voltage reference input/output

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

Table 3. Pin description (LVDS/DDR) digital outputs)

Symbol	Pin [1]	Type [2]	Description
D9_D10_M	17	O	differential output data D9 and D10 multiplexed, complement
D9_D10_P	18	O	differential output data D9 and D10 multiplexed, true
D7_D8_M	19	O	differential output data D7 and D8 multiplexed, complement
D7_D8_P	20	O	differential output data D7 and D8 multiplexed, true
D5_D6_M	21	O	differential output data D5 and D6 multiplexed, complement
D5_D6_P	22	O	differential output data D5 and D6 multiplexed, true
D3_D4_M	23	O	differential output data D3 and D4 multiplexed, complement
D3_D4_P	24	O	differential output data D3 and D4 multiplexed, true
D1_D2_M	25	O	differential output data D1 and D2 multiplexed, complement
D1_D2_P	26	O	differential output data D1 and D2 multiplexed, true
LOW_D0_M	27	O	differential output data D0 multiplexed, complement
LOW_D0_P	28	O	differential output data D0 multiplexed, true
n.c.	29	-	not connected

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Table 3. Pin description *...continued* (LVDS/DDR) digital outputs)

Symbol	Pin [1]	Type [2]	Description
n.c.	30	-	not connected
DAVM	31	O	data valid output clock, complement
DAVP	32	O	data valid output clock, true

[1] Pins 1 to 16 and pins 33 to 40 are the same for both CMOS and LVDS DDR outputs (see Table 2)

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_O	output voltage	pins D10 to D0 or pins D9_D10_P to D0_D1_P and pins D9_D10_M to D0_D1_M	–0.4	+3.9	V
$V_{DDA(3V)}$	analog supply voltage 3 V	on pin VDDA3V	–0.5	+4.6	V
$V_{DDA(5V)}$	analog supply voltage 5 V	on pin VDDA5V	–0.5	+6.0	V
V_{DDO}	output supply voltage		–0.5	+4.6	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	30.5	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	13.3	K/W

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

9. Static characteristics

Table 6. Static characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDA(5V)}$	analog supply voltage 5 V		4.75	5.0	5.25	V
$V_{DDA(3V)}$	analog supply voltage 3 V		2.85	3.0	3.4	V
V_{DDO}	output supply voltage	CMOS mode	1.65	1.8	3.6	V
		LVDS DDR mode	2.85	3.0	3.6	V
$I_{DDA(5V)}$	analog supply current 5 V	f_{clk} = 125 Msps; f_i = 70 MHz	-	46	-	mA

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Table 6. Static characteristics[1] *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA(3V)}$	analog supply current 3 V	f_{clk} = 125 Msps; f_i = 70 MHz	-	205	-	mA
I_{DDO}	output supply current	CMOS mode; f_{clk} = 125 Msps; f_i = 70 MHz	-	11	-	mA
		LVDS DDR mode: f_{clk} = 125 Msps; f_i = 70 MHz	-	39	-	mA
P	power dissipation	analog supply only	-	840	-	mW
		Power-down mode	-	2	-	mW
		Standby mode	-	40	-	mW
Clock inputs: pins CLKP and CLKM						
LVPECL						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	1.6	-	V
SINE wave						
$V_{i(clk)dif}$	differential clock input voltage	peak	-	±3.0	-	V
LVCMOS						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA(3V)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA(3V)}$	-	-	V
Logic inputs: pins PWD and $\overline{OE}$						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	$V_{DDA(3V)}$	V
I_{IL}	LOW-level input current		-	55	-	μA
I_{IH}	HIGH-level input current		-	65	-	μA
Serial peripheral interface: pins $\overline{CS}$, SDIO/ODS, SCLK/DFS						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDA(3V)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA(3V)}$	-	$V_{DDA(3V)}$	V
I_{IL}	LOW-level input current		−10	-	+10	μA
I_{IH}	HIGH-level input current		−50	-	+50	μA
C_I	input capacitance		-	4	-	pF
Digital outputs, CMOS mode: pins D10 to D0, OTR, DAV						
Output levels, V_{DDO} = 3 V						
V_{OL}	LOW-level output voltage		OGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage		$0.8V_{DDO}$	-	V_{DDO}	V
C_O	output capacitance	high impedance; $\overline{OE}$ = HIGH	-	3	-	pF
Output levels, V_{DDO} = 1.8 V						
V_{OL}	LOW-level output voltage		OGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage		$0.8V_{DDO}$	-	V_{DDO}	V
Digital outputs, LVDS mode: pins D9_D10_P to D0_D1_P, D9_D10_M to D0_D1_M, DAVP and DAVM						
Output levels, V_{DDO} = 3 V only, R_{load} = 100 Ω						
$V_{O(offset)}$	output offset voltage	output buffer current set to 3.5 mA	-	1.2	-	V

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Table 6. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(dif)}$	differential output voltage	output buffer current set to 3.5 mA	-	350	-	mV
C_O	output capacitance		-	3	-	pF
Analog inputs: pins INP and INM						
I_I	input current		−5	-	+5	μA
R_I	input resistance		-	550	-	Ω
C_I	input capacitance		-	1.3	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{INP} = V_{INM}$	0.9	1.5	2	V
B_i	input bandwidth		-	600	-	MHz
$V_{I(dif)}$	differential input voltage	peak-to-peak	1		2	V
Common mode output voltage: pin VCM						
$V_{O(cm)}$	common-mode output voltage		-	$0.5V_{DDA(3V)}$	-	V
$I_{O(cm)}$	common-mode output current		-	4	-	mA
I/O reference voltage: pin VREF						
V_{VREF}	voltage on pin VREF	output	-	0.5 to 1	-	V
		input	0.5	-	1	V
Accuracy						
INL	integral non-linearity		-	±0.2	-	LSB
DNL	differential non-linearity	guaranteed no missing codes	-	±0.1	-	LSB
E_{offset}	offset error		-	±2	-	mV
E_G	gain error		-	±0.5	-	%FS
Supply						
PSRR	power supply rejection ratio	200 mV (p-p) on $V_{DDA(3V)}$	-	−54	-	dBc

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V; T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

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10. Dynamic characteristics

10.1 Dynamic characteristics

Table 7. Dynamic characteristics[1]

Symbol	Parameter	Conditions	ADC1115S125			Unit
			Min	Typ	Max	
Analog signal processing						
α_{2H}	second harmonic level	f_i = 3 MHz	-	88	-	dBc
		f_i = 30 MHz	-	87	-	dBc
		f_i = 70 MHz	-	85	-	dBc
		f_i = 170 MHz	-	83	-	dBc
α_{3H}	third harmonic level	f_i = 3 MHz	-	87	-	dBc
		f_i = 30 MHz	-	86	-	dBc
		f_i = 70 MHz	-	84	-	dBc
		f_i = 170 MHz	-	82	-	dBc
THD	total harmonic distortion	f_i = 3 MHz	-	84	-	dBc
		f_i = 30 MHz	-	83	-	dBc
		f_i = 70 MHz	-	81	-	dBc
		f_i = 170 MHz	-	79	-	dBc
ENOB	effective number of bits	f_i = 3 MHz	-	10.7	-	bits
		f_i = 30 MHz	-	10.7	-	bits
		f_i = 70 MHz	-	10.7	-	bits
		f_i = 170 MHz	-	10.6	-	bits
SNR	signal-to-noise ratio	f_i = 3 MHz	-	66.2	-	dBFS
		f_i = 30 MHz	-	66.2	-	dBFS
		f_i = 70 MHz	-	66.0	-	dBFS
		f_i = 170 MHz	-	65.8	-	dBFS
SFDR	spurious-free dynamic range	f_i = 3 MHz	-	87	-	dBc
		f_i = 30 MHz	-	86	-	dBc
		f_i = 70 MHz	-	84	-	dBc
		f_i = 170 MHz	-	82	-	dBc
IMD	Intermodulation distortion	f_i = 3 MHz	-	89	-	dBc
		f_i = 30 MHz	-	88	-	dBc
		f_i = 70 MHz	-	86	-	dBc
		f_i = 170 MHz	-	84	-	dBc

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V; T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

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10.2 Clock and digital output timing

Table 8. Clock and digital output timing characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock timing input: pins CLKP and CLKM							
f_{clk}	clock frequency			100	-	125	MHz
$t_{lat(data)}$	data latency time			-	13.5	-	clock cycles
δ_{clk}	clock duty cycle	DCS_EN = 1		30	50	70	%
		DCS_EN = 0		45	50	55	%
$t_{d(s)}$	sampling delay time			-	0.8	-	ns
t_{wake}	wake-up time			-	76	-	µs
CMOS Mode timing output: pins D10 to D0 and DAV							
t_{PD}	propagation delay	DATA		8.2	9.7	11.3	ns
		DAV		-	3.4	-	ns
t_{su}	set-up time			-	5.6	-	ns
t_h	hold time			-	2.8	-	ns
t_r	rise time	DATA	[2]	0.39	-	2.4	ns
		DAV		0.26	-	2.4	ns
t_f	fall time	DATA	[2]	0.19	-	2.4	ns
LVDS DDR mode timing output: pins D9_D10_P to D0_D1_P, D9_D10_M to D0_D1_M, DAVP and DAVM							
t_{PD}	propagation delay	DATA		2.2	4.0	6.6	ns
		DAV		-	2.2	-	ns
t_{su}	set-up time			-	1.9	-	ns
t_h	hold time			-	1.7	-	ns
t_r	rise time	DATA	[3]	0.5	-	5	ns
		DAV		0.18	-	2.4	ns
t_f	fall time	DATA	[3]	0.15	-	1.6	ns

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V; T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

[2] Measured between 20 % to 80 % of V_{DDO}.

[3] Rise time measured from −50 mV to +50 mV; fall time measured from +50 mV to −50 mV.

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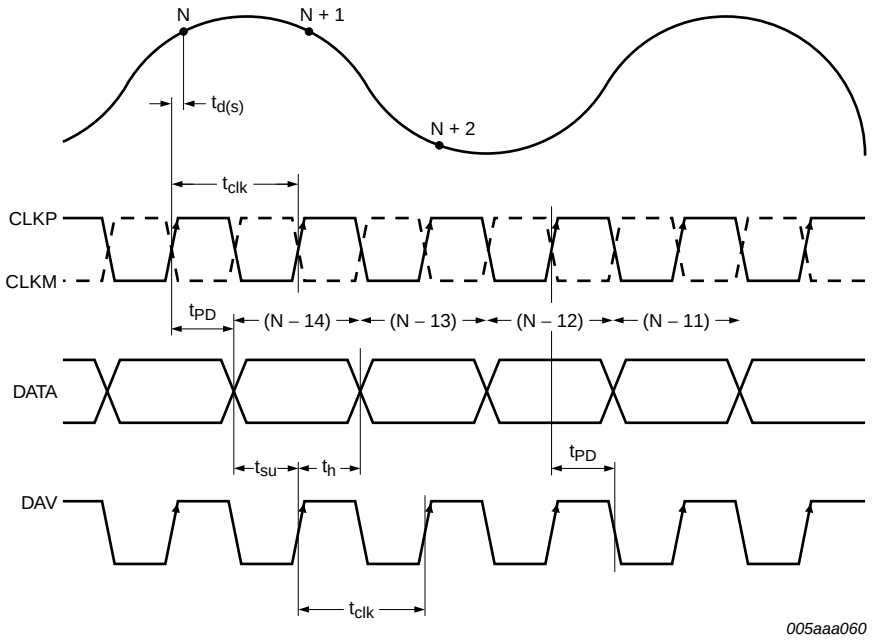


Fig 4. CMOS mode timing

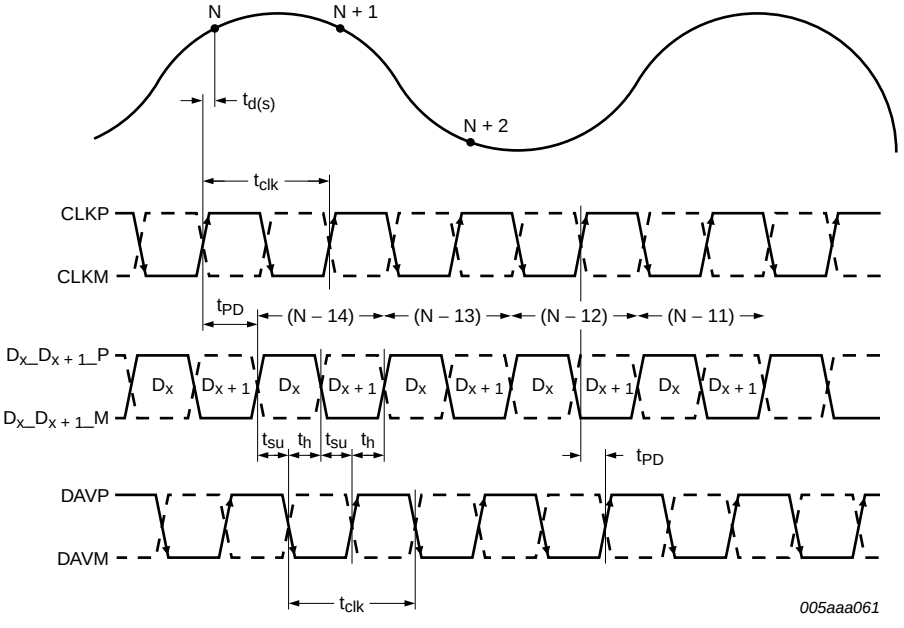


Fig 5. LDVS DDR mode timing

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10.3 SPI timings

Table 9. SPI timings characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		-	40	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		-	16	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		-	16	-	ns
t_{su}	set-up time	data to SCLK HIGH	-	5	-	ns
		$\overline{CS}$ to SCLK HIGH	-	5	-	ns
t_h	hold time	data to SCLK HIGH	-	2	-	ns
		$\overline{CS}$ to SCLK HIGH	-	2	-	ns
$f_{clk(max)}$	maximum clock frequency		-	25	-	MHz

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V.

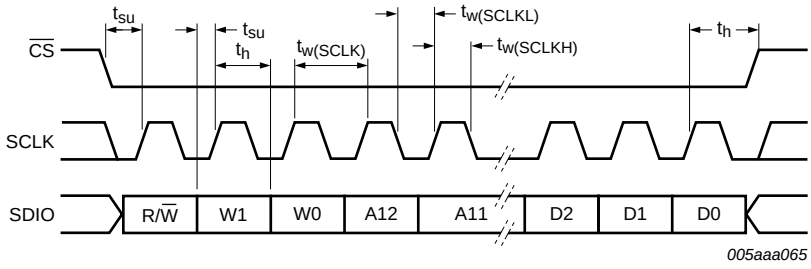
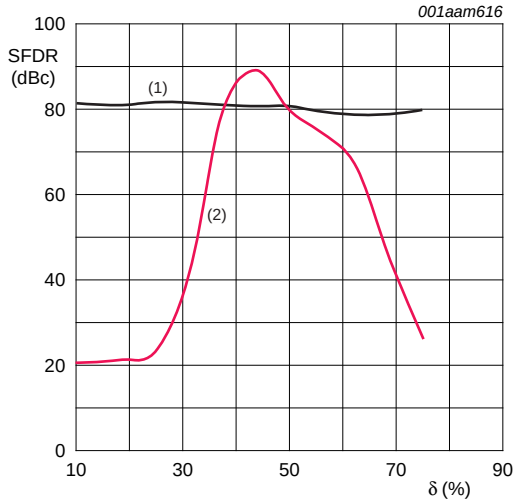


Fig 6. SPI timing

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10.4 Typical characteristics

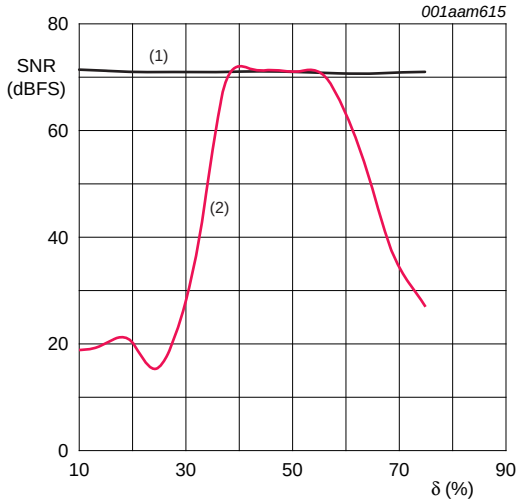


T = 25 °C; V_{DD} = 3 V; f_i = 170 MHz; f_s = 125 Msps

(1) DCS on

(2) DCS off

Fig 7. Spurious-free dynamic range as a function of duty cycle (δ)

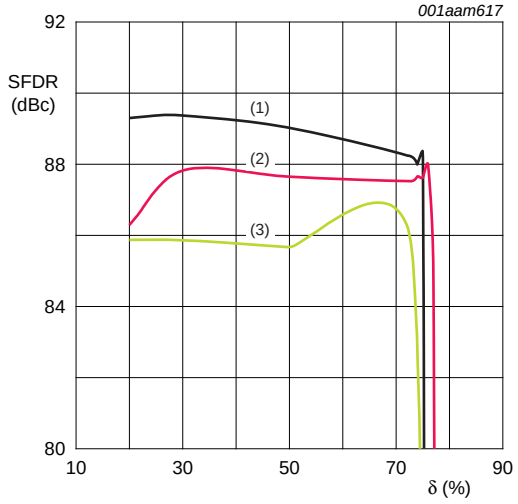


T = 25 °C; V_{DD} = 3 V; f_i = 170 MHz; f_s = 125 Msps

(1) DCS on

(2) DCS off

Fig 8. Signal-to-noise ratio as a function of duty cycle (δ)

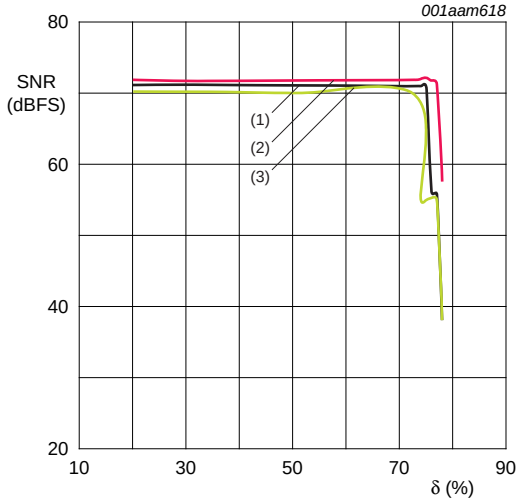


(1) T_{amb} = −40 °C, typical supply voltages

(2) T_{amb} = +25 °C, typical supply voltages

(3) T_{amb} = +90 °C, typical supply voltages

Fig 9. Spurious-free dynamic range as a function of duty cycle (δ)



(1) T_{amb} = −40 °C, typical supply voltages

(2) T_{amb} = +25 °C, /typical supply voltages

(3) T_{amb} = +90 °C, typical supply voltages

Fig 10. Signal-to-noise ratio as a function of duty cycle (δ)

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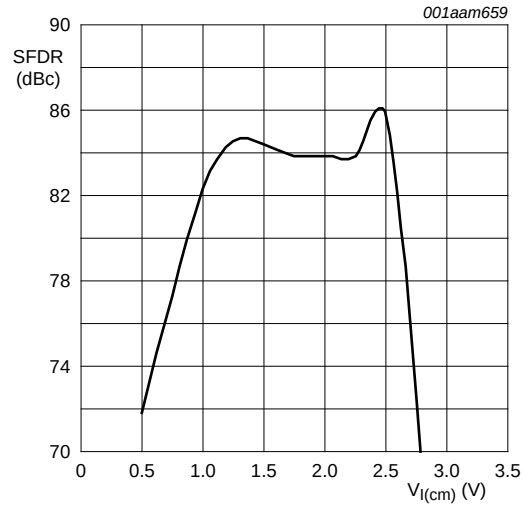


Fig 11. Spurious-free dynamic range as a function of common-mode input voltage ($V_{i(cm)}$)

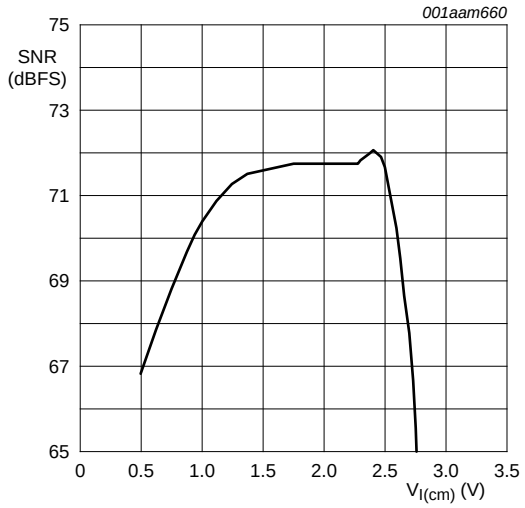


Fig 12. Signal-to-noise ratio as a function of common-mode input voltage ($V_{i(cm)}$)

11. Application information

11.1 Device control

The ADC1115S125 can be controlled via the Serial Peripheral Interface (SPI control mode) or directly via the I/O pins (Pin control mode).

11.1.1 SPI and Pin control modes

The device enters Pin control mode at power-up, and remains in this mode as long as pin $\overline{CS}$ is held HIGH. In Pin control mode, the SPI pins SDIO, $\overline{CS}$ and SCLK are used as static control pins.

SPI control mode is enabled by forcing pin $\overline{CS}$ LOW. Once SPI control mode has been enabled, the device remains in this mode. The transition from Pin control mode to SPI control mode is illustrated in Figure 13.

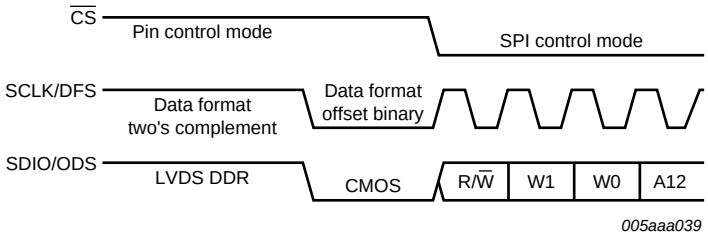


Fig 13. Control mode selection

When the device enters SPI control mode, the output data standard and data format are determined by the level on pin SDIO as soon as a transition is triggered by a falling edge on $\overline{CS}$.

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11.1.2 Operating mode selection

The active ADC1115S125 operating mode (Power-up, Power-down or Sleep) can be selected via the SPI interface (see Table 19) or using pins PWD and $\overline{OE}$ in Pin control mode, as described in Table 10.

Table 10. Operating mode selection via pin PWD and $\overline{OE}$

Pin PWD	Pin $\overline{OE}$	Operating mode	Output high-Z
0	0	Power-up	no
0	1	Power-up	yes
1	0	Sleep	yes
1	1	Power-down	yes

11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see Table 23) or using pin ODS in Pin control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.

11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, two's complement or gray code; see Table 23) or using pin DFS in Pin control mode (offset binary or two's complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, two's complement is selected.

11.2 Analog inputs

11.2.1 Input stage

The analog input of the ADC1115S125 supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs. The ADC inputs are internally biased and need to be decoupled.

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.3 and Table 21).

The equivalent circuit of the input buffer followed by the Sample and Hold (S/H) input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics, is shown in Figure 14.

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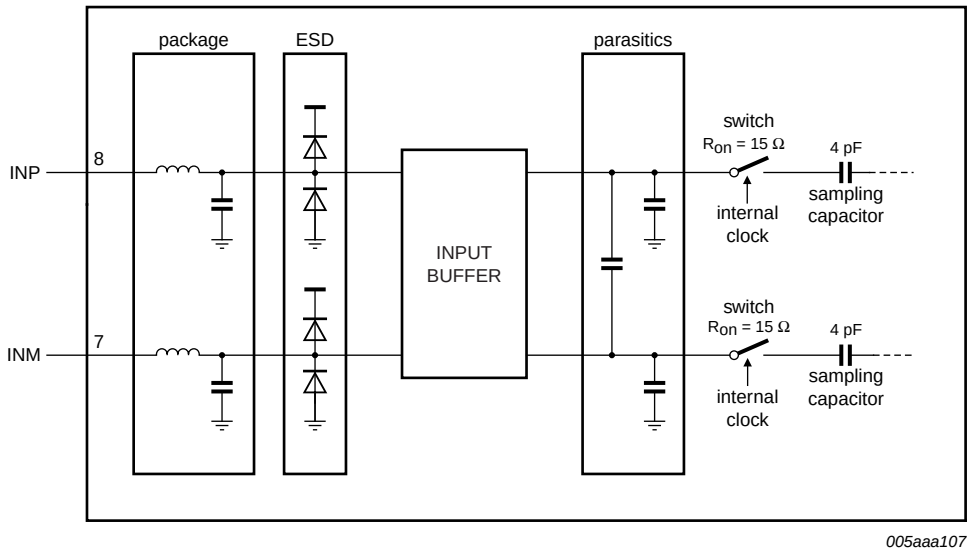


Fig 14. Input sampling circuit and input buffer

The integrated input buffer offers the following advantages:

- The kickback effect is avoided - the charge injection and glitches generated by the S/H input stage are isolated from the input circuitry. So there's no need for additional filtering.
- The input capacitance is very low and constant over a wide frequency range, which makes the ADC1115S125 easy to drive.

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

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11.2.2 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 15 would be suitable for a baseband application.

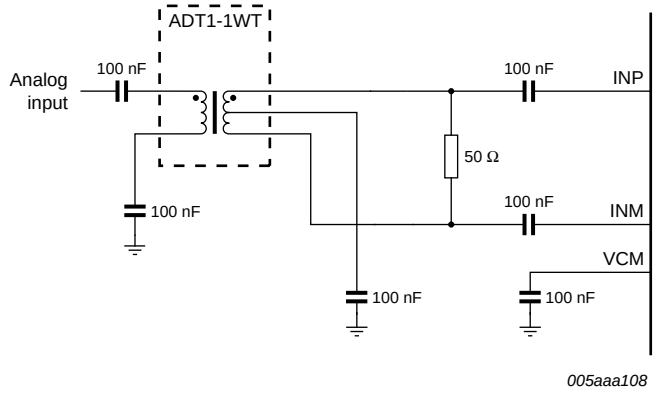


Fig 15. Single transformer configuration suitable for baseband applications

The configuration shown in Figure 16 is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

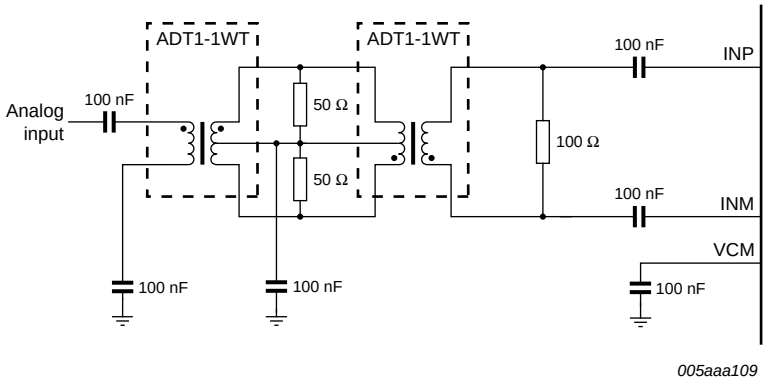


Fig 16. Dual transformer configuration suitable for high intermediate frequency application

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11.3 System reference and power management

11.3.1 Internal/external references

The ADC1115S125 has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (programmable in 1 dB steps between 0 dB and −6 dB via control bits INTREF[2:0] when bit INTREF_EN = logic 1; see Table 21). See Figure 18 to Figure 21. The equivalent reference circuit is shown in Figure 17. External reference is also possible by providing a voltage on pin VREF as described in Figure 20.

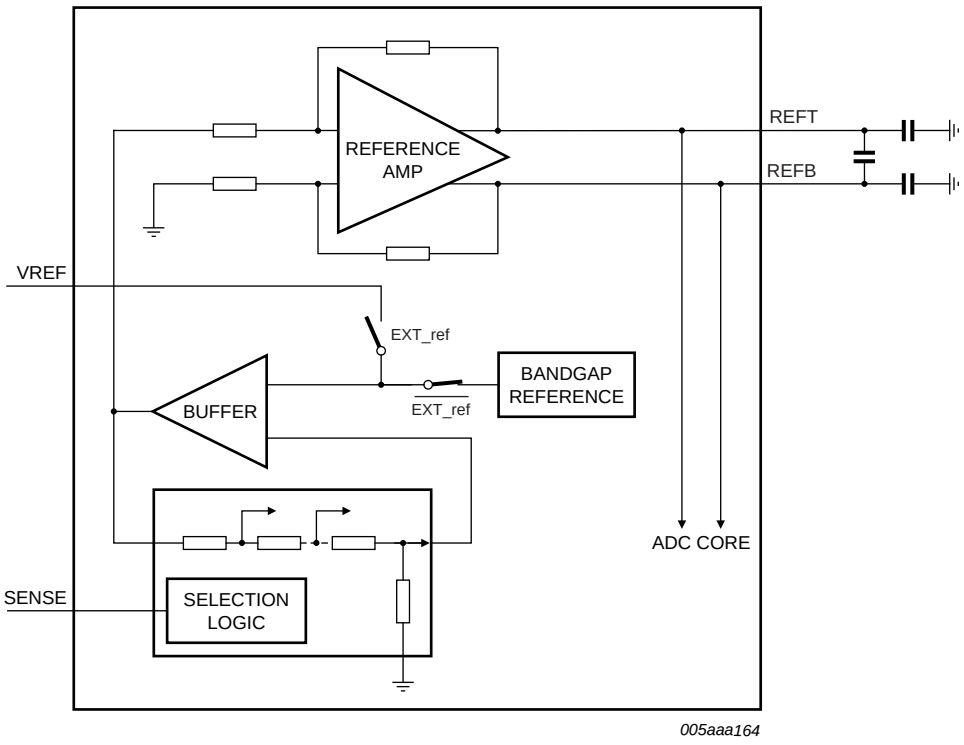


Fig 17. Reference equivalent schematic

If bit INTREF_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in Table 11.

Table 11. Reference selection

Selection	SPI bit INTREF_EN	SENSE pin	VREF pin	Full-scale (p-p)
internal (Figure 18)	0	AGND	330 pF capacitor to AGND	2 V
internal (Figure 19)	0	pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND		1 V
external (Figure 20)	0	$V_{DDA(3V)}$	external voltage between 0.5 V and 1 V[1]	1 V to 2 V
internal via SPI (Figure 21)	1	pin VREF connected to pin SENSE and via 330 pF capacitor to AGND		1 V to 2 V

[1] The voltage on pin VREF is doubled internally to generate the internal reference voltage.

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Figure 18 to Figure 21 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

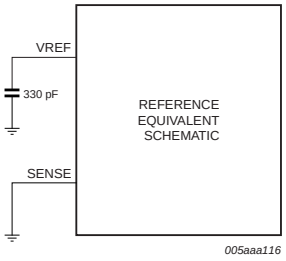


Fig 18. Internal reference, 2 V (p-p) full scale

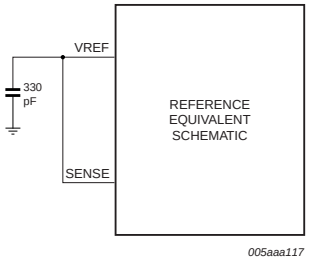


Fig 19. Internal reference, 1 V (p-p) full scale

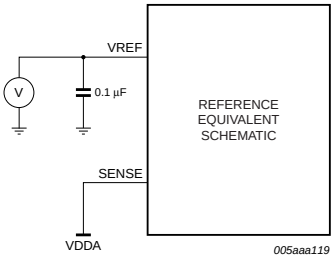


Fig 20. External reference, 1 V (p-p) to 2 V (p-p) full-scale

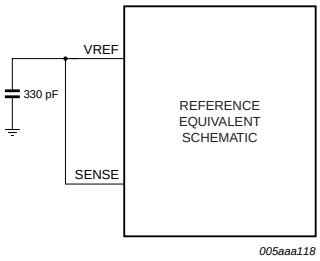


Fig 21. Internal reference via SPI, 1 V (p-p) to 2 V (p-p) full-scale

11.3.2 Programmable full-scale

The full-scale is programmable between 1 V (peak-to-peak) to 2 V (peak-to-peak) (see Table 12).

Table 12. Reference SPI gain control

INTREF	Gain	Full-scale (p-p)
000	0 dB	2 V
001	−1 dB	1.78 V
010	−2 dB	1.59 V
011	−3 dB	1.42 V
100	−4 dB	1.26 V
101	−5 dB	1.12 V
110	−6 dB	1 V
111	reserved	x

11.3.3 Common-mode output voltage ($V_{O(cm)}$)

A 0.1 µF filter capacitor should be connected between pin VCM and ground.

11.3.4 Biasing

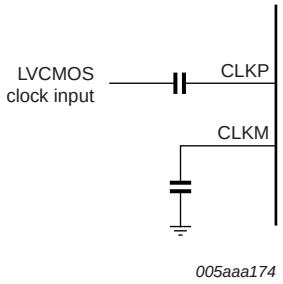
The common-mode input voltage ($V_{I(cm)}$) on pins INP and INM is set internally. The input buffer bias current can be set to one of three levels (high, medium or low) via the SPI (see Table 22).

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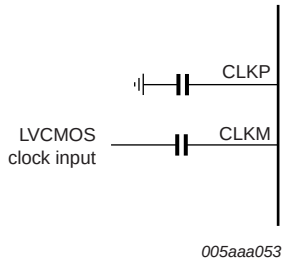
11.4 Clock input

11.4.1 Drive modes

The ADC1115S can be driven differentially (LVPECL). It can also be driven by a single-ended Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) signal connected to pin CLKP (pin CLKM should be connected to ground via a capacitor) or CLKM (pin CLKP should be connected to ground via a capacitor).

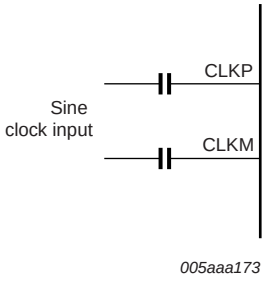


a. Rising edge LVCMOS

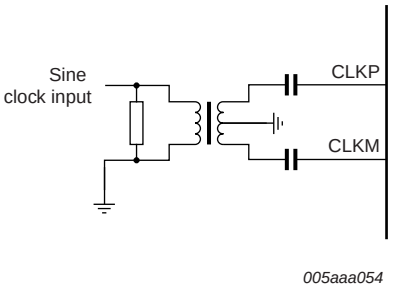


b. Falling edge LVCMOS

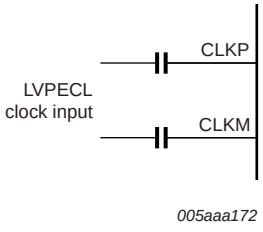
Fig 22. LVCMOS single-ended clock input



a. Sine clock input



b. Sine clock input (with transformer)



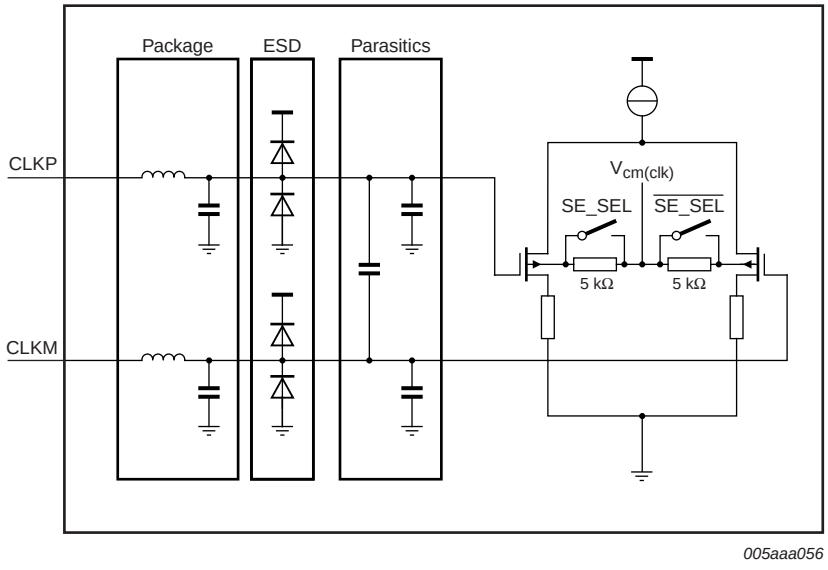
c. LVPECL clock input1

Fig 23. Differential clock input

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11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 24. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.



$V_{cm(clk)}$ = common-mode voltage of the differential input stage.

Fig 24. Equivalent input circuit

Single-ended or differential clock inputs can be selected via the SPI interface (see Table 20). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting bit SE_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

11.4.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS_EN = logic 1; see Table 20), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = logic 0), the input clock signal should have a duty cycle of between 45% and 55%.

11.4.4 Clock input divider

The ADC1115S125 contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = logic 1; see Table 20). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

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11.5 Digital outputs

11.5.1 Digital output buffers: CMOS mode

The digital output buffers can be configured as CMOS by setting bit LVDS_CMOS to logic 0 (see Table 23).

Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in Figure 25. The buffer is powered by a separate OGND/V_{DDO} to ensure 1.8 V to 3.3 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.

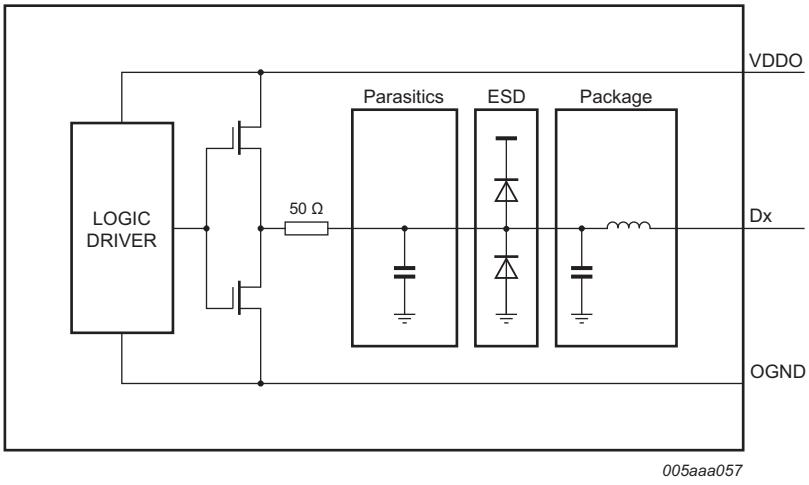


Fig 25. CMOS digital output buffer

The output resistance is 50 Ω and is the combination of the an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both data and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see Table 30):

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11.5.2 Digital output buffers: LVDS DDR mode

The digital output buffers can be configured as LVDS DDR by setting bit LVDS_CMOS to logic 1 (see Table 23).

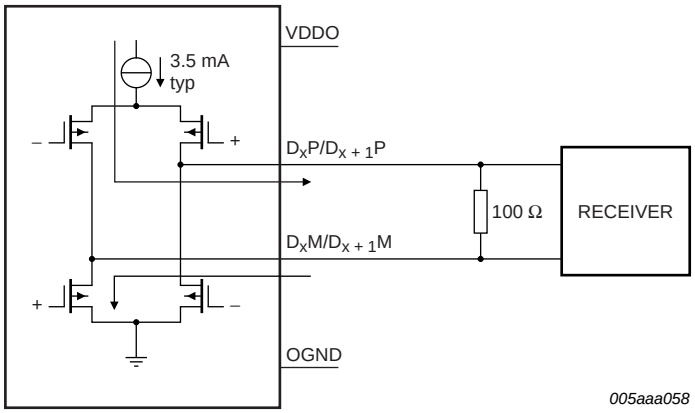


Fig 26. LVDS DDR digital output buffer - externally terminated

Each output should be terminated externally with a 100 Ω resistor (typical) at the receiver side (Figure 26) or internally via SPI control bits LVDS_INT_TER[2:0] (see Figure 27 and Table 32).

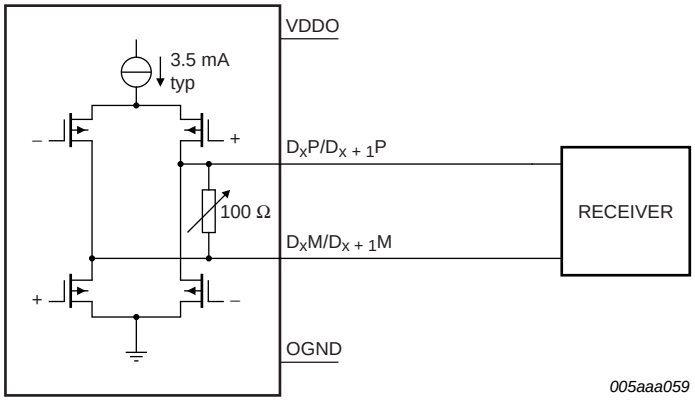


Fig 27. LVDS DDR digital output buffer - internally terminated

The default LVDS DDR output buffer current is set to 3.5 mA. It can be programmed via the SPI (bits DAVI[1:0] and DATAI[1:0]; see Table 31) in order to adjust the output logic voltage levels.

Table 13. LVDS DDR output register 2

LVDS_INT_TER[2:0]	Resistor value (Ω)
000	no internal termination
001	300
010	180
011	110
100	150

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Table 13. LVDS DDR output register 2 *…continued*

LVDS_INT_TER[2:0]	Resistor value (Ω)
101	100
110	81
111	60

11.5.3 DAta Valid (DAV) output clock

A data valid output clock signal (DAV) is provided that can be used to capture the data delivered by the ADC1115S125. Detailed timing diagrams for CMOS and LVDS DDR modes are provided in Figure 4 and Figure 5 respectively.

11.5.4 Out-of-Range (OTR)

An out-of-range signal is provided on pin OTR. The latency of OTR is fourteen clock cycles. The OTR response can be speeded up by enabling Fast OTR (bit FASTOTR = logic 1; see Table 29). In this mode, the latency of OTR is reduced to only four clock cycles. The Fast OTR detection threshold (below full-scale) can be programmed via bits FASTOTR_DET[2:0].

Table 14. Fast OTR register

FASTOTR_DET[2:0]	Detection level (dB)
000	−20.56
001	−16.12
010	−11.02
011	−7.82
100	−5.49
101	−3.66
110	−2.14
111	−0.86

11.5.5 Digital offset

By default, the ADC1115S125 delivers output code that corresponds to the analog input. However it is possible to add a digital offset to the output code via the SPI (bits DIG_OFFSET[5:0]; see Table 25).

11.5.6 Test patterns

For test purposes, the ADC1115S125 can be configured to transmit one of a number of predefined test patterns (via bits TESTPAT_SEL[2:0]; see Table 26). A custom test pattern can be defined by the user (TESTPAT_USER; see Table 27 and Table 28) and is selected when TESTPAT_SEL[2:0] = 101. The selected test pattern is transmitted regardless of the analog input.

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11.5.7 Output codes versus input voltage

Table 15. Output codes

$V_{INP} - V_{INM}$	Offset binary	Two's complement	OTR pin
< −1	000 0000 0000	100 0000 0000	1
−1.0000000	000 0000 0000	100 0000 0000	0
−0.9990234	000 0000 0001	100 0000 0001	0
−0.9980469	000 0000 0010	100 0000 0010	0
−0.9970703	000 0000 0011	100 0000 0011	0
−0.996093	000 0000 0100	100 0000 0100	0
....	....	....	0
−0.0019531	011 1111 1110	111 1111 1110	0
−0.0009766	011 1111 1111	111 1111 1111	0
0.0000000	**100 0000 0000**	**000 0000 0000**	0
+0.0009766	100 0000 0001	000 0000 0001	0
+0.0019531	100 0000 0010	000 0000 0010	0
....	....	....	0
+0.9960938	111 1111 1011	011 1111 1011	0
+0.9970703	111 1111 1100	011 1111 1100	0
+0.9980469	111 1111 1101	011 1111 1101	0
+0.9990234	111 1111 1110	011 1111 1110	0
+1.0000000	111 1111 1111	011 1111 1111	0
> +1	111 1111 1111	011 1111 1111	1

11.6 Serial Peripheral Interface (SPI)

11.6.1 Register description

The ADC1115S125 serial interface is a synchronous serial communications port that allows easy interfacing with many commonly-used microprocessors. It provides access to the registers that control the operation of the chip.

This interface is configured as a 3-wire type (SDIO as bidirectional pin)

Pin SCLK is the serial clock input and $\overline{CS}$ is the chip select pin.

Each read/write operation is initiated by a LOW level on CS. A minimum of three bytes is transmitted (two instruction bytes and at least one data byte). The number of data bytes is determined by the value of bits W1 and W2 (see Table 17).

Table 16. Instruction bytes for the SPI

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/$\overline{W}$[1]	W1[2]	W0[2]	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

[1] Bit R/$\overline{W}$ indicates whether it is a read (logic 1) or a write (logic 0) operation.

[2] Bits W1 and W0 indicate the number of bytes to be transferred after the instruction byte (see Table 17).

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Table 17. Number of data bytes to be transferred after the instruction bytes

W1	W0	Number of bytes transmitted
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 bytes or more

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is increased to access subsequent addresses.

The steps involved in a data transfer are as follows:

1. A falling edge on $\overline{CS}$ in combination with a rising edge on SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but is always a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on $\overline{CS}$ indicates the end of data transmission.

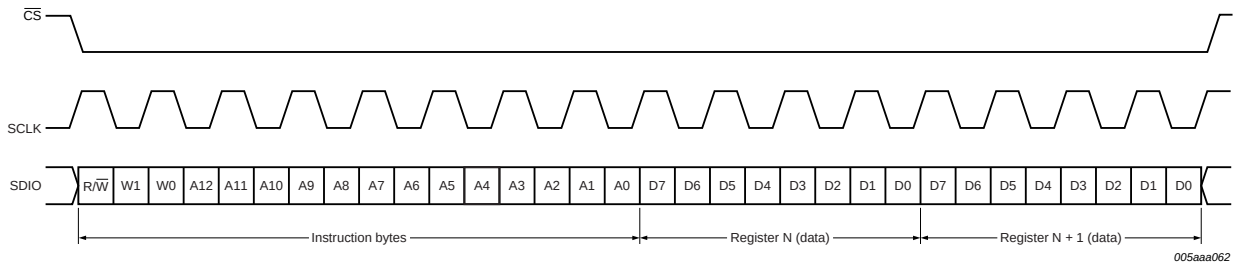


Fig 28. SPI mode timing

11.6.2 Default modes at start-up

During circuit initialization, it does not matter which output data standard has been selected. At power-up, the device enters Pin control mode.

A falling edge on $\overline{CS}$ triggers a transition to SPI control mode. When the ADC1115S125 enters SPI control mode, the output data standard (CMOS/LVDS DDR) is determined by the level on pin SDIO (see Figure 29). Once in SPI control mode, the output data standard can be changed via bit LVDS/CMOS in Table 23.

When the ADC1115S125 enters SPI control mode, the output data format (two's complement or offset binary) is determined by the level on pin SCLK (gray code can only be selected via the SPI). Once in SPI control mode, the output data format can be changed via bit DATA_FORMAT[1:0] in Table 23.

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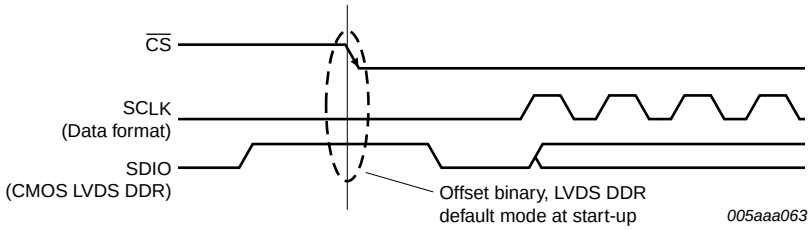


Fig 29. Default mode at start-up: SCLK LOW = offset binary; SDIO HIGH = LVDS DDR

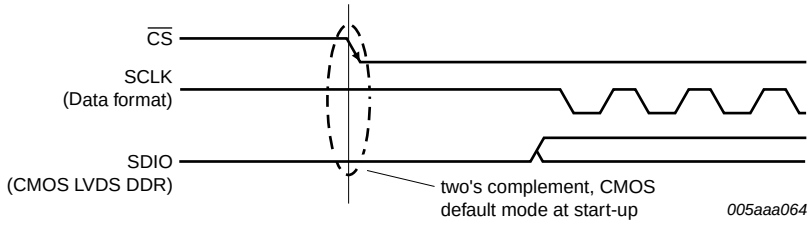


Fig 30. Default mode at start-up: SCLK HIGH = two's complement; SDIO LOW = CMOS

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11.6.3 Register allocation map

Table 18. Register allocation map

Addr. Hex	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin
0005	Reset and operating mode	R/W	SW_RST	RESERVED[2:0]			-	-	OP_MODE[1:0]		0000 0000
0006	Clock	R/W	-	-	-	SE_SEL	DIFF_SE	-	CLKDIV	DCS_EN	0000 0001
0008	Internal reference	R/W	-	-	-	-	INTREF_EN	INTREF[2:0]			0000 0000
0010	Input buffer	R/W	-	-	-	-	-	-	IB_IBIAS[1:0]	-	0000 0011
0011	Output data standard.	R/W	-	-	-	LVDS_CMOS	OUTBUF	OUTBUS_SWAP	DATA_FORMAT[1:0]		0000 0000
0012	Output clock	R/W	-	-	-	-	DAVINV	DAVPHASE[2:0]			0000 1110
0013	Offset	R/W	-	-	DIG_OFFSET[5:0]						0000 0000
0014	Test pattern 1	R/W	-	-	-	-	-	TESTPAT_SEL[2:0]			0000 0000
0015	Test pattern 2	R/W	TESTPAT_USER[10:3]								0000 0000
0016	Test pattern 3	R/W	TESTPAT_USER[2:0]			-	-	-	-	-	0000 0000
0017	Fast OTR	R/W	-	-	-	-	FASTOTR	FASTOTR_DET[2:0]			0000 0000
0020	CMOS output	R/W	-	-	-	-	DAV_DRV[1:0]		DATA_DRV[1:0]		0000 1110
0021	LVDS DDR O/P 1	R/W	-	-	DAVI_x2_EN	DAVI[1:0]		DATAI_x2_EN	DATAI[1:0]		0000 0000
0022	LVDS DDR O/P 2	R/W	-	-	-	-	BIT_BYTE_WISE	LVDS_INT_TER[2:0]			0000 0000

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Table 19. Reset and operating mode control register (address 0005h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W		reset digital section
			0	**no reset**
			1	performs a reset on SPI registers
6 to 4	RESERVED[2:0]		**000**	**reserved**
3 to 2	-		00	not used
1 to 0	OP_MODE[1:0]	R/W		operating mode
			00	**normal (Power-up)**
			01	Power-down
			10	Sleep
			11	normal (Power-up)

Table 20. Clock control register (address 0006h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	-		000	not used
4	SE_SEL	R/W		single-ended clock input pin select
			0	**CLKM**
			1	CLKP
3	DIFF_SE	R/W		differential/single ended clock input select
			0	**fully differential**
			1	single-ended
2	-		0	not used
1	CLKDIV	R/W		clock input divide by 2
			0	**disabled**
			1	enabled
0	DCS_EN	R/W		duty cycle stabilizer
			0	disabled
			1	**enabled**

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Table 21. Internal reference control register (address 0008h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	INTREF_EN	R/W		programmable internal reference enable
			0	**disable**
			1	active
2 to 0	INTREF[2:0]	R/W		programmable internal reference
			000	**0 dB (FS = 2 V)**
			001	−1 dB (FS = 1.78 V)
			010	−2 dB (FS = 1.59 V)
			011	−3 dB (FS = 1.42 V)
			100	−4 dB (FS = 1.26 V)
			101	−5 dB (FS = 1.12 V)
			110	−6 dB (FS = 1 V)
			111	reserved

Table 22. Input buffer control register (address 0010h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	-		000000	not used
1 to 0	IB_IBIAS[1:0]	R/W		input buffer bias current
			00	not used
			01	medium
			10	low
			11	**high**

Table 23. Output data standard control register (address 0011h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	-		000	not used
4	LVDS_CMOS	R/W		output data standard: LVDS DDR or CMOS
			0	**CMOS**
			1	LVDS DDR
3	OUTBUF	R/W		output buffers enable
			0	**output enabled**
			1	output disabled (high Z)
2	OUTBUS_SWAP	R/W		output bus swapping
			0	**no swapping**
			1	output bus is swapped (MSB becomes LSB and vice versa)

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Table 23. Output data standard control register (address 0011h) bit description *…continued*
Default values are highlighted.

Bit	Symbol	Access	Value	Description
1 to 0	DATA_FORMAT[1:0]	R/W		output data format
			00	**offset binary**
			01	two's complement
			10	gray code
			11	offset binary

Table 24. Output clock register (address 0012h) bit description
Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	DAVINV	R/W		output clock data valid (DAV) polarity
			0	normal
			1	**inverted**
2 to 0	DAVPHASE[2:0]	R/W		DAV phase select
			000	output clock shifted (ahead) by 3 ns
			001	output clock shifted (ahead) by 2.5 ns
			010	output clock shifted (ahead) by 2 ns
			011	output clock shifted (ahead) by 1.5 ns
			100	output clock shifted (ahead) by 1 ns
			101	output clock shifted (ahead) by 0.5 ns
			110	**default value as defined in timing section**
			111	output clock shifted (delayed) by 0.5 ns

Table 25. Offset register (address 0013h) bit description
Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	-		00	not used
5 to 0	DIG_OFFSET[5:0]	R/W		digital offset adjustment
			011111	+31 LSB
			...	...
			000000	**0**
			...	...
			100000	–32 LSB

Table 26. Test pattern register 1 (address 0014h) bit description
Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-		00000	not used

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Table 26. Test pattern register 1 (address 0014h) bit description *…continued*

Default values are highlighted.

Bit	Symbol	Access	Value	Description
2 to 0	TESTPAT_SEL[2:0]	R/W		digital test pattern select
			000	**off**
			001	mid scale
			010	–FS
			011	+FS
			100	toggle ‘1111..1111’/’0000..0000’
			101	custom test pattern
			110	‘1010..1010.’
			111	‘010..1010’

Table 27. Test pattern register 2 (address 0015h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	TESTPAT_USER[10:3]	R/W	**00000000**	**custom digital test pattern (bits 10 to 3)**

Table 28. Test pattern register 3 (address 0016h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	TESTPAT_USER[2:0]	R/W	**000**	**custom digital test pattern (bits 2 to 0)**
4 to 0	-		00000	not used

Table 29. Fast OTR register (address 0017h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	FASTOTR	R/W		fast Out-of-Range (OTR) detection
			0	**disabled**
			1	enabled
2 to 0	FASTOTR_DET[2:0]	R/W		set fast OTR detect level
			000	**–20.56 dB**
			001	–16.12 dB
			010	–11.02 dB
			011	–7.82 dB
			100	–5.49 dB
			101	–3.66 dB
			110	–2.14 dB
			111	–0.86 dB

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Table 30. CMOS output register (address 0020h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3 to 2	DAV_DRV[1:0]	R/W		drive strength for DAV CMOS output buffer
			00	low
			01	medium
			10	high
			11	**very high**
1 to 0	DATA_DRV[1:0]	R/W		drive strength for DATA CMOS output buffer
			00	low
			01	medium
			10	**high**
			11	very high

Table 31. LVDS DDR output register 1 (address 0021h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	-		00	not used
5	DAVI_x2_EN	R/W		double LVDS current for DAV LVDS buffer
			0	**disabled**
			1	enabled
4 to 3	DAVI[1:0]	R/W		LVDS current for DAV LVDS buffer
			00	**3.5 mA**
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA
2	DATAI_x2_EN	R/W		double LVDS current for DATA LVDS buffer
			0	**disabled**
			1	enabled
1 to 0	DATAI[1:0]	R/W		LVDS current for DATA LVDS buffer
			00	**3.5 mA**
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA

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Table 32. LVDS DDR output register 2 (address 0022h) bit description

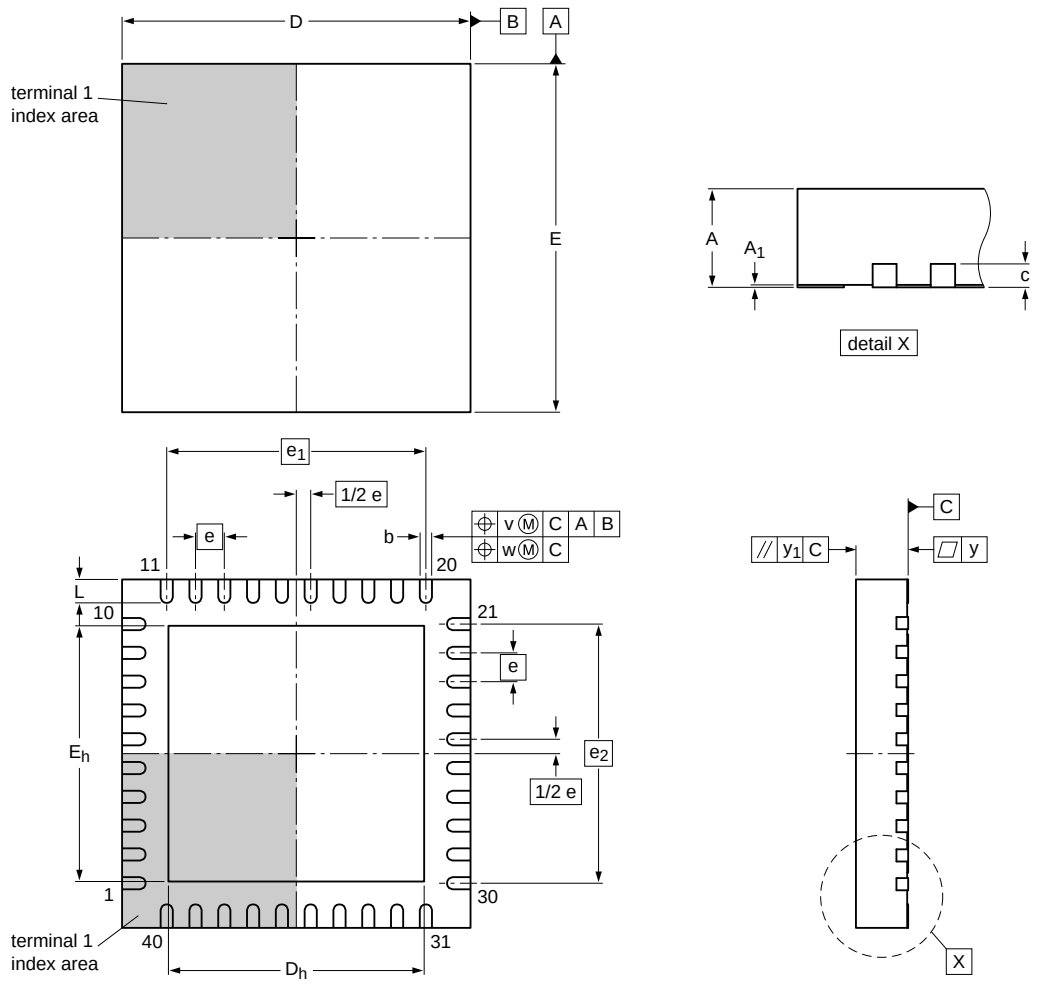
Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-		0000	not used
3	BIT/BYTE_WISE	R/W		DDR mode for LVDS output
			0	**bit wise (even data bits output on DAV rising edge / odd data bits output on DAV falling edge)**
			1	byte wise (MSB data bits output on DAV rising edge / LSB data bits output on DAV falling edge)
2 to 0	LVDS_INTTER[2:0]	R/W		internal termination for LVDS buffer (DAV and DATA)
			000	**no internal termination**
			001	300 Ω
			010	180 Ω
			011	110 Ω
			100	150 Ω
			101	100 Ω
			110	81 Ω
			111	60 Ω

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12. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-6**



Dimensions

Unit		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
	max	1.00	0.05	0.30		6.1	4.55	6.1	4.55				0.5				
mm	nom	0.85	0.02	0.21	0.2	6.0	4.40	6.0	4.40	0.5	4.5	4.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	4.25	5.9	4.25				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-6_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-6		MO-220	- - -			~~09-02-23~~ 09-03-04

Fig 31. Package outline SOT618-6 (HVQFN40)

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13. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1115S125 v.3	20120702	Product data sheet	-	ADC1115S125 v.2
ADC1115S125 v.2	20101217	Product data sheet	-	ADC1115S125 v.1
Modifications:	• Data sheet status changed from Preliminary to Product. • Text and drawings updated throughout entire data sheet. • Section 10.4 “Typical characteristics” added to the data sheet.			
ADC1115S125 v.1	20100412	Preliminary data sheet	-	-

14. Contact information

For more information or sales office addresses, please visit: **http://www.idt.com**

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