SLUS374C − JULY 1999 − REVISED NOVEMBER 2005

3-V TO 8-V HOT SWAP POWER MANAGER

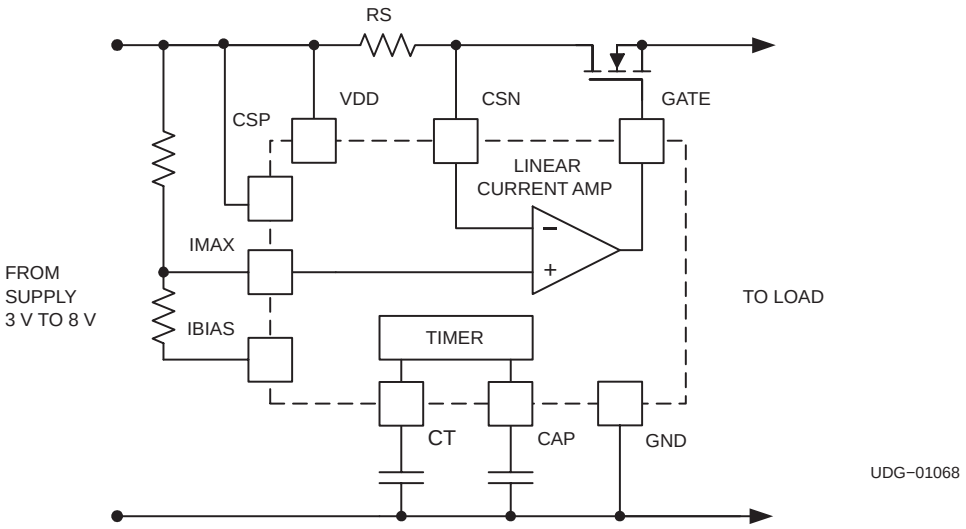
FEATURES

- **Precision Fault Threshold**
- **Charge Pump for Low $R_{DS(on)}$ High Side Drive**
- **Differential Sense Inputs**
- **Programmable Average Power Limiting**
- **Programmable Linear Current Control**
- **Programmable Fault Time**
- **Fault Output Indicator**
- **Manual and Automatic Reset Modes**
- **Shutdown Control With Programmable Softstart**
- **Undervoltage Lockout**
- **Electronic Circuit Breaker Function**

DESCRIPTION

The UCC3919 family of hot swap power managers provide complete power management, hot swap, and fault handling capability. The UCC3919 features a duty ratio current limiting technique, which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. The UCC3919 has two reset modes, selected with the TTL/CMOS compatible L/R pin. In one mode, when a fault occurs the IC repeatedly tries to reset itself at a user defined rate, with user defined maximum output current and pass transistor power dissipation. In the other mode the output latches off and stays off until either the L/R pin is reset or the shutdown pin is toggled. The on board charge pump circuit provides the necessary gate voltage for an external N-channel power FET.

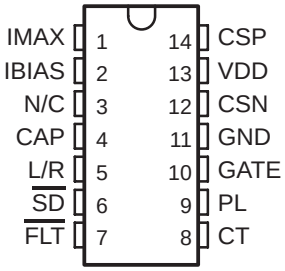
TYPICAL APPLICATION DIAGRAM



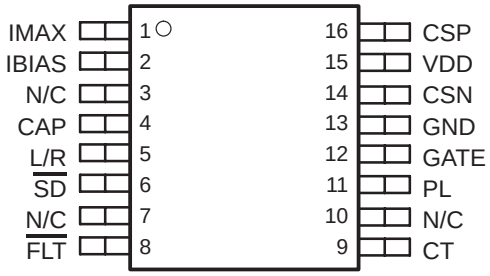
AVAILABLE OPTIONS

T_J	PACKAGE DEVICES		
	D PACKAGE	N PACKAGE	PW PACKAGE
0°C to 70°C	UCC3919D	UCC3919N	UCC3919PW
−40°C to 85°C	UCC2919D	UCC2919N	UCC2919PW

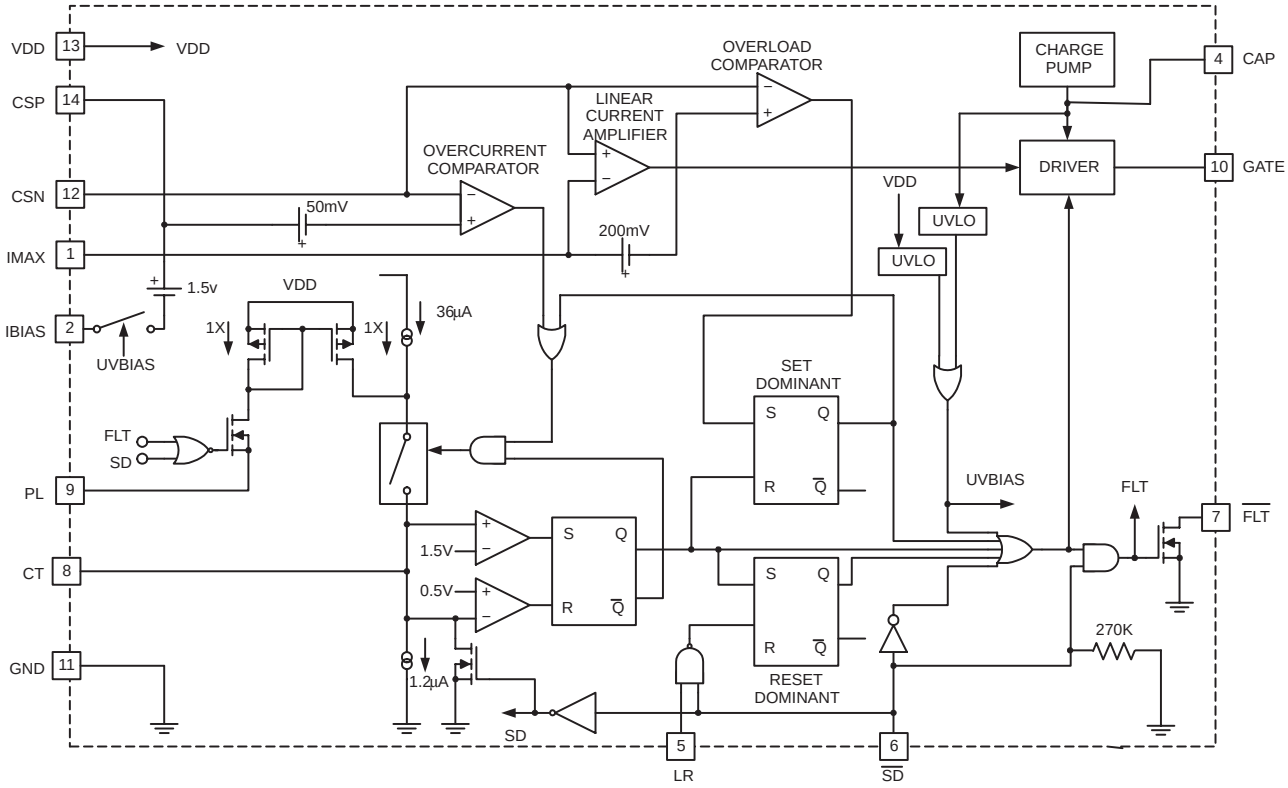
N PACKAGE
TOP VIEW



D AND PW PACKAGES
(TOP VIEW)



functional block diagram



NOTE: Pins shown for 14-pin package.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

VDD . . . . . –0.3 V to 10 V
Pin voltage (all pins except CAP and GATE) . . . . . –0.3 V to VDD + 0.3 V
Pin voltage (CAP and GATE) . . . . . –0.3 V to 18 V
PL current . . . . . 0.5 mA to –10 mA
IBIAS current . . . . . 0 mA to 3 mA
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Junction temperature, T_J . . . . . –55°C to 150°C
Lead temperature (soldering, 10sec.) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

electrical characteristics, VDD = 5 V, T_A = 0°C to 70°C for the UCC3919, –40°C to 85°C for the UCC2919, all voltages are with respect to GND, $T_A = T_J$, (unless otherwise specified)

input supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current	VDD = 3 V		0.5	1	mA
	VDD = 8 V		1	1.5	mA
Shutdown current	$\overline{SD}$ = 0.2 V		1	7	µA

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Minimum voltage to start		2.35	2.75	3	V
Minimum voltage after start		1.9	2.25	2.5	V
Hysteresis		0.25	0.5	0.75	V

IBIAS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output voltage, (0 µA < I_{OUT} < 15 µA)	25°C, referred to CSP	1.47	1.5	1.53	V
	Over temperature range, referred to CSP	1.44	1.5	1.56	V
Maximum output current		1	2		mA

electrical characteristics, VDD = 5 V, T_A = 0°C to 70°C for the UCC3919, –40°C to 85°C for the UCC2919, all voltages are with respect to GND, $T_A = T_J$, (unless otherwise specified)

current sense

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Over current comparator offset	Referred to CSP,		3 V ≤ VDD ≤ 8 V	–55	–50	–45	mV
Linear current amplifier offset	V_{IMAX} = 100 mV,	referred to CSP,	3 V ≤ VDD ≤ 8 V	–120	–100	–80	mV
	V_{IMAX} = 400 mV,	referred to CSP,	3 V ≤ VDD ≤ 8 V	–440	–400	–360	mV
Overload comparator offset	V_{IMAX} = 100 mV,	referred to CSP,	3 V ≤ VDD ≤ 8 V	–360	–300	–240	mV
CSN input common mode voltage range	Referred to VDD,	3 V ≤ VDD ≤ 8 V,	See Note 1	–1.5		0.2	V
CSP input common mode voltage range	Referred to VDD,	3 V ≤ VDD ≤ 8 V,	See Note 1	0		0.2	V
Input bias current CSN					1	5	µA
Input bias current CSP					100	200	µA

current fault timer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CT charge current	V_{CT} = 1 V	–56	–35	–16	µA
CT discharge current	V_{CT} = 1 V	0.5	1.2	1.9	µA
On time duty cycle in fault	I_{PL} = 0	1.5	3	6	%
CT fault threshold		1.0	1.5	1.7	V
CT reset threshold		0.25	0.5	0.75	V

IMAX

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input bias current	V_{IMAX} = 100 mV,	referred to CSP	–1	0	1	µA

power limiting

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Voltage on PL	I_{PL} = –250 µA,	referred to VDD	–1.0	–1.4	–1.9	V
	I_{PL} = –1.5 mA,	referred to VDD	–0.5	–1.8	–2.2	V
On time duty cycle in fault	I_{PL} = –250 µA		0.25	0.5	1	%
	I_{PL} = –1.5 mA		0.05	0.1	0.2	%

NOTES: 1. Ensured by design. Not 100% production tested.

electrical characteristics, VDD = 5 V, T_A = 0°C to 70°C for the UCC3919, –40°C to 85°C for the UCC2919, all voltages are with respect to GND, $T_A = T_J$, (unless otherwise specified)

$\overline{SD}$ and L/R inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage low				0.8	V
Input voltage high		2			V
L/R input current		1	3	6	µA
$\overline{SD}$ internal pulldown impedance		100	270	500	kΩ

$\overline{FLT}$ output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output leakage current	VDD = 5 V			10	µA
Output low voltage	I_{OUT} = 10 mA			1	V

FET gate driver and charge pump

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak output current	V_{CAP} = 15 V,	V_{GATE} = 10 V	–3	–1	–0.25	mA
Peak sink current	V_{GATE} = 5 V			20		mA
Fault delay				100	300	ns
Maximum output voltage	VDD = 3 V,	average I_{OUT} = 1 µA	8	10	12	V
	VDD = 8 V,	average I_{OUT} = 1 µA	12	14	16	V
Charge pump UVLO minimum voltage to start	VDD = 3 V		6.5	8.8	10.1	V
	VDD = 8 V		6.5	9.9	11.5	V
Charge pump source impedance	VDD = 5 V,	average I_{OUT} = 1 µA	50	100	150	kΩ

pin descriptions

CAP

A capacitor is placed from this pin to ground to filter the output of the on board charge pump. A 0.01-µF to 0.1-µF capacitor will work in most applications. Refer to TI literature number SLUA339 application note, *Sizing the UCC3919 Charge−Pump Capacitor*, to determine the exact capacitance.

CSN

The negative current sense input signal.

CSP

The positive current sense input signal. Input to the duty cycle timer.

CT

Input to the duty cycle timer. A capacitor is connected from this pin to ground, setting the off time and maximum on time of the over-current protection circuit.

$\overline{FLT}$

Fault indicator. This open drain output will pull low under any fault condition where the output driver is disabled. This output is disabled when the IC is in low current standby mode.

pin descriptions (continued)

GATE

The output of the linear current amplifier. This pin drives the gate of an external N-channel MOSFET pass transistor. The linear current amplifier control loop is internally compensated, and ensured stable for output load (gate) capacitance between 100 pF and 0.01 μF. In applications where the GATE voltage (or charge pump voltage) exceeds the maximum gate-to-source voltage ratings (VGS) for the external N-channel MOSFET, a Zener clamp may be added to the gate of the MOSFET. No additional series resistance is required since the internal charge pump has a finite output impedance of 100-kΩ typical.

GND

The ground reference for the device.

IBIAS

Output of the on board bias generator internally regulated to 1.5 V below CSP. A resistor divider between this pin and CSP can be used to generate the IMAX voltage. The bias circuit is internally compensated, and requires no bypass capacitance. If an external bypass is required due to a noisy environment, the circuit will be stable with up to 0.001 μF of capacitance. The bypass must be to CSP, since the bias voltage is generated with respect to CSP. Resistor R2 (Figure 5) should be greater than 50 kΩ to minimize the effect of the finite input impedance of the IBIAS pin on the IMAX threshold.

IMAX

Used to program the maximum allowable sourcing current. The voltage on this pin is with respect to CSP. If the voltage across the shunt resistor exceeds this voltage the linear current amplifier lowers the voltage at GATE to limit the output current to this level. If the voltage across the shunt resistor goes more than 200 mV beyond this voltage, the gate drive pin GATE is immediately driven low and kept low for one full off time interval.

L/R

Latch/Reset. This pin sets the reset mode. If L/R is low and a fault occurs the device will begin duty ratio current limiting. If L/R is high and a fault occurs, GATE will go low and stay low until L/R is set low. This pin is internally pulled low by a 3-μA nominal pulldown.

PL

Power Limit. This pin is used to control average power dissipation in the external MOSFET. If a resistor is connected from this pin to the source of the external MOSFET, the current in the resistor will be roughly proportional to the voltage across the FET. As the voltage across the FET increases, this current is added to the fault timer charge current, reducing the on time duty cycle from its nominal value of 3% and limiting the average power dissipation in the FET.

$\overline{\text{SD}}$

Shutdown pin. If this pin is taken low, GATE will go low, and the IC will go into a low current standby mode and CT will be discharged. This TTL compatible input must be driven high to turn on.

VDD

The power connection for the device.

APPLICATION INFORMATION

The UCC3919 monitors the voltage drop across a high side sense resistor and compares it against three different voltage thresholds. These are discussed below. Figure 1 shows the UCC3919 waveforms under fault conditions.

fault threshold

The first threshold is fixed at 50 mV. If the current is high enough such that the voltage on CSN is 50 mV below CSP, the timing capacitor C_T begins to charge at about 35 μA if the PL pin is open. (Power limiting will be discussed later). If this threshold is exceeded long enough for C_T to charge to 1.5 V, a fault is declared and the external MOSFET will be turned off. It will either be latched off (until the power to the circuit is cycled, the L/R pin is taken low, or the $\overline{SD}$ pin is toggled), or will retry after a fixed off time (when C_T has discharged to 0.5 V), depending on whether the L/R pin is set high or low by the user. The equation for this current threshold is simply:

$$I_{FAULT} = \frac{0.05}{R_{SENSE}} \quad (1)$$

The first time a fault occurs, C_T is at ground, and must charge to 1.5 V. Therefore:

$$t_{FAULT} = t_{ON(sec)} = \frac{C_t(\mu F) \times 1.5}{35} \quad (2)$$

In the retry mode, the timing capacitor will already be charged to 0.5 V at the end of the off time, so all subsequent cycles will have a shorter ton time, given by:

$$t_{FAULT} \cong t_{ON(sec)} = \frac{C_T(\mu F)}{35} \quad (3)$$

Note that these equations for t_{ON} are without the power limiting feature (R_{PL} pin open). The effects of power limiting on t_{ON} will be discussed later.

The off time in the retry mode is set by C_T and an internal 1.2-μA sink current. It is the time it takes C_T to discharge from 1.5 V to 0.5 V. The equation for the off time is therefore:

$$t_{OFF(sec)} = \frac{C_T \mu F}{1.2} \quad (4)$$

shutdown characteristics

When the $\overline{SD}$ pin is set to TTL high (above 2 V) the UCC3919 is ensured to be enabled. When $\overline{SD}$ is set to a low TTL (below 0.8 V) the UCC3919 is ensured to be disabled, but may not be in ultra low current sleep mode. When $\overline{SD}$ is set to 0.2 V or less, the UCC3919 is ensured to be disabled and in ultra low current sleep mode. See Figure 1. At cold temperatures, (below 0°C), the UCC2919 shutdown supply current delays gradually over time and may take >1 minute to drop below the 7-μA shutdown current limit. However, the gate output is driven low immediately when the SD pin is pulled low and does not exhibit a temperature dependency.

APPLICATION INFORMATION

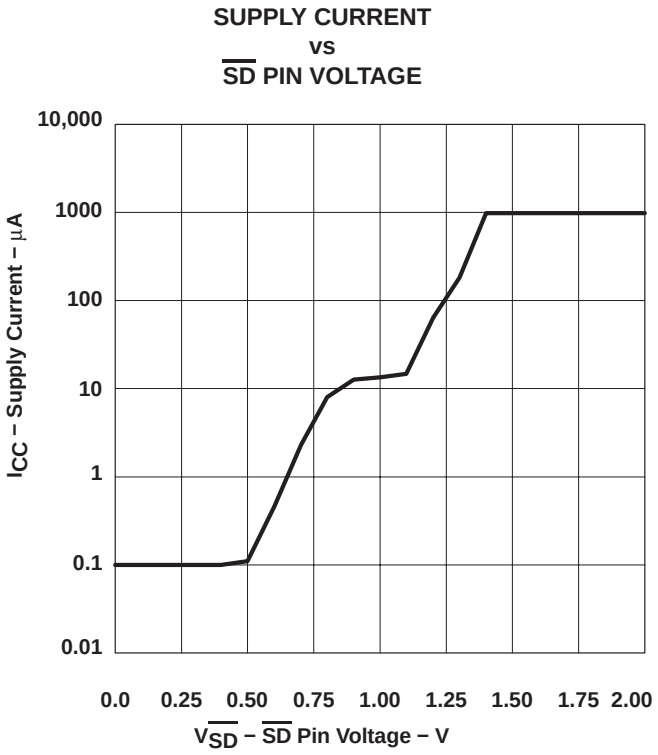


Figure 1

IMAX threshold

The second threshold is programmed by the voltage on IMAX (measured with respect to the CSP pin). This controls the maximum current, I_{MAX}, that the UCC3919 will allow to flow into the load during the MOSFET on time. A resistive divider connected between IBIAS and CSP generates the programming voltage. When the drop across the sense resistor reaches this voltage, a linear amplifier reduces the voltage on GATE to control the external MOSFET in a constant current mode.

During this time C_T is charging, as described above. If this condition lasts long enough for C_T to charge to 1.5 V, a fault will be declared and the MOSFET will be turned off. The I_{MAX} current is calculated as follows:

$$I_{MAX} = \frac{V_{CSP} - V_{IMAX}}{R_{SENSE}} \quad (5)$$

Note that if the voltage on the IMAX pin is programmed to be less than 50 mV below CSP, then the UC3919 will control the MOSFET in a constant current mode all the time. No fault will be declared and the MOSFET will remain on because I_{MAX} is less than I_{FAULT}.

APPLICATION INFORMATION

overload threshold

There is a third threshold which, if exceeded, will declare a fault and shutdown the external MOSFET immediately, without waiting for C_T to charge. This *overload* threshold is 200 mV greater than the I_{MAX} threshold (again, this is with respect to CSP). This feature protects the circuit in the event that the external MOSFET is on, with a load current below I_{MAX}, and a short is quickly applied across the output. This allows hot-swapping in cases where the UCC3919 is already powered up (on the backplane) and capacitors are added across the output bus. In this case, the load current could rise too quickly for the linear amplifier to reduce the voltage on GATE and limit the current to I_{MAX}. If the overload threshold is reached, the MOSFET will be turned off quickly and a fault declared. A latch is set so that C_T can be charged, ensuring that the MOSFET will remain off for the same period as defined above before retrying. The overload current is:

$$I_{OVERLOAD} = \frac{V_{CSP} - V_{IMAX} + 0.2}{R_{SENSE}} = I_{MAX} + \frac{0.2}{R_{SENSE}} \quad (6)$$

Note that $I_{OVERLOAD}$ may be much greater than I_{MAX}, depending on the value of R_{SENSE}.

power limiting

A power limiting feature is included which allows the power dissipated in the external MOSFET to be held relatively constant during a short, for different values of input voltage. This is accomplished by connecting a resistor from the output (source of the external MOSFET) to PL. When the output voltage drops due to a short or overload, an internal bias current is generated which is equal to:

$$I_{PL} \cong \frac{\left(V_{IN} - V_{OUT} - V_{PL}\right)}{R_{PL}} \quad (7)$$

This current is used to help charge the timing capacitor in the event that the load current exceeds I_{FAULT}. (A simplified schematic of the circuit internal to the UCC3919 is shown in Figure 2.) The result is that the on time of the MOSFET during current limit is reduced as the input voltage is increased. This reduces the effective duty cycle, holding the average power dissipated constant.

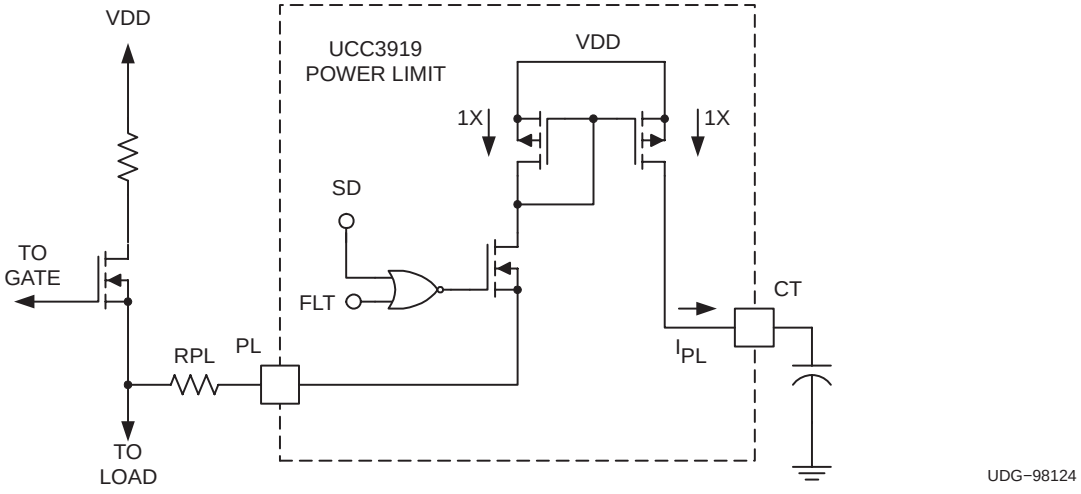


Figure 2. Power Limiting Circuit

APPLICATION INFORMATION

It can be seen that power limiting will only occur when I_{PL} is > 0 (it cannot be negative). For power limiting to begin to occur, the voltage drop across the MOSFET must be greater than $V_{DD}-V_{PL}$ or 1.4 V(typ).

$$V_{IN} - V_{OUT} \geq 1.4\ V \tag{8}$$

The on time using R_{PL} is defined as:

$$t_{ON} = \frac{C_T \times \Delta V}{I_{PL} + 35 \times 10^{-6}}, \quad \text{where } \Delta V = 1\ V \tag{9}$$

The graph in Figure 4 illustrates the effect of R_{PL} on the average MOSFET power dissipation into a short. The equation for the average power dissipation during a short is:

$$P_{DISS} = \frac{I_{MAX} \times V_{IN} \times 1.2 \times 10^{-6}}{I_{PL} + 35 \times 10^{-6}}, \text{ or} \tag{10}$$

$$P_{DISS} = \frac{I_{MAX} \times V_{IN} \times t_{ON}}{t_{ON} + t_{OFF}}$$

If PL is left unconnected, the power limiting feature will not be exercised. In the retry mode, the duty cycle during a fault will be nominally 3%, independent of input voltage. The average power dissipation in the external MOSFET with a shorted output will be proportional to input voltage, as shown by the equation:

$$P_{DISS} = I_{MAX} \times V_{IN} \times 0.033 \tag{11}$$

calculating $C_{T(min)}$ for a given load capacitance without power limiting

To ensure recovery from an overload when operating in the retry mode, there is a maximum total output capacitance which can be charged for a given t_{ON} (fault time) before causing a fault. For a worst case situation of a constant current load below the fault threshold, $C_{T(min)}$ for a given output load capacitance (without power limiting) can be calculated from:

$$C_{T(min)} = \frac{V_{IN} \times C_{OUT} \times 35 \times 10^{-6}}{I_{MAX} - I_{LOAD}} \tag{12}$$

A larger load capacitance or a smaller C_T will cause a fault when recovering from an overload, causing the circuit to get stuck in a continuous hiccup mode. To handle larger capacitive loads, increase the value of C_T. The equation can be easily re-written, if desired, to solve for $C_{OUT(max)}$ for a given value of C_T.

For a resistive load of value R_L and an output cap C_{OUT}, $C_{T(min)}$ can be smaller than in the constant current case, and can be estimated from:

$$C_{T(min)} = \frac{-C_{OUT} \times R_L \times \ell n\left(1 - \frac{V_{IN}}{I_{MAX} \times R_L}\right)}{28 \times 10^3} \tag{13}$$

Note that in the latch mode (or when first turning on in the retry mode), since the timing capacitor is not recovering from a previous fault, it is charging from 0 V rather than 0.5 V. This allows up to 50% more load capacitance without causing a fault.

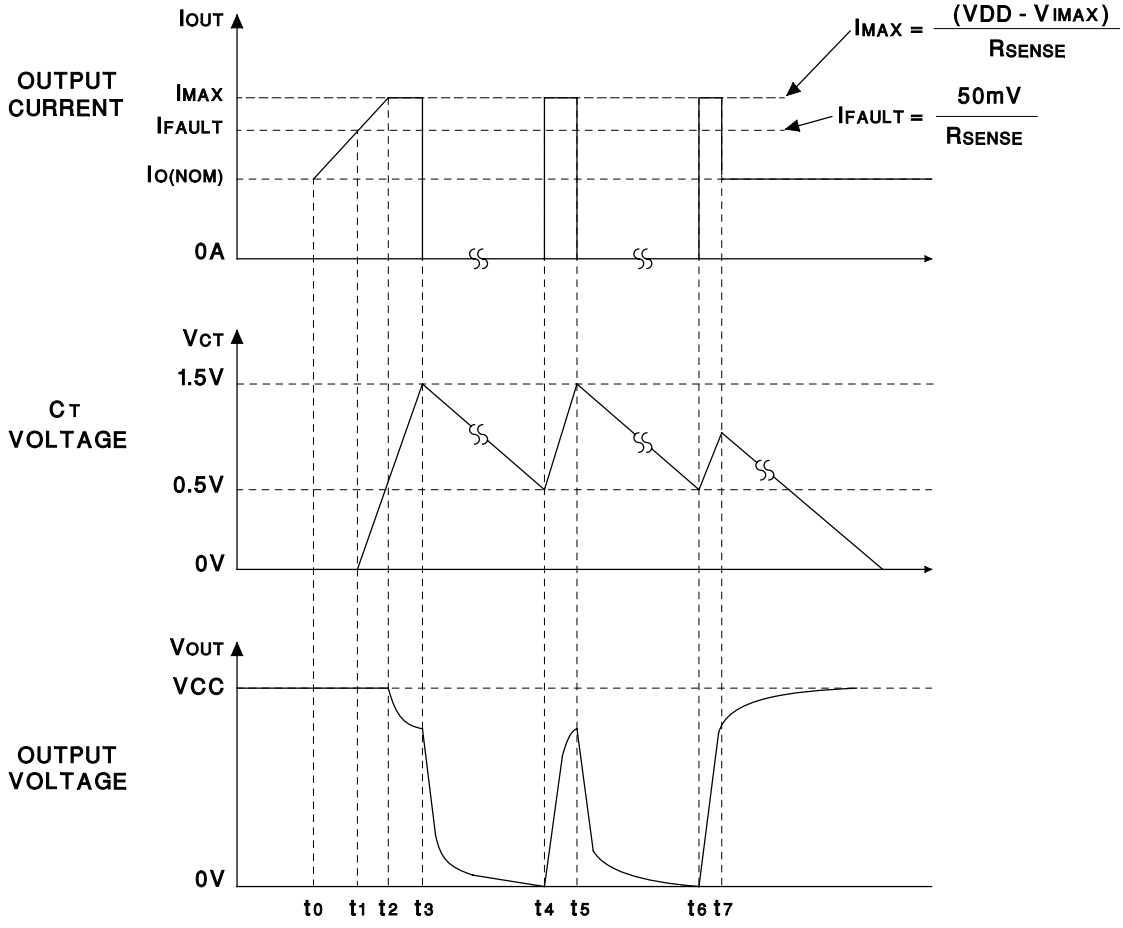
APPLICATION INFORMATION

estimating $C_{T(min)}$ when using power limiting

If power limiting is used, the calculation of $C_{T(min)}$ for a given C_{OUT} becomes considerably more complex, especially with a resistive load. This is because the C_T charge current becomes a function of V_{OUT}, which is changing with time. The amount of capacitance that can be charged (without causing a fault) when using power limiting will be significantly reduced for the same value C_T, due to the shorter t_{ON} time.

The charge current contribution from the power limiting circuit is defined as:

$$I_{PL} \cong \frac{\left(V_{IN} - V_{OUT} - V_{PL}\right)}{R_{PL}} \tag{14}$$



t0: Normal condition − Output current is nominal, output voltage is at positive rail, V_{CC}.
t1: Fault control reached − Output current rises above the programmed fault value, C_T begins to charge with 35 µA + I_{PL}.
t2: Maximum current reached − Output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.
t3: Fault occurs − C_T has charged to 1.5 V, fault output goes low, the FET turns off allowing no output current to flow, V_{OUT} discharges to GND.
t4: Retry − C_T has discharged to 0.5 V, but fault current is still exceeded, C_T begins charging again, FET is on, V_{OUT} increases.
t3 to t5: Illustrates < 3% duty cycle depending upon R_{PL} selected.
t6 = t4
t7: Fault released, normal condition − return to normal operation of the circuit breaker

Figure 3.

APPLICATION INFORMATION

constant current load

For a constant current load in parallel with a load capacitor, the load capacitor will charge linearly. During that time:

$$I_{PL(avg)} \cong \frac{\left(V_{IN} - V_{PL}\right)^2}{2 \times R_{PL} \times V_{IN}} \quad (15)$$

Modifying equation (12) yields:

$$C_{T(min)} \cong \frac{V_{IN} \times C_{OUT} \times \left[\frac{\left(V_{IN} - V_{PL}\right)^2}{2 \times R_{PL} \times V_{IN}} + 35 \times 10^{-6}\right]}{I_{MAX} - I_{LOAD}} \quad (16)$$

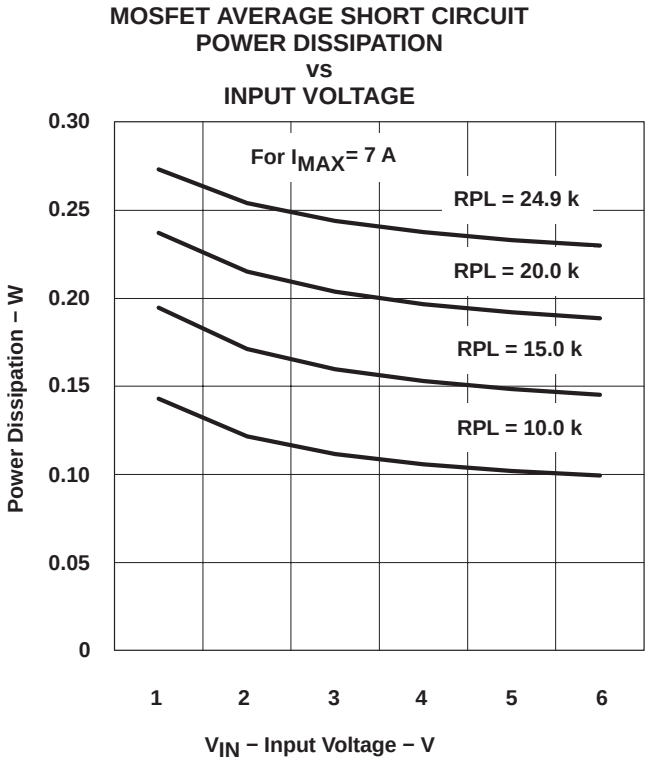


Figure 4

APPLICATION INFORMATION

parallel R-C load

Determining $C_{T(min)}$ for a parallel R-C load is more complex. First, the expression for the output voltage as a function of time is:

$$V_{OUT(t)} = I_{MAX} \times R_{LOAD}\left(1 - e^{-\frac{T_{START}}{R_{LOAD} \times C_{OUT}}}\right) \quad (17)$$

Solving for T_{START} when $V_{OUT} = V_{IN}$ yields:

$$T_{START} = -R_{LOAD} \times C_{OUT} \times \ell n\left(1 - \left(\frac{V_{IN}}{I_{MAX} \times R_{LOAD}}\right)\right) \quad (18)$$

Assuming that the device is operating in the retry mode, where C_T is charging from 0.5 V to just below 1.5 V in time (t), C_T is defined as:

$$C_T = \frac{I_{CT} \times dt}{dV} = I_{CT} \times dt, \text{ where} \quad (19)$$

$$I_{CT} = \left(I_{PL} + 35 \times 10^{-6}\right)$$

Substituting equation (15) into (19) yields:

$$C_{T(min)} = \left[\frac{\left(V_{IN} - V_{PL}\right)^2}{2 \times R_{PL} \times V_{IN}} + 35 \times 10^{-6}\right] \times dt \quad (20)$$

This yields the following expression for $C_{T(min)}$ for a resistive load with power limiting. By substituting the value calculated for T_{START} in equation (18) for dt, $C_{T(min)}$ is determined.

$$C_{T(min)} = \left[\frac{\left(V_{IN} - V_{PL}\right)^2}{2 \times R_{PL} \times V_{IN}} + 35 \times 10^{-6}\right] \times T_{START} \quad (21)$$

APPLICATION INFORMATION

example

The example in Figure 5 shows the UCC3919 in a typical application. A low value sense resistor and N-channel MOSFET minimize losses. With the values shown for R1, R2, and R_S, the overcurrent fault will be 5-A nominal. Linear current limiting (I_{MAX}) will occur at 7.14 A and the overload comparator will trip at 27 A. The calculations are shown below.

$$I_{FAULT} = \frac{0.05}{R_S} = \frac{0.05}{0.01} = 5\ A \tag{22}$$

$$I_{MAX} = \frac{V_{CSP} - V_{IMAX}}{R_S} = \frac{1.5 \times R1}{(R1 + R2) \times R_S} = 7.14\ A \tag{23}$$

$$I_{OVERLOAD} = I_{MAX} + \frac{0.2}{R_S} = 7.14\ A + \frac{0.2}{0.01} = 27.14\ A \tag{24}$$

$$T_{OFF(sec)} = \frac{C_T \mu F}{1.2} = \frac{0.01}{1.2} = 8.33\ ms \tag{25}$$

With the value shown for R_{PL}:

$$I_{PL(typ)}(\text{output shorted}) = \left(\frac{V_{IN} - V_{PL}}{R_{PL}}\right) = \left(\frac{5 - 1.6}{10\ k}\right) = 340\ \mu A \tag{26}$$

$$t_{ON}\ (\text{shorted}) = \frac{C_T}{I_{PL} + 35 \times 10^{-6}} = \frac{0.01 \times 10^{-6}}{375\ \mu A} = 27\ \mu s \tag{27}$$

$$P_{DISS}\ (\text{shorted}) = \frac{I_{MAX} \times V_{IN} \times t_{ON}}{t_{ON} + t_{OFF}} = \frac{7.14 \times 5 \times 27\ \mu s}{27\ \mu s + 8.33 \times 10^{-3}} = 0.12\ W \tag{28}$$

For a worst case 1 Ω resistive load: $C_{OUT(max)} \cong 47\ \mu F$.

For a worst case 5 A constant current load: $C_{OUT(max)} \cong 27\ \mu F$.

With L/R grounded, the part will operate in the retry or *hiccup* mode. The values shown for C_T and R_{PL} will yield a nominal duty cycle of 0.32% and an off time of 8.3 ms. With a shorted output, the average steady state power dissipation in Q1 will be less than 100 mW over the full input voltage range.

If power limiting is disabled by opening R_{PL}, then:

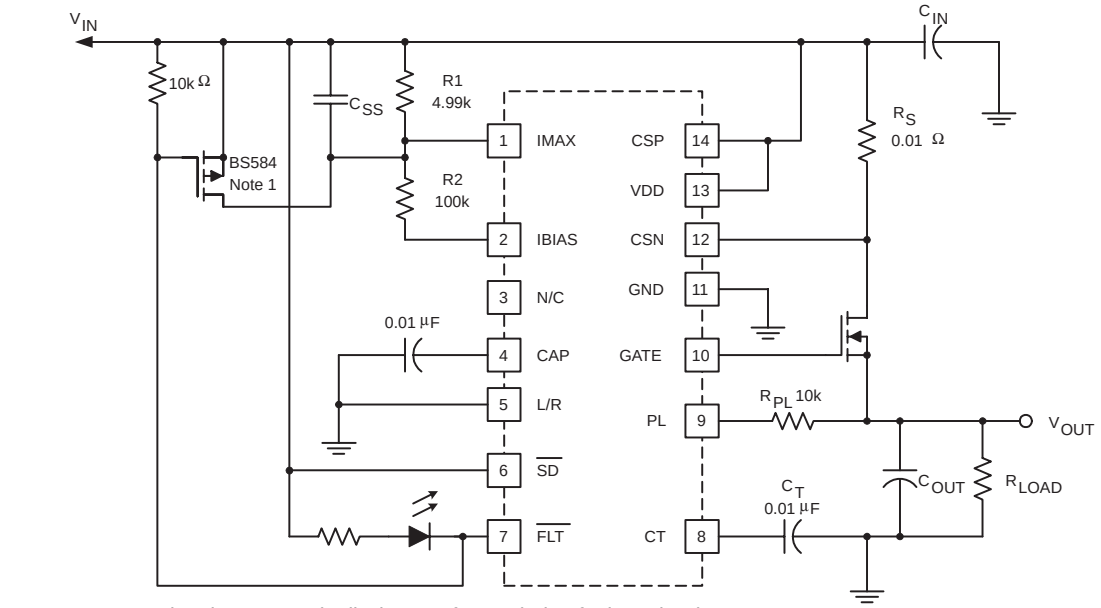
$$t_{FAULT} = t_{ON(sec)} = \frac{C_T \mu F \times 1}{35} = 287\ \mu s \tag{29}$$

$$P_{DISS}\ (\text{shorted}) = \frac{I_{MAX} \times V_{IN} \times t_{ON}}{t_{ON} + t_{OFF}} = \frac{7.14 \times 5 \times 287 \times 10^{-6}}{287 \times 10^{-6} + 8.33 \times 10^{-3}} = 1.2\ W\ (\text{with} V_{IN} = 5\ V) \tag{30}$$

For a worst case 1-Ω resistive load: $C_{OUT(max)} \cong 220\ \mu F$.

For a worst case 5 A constant current load: $C_{OUT(max)} \cong 120\ \mu F$.

APPLICATION INFORMATION



NOTES: 1. Optional FET speeds discharge of C_{SS} during fault or shutdown

UDG−98137

Figure 5. Application Circuit

THERMAL INFORMATION

steady state conditions

In normal operation, with a steady state load current below I_{FAULT}, the power dissipation in the external MOSFET will be:

$$P_{DISS} = R_{DS(on)} \times I_{LOAD}^{2} \quad (31)$$

The junction temperature of the MOSFET can be calculated from:

$$T_J = T_A + \left(P_{DISS} \times \theta_{JA}\right) \quad (32)$$

Where T_A is the ambient temperature and θ_{JA} is the MOSFET's thermal resistance from junction to ambient. If the device is on a heatsink, then the following equation applies:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (33)$$

Where θ_{JC} is the MOSFET's thermal resistance from junction to case, θ_{CS} is the thermal resistance from case to sink, and θ_{SA} is the thermal resistance of the heatsink to ambient.

The calculated T_J must be lower than the MOSFET's maximum junction temperature rating, therefore:

$$\theta_{JA} < \frac{T_{J(max)} - T_A}{P_{DISS}} \quad (34)$$

THERMAL INFORMATION

transient thermal impedance

During a fault condition in the retry mode, the average MOSFET power dissipation will generally be quite low due to the low duty cycle, as defined by:

$$P_{DISS(avg)} = \frac{I_{MAX} \times V_{IN} \times t_{ON}}{t_{ON} + t_{OFF}} \text{ (with output shorted)} \quad (35)$$

(In the latch mode, t_{OFF} will be the time between a fault and the time the device is reset.)

However, the pulse power in the MOSFET during t_{ON}, with the output shorted, is:

$$P_{DISS(pulse)} = I_{MAX} \times V_{IN} \text{ (with output shorted)} \quad (36)$$

In choosing t_{ON} for a given V_{IN}, I_{MAX}, and duty cycle it is important to consult the manufacturer's transient thermal impedance curves for the MOSFET to make sure the device is within its safe operating area. These curves provide the user with the effective thermal impedance of the device for a given time duration pulse and duty cycle. Note that some of the impedance curves are normalized to one, in which case the transient impedance values must be multiplied by the dc (steady state) thermal resistance, θ_{JC}.

For duty cycles not shown in the manufacturer's curves, the transient thermal impedance for any duty cycle and t_{ON} time (given a square pulse) can be estimated from [1]:

$$\theta_{JC(trans)} = \left(D \times \theta_{JC}\right) + (1 - D) \times \theta_{SP} \quad (37)$$

where D is the duty cycle: $\frac{t_{ON}}{t_{ON} + t_{OFF}}$.

and θ_{SP} is the single pulse thermal impedance given in the transient thermal impedance curves for the time duration of interest (t_{ON}). Note that these are absolute numbers, not normalized. If the given single pulse impedance is normalized, it must first be multiplied by θ_{JC} before using in the equation above.

This effective transient thermal impedance, when multiplied by the pulse power, will give the transient temperature rise of the die. To keep the junction temperature below the maximum rating, the following must be true:

$$\theta_{JC(trans)} = \frac{T_{J(max)} - T_C}{P_{DISS(pulse)}} \quad (38)$$

If necessary, the junction temperature rise can be reduced by reducing ton (using a smaller value for C_T), or by reducing the duty cycle using the power limiting feature already discussed. Note that in either case, the amount of load capacitance, C_{OUT}, that can be charged before causing a fault, will also be reduced.

THERMAL INFORMATION

safety recommendations

Although the UCC3919 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. for this reason, if the UCC3919 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3919 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

references

1. International Rectifier, *HEXFET Power MOSFET Designer's Manual*, Application Note 949B, Current Ratings, Safe Operating Area, and High Frequency Switching Performance of Power HEXFETs, pp.1553−1565, September 1993.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UCC2919D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2919DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2919DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2919DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2919N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
UCC2919PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2919PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3919D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3919DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3919DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3919DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3919N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
UCC3919PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3919PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3919PWTR	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI
UCC3919PWTRG4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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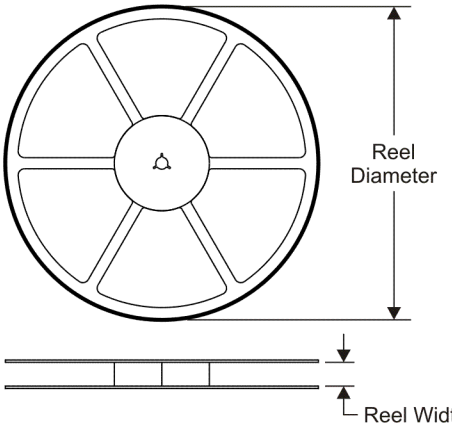
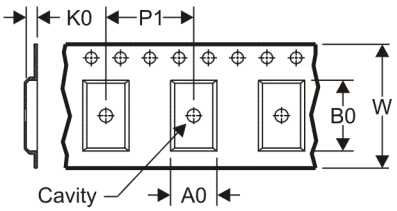
TAPE AND REEL INFORMATION

REEL DIMENSIONS

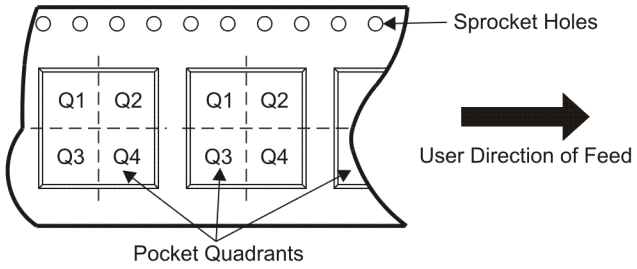


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

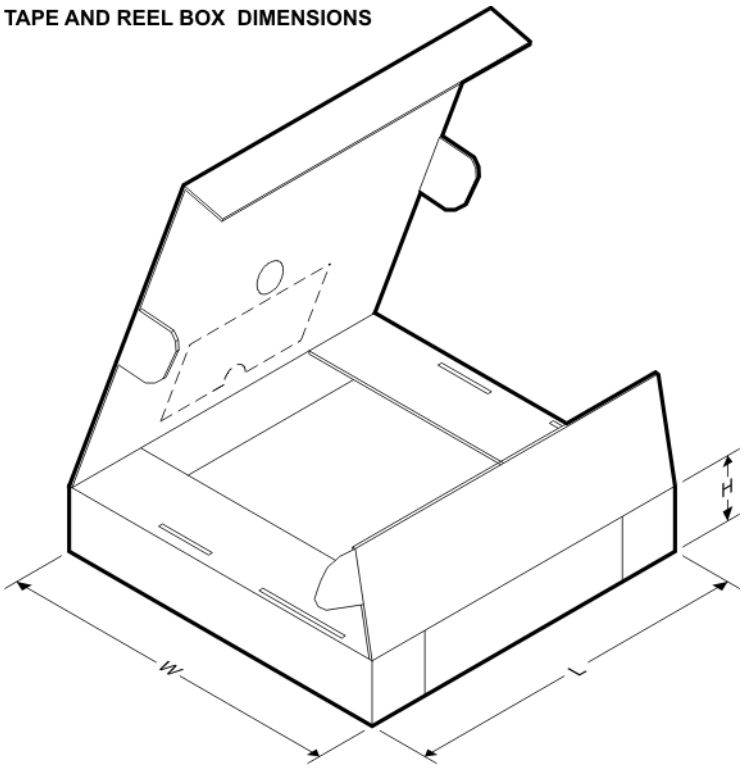
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC3919DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

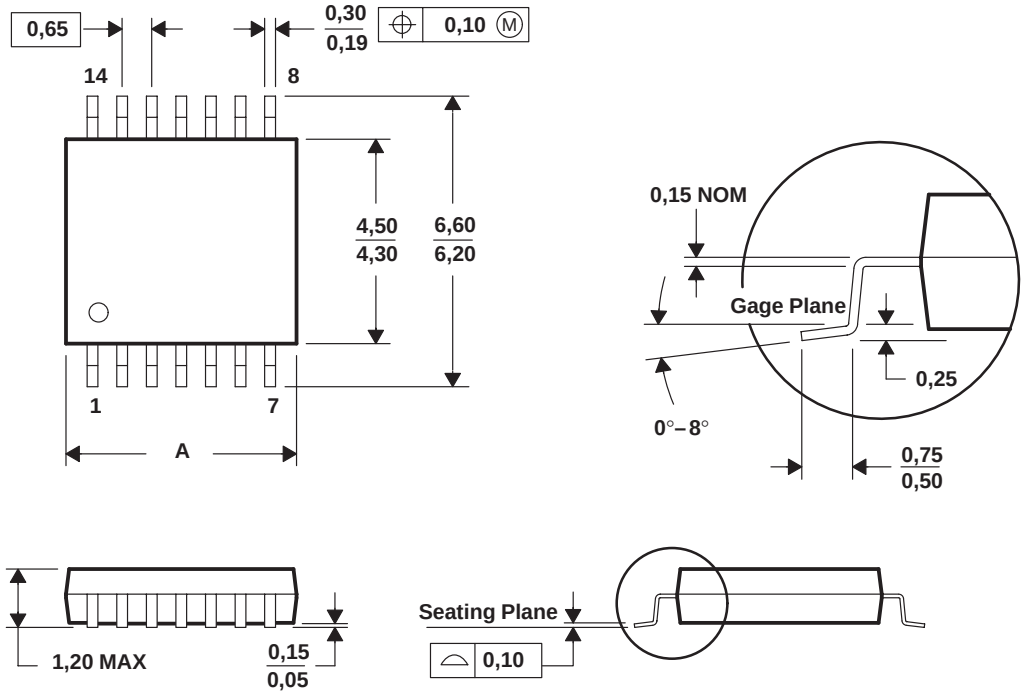


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC3919DTR	SOIC	D	16	2500	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

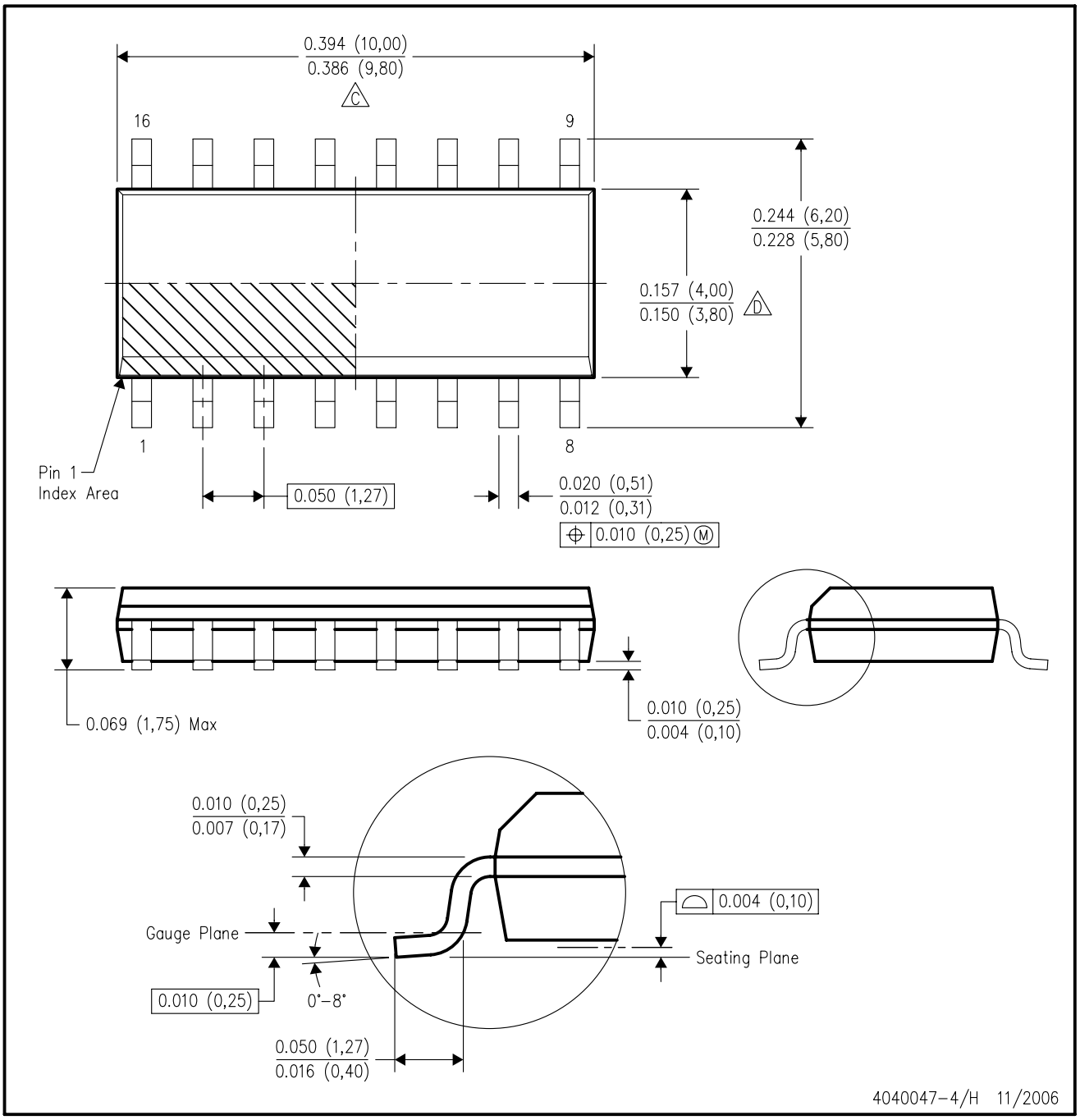


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

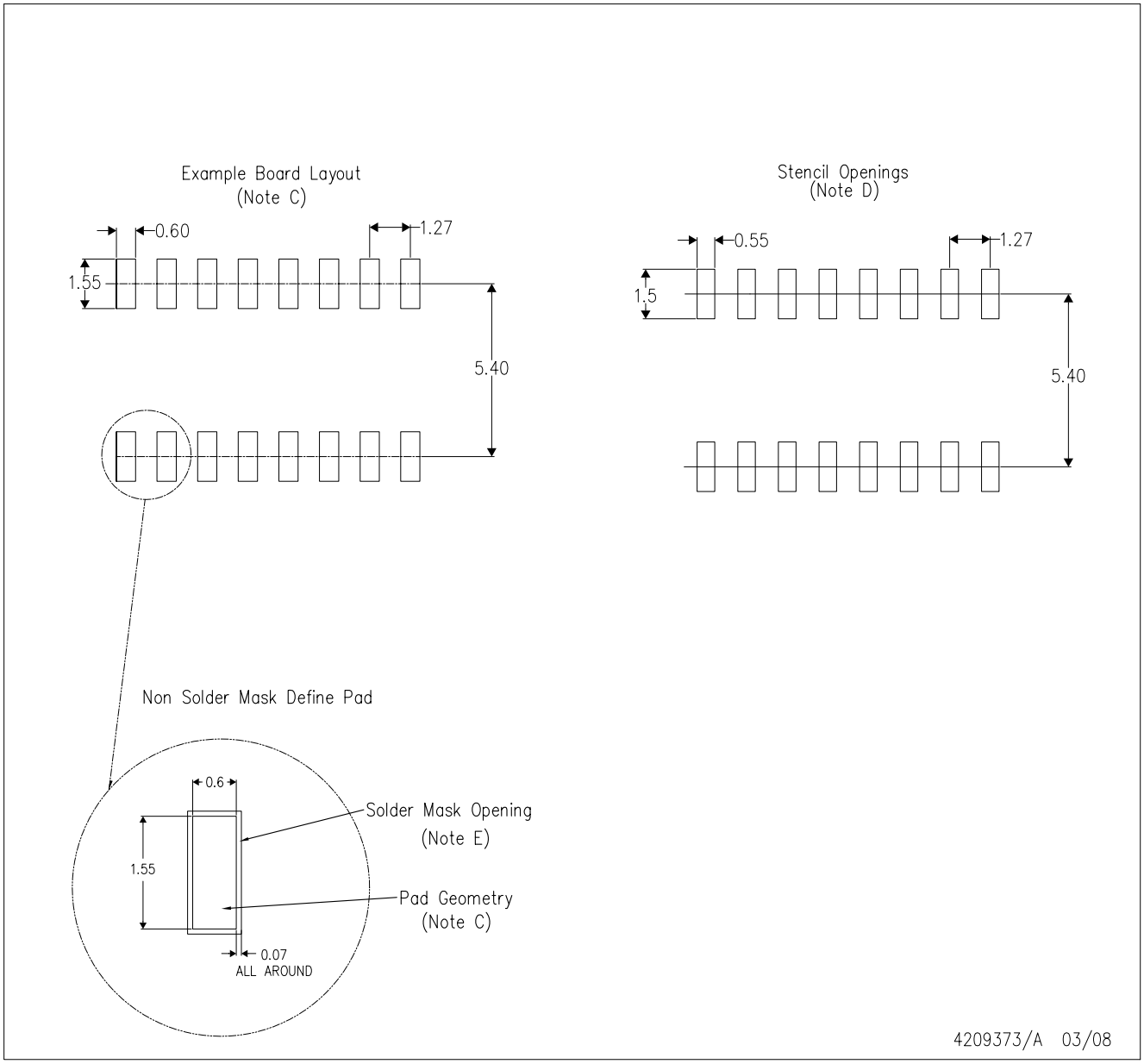
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)

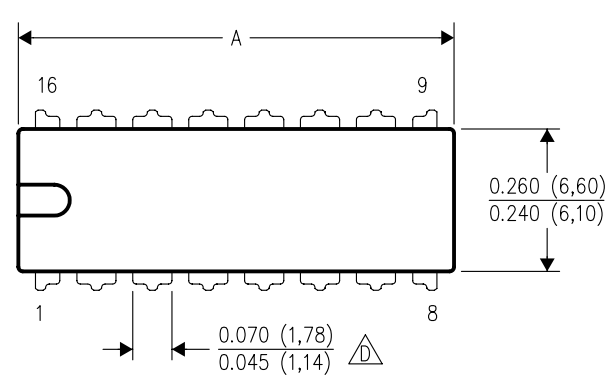


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

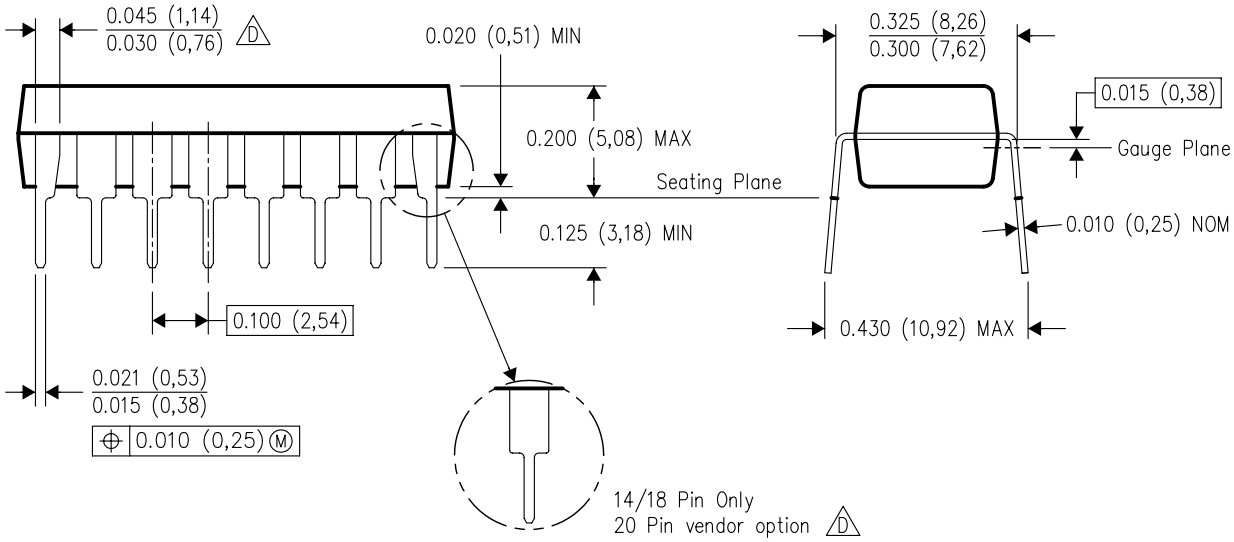
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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