–48V Hot Swap Controller with Sequencer

FEATURES

- **Allows Safe Board Insertion and Removal from a Live –48V Backplane**
- **Floating Topology Permits Very High Voltage Operation**
- **Adjustable Analog Current Limit with Breaker Timer Ideal for Two Battery Feeds**
- **Fast Response Time Limits Peak Fault Current**
- **Three Sequenced Power Good Outputs**
- **Improved Ruggedness Shunt Regulator**
- Adjustable Soft-Start Current Limit
- Adjustable Timer with Drain Voltage Accelerated Response
- Latchoff After Fault
- Available in a 16-Pin SSOP Package

APPLICATIONS

- –48V Distributed Power Systems
- Negative Power Supply Control
- Central Office Switching
- High Availability Servers
- Disk Arrays

DESCRIPTION

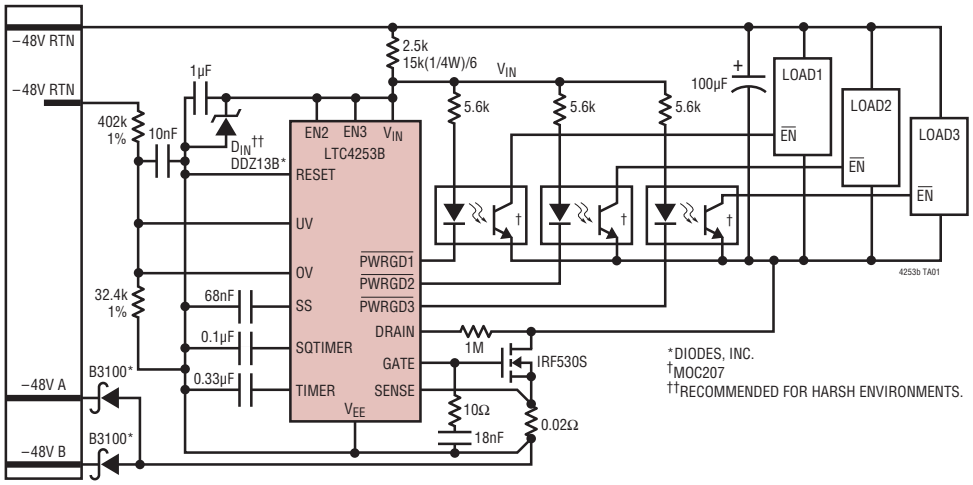
The LTC®4253B negative voltage Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane. Output current is controlled by three stages of current-limiting: a timed circuit breaker, active current limiting and a fast feedforward path that limits peak current under worst-case catastrophic fault conditions. The LTC4253B latches off after a circuit fault.

Adjustable undervoltage and overvoltage detectors disconnect the load whenever the input supply exceeds the desired operating range. The LTC4253B's supply input is shunt-regulated, allowing safe operation with very high supply voltages. A multifunction timer delays initial start-up and controls the circuit breaker's response time. The circuit breaker's response time can be accelerated by sensing excessive MOSFET drain voltage, keeping the MOSFET within its safe operating area (SOA). An adjustable soft-start circuit controls MOSFET inrush current at start-up.

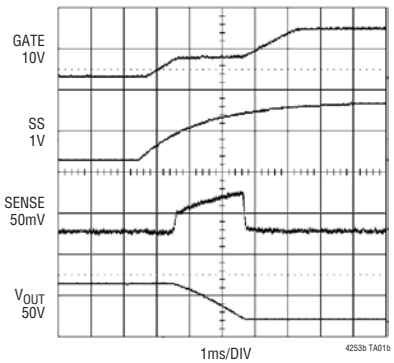
Three power good outputs are sequenced by an adjustable timer and two ENABLE inputs to enable external power modules at start-up or disable them if the circuit breaker trips. The LTC4253B improves the ruggedness of the LTC4253 shunt regulator.

TYPICAL APPLICATION

–48V/2.5A Hot Swap Controller



Start-Up Behavior

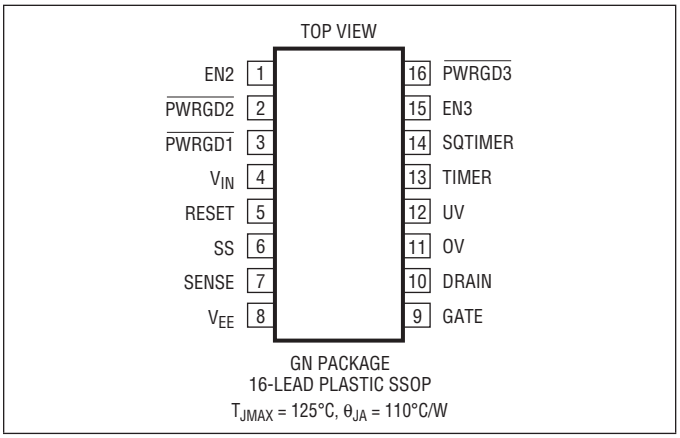


ABSOLUTE MAXIMUM RATINGS

(Note 1), All voltages referred to V_{EE}

Current into V_{IN} (100µs Pulse) 100mA
Current into DRAIN (100µs Pulse) 20mA
V_{IN}, DRAIN Minimum Voltage ..... –0.3V
Input/Output (Except SENSE
and DRAIN) Voltage ..... –0.3V to 16V
SENSE Voltage ..... –0.6V to 16V
Current Out of SENSE (20µs Pulse) ..... –200mA
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC4253BC ..... 0°C to 70°C
LTC4253BI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4253BCGN#PBF	LTC4253BCGN#TRPBF	4253B	16-Lead Plastic SSOP	0°C to 70°C
LTC4253BIGN#PBF	LTC4253BIGN#TRPBF	4253B	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_Z	V_{IN} – V_{EE} Zener Voltage	I_{IN} = 2mA	●	11.5	13	14.5	V
R_Z	V_{IN} – V_{EE} Zener Dynamic Impedance	I_{IN} = (2mA to 30mA)			5		Ω
I_{IN}	V_{IN} Supply Current	UV = OV = 4V, V_{IN} = (V_Z – 0.3V)	●		0.8	2	mA
V_{LKO}	V_{IN} Undervoltage Lockout	Coming Out of UVLO (Rising V_{IN})	●		9.2	11.5	V
V_{LKH}	V_{IN} Undervoltage Lockout Hysteresis		●	0.5	1	1.5	V
V_{IH}	TTL Input High Voltage		●	2			V
V_{IL}	TTL Input Low Voltage		●			0.8	V
V_{HYST}	TTL Input Buffer Hysteresis				600		mV
I_{RESET}	RESET Input Current	$V_{EE} \le V_{RESET} \le V_{IN}$	●		±0.1	±10	µA
I_{EN}	EN2, EN3 Input Current	V_{EN} = 4V V_{EN} = 0V	● ●	60	120 ±0.1	180 ±10	µA µA
V_{CB}	Circuit Breaker Current Limit Voltage	V_{CB} = (V_{SENSE} – V_{EE})	●	40	50	60	mV
V_{ACL}	Analog Current Limit Voltage	V_{ACL} = (V_{SENSE} – V_{EE}), SS = Open or 2.2V	●	80	100	120	mV
V_{FCL}	Fast Current Limit Voltage	V_{FCL} = (V_{SENSE} – V_{EE})	●	150	200	300	mV
V_{SS}	SS Voltage	After End of SS Timing Cycle	●	2	2.2	2.4	V
I_{SS}	SS Pin Current	UV = OV = 4V, V_{SENSE} = V_{EE}, V_{SS} = 0V (Sourcing)	●	12	22	32	µA
		UV = OV = 0V, V_{SENSE} = V_{EE}, V_{SS} = 1V (Sinking)			28		mA
R_{SS}	SS Output Impedance				100		kΩ
V_{OS}	Analog Current Limit Offset Voltage				10		mV
$\frac{V_{ACL} + V_{OS}}{V_{SS}}$	Ratio (V_{ACL} + V_{OS}) to SS Voltage				0.05		V/V
I_{GATE}	GATE Pin Output Current	UV = OV = 4V, V_{SENSE} = V_{EE}, V_{GATE} = 0V (Sourcing)	●	30	50	70	µA
		UV = OV = 4V, V_{SENSE} – V_{EE} = 0.15V, V_{GATE} = 3V (Sinking)			17		mA
		UV = OV = 4V, V_{SENSE} – V_{EE} = 0.3V, V_{GATE} = 1V (Sinking)			190		mA
V_{GATE}	External MOSFET Gate Drive	V_{GATE} – V_{EE}, I_{IN} = 2mA	●	10	12	V_Z	V
V_{GATEL}	Gate Low Threshold	Before Gate Ramp Up			0.5		V
V_{GATEH}	Gate High Threshold	V_{GATEH} = V_{IN} – V_{GATE}, for $\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Status			2.8		V
V_{UVHI}	UV Pin Threshold HIGH	UV Low to High	●	3.075	3.225	3.375	V
V_{UVLO}	UV Pin Threshold LOW	UV High to Low	●	2.775	2.925	3.075	V
V_{UVHST}	UV Pin Hysteresis			230	300	350	mV
V_{OVHI}	OV Pin Threshold HIGH	OV Low to High	●	5.85	6.15	6.45	V
V_{OVLO}	OV Pin Threshold LOW	OV High to Low	●	5.55	5.85	6.15	V
V_{OVHST}	OV Pin Hysteresis			230	300	350	mV
I_{SENSE}	SENSE Pin Input Current	UV = OV = 4V, V_{SENSE} = 50mV (Sourcing)	●		15	30	µA
I_{INP}	UV, OV Pin Input Current	UV = OV = 4V	●		±0.1	±1	µA
V_{TMRH}	TIMER Pin Voltage High Threshold		●	3.5	4	4.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

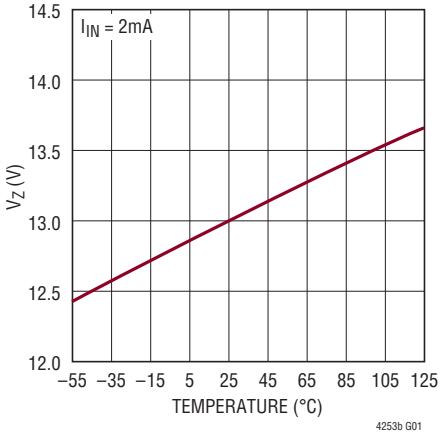
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TMRL}	TIMER Pin Voltage Low Threshold		●	0.8	1	1.2	V
I_{TMR}	TIMER Pin Current	Timer On (Initial Cycle/Latchoff, Sourcing), V_{TMR} = 2V	●	3	5	7	µA
		Timer Off (Initial Cycle, Sinking), V_{TMR} = 2V			28		mA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 0µA), V_{TMR} = 2V	●	120	200	280	µA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 50µA), V_{TMR} = 2V			600		µA
		Timer Off (Circuit Breaker, Sinking), V_{TMR} = 2V	●	3	5	7	µA
$\frac{\Delta I_{TMRACC}}{\Delta I_{DRN}}$	$\frac{I_{TMR}\text{ at }I_{DRN}=50\mu A - I_{TMR}\text{ at }I_{DRN}=0\mu A}{50\mu A}$	Timer On (Circuit Breaker with I_{DRN} = 50µA)	●	7	8	9	µA/µA
V_{SQTMRH}	SQTIMER Pin Voltage High Threshold		●	3.5	4	4.5	V
V_{SQTMRL}	SQTIMER Pin Voltage Low Threshold				0.33		V
I_{SQTMR}	SQTIMER Pin Current	SQTIMER On (Power Good Sequence, Sourcing), V_{SQTMR} = 2V	●	3	5	7	µA
		SQTIMER Off (Power Good Sequence, Sinking), V_{SQTMR} = 2V			28		mA
V_{DRNL}	DRAIN Pin Voltage Low Threshold	For $\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Status	●	2	2.39	3	V
I_{DRNL}	DRAIN Leakage Current	V_{DRAIN} = 5V V_{DRAIN} = 4V			±0.1	±1	µA µA
V_{DRNCL}	DRAIN Pin Clamp Voltage	I_{DRN} = 50µA	●	6	7	8.5	V
V_{PGL}	$\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Output Low Voltage	I_{PG} = 1.6mA I_{PG} = 5mA	● ●		0.25	0.4 1.2	V V
I_{PGH}	$\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Output High Current	V_{PG} = 0V (Sourcing)	●	30	50	70	µA
t_{SQ}	SQTIMER Default Ramp Period	SQTIMER Pin Floating, V_{SQTMR} Ramps from 0.5V to 3.5V			250		µs
t_{SS}	SS Default Ramp Period	SS Pin Floating, V_{SS} Ramps from 0.2V to 2V			250		µs
t_{PLLUG}	UV Low to GATE Low		●		0.4	5	µs
t_{PHLOG}	OV High to GATE Low		●		0.4	5	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

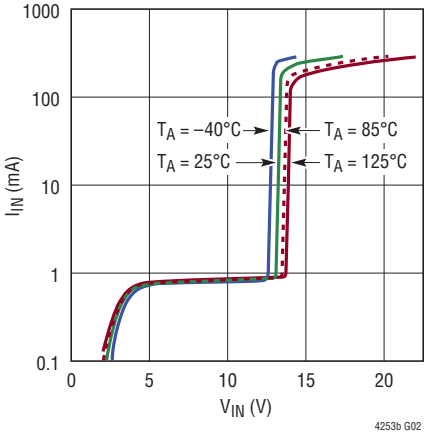
Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE} unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS

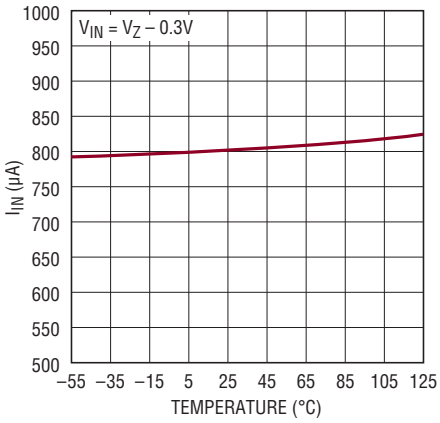
V_Z vs Temperature



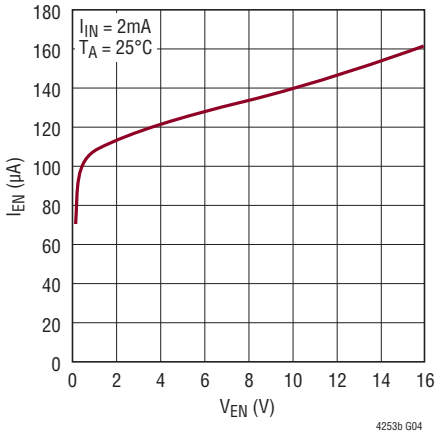
I_{IN} vs V_{IN}



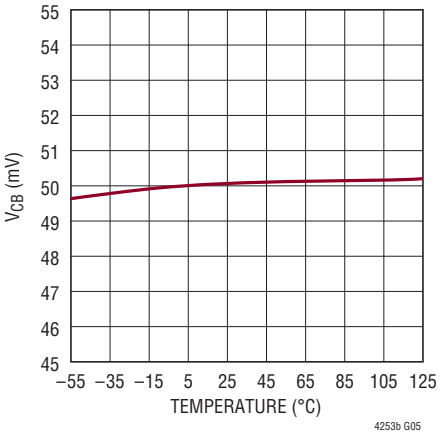
I_{IN} vs Temperature



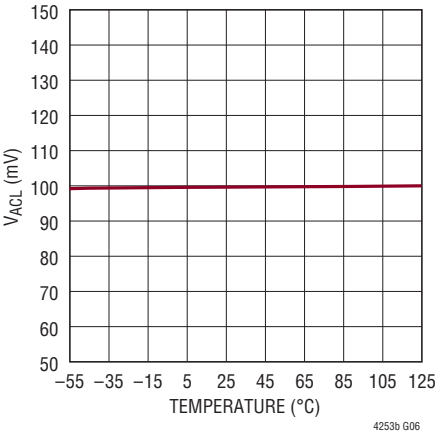
I_{EN} vs V_{EN}



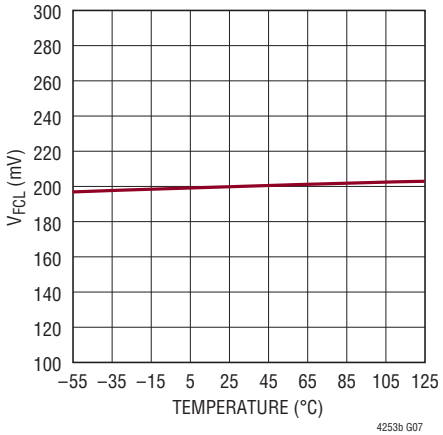
Circuit Breaker Current Limit Voltage V_{CB} vs Temperature



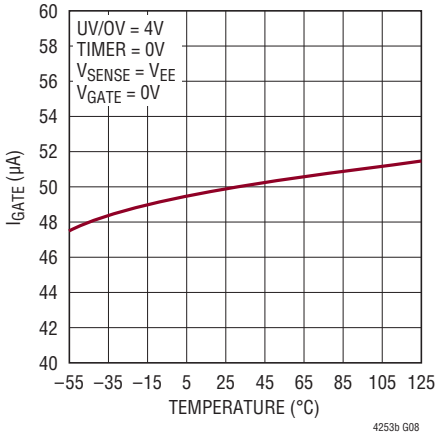
Analog Current Limit Voltage V_{ACL} vs Temperature



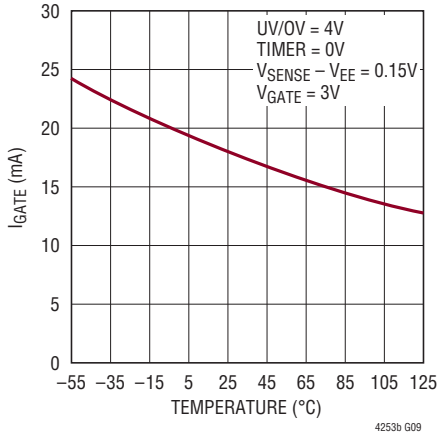
Fast Current Limit Voltage V_{FCL} vs Temperature



I_{GATE} (Source) vs Temperature

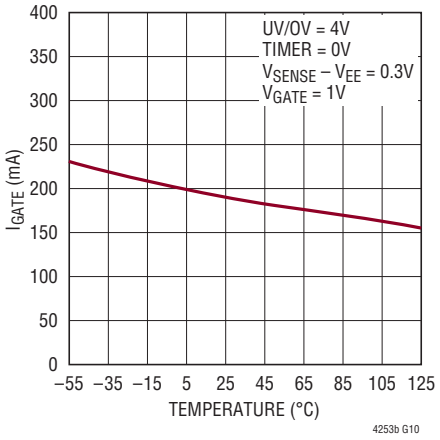


I_{GATE} (ACL, Sink) vs Temperature

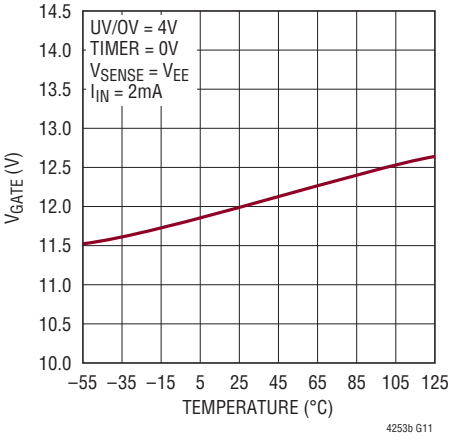


TYPICAL PERFORMANCE CHARACTERISTICS

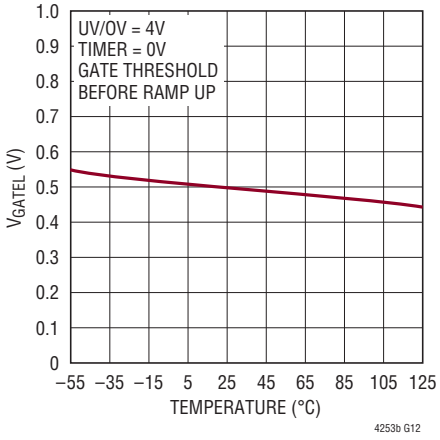
I_{GATE} (FCL, Sink) vs Temperature



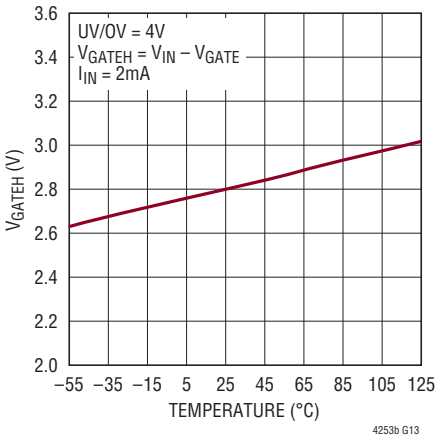
V_{GATE} vs Temperature



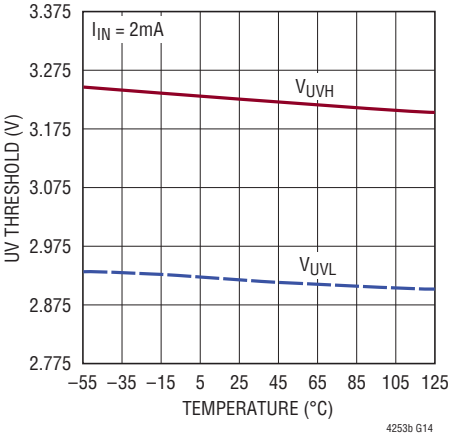
V_{GATEL} vs Temperature



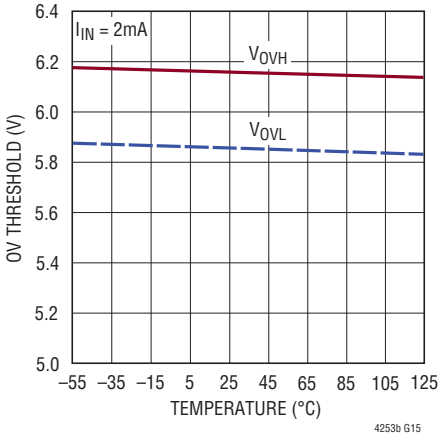
V_{GATEH} vs Temperature



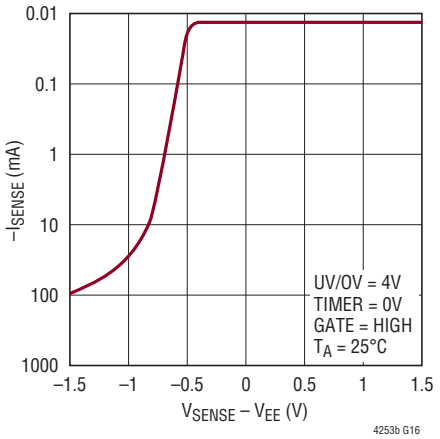
UV Threshold vs Temperature



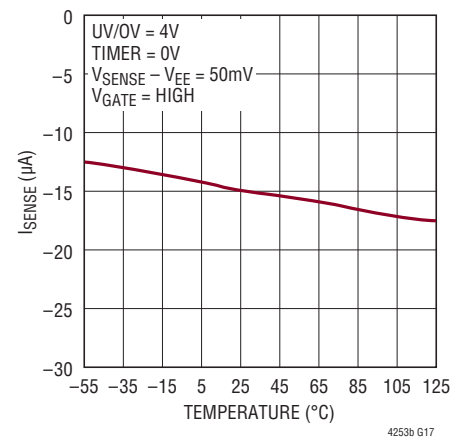
OV Threshold vs Temperature



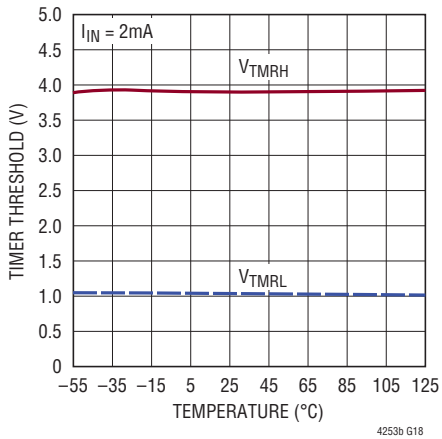
I_{SENSE} vs ($V_{SENSE} – V_{EE}$)



I_{SENSE} vs Temperature

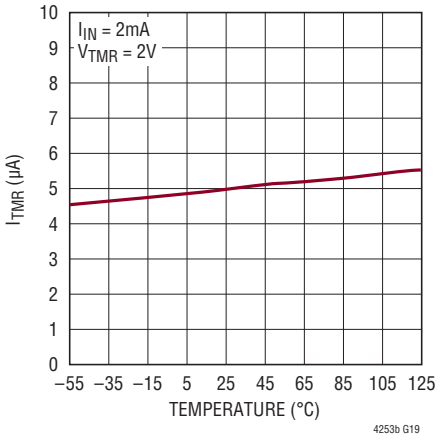


TIMER Threshold vs Temperature

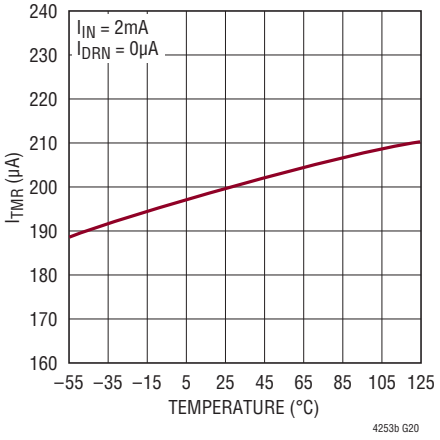


TYPICAL PERFORMANCE CHARACTERISTICS

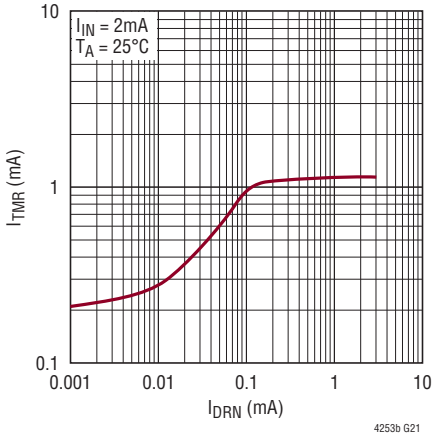
I_{TMR} (Initial Cycle, Sourcing) vs Temperature



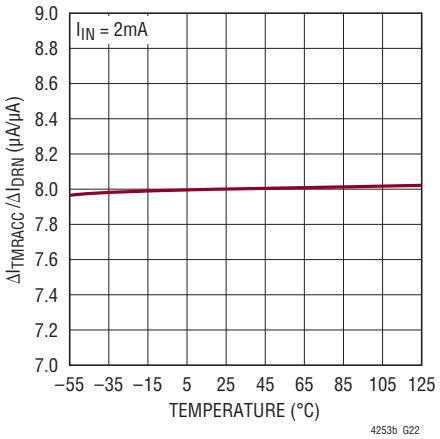
I_{TMR} (Circuit Breaker, Sourcing) vs Temperature



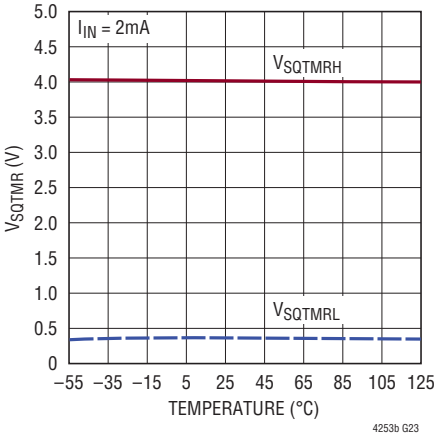
I_{TMR} vs I_{DRN}



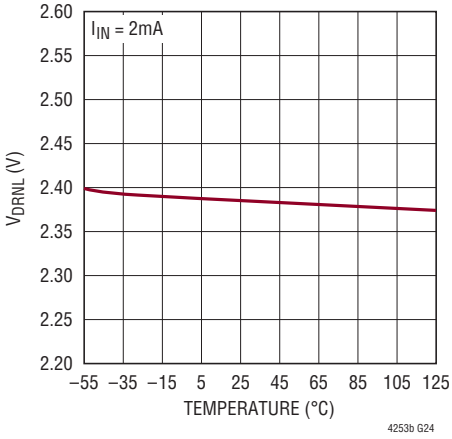
$\Delta I_{TMRACC}/\Delta I_{DRN}$ vs Temperature



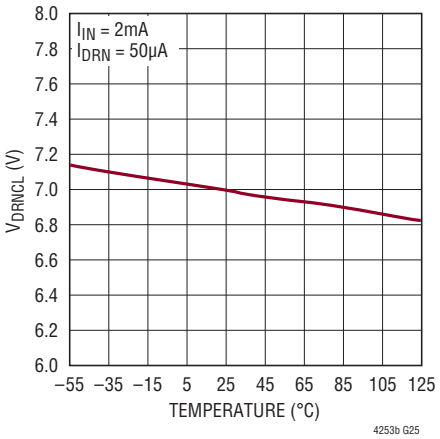
SQTIMER Threshold vs Temperature



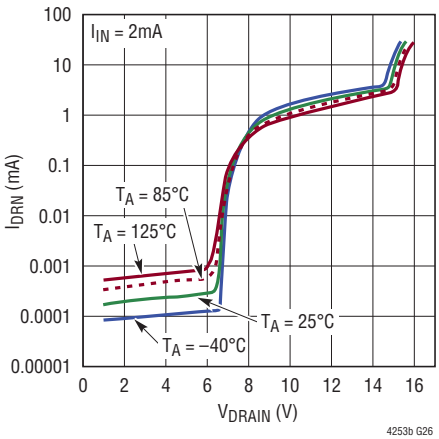
V_{DRNL} vs Temperature



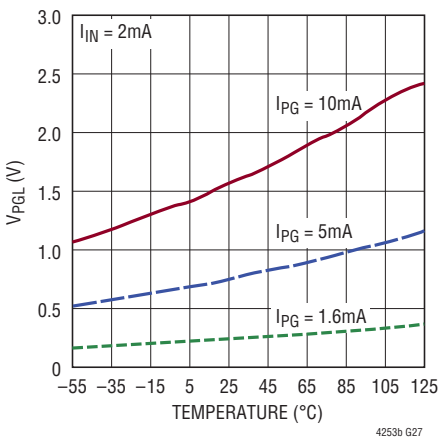
V_{DRNCL} vs Temperature



I_{DRN} vs V_{DRAIN}

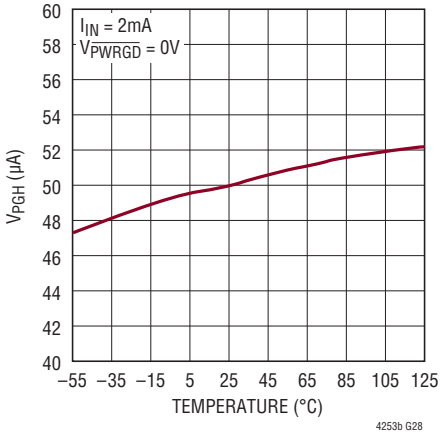


V_{PGL} vs Temperature

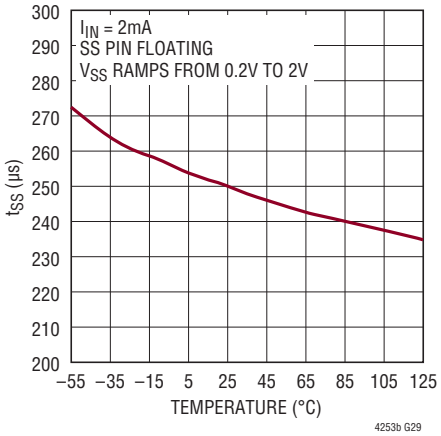


TYPICAL PERFORMANCE CHARACTERISTICS

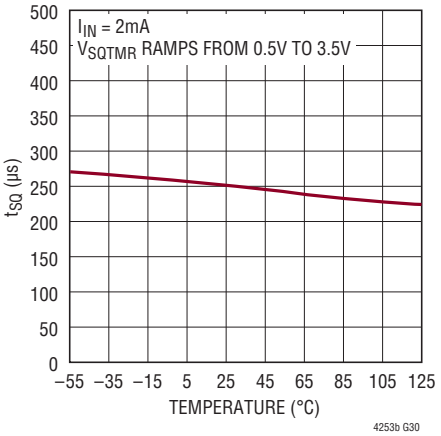
I_{PGH} vs Temperature



t_{SS} vs Temperature



t_{SQ} vs Temperature



PIN FUNCTIONS

EN2 (Pin 1): Power Good Status Output Two Enable. This is a TTL compatible input that is used to control $\overline{PWRGD2}$ and $\overline{PWRGD3}$ outputs. When EN2 is driven low, both $\overline{PWRGD2}$ and $\overline{PWRGD3}$ will go high. When EN2 is driven high, $\overline{PWRGD2}$ will go low provided $\overline{PWRGD1}$ has been active for more than one power good sequence delay (t_{SQT}) provided by the sequencing timer. EN2 can be used to control the power good sequence. This pin is internally pulled low by a 120µA current source.

$\overline{PWRGD2}$ (Pin 2): Power Good Status Output Two. Power good sequence starts with $\overline{PWRGD1}$ latching active low. $\overline{PWRGD2}$ will latch active low after EN2 goes high and after one power good sequence delay t_{SQT} provided by the sequencing timer from the time $\overline{PWRGD1}$ goes low, whichever comes later. $\overline{PWRGD2}$ is reset by $\overline{PWRGD1}$ going high or EN2 going low. This pin is internally pulled high by a 50µA current source.

$\overline{PWRGD1}$ (Pin 3): Power Good Status Output One. At start-up, $\overline{PWRGD1}$ latches active low and starts the power good sequence when the DRAIN pin is below 2.39V and GATE is within 2.8V of V_{IN}. $\overline{PWRGD1}$ status is reset by UV, V_{IN} (UVLO), RESET going high or circuit breaker fault time-out. This pin is internally pulled high by a 50µA current source.

V_{IN} (Pin 4): Positive Supply Input. Connect this pin to the positive side of the supply through a dropping resistor. A shunt regulator clamps V_{IN} at 13V above V_{EE}. An internal undervoltage lockout (UVLO) circuit holds GATE low until the V_{IN} pin is greater than V_{LKO}, overriding UV and OV. If UV is high, OV is low and V_{IN} comes out of UVLO, TIMER starts an initial timing cycle before initiating GATE ramp up. If V_{IN} drops below approximately 8.2V, GATE pulls low immediately.

PIN FUNCTIONS

RESET (Pin 5): Circuit Breaker Reset Pin. This is an asynchronous TTL compatible input. RESET going high will pull GATE, SS, TIMER, SQTIMER low and the $\overline{PWRGD}$ outputs high. The RESET pulse must be wide enough to discharge any voltage on the TIMER pin below V_{TMRL}. After the reset of a latched fault, the chip waits for the interlock conditions before recovering as described in Interlock Conditions in the Operation section.

SS (Pin 6): Soft-Start Pin. This pin is used to ramp inrush current during start up, thereby effecting control over di/dt. A 20X attenuated version of the SS pin voltage is presented to the current limit amplifier. This attenuated voltage limits the MOSFET's drain current through the sense resistor during the soft-start current limiting. At the beginning of the start-up cycle, the SS capacitor (C_{SS}) is ramped by a 22µA current source. The GATE pin is held low until SS exceeds 20 • V_{OS} = 0.2V. SS is internally shunted by a 100k R_{SS} which limits the SS pin voltage to 2.2V. This corresponds to an analog current limit SENSE voltage of 100mV. If the SS capacitor is omitted, the SS pin ramps up in about 250µs. The SS pin is pulled low under any of the following conditions: UVLO at V_{IN}, UV, OV, during the initial timing cycle, a circuit breaker fault time-out or the RESET pin going high.

SENSE (Pin 7): Circuit Breaker/Current Limit Sense Pin. Load current is monitored by a sense resistor R_S connected between SENSE and V_{EE}, and controlled in three steps. If SENSE exceeds V_{CB} (50mV), the circuit breaker comparator activates a (200µA + 8 • I_{DRN}) TIMER pull-up current. If SENSE exceeds V_{ACL}, the analog current-limit amplifier pulls GATE down to regulate the MOSFET current at V_{ACL}/R_S. In the event of a catastrophic short-circuit, SENSE may overshoot V_{ACL}. If SENSE reaches V_{FCL} (200mV), the fast current-limit comparator pulls GATE low with a strong pull-down. To disable the circuit breaker and current limit functions, connect SENSE to V_{EE}.

V_{EE} (Pin 8): Negative Supply Voltage Input. Connect this pin to the negative side of the power supply.

GATE (Pin 9): N-channel MOSFET Gate Drive Output. This pin is pulled high by a 50µA current source. GATE is pulled low by invalid conditions at V_{IN} (UVLO), UV, OV, during the initial timing cycle, a circuit breaker fault time-out or the RESET pin going high. GATE is actively servoed to control the fault current as measured at SENSE. Compensation capacitor, C_C, at GATE stabilizes this loop. A comparator monitors GATE to ensure that it is low before allowing an initial timing cycle, then the GATE ramps up after an overvoltage event or restart after a current limit fault. During GATE start-up, a second comparator detects GATE within 2.8V of V_{IN} before $\overline{PWRGD1}$ can be set and power good sequencing starts.

DRAIN (Pin 10): Drain Sense Input. Connecting an external resistor, R_D between this pin and the MOSFET's drain (V_{OUT}) allows voltage sensing below 6.15V and current feedback to TIMER. A comparator detects if DRAIN is below 2.39V and together with the GATE high comparator, sets the $\overline{PWRGD1}$ flag. If V_{OUT} is above V_{DRNCL}, the DRAIN pin is clamped at approximately V_{DRNCL}. R_D current is internally multiplied by 8 and added to TIMER's 200µA during a circuit breaker fault cycle. This reduces the fault time and MOSFET heating.

OV (Pin 11): Overvoltage Input. For the LTC4253B, the threshold at the OV pin is set at 6.15V with 0.3V hysteresis. If OV > 6.15V, GATE pulls low. When OV returns below 5.85V, GATE start-up begins without an initial timing cycle. If OV occurs in the middle of an initial timing cycle, the initial timing cycle is restarted after OV goes away. OV does not reset the latched fault or $\overline{PWRGD1}$ flag. The internal UVLO at V_{IN} always overrides OV. A 1nF to 10nF capacitor at OV prevents transients and switching noise from affecting the OV thresholds and prevents glitches at the GATE.

PIN FUNCTIONS

UV (Pin 12): Undervoltage Input. For the LTC4253B, the threshold at the UV pin is set at 3.225V with 0.3V hysteresis. If UV < 2.925V, $\overline{PWRGD1}$ pulls high, both GATE and TIMER pull low. If UV rises above 3.225V, this initiates an initial timing cycle followed by GATE start-up. The internal UVLO at V_{IN} always overrides UV. A low at UV resets an internal fault latch. A 1nF to 10nF capacitor at UV prevents transients and switching noise from affecting the UV thresholds and prevents glitches at the GATE pin.

TIMER (Pin 13): Timer Input. Timer is used to generate an initial timing delay at start-up, and to delay shutdown in the event of an output overload (circuit breaker fault). Timer starts an initial timing cycle when the following conditions are met: RESET is low, UV is high, OV is low, V_{IN} clears UVLO, TIMER pin is low, GATE pin is lower than V_{GATEL}, SS < 0.2V, and $V_{SENSE} - V_{EE} < V_{CB}$. A pull-up current of 5µA then charges C_T, generating a time delay. If C_T charges to V_{TMRH} (4V), the timing cycle terminates. TIMER quickly pulls low and GATE is activated.

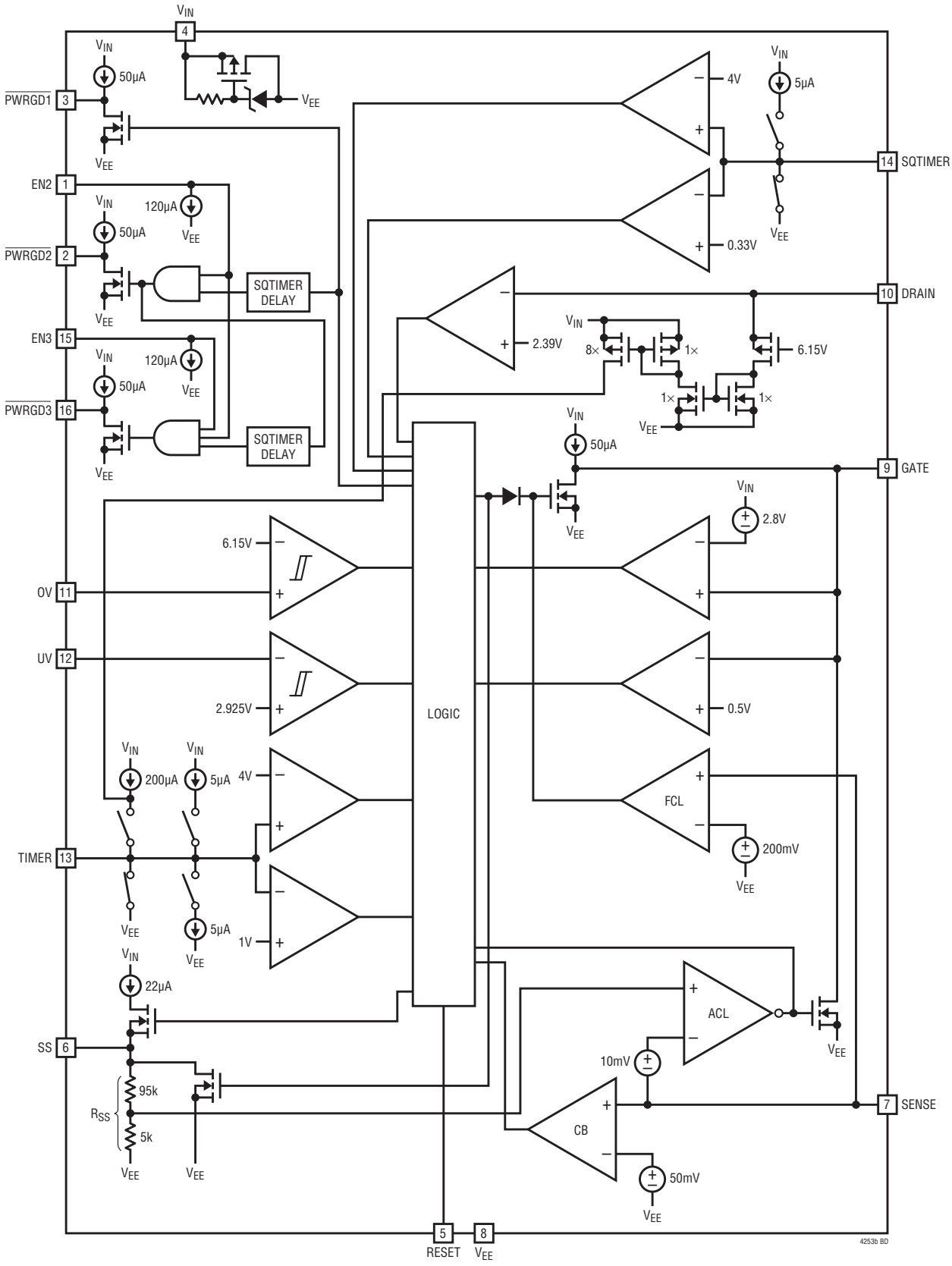
If SENSE exceeds 50mV while GATE is high, a circuit breaker cycle begins with a 200µA pull-up current charging C_T. If DRAIN is approximately 7V during this cycle, the timer pull-up has an additional current of 8 • I_{DRN}. If SENSE drops below 50mV before TIMER reaches 4V, a 5µA pull-down current slowly discharges the C_T. In the event that C_T eventually integrates up to the V_{TMRH} (4V) threshold, the circuit breaker trips, GATE quickly pulls low and $\overline{PWRGD1}$ pulls high. TIMER latches high with a 5µA pull-up source. This latched fault may be cleared by driving RESET high until TIMER is pulled low. Other ways of clearing the fault include pulling the V_{IN} pin momentarily below ($V_{LKO} - V_{LKH}$), pulling TIMER low with an external device or pulling UV below 2.925V.

SQTIMER (Pin 14): Sequencing Timer Input. The sequencing timer provides a delay t_{SQT} for the power good sequencing. This delay is adjusted by connecting an appropriate capacitor to this pin. If the SQTIMER capacitor is omitted, the SQTIMER pin ramps from 0V to 4V in about 300µs.

EN3 (Pin 15): Power Good Status Output Three Enable. This is a TTL compatible input that is used to control the $\overline{PWRGD3}$ output. When EN3 is driven low, $\overline{PWRGD3}$ will go high. When EN3 is driven high, $\overline{PWRGD3}$ will go low provided $\overline{PWRGD2}$ has been active for for more than one power good sequence delay (t_{SQT}). EN3 can be used to control the power good sequence. This pin is internally pulled low by a 120µA current source.

$\overline{PWRGD3}$ (Pin 16): Power Good Status Output Three. Power good sequence starts with $\overline{PWRGD1}$ latching active low. $\overline{PWRGD3}$ will latch active low after EN3 goes high and after one power good sequence delay t_{SQT} provided by the sequencing timer from the time $\overline{PWRGD2}$ goes low, whichever comes later. $\overline{PWRGD3}$ is reset by $\overline{PWRGD1}$ going high or EN3 going low. This pin is internally pulled high by a 50µA current source.

BLOCK DIAGRAM



OPERATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors can draw huge transient currents from the power bus as they charge. The flow of current damages the connector pins and glitches the power bus, causing other boards in the system to reset. The LTC4253B is designed to turn on a circuit board supply in a controlled manner, allowing insertion or removal without glitches or connector damage.

Initial Start-Up

The LTC4253B resides on a removable circuit board and control the path between the connector and load or power conversion circuitry with an external MOSFET switch (see Figure 1). Both inrush control and short-circuit protection are provided by the MOSFET.

A detailed schematic is shown in Figure 2. –48V and –48RTN receive power through the longest connector pins and are the first to connect when the board is inserted. The GATE pin holds the MOSFET off during this time. UV/OV determines whether or not the MOSFET should be turned on based upon internal high accuracy thresholds and an external divider. UV/OV does double duty by also monitoring whether or not the connector is seated. The top of the divider detects –48RTN by way of a short connector pin that is the last to mate during the insertion sequence.

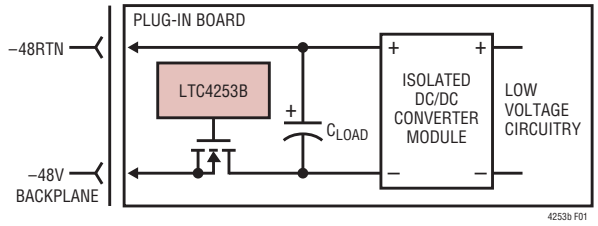


Figure 1. Basic LTC4253B Hot Swap Topology

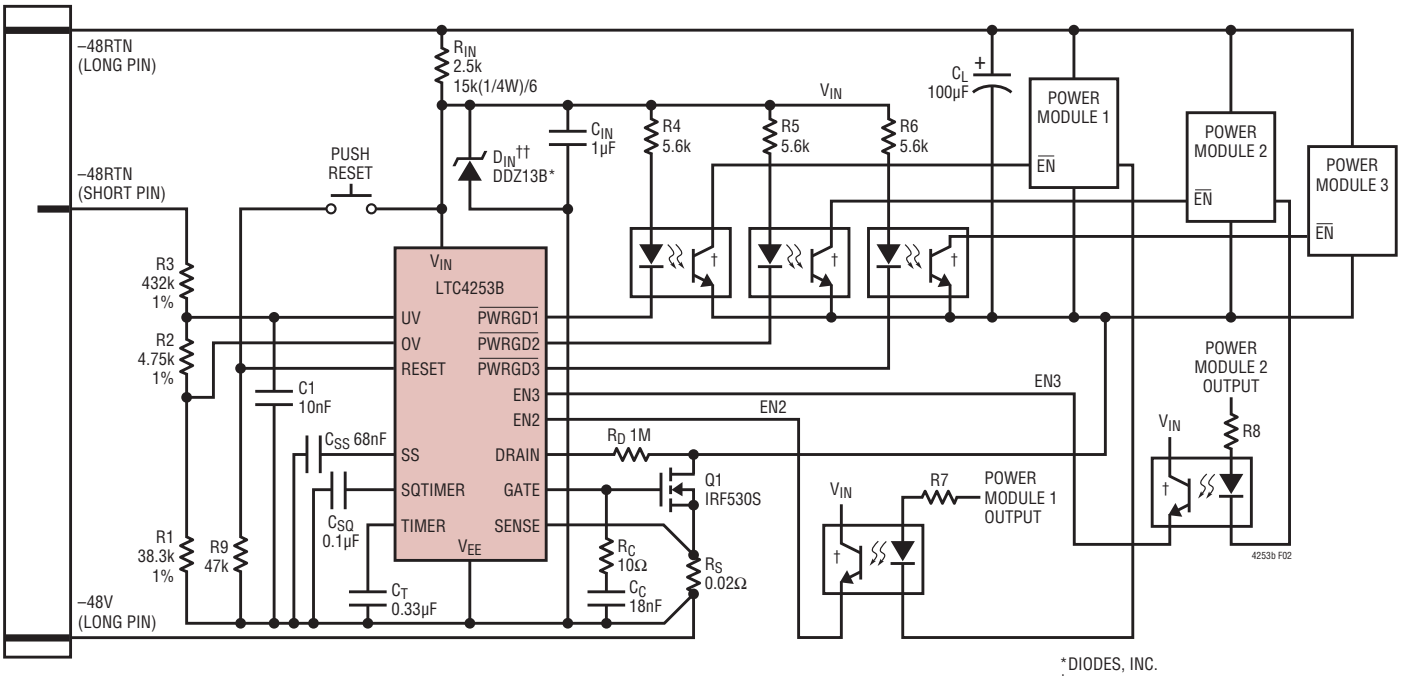


Figure 2. –48V/2.5A Application with a Wider Operating Range

OPERATION

Interlock Conditions

A start-up sequence commences once these "interlock" conditions are met:

1. The input voltage V_{IN} exceeds V_{LKO} (UVLO).
2. The voltage at UV > V_{UVHI}.
3. The voltage at OV < V_{OVLO}.
4. The input voltage at RESET < 0.8V.
5. The (SENSE – V_{EE}) voltage < 50mV (V_{CB})
6. The voltage at SS is < 0.2V (20 • V_{OS})
7. The voltage on the TIMER capacitor (C_T) is < 1V (V_{TMRL}).
8. The voltage at GATE is < 0.5V (V_{GATEL})

The first four conditions are continuously monitored and the latter four are checked prior to initial timing or GATE ramp-up. Upon exiting an OV condition, the TIMER pin voltage requirement is inhibited. Details are described in the Applications Information, Timing Waveforms section.

If RESET < 0.8V occurs after the LTC4253B comes out of UVLO (interlock condition 1) and undervoltage (interlock condition 2), GATE and SS are released without an initial TIMER cycle once the other interlock conditions are met (see Figure 12a). If not, TIMER begins the start-up sequence by sourcing 5µA into C_T. If V_{IN}, UV or OV falls out of range or RESET asserts, the start-up cycle stops and TIMER discharges C_T to less than 1V, then waits until the aforementioned conditions are once again met. If C_T successfully charges to 4V, TIMER pulls low and both SS and GATE pins are released. GATE sources 50µA (I_{GATE}), charging the MOSFET gate and associated capacitance. The SS voltage ramp limits V_{SENSE} to control the inrush current. $\overline{PWRGD1}$ pulls active low when GATE is within 2.8V of V_{IN} and DRAIN is lower than V_{DRNL}. This sets off the power good sequence in which $\overline{PWRGD2}$ and then $\overline{PWRGD3}$ is subsequently pulled low after a delay, adjustable through the SQTIMER capacitor C_{SQ} or by external control inputs EN2 and EN3. In this way, external loads or power modules controlled by the three $\overline{PWRGD}$ signals are turned on in a controlled manner without overloading the power bus.

Two modes of operation are possible during the time the MOSFET is first turned on, depending on the values of external components, MOSFET characteristics and nominal design current. One possibility is that the MOSFET will turn on gradually so that the inrush into the load capacitance remains a low value. The output will simply ramp to –48V and the LTC4253B will fully enhance the MOSFET. A second possibility is that the load current exceeds the soft-start current limit threshold of $[V_{SS}(t)/20 – V_{OS}]/R_S$. In this case the LTC4253B ramps the output by sourcing soft-start limited current into the load capacitance. If the soft-start voltage is below 1.2V, the circuit breaker TIMER is held low. Above 1.2V, TIMER ramps up. It is important to set the timer delay so that, regardless of which start-up mode is used, the TIMER ramp is less than one circuit breaker delay time. If this condition is not met, the LTC4253B may shut down after one circuit breaker delay time.

Board Removal

When the board is withdrawn from the card cage, the UV/OV divider is the first to lose connection. This shuts off the MOSFET and commutates the flow of current in the connector. When the power pins subsequently separate there is no arcing.

Current Control

Three levels of protection handle short-circuit and overload conditions. Load current is monitored by SENSE and resistor R_S. There are three distinct thresholds at SENSE: 50mV for a timed circuit breaker function; 100mV for an analog current limit loop; and 200mV for a fast, feedforward comparator which limits peak current in the event of a catastrophic short-circuit.

If, due to an output overload, the voltage drop across R_S exceeds 50mV, TIMER sources 200µA into C_T. C_T eventually charges to a 4V threshold and the LTC4253B shuts off. If the overload goes away before C_T reaches 4V and SENSE measures less than 50mV, C_T slowly discharges (5µA). In this way the LTC4253B's circuit breaker function responds to low duty cycle overloads, and accounts for the fast heating and slow cooling characteristic of the MOSFET.

OPERATION

Higher overloads are handled by an analog current limit loop. If the drop across R_S reaches V_{ACL}, the current limiting loop servos the MOSFET gate and maintains a constant output current of V_{ACL}/R_S. In current limit mode, V_{OUT} (MOSFET drain-source voltage drop) typically rises and this increases MOSFET heating. If $V_{OUT} > V_{DRNCL}$, connecting an external resistor, R_D between V_{OUT} and DRAIN allows the fault timing cycle to be shortened by accelerating the charging of the TIMER capacitor. The TIMER pull-up current is increased by 8 • I_{DRN}. Note that because SENSE > 50mV, TIMER charges C_T during this time, and the LTC4253B eventually shuts down.

Low impedance failures on the load side of the LTC4253B, coupled with 48V or more driving potential, can produce current slew rates well in excess of 50A/µs. Under these conditions, overshoot is inevitable. A fast SENSE comparator with a threshold of 200mV detects overshoot and pulls GATE low much harder and hence much faster than the weaker current limit loop. The V_{ACL}/R_S current limit loop then takes over and servos the current as previously described. As before, TIMER runs and shuts down the LTC4253B when C_T reaches 4V.

If C_T reaches 4V, the LTC4253B latches off with a 5µA pull-up current source. The LTC4253B circuit breaker latch is reset by either pulling the RESET pin active high until TIMER goes low, pulling UV momentarily low, dropping the input voltage V_{IN} below the internal UVLO threshold or pulsing TIMER momentarily low with a switch.

Although short-circuits are the most obvious fault type, several operating conditions may invoke overcurrent protection. Noise spikes from the backplane or load, input steps caused by the connection of a second, higher voltage supply, transient currents caused by faults on adjacent circuit boards sharing the same power bus or the insertion of non-hot swappable products could cause higher than anticipated input current and temporary detection of an overcurrent condition. The action of TIMER and C_T rejects these events allowing the LTC4253B to “ride out” temporary overloads and disturbances that could trip a simple current comparator and, in some cases, blow a fuse.

APPLICATIONS INFORMATION (Refer to Block Diagram)

SHUNT REGULATOR

A fast responding shunt regulator clamps the V_{IN} pin to 13V (V_Z). Power is derived from –48RTN by an external current limiting resistor, R_{IN}. A 1µF decoupling capacitor, C_{IN} filters supply transients and contributes a short delay at start-up.

To meet creepage requirements R_{IN} may be split into two or more series connected units. This introduces a wider total spacing than is possible with a single component while at the same time ballasting the potential across the gap under each resistor. The LTC4253B is fundamentally a low voltage device that operates with –48V as its reference ground. To further protect against arc discharge into its pins, the area in and around the LTC4253B and all associated components should be free of any other planes such as chassis ground, return, or secondary-side power and ground planes.

V_{IN} may be biased with additional current up to 30mA, to accommodate external loading such as the $\overline{\text{PWRGD}}$ opto-couplers shown in Figure 2. As an alternative to running higher current, simply buffer V_{IN} with an emitter follower. A method that cascodes the $\overline{\text{PWRGD}}$ outputs is shown in Figure 16.

V_{IN} is rated to handle 30mA within the thermal limits of the package, and is tested to survive a 100µs, 100mA

APPLICATIONS INFORMATION

pulse. To protect V_{IN} against damage from higher amplitude spikes, clamp V_{IN} to V_{EE} with a 13V Zener diode. Star connect V_{EE} and all V_{EE}-referred components to the sense resistor Kelvin terminal as illustrated in Figure 2, keeping trace lengths between V_{IN}, C_{IN}, D_{IN} and V_{EE} as short as possible.

INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

A hysteretic comparator, UVLO, monitors V_{IN} for undervoltage. The thresholds are defined by V_{LKO} and its hysteresis V_{LKH}. When V_{IN} rises above V_{LKO}, the chip is enabled; below ($V_{LKO} – V_{LKH}$), it is disabled and GATE is pulled low. The UVLO function at V_{IN} should not be confused with the UV and OV pins. These are completely separate functions.

UV/OV COMPARATORS

A UV hysteretic comparator detects undervoltage conditions at the UV pin, with the following thresholds:

UV low-to-high (V_{UVHI}) = 3.225V

UV high-to-low (V_{UVLO}) = 2.925V

An OV hysteretic comparator detects overvoltage conditions at the OV pin, with the following thresholds:

OV low-to-high (V_{OVHI}) = 6.150V

OV high-to-low (V_{OVLO}) = 5.850V

The UV and OV trip point ratio is designed to match the standard telecom operating range of 43V to 82V when connected together as in the Typical Application. A resistive divider is used to scale the supply voltage. Using 402k and 32.4k gives a typical operating range of 43.2V to 82.5V. The undervoltage shutdown and overvoltage recovery thresholds are then 39.2V and 78.4V. 1% divider resistors are recommended to preserve threshold accuracy.

The resistive divider values shown set a standing current of slightly more than 100µA and define an impedance at UV/OV of 30kΩ. In most applications, 30kΩ impedance coupled with 300mV UV hysteresis make the LTC4253B insensitive to noise. If more noise immunity is desired, add a 1nF to 10nF filter capacitor from UV/OV to V_{EE}.

The separate UV and OV pins can be used for wider operating range such as 35.6V to 76.3V range as shown in Figure 2. Other combinations are possible with different resistors arrangement.

UV/OV OPERATION

A low input to the UV comparator will reset the chip and pull the GATE and TIMER pins low. A low-to-high UV transition will initiate an initial timing sequence if the other interlock conditions are met. A high-to-low transition in the UV comparator immediately shuts down the LTC4253B, pulls the MOSFET gate low and resets the three latched $\overline{PWRGD}$ signals high.

An overvoltage condition is detected by the OV comparator and pulls GATE low, thereby shutting down the load, but it will not reset the circuit breaker TIMER and $\overline{PWRGD}$ flags. Returning from the overvoltage condition will restart the GATE pin if all the interlock conditions except TIMER are met. Only during the initial timing cycle does OV condition have an effect of resetting TIMER.

DRAIN

Connecting an external resistor, R_D, to this dual function DRAIN pin allows V_{OUT} (MOSFET drain-source voltage drop) sensing without it being damaged by large voltage transients. Below 5V, negligible pin leakage allows a DRAIN low comparator to detect V_{OUT} less than 2.39V (V_{DRNL}). This, together with the GATE low comparator, sets the $\overline{PWRGD}$ flag.

When $V_{OUT} > V_{DRNCL}$, the DRAIN pin is clamped at V_{DRNCL} and the current flowing in R_D is given by:

$$I_{DRN} \approx \frac{V_{OUT} - V_{DRNCL}}{R_D} \quad (1)$$

This current is scaled up 8 times during a circuit breaker fault before being added to the nominal 200µA. This accelerates the fault TIMER pull-up when the MOSFET's drain-source voltage exceeds V_{DRNCL} and effectively shortens the MOSFET heating duration.

APPLICATIONS INFORMATION

TIMER

The operation of the TIMER pin is somewhat complex as it handles several key functions. A capacitor C_T is used at TIMER to provide timing for the LTC4253B. Four different charging and discharging modes are available at TIMER:

1. 5µA slow charge; initial timing delay.
2. (200µA + 8 • I_{DRN}) fast charge; circuit breaker delay.
3. 5µA slow discharge; circuit breaker "cool-off."
4. Low impedance switch; resets the TIMER capacitor after an initial timing delay, in UVLO, in UV and in OV during initial timing and when RESET is high.

For initial timing delay, the 5µA pull-up is used. The low impedance switch is turned off and the 5µA current source is enabled when the interlock conditions are met. C_T charges to 4V in a time period given by:

$$t = \frac{4V \bullet C_T}{5\mu A} \quad (2)$$

When C_T reaches V_{TMRH} (4V), the low impedance switch turns on and discharges C_T. A GATE start-up cycle begins and both SS and GATE outputs are released.

CIRCUIT BREAKER TIMER OPERATION

If the SENSE pin detects more than 50mV drop across R_S, the TIMER pin charges C_T with (200µA + 8 • I_{DRN}). If C_T charges to 4V, the GATE pin pulls low and the LTC4253B latches off. The LTC4253B remains latched off until the RESET pin is momentarily pulsed high, the UV pin is momentarily pulsed low, the TIMER pin is momentarily discharged low by an external switch or V_{IN} dips below UVLO and is then restored. The circuit breaker timeout period is given by:

$$t = \frac{4V \bullet C_T}{200\mu A + 8 \bullet I_{DRN}} \quad (3)$$

If $V_{OUT} < 5V$, an internal PMOS isolates DRAIN pin leakage current and this makes $I_{DRN} = 0$ in Equation (3). If V_{OUT} is above V_{DRNCL} during the circuit breaker fault period, the charging of C_T is accelerated by 8 • I_{DRN} of Equation (1).

Intermittent overloads may exceed the 50mV threshold at SENSE but, if their duration is sufficiently short, TIMER will not reach 4V and the LTC4253B will not shut the external MOSFET off. To handle this situation, the TIMER discharges C_T slowly with a 5µA pull-down whenever the SENSE voltage is less than 50mV. Therefore, any intermittent overload with $V_{OUT} < 5V$ and an aggregate duty cycle of more than 2.5% will eventually trip the circuit breaker and shut down the LTC4253B. Figure 3 shows the circuit breaker response time in seconds normalized to 1µF. The asymmetric charging and discharging of C_T is a fair gauge of MOSFET heating.

The normalized circuit response time is estimated by:

$$\frac{t}{C_T(\mu F)} = \frac{4}{\left[\left(205 + 8 \bullet I_{DRN}\right) \bullet D - 5\right]} \text{ for } D > 2.5\% \quad (4)$$

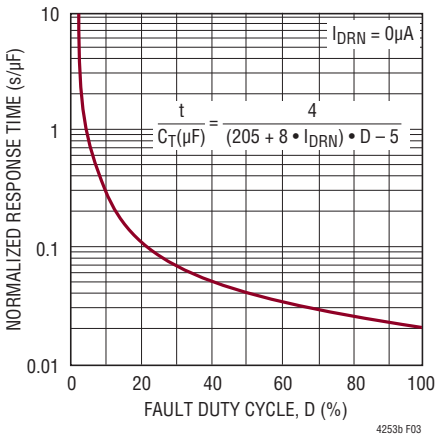


Figure 3. Circuit Breaker Response Time

APPLICATIONS INFORMATION

POWER GOOD SEQUENCING

After the initial TIMER cycle, GATE ramps up to turn on the external MOSFET which in turn pulls DRAIN low.

When GATE is within 2.8V of V_{IN} and DRAIN is lower than V_{DRNL}, the power good sequence starts with $\overline{PWRGD1}$ pulling active low. This starts off a 5µA pull-up on the SQTIMER pin which ramps up until it reaches the 4V threshold then pulls low. When the SQTIMER pin floats, this delay t_{SQT} is about 300µs. Connecting an external capacitor C_{SQ} from SQTIMER to V_{EE} modifies the delay to:

$$t_{SQT} = \frac{4V \bullet C_{SQ}}{5\mu A} \quad (5)$$

$\overline{PWRGD2}$ asserts when EN2 goes high and $\overline{PWRGD1}$ has asserted for more than one t_{SQT}. When $\overline{PWRGD2}$ successfully pulls low, SQTIMER ramps up on another delay cycle. $\overline{PWRGD3}$ asserts when EN2 and EN3 go high and $\overline{PWRGD2}$ has asserted for more than one t_{SQT}.

All three $\overline{PWRGD}$ signals are reset in UVLO, in UV condition, if RESET is high or when C_T charges up to 4V. In addition, $\overline{PWRGD2}$ is reset by EN2 going low. $\overline{PWRGD3}$ is reset by EN2 or EN3 going low. An overvoltage condition has no effect on the $\overline{PWRGD}$ flags. A 50µA current pulls each $\overline{PWRGD}$ pin high when reset. As power modules signal common are different from $\overline{PWRGD}$, optoisolation is recommended. These three pins can sink an optodiode current. Figure 16 shows an NPN configuration for the $\overline{PWRGD}$ interface. A limiting base resistor should be used for each NPN and the module enable input should have protection from negative bias current.

SOFT-START

Soft-start is effective in limiting the inrush current during GATE start-up. Unduly long soft-start intervals can exceed the MOSFET's SOA duration if powering-up into an active load. When the SS pin floats, an internal current source ramps SS from 0V to 2.2V in about 300µs. Connecting an external capacitor, C_{SS}, from SS to ground modifies the ramp to approximate an RC response of:

$$V_{SS}(t) \approx V_{SS}\left(1 - e^{\frac{-t}{R_{SS}C_{SS}}}\right) \quad (6)$$

An internal resistor divider (95k/5k) scales $V_{SS}(t)$ down by 20 times to give the analog current limit threshold:

$$V_{ACL}(t) = \frac{V_{SS}(t)}{20} - V_{OS} \quad (7)$$

This allows the inrush current to be limited to $V_{ACL}(t)/R_S$. The offset voltage, V_{OS} (10mV), ensures C_{SS} is sufficiently discharged and the ACL amplifier is in current limit mode before GATE start-up. SS is discharged low during UVLO at V_{IN} , UV, OV, during the initial timing cycle, a latched circuit breaker fault or the RESET pin going high.

GATE

GATE is pulled low to V_{EE} under any of the following conditions: in UVLO, when RESET pulls high, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or a latched circuit breaker fault. When GATE turns on, a 50µA current source charges the MOSFET gate and any associated external capacitance. V_{IN} limits the gate drive to no more than 14.5V.

Gate-drain capacitance (C_{GD}) feedthrough at the first abrupt application of power can cause a gate-source voltage sufficient to turn on the MOSFET. A unique circuit pulls GATE low with practically no usable voltage at V_{IN} and eliminates current spikes at insertion. A large external gate-source capacitor is thus unnecessary for the purpose of compensating C_{GD}. Instead, a smaller value (≥10nF) capacitor C_C is adequate. C_C also provides compensation for the analog current limit loop.

GATE has two comparators: the GATE low comparator looks for <0.5V threshold prior to initial timing; the GATE high comparator looks for <2.8V relative to V_{IN} and, together with DRAIN low comparator, sets $\overline{PWRGD1}$ output during GATE start-up.

APPLICATIONS INFORMATION

Sense

The SENSE pin is monitored by the circuit breaker (CB) comparator, the analog current limit (ACL) amplifier, and the fast current limit (FCL) comparator. Each of these three measures the potential of SENSE relative to V_{EE}. When SENSE exceeds 50mV, the CB comparator activates the 200µA TIMER pull-up. At 100mV the ACL amplifier servos the MOSFET current, and at 200mV the FCL comparator abruptly pulls GATE low in an attempt to bring the MOSFET current under control. If any of these conditions persists long enough for TIMER to charge C_T to 4V (see Equation 3), the LTC4253B shuts down and pulls GATE low.

If the SENSE pin encounters a voltage greater than V_{ACL}, the ACL amplifier will servo GATE downwards in an attempt to control the MOSFET current. Since GATE overdrives the MOSFET in normal operation, the ACL amplifier needs time to discharge GATE to the threshold of the MOSFET. For a mild overload the ACL amplifier can control the MOSFET current, but in the event of a severe overload the current may overshoot. At SENSE = 200mV the FCL comparator takes over, quickly discharging the GATE pin to near V_{EE} potential. FCL then releases, and the ACL amplifier takes over. All the while TIMER is running. The effect of FCL is to add a nonlinear response to the control loop in favor of reducing MOSFET current.

Owing to inductive effects in the system, FCL typically overcorrects the current limit loop, and GATE undershoots. A zero in the loop (resistor R_C in series with the gate capacitor) helps the ACL amplifier to recover.

SHORT-CIRCUIT OPERATION

Circuit behavior arising from a load side low impedance short is shown in Figure 4. Initially the current overshoots the analog current limit level of V_{SENSE} = 200mV (trace 2) as the GATE pin works to bring V_{GS} under control (trace 3). The overshoot glitches the backplane in the negative direction and when the current is reduced to 100mV/R_S, the backplane responds by glitching in the positive direction. TIMER commences charging C_T (trace 4) while the analog current limit loop maintains the fault current at 100mV/R_S, which in this case is 5A (trace 2). Note that the backplane voltage (trace 1) sags under load. Timer pull-up is accelerated by V_{OUT}. When C_T reaches 4V, GATE turns off, the $\overline{PWRGD}$ signals pull high, the load current drops to zero and the backplane rings up to over 100V. The transient associated with the GATE turn-off can be controlled with a snubber to reduce ringing and a transient voltage suppressor (such as Diodes Inc. SMAT70A) to clip off large spikes. The choice of RC for the snubber is usually done experimentally. The value of the snubber capacitor is usually chosen between 10 to 100 times the MOSFET C_{OSS}. The value of the snubber resistor is typically between 3Ω to 100Ω.

A low impedance short on one card may influence the behavior of others sharing the same backplane. The initial glitch and backplane sag as seen in Figure 4 trace 1, can rob charge from output capacitors on the adjacent card. When the faulty card shuts down, current flows in to refresh the capacitors. If LTC4253B is used by the other cards, they respond by limiting the inrush current to a value of V_{ACL}/R_S. If C_T is sized correctly, the capacitors will recharge long before C_T times out.

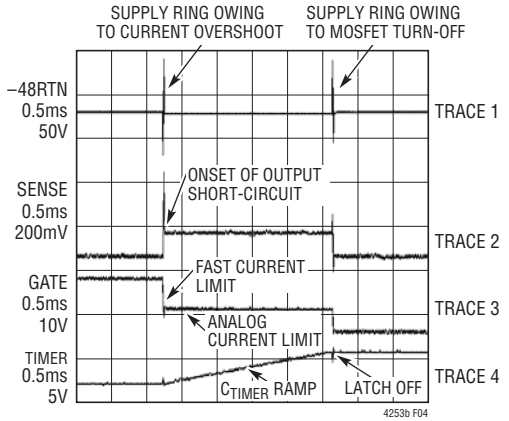


Figure 4. Output Short-Circuit Behavior of LTC4253B

APPLICATIONS INFORMATION

MOSFET SELECTION

The external MOSFET switch must have adequate safe operating area (SOA) to handle short-circuit conditions until TIMER times out. These considerations take precedence over DC current ratings. A MOSFET with adequate SOA for a given application can always handle the required current but the opposite may not be true. Consult the manufacturer's MOSFET data sheet for safe operating area and effective transient thermal impedance curves.

MOSFET selection is a 3-step process by assuming the absence of soft-start capacitor. First, R_S is calculated and then the time required to charge the load capacitance is determined. This timing, along with the maximum short-circuit current and maximum input voltage, defines an operating point that is checked against the MOSFET's SOA curve.

To begin a design, first specify the required load current and load capacitance, I_L and C_L. The circuit breaker current trip point (V_{CB}/R_S) should be set to accommodate the maximum load current. Note that maximum input current to a DC/DC converter is expected at $V_{SUPPLY(MIN)}$. R_S is given by:

$$R_S = \frac{V_{CB(MIN)}}{I_{L(MAX)}} \quad (8)$$

where $V_{CB(MIN)}$ = 40mV represents the guaranteed minimum circuit breaker threshold.

During the initial charging process, the LTC4253B may operate the MOSFET in current limit, forcing (V_{ACL}) between 80mV to 120mV across R_S. The minimum inrush current is given by:

$$I_{INRUSH(MIN)} = \frac{V_{ACL(MIN)}}{R_S} \quad (9)$$

Maximum short-circuit current limit is calculated using the maximum V_{SENSE}. This gives

$$I_{SHORTCIRCUIT(MAX)} = \frac{V_{ACL(MAX)}}{R_S} \quad (10)$$

The TIMER capacitor C_T must be selected based on the slowest expected charging rate; otherwise TIMER might time out before the load capacitor is fully charged. A value for C_T is calculated based on the maximum time it takes the load capacitor to charge. That time is given by:

$$t_{CL(CHARGE)} = \frac{C \bullet V}{I} = \frac{C_L \bullet V_{SUPPLY(MAX)}}{I_{INRUSH(MIN)}} \quad (11)$$

The maximum current flowing in the DRAIN pin is given by:

$$I_{DRN(MAX)} = \frac{V_{SUPPLY(MAX)} - V_{DRNCL}}{R_D} \quad (12)$$

Approximating a linear charging rate, I_{DRN} drops from $I_{DRN(MAX)}$ to zero, the I_{DRN} component in Equation (3) can be approximated with 0.5 • $I_{DRN(MAX)}$. Rearranging the equation, TIMER capacitor C_T is given by:

$$C_T = \frac{t_{CL(CHARGE)} \bullet (200\mu A + 4 \bullet I_{DRN(MAX)})}{4V} \quad (13)$$

Returning to Equation (3), the TIMER period is calculated and used in conjunction with $V_{SUPPLY(MAX)}$ and $I_{SHORTCIRCUIT(MAX)}$ to check the SOA curves of a prospective MOSFET.

As a numerical design example for the LTC4253B, consider a 30W load, which requires 1A input current at 36V. If $V_{SUPPLY(MAX)}$ = 72V and C_L = 100µF, R_D = 1MΩ, Equation (8) gives R_S = 40mΩ; Equation (13) gives C_T = 414nF. To account for errors in R_S, C_T, TIMER current (200µA), TIMER threshold (4V), R_D, DRAIN current multiplier and DRAIN voltage clamp (V_{DRNCL}), the calculated value should be multiplied by 1.5, giving the nearest standard value of C_T = 680nF.

If a short-circuit occurs, a current of up to 120mV/40mΩ = 3A will flow in the MOSFET for 6.3ms as dictated by C_T = 680nF in Equation (3). The MOSFET must be selected based on this criterion. The IRF530S can handle 100V and 3A for 10ms and is safe to use in this application.

APPLICATIONS INFORMATION

Computing the maximum soft-start capacitor value during soft-start to a load short is complicated by the nonlinear MOSFET's SOA characteristics and the $R_{SS}C_{SS}$ response. An overconservative but simple approach begins with the maximum circuit breaker current, given by:

$$I_{CB(MAX)} = \frac{V_{CB(MAX)}}{R_S} \quad (14)$$

where $V_{CB(MAX)}$ is 60mV.

From the SOA curves of a prospective MOSFET, determine the time allowed, $t_{SOA(MAX)}$. C_{SS} is given by:

$$C_{SS} = \frac{t_{SOA(MAX)}}{0.916 \bullet R_{SS}} \quad (15)$$

In the above example, 60mV/40mΩ gives 1.5A. $t_{SOA(MAX)}$ for the IRF530S is 40ms. From Equation (15), C_{SS} = 437nF. Actual board evaluation showed that C_{SS} = 100nF was appropriate. The ratio ($R_{SS} \bullet C_{SS}$) to $t_{CL(CHARGE)}$ is a good gauge as large ratios may result in the time-out period expiring prematurely. This gauge is determined empirically with board level evaluation.

SUMMARY OF DESIGN FLOW

To summarize the design flow, consider the Typical Application shown on the front page. It was designed for 80W and C_L = 100µF.

Calculate maximum load current: 80W/43V = 1.86A.

Calculate R_S: from Equation (8) R_S = 20mΩ.

Calculate $I_{SHORTCIRCUIT(MAX)}$: from Equation (10) $I_{SHORTCIRCUIT(MAX)}$ = 6A.

Select a MOSFET that can handle 6A at 82V: IRF530S.

Calculate C_T: from Equation (13) C_T = 256nF. Select C_T = 330nF, which gives the circuit breaker time-out period t_{MAX} = 1.65ms.

Consult MOSFET SOA curves: the IRF530S can handle 6A at 100V for 2.5ms, so it is safe to use in this application.

Calculate C_{SS}: using Equations (14) and (15) select C_{SS} = 68nF.

FREQUENCY COMPENSATION

The LTC4253B typical frequency compensation network for the analog current limit loop is a series R_C (10Ω) and C_C connected from GATE to V_{EE}. Figure 5 depicts the relationship between the compensation capacitor C_C and the MOSFET's C_{ISS}. The line in Figure 5 is used to select a starting value for C_C based upon the MOSFET's C_{ISS} specification. Optimized values for C_C are shown for several popular MOSFETs. Differences in the optimized value of C_C versus the starting value are small. Nevertheless, compensation values should be verified by board level short-circuit testing.

As seen in Figure 4, at the onset of a short-circuit event, the input supply voltage can ring dramatically due to series inductance. If this voltage avalanches the MOSFET, current continues to flow through the MOSFET to the output. The analog current limit loop cannot control this current flow and therefore the loop undershoots. This effect cannot be eliminated by frequency compensation. A Zener diode is required to clamp the input supply voltage and prevent MOSFET avalanche.

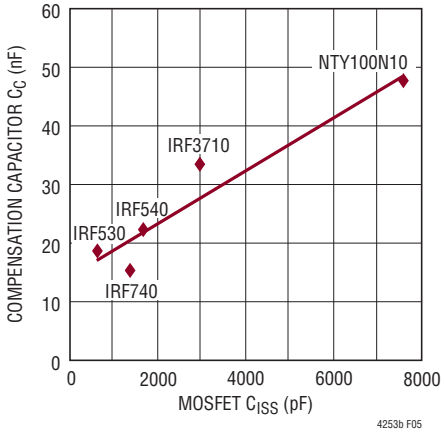


Figure 5. Recommended Compensation Capacitor C_C vs MOSFET C_{ISS} for the LTC4253B

APPLICATIONS INFORMATION

SENSE RESISTOR CONSIDERATIONS

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4253B's V_{EE} and SENSE pins are strongly recommended. The drawing in Figure 6 illustrates the correct way of making connections between the LTC4253B and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

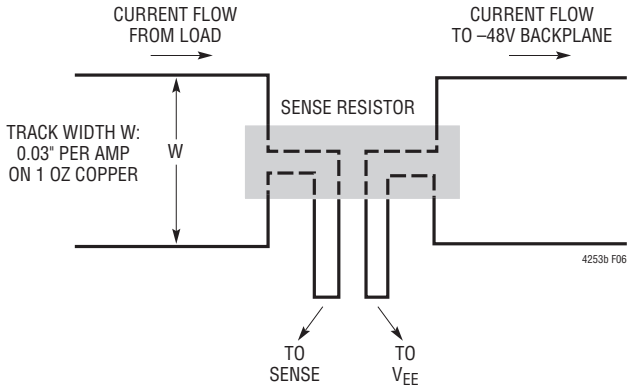


Figure 6. Making PCB Connections to the Sense Resistor

TIMING WAVEFORMS

System Power-Up

Figure 7 details the timing waveforms for a typical power-up sequence in the case where a board is already installed in the backplane and system power is applied abruptly. At time point 1, the supply ramps up, together with UV/OV, V_{OUT} and DRAIN. V_{IN} and the $\overline{PWRGD}$ signals follow at a slower rate as set by the V_{IN} bypass capacitor. At time point 2, V_{IN} exceeds V_{LKO} and the internal logic checks for UV > V_{UVHI}, OV < V_{OVLO}, RESET < 0.8V, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS}, and TIMER < V_{TMRL}. When all conditions are met, initial timing starts and the TIMER capacitor is charged by a 5µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be satisfied before the GATE start-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS} (as in Equation 6); GATE is held low by the analog current limit (ACL) amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 50µA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current flows into the load capacitor at time point 5. At time point 6, load current reaches SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed, the SENSE voltage is regulated at $V_{ACL}(t)$ (Equation 7) and soft-start limits the slew rate of the load current. If the SENSE voltage (V_{SENSE} – V_{EE}) reaches the V_{CB} threshold at time point 7, circuit breaker TIMER activates. The TIMER capacitor, C_T, is charged by a (200µA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline. At time point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB}, the fault TIMER ends, followed by a 5µA discharge cycle (cool-off). The duration between time points 7 and 9 must be shorter than one circuit breaker delay to avoid fault time-out during GATE ramp-up. When GATE ramps past the V_{GATEH} threshold at time point A, $\overline{PWRGD1}$ pulls low. At time point B, GATE reaches its maximum voltage as determined by V_{IN}. At time point A, SQTIMER starts its ramp-up to 4V. Having satisfied the requirement that $\overline{PWRGD1}$ is low for more than one t_{SQT}, $\overline{PWRGD2}$ pulls low after EN2 pulls high above the V_{IH} threshold at time point C. This sets off the second SQTIMER ramp-up. Having satisfied the requirement that $\overline{PWRGD2}$ is low for more than one t_{SQT}, $\overline{PWRGD3}$ pulls low after EN3 pulls high at time point D.

APPLICATIONS INFORMATION

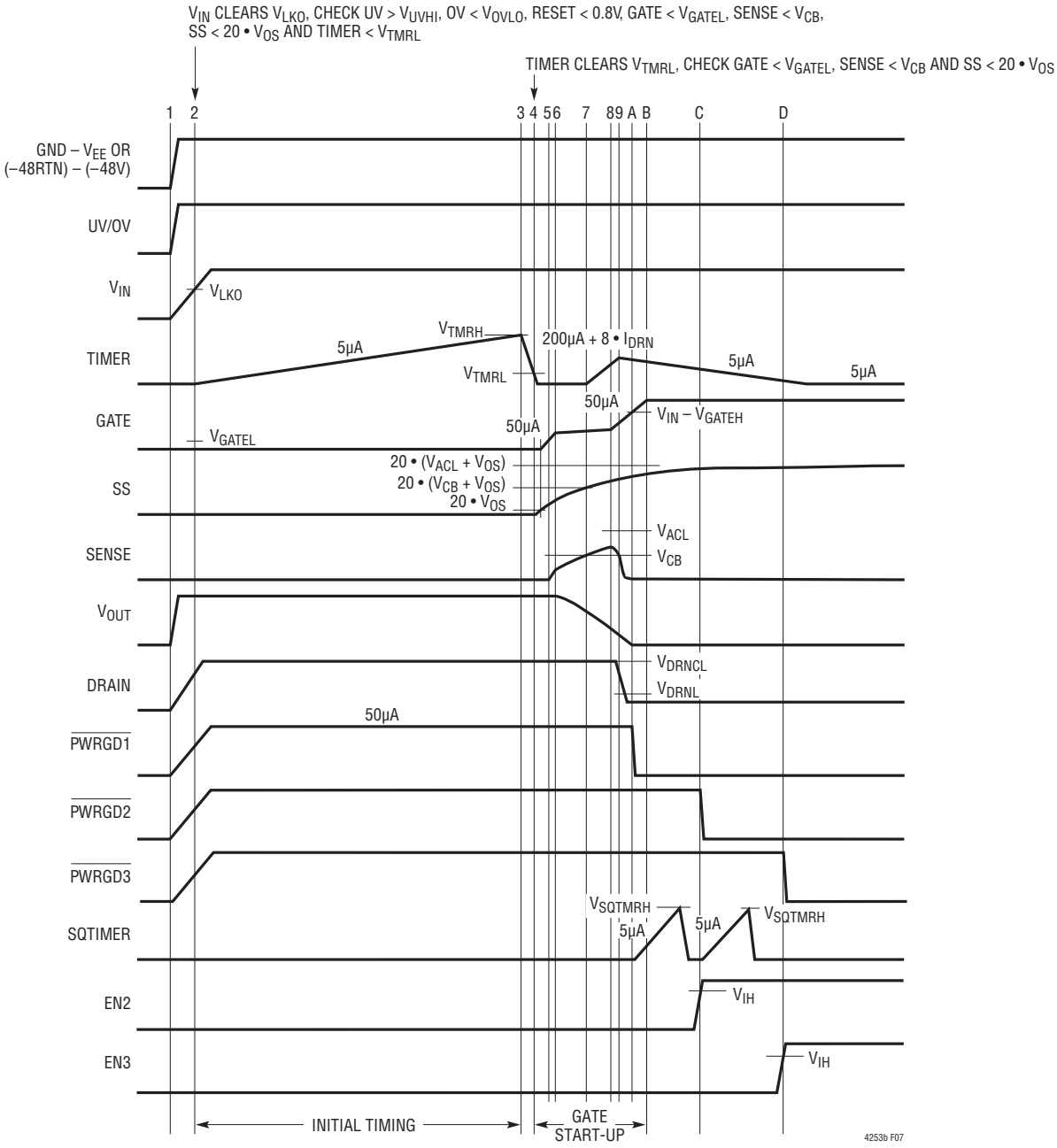


Figure 7. System Power-Up Timing (All Waveforms Are Referenced to V_{EE})

APPLICATIONS INFORMATION

Live Insertion with Short Pin Control of UV/OV

In the example shown in Figure 8, power is delivered through long connector pins whereas the UV/OV divider makes contact through a short pin. This ensures the power connections are firmly established before the LTC4253B is activated. At time point 1, the power pins make contact and V_{IN} ramps through V_{LKO}. At time point 2, the UV/OV divider makes contact and its voltage exceeds V_{UVHI}. In

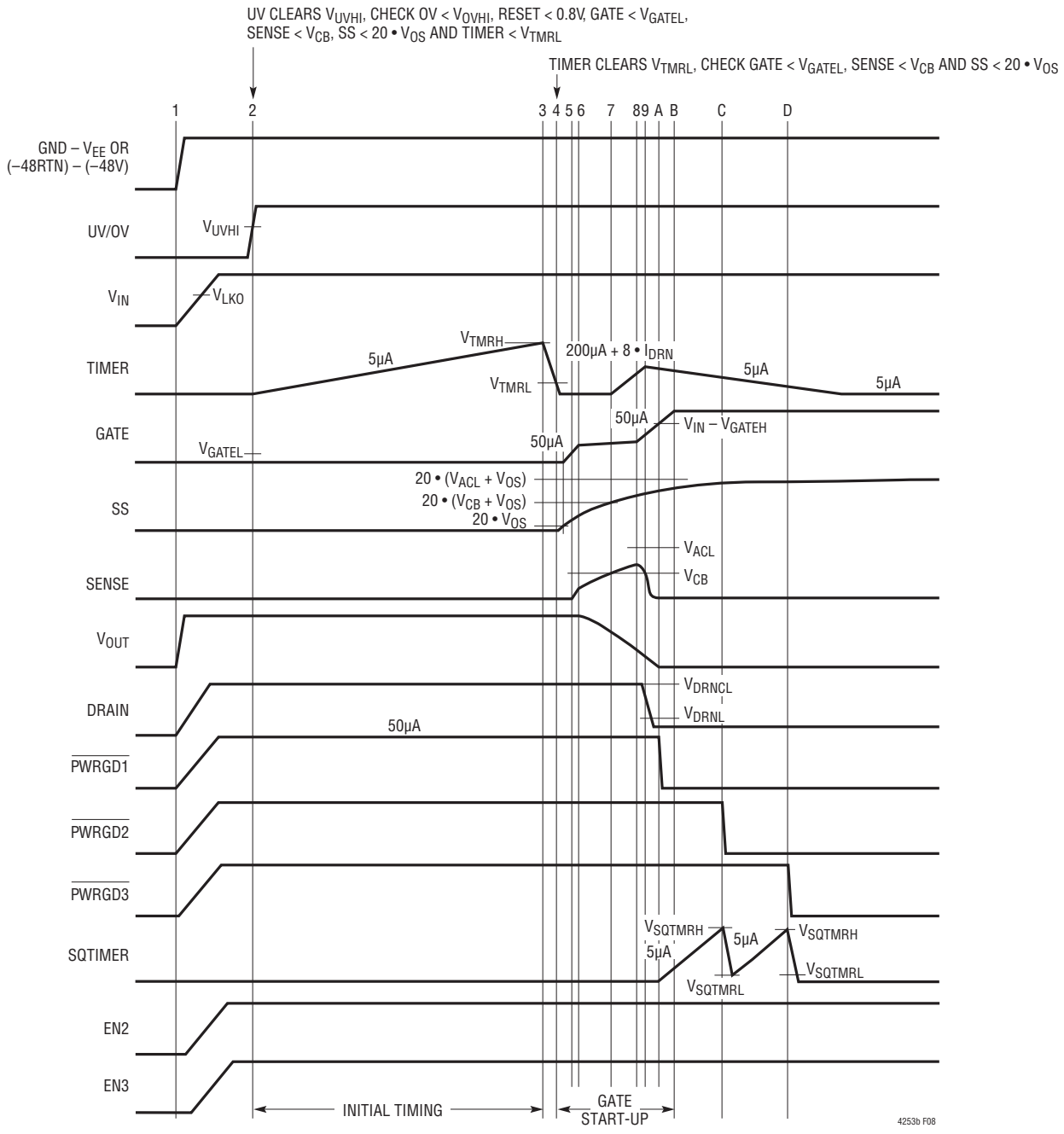


Figure 8. Power-Up Timing with a Short Pin (All Waveforms Are Referenced to VEE)

APPLICATIONS INFORMATION

addition, the internal logic checks for OV < V_{OVHI}, RESET < 0.8V, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS} and TIMER < V_{TMRL}. When all conditions are met, initial timing starts and the TIMER capacitor is charged by a 5µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be satisfied before the GATE start-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS}; GATE is held low by the analog current limit amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 50µA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor at time point 5. At time point 6, load current reaches SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed and the SENSE voltage is regulated at $V_{ACL}(t)$ and soft-start limits the slew rate of the load current. If the SENSE voltage (V_{SENSE} – V_{EE}) reaches the V_{CB} threshold at time point 7, the circuit breaker TIMER activates. The TIMER capacitor, C_T is charged by a (200µA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline. At point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB} and the fault TIMER ends, followed by a 5µA discharge current source (cool-off). When GATE ramps past V_{GATEH} threshold at time point A, $\overline{PWRGD1}$ pulls low, starting off the $\overline{PWRGD}$ sequence. $\overline{PWRGD2}$ pulls low at time point C when EN2 is high and $\overline{PWRGD1}$ is low for more than one t_{SQT}. $\overline{PWRGD3}$ pulls low at time point D when EN2 and EN3 is high and $\overline{PWRGD2}$ is low for more than one t_{SQT}. At time point B, GATE reaches its maximum voltage as determined by V_{IN}.

Undervoltage Timing

In Figure 9 when the UV pin drops below V_{UVLO} at time point 1, the LTC4253B shuts down with TIMER, SS and GATE pulled low. If current has been flowing, the SENSE pin voltage decreases to zero as GATE collapses. When UV recovers and clears V_{UVHI} at time point 2, an initial time cycle begins followed by a start-up cycle.

V_{IN} Undervoltage Lockout Timing

V_{IN} undervoltage lockout comparator, UVLO has a similar timing behavior as the UV pin timing except it looks at V_{IN} < (V_{LKO} – V_{LKH}) to shut down and V_{IN} > V_{LKO} to start. In an undervoltage lockout condition, both UV and OV comparators are held off. When V_{IN} exits undervoltage lockout, the UV and OV comparators are enabled.

Overvoltage Timing

During normal operation, if the OV pin exceeds V_{OVHI} as shown at time point 1 of Figure 10, the TIMER and $\overline{PWRGD}$ status are unaffected; SS and GATE pull down; load disconnects. At time point 2, OV recovers and drops below the V_{OVLO} threshold; GATE start-up begins. If the overvoltage glitch is long enough to deplete the load capacitor, time points 4 through 7 may occur.

Circuit Breaker Timing

In Figure 11a, the TIMER capacitor charges at 200µA if the SENSE pin exceeds V_{CB} but V_{DRN} is less than 5V. If the SENSE pin returns below V_{CB} before TIMER reaches the V_{TMRH} threshold, TIMER is discharged by 5µA. In Figure 11b, when TIMER exceeds V_{TMRH}, GATE pulls down immediately and the chip shuts down. In Figure 11c, multiple momentary faults cause the TIMER capacitor to integrate and reach V_{TMRH} followed by GATE pull down and the chip shuts down. During chip shutdown, the LTC4253B latches TIMER high with a 5µA pull-up current source.

APPLICATIONS INFORMATION

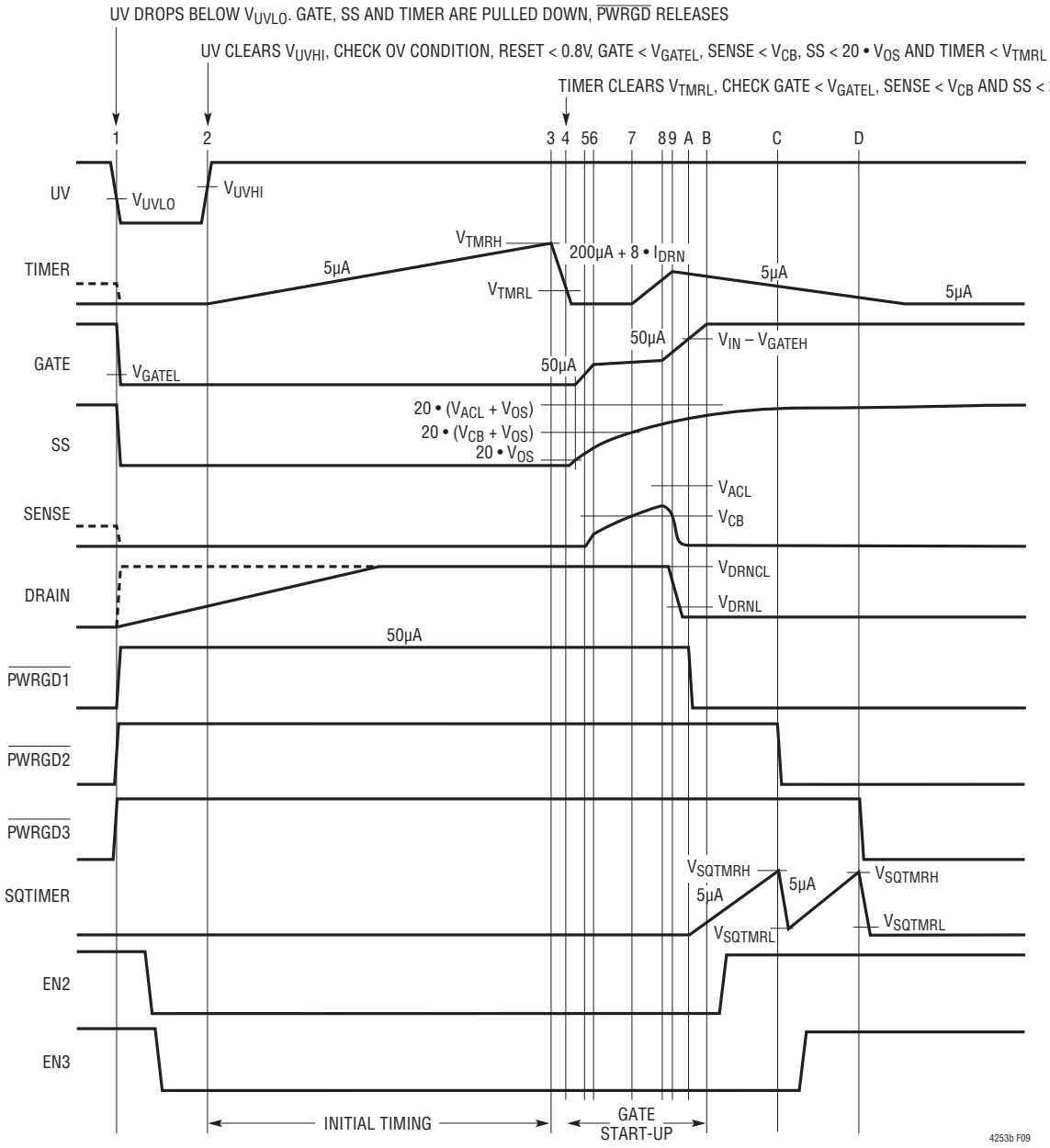


Figure 9. Undervoltage Timing (All Waveforms Are Referenced to V_{EE})

APPLICATIONS INFORMATION

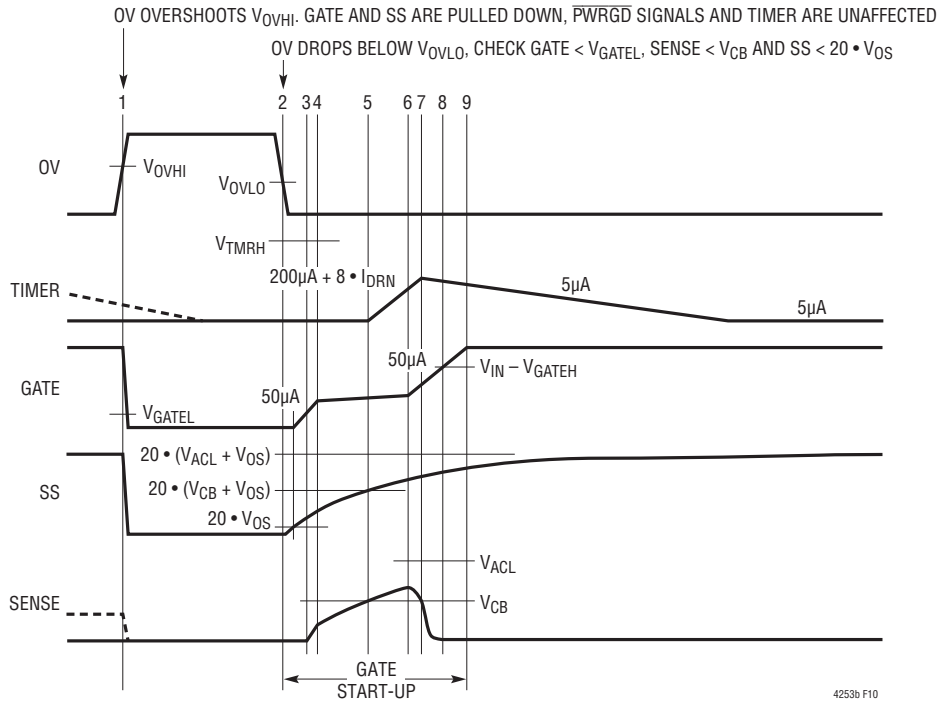
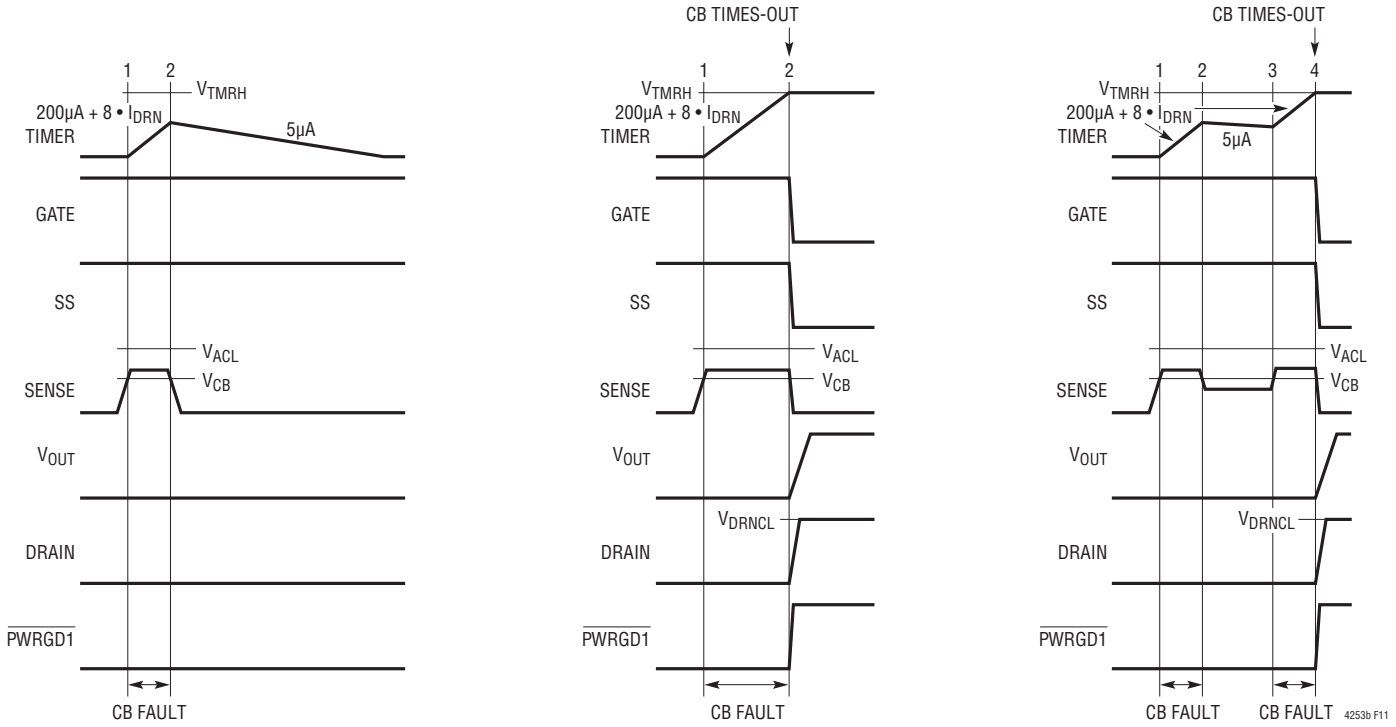


Figure 10. Overvoltage Timing (All Waveforms Are Referenced to V_{EE})



(11a) Momentary Circuit Breaker Fault

(11b) Circuit Breaker Time-Out

(11c) Multiple Circuit Breaker Fault

Figure 11. Circuit Breaker Timing Behavior (All Waveforms Are Referenced to V_{EE})

APPLICATIONS INFORMATION

Resetting a Fault Latch

A latched circuit breaker fault of the LTC4253B has the benefit of a long cooling time. The latched fault can be reset by pulsing the RESET pin high until the TIMER pin is pulled below V_{TMRL}(1V) as shown in Figure 12b. After the RESET pulse, SS and GATE ramp up without an initial timing cycle provided the interlock conditions are satisfied.

Alternative methods of reset include using an external switch to pulse the UV pin below V_{UVLO} or the V_{IN} pin below ($V_{LKO} – V_{LKH}$). Pulling the TIMER pin below V_{TMRL} and the SS pin to 0V then simultaneously releasing them also achieves a reset. An initial timing cycle is generated for reset by pulsing the UV pin or V_{IN} pin, while no initial timing cycle is generated for reset by pulsing of the TIMER and SS pins.

Using Reset as an ON/OFF Switch

The asynchronous RESET pin can be used as an ON/OFF function to cut off supply to the external power modules or loads controlled by the LTC4253B. Pulling RESET high will pull GATE, SS, TIMER and SQTIMER low and the $\overline{PWRGD}$ signal high. The supply is fully cut off if the RESET pulse is maintained wide enough to fully discharge the GATE and SS pins. As long as RESET is high, GATE, SS, TIMER and SQTIMER are strapped to V_{EE} and the supply is cut off. When RESET is released, if the LTC4253B are in UVLO, UV, OV or $V_{SENSE} > V_{CB}$, turn-on is delayed until the interlock conditions are met before recovering as described in the Operation, Interlock Conditions section. If not, the GATE pin will ramp up in a soft start cycle without going through an initial cycle as in Figure 12c.

Analog Current Limit and Fast Current Limit

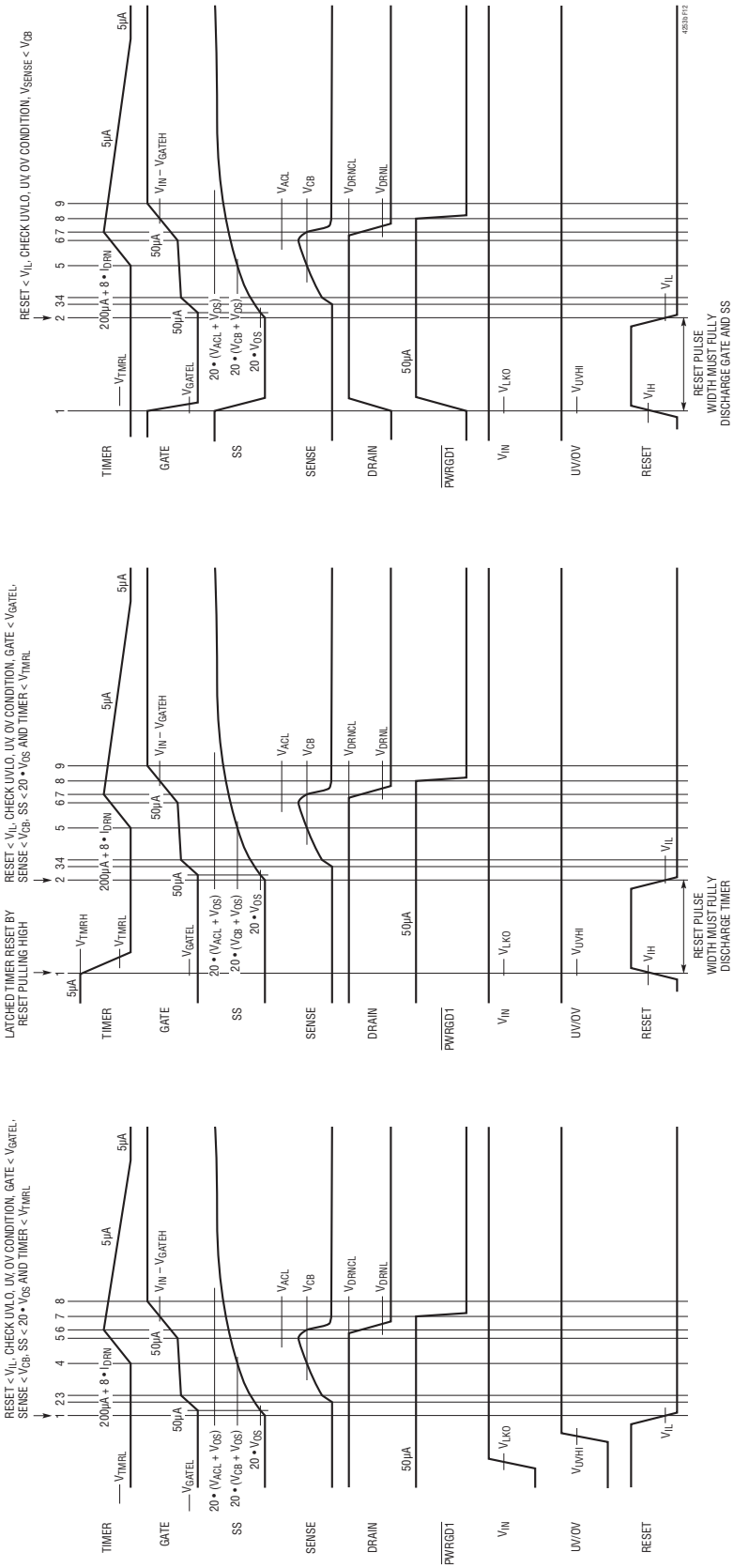
In Figure 13a, when SENSE exceeds V_{ACL}, GATE is regulated by the analog current limit amplifier loop. When SENSE drops below V_{ACL}, GATE is allowed to pull up. In Figure 13b, when a severe fault occurs, SENSE exceeds V_{FCL} and GATE immediately pulls down until the analog current amplifier establishes control. If the severe fault causes V_{OUT} to exceed V_{DRNCL}, the DRAIN pin is clamped at V_{DRNCL}. I_{DRN} flows into the DRAIN pin and is multiplied by 8. This extra current is added to the TIMER pull-up current of 200µA. This accelerated TIMER current of (200µA + 8 • I_{DRN}) produces a shorter circuit breaker fault delay. Careful selection of C_T, R_D and MOSFET helps prevent SOA damage in a low impedance fault condition.

Soft-Start

If the SS pin is not connected, this pin defaults to a linear voltage ramp, from 0V to 2.2V in about 300µs at GATE start-up, as shown in Figure 14a. If a soft-start capacitor, C_{SS}, is connected to this SS pin, the soft-start response is modified from a linear ramp to an RC response (Equation 6), as shown in Figure 14b. This feature allows load current to slowly ramp-up at GATE start-up. Soft-start is initiated at time point 3 by a TIMER transition from V_{TMRH} to V_{TMRL} (time points 1 and 2), by the OV pin falling below the V_{OVLO} threshold after an OV condition or by the RESET pin falling < 0.8V after a Reset condition. When the SS pin is below 0.2V, the analog current limit amplifier keeps GATE low. Above 0.2V, GATE is released and 50µA ramps up the compensation network and GATE capacitance at time point 4. Meanwhile, the SS pin voltage continues to ramp up. When GATE reaches the MOSFET's threshold, the MOSFET begins to conduct. Due to the MOSFET's high g_m, the MOSFET current quickly reaches the soft-start control value of V_{ACL}(t) (Equation 7). At time point 6, the GATE voltage is controlled by the current limit amplifier. The soft-start control voltage reaches the circuit breaker voltage, V_{CB} at time point 7 and the circuit breaker TIMER activates. As the load capacitor nears full charge, load current begins to decline below V_{ACL}(t). The current limit loop shuts off and GATE releases at time point 8. At time point 9, SENSE voltage falls below V_{CB} and TIMER deactivates.

Large values of C_{SS} can cause premature circuit breaker time-out as V_{ACL}(t) may marginally exceed the V_{CB} potential during the circuit breaker delay. The load capacitor is unable to achieve full charge in one GATE start-up cycle. A more serious side effect of a large C_{SS} value is that SOA duration may be exceeded during soft-start into a low impedance load. A soft-start voltage below V_{CB} will not activate the circuit breaker TIMER.

APPLICATIONS INFORMATION



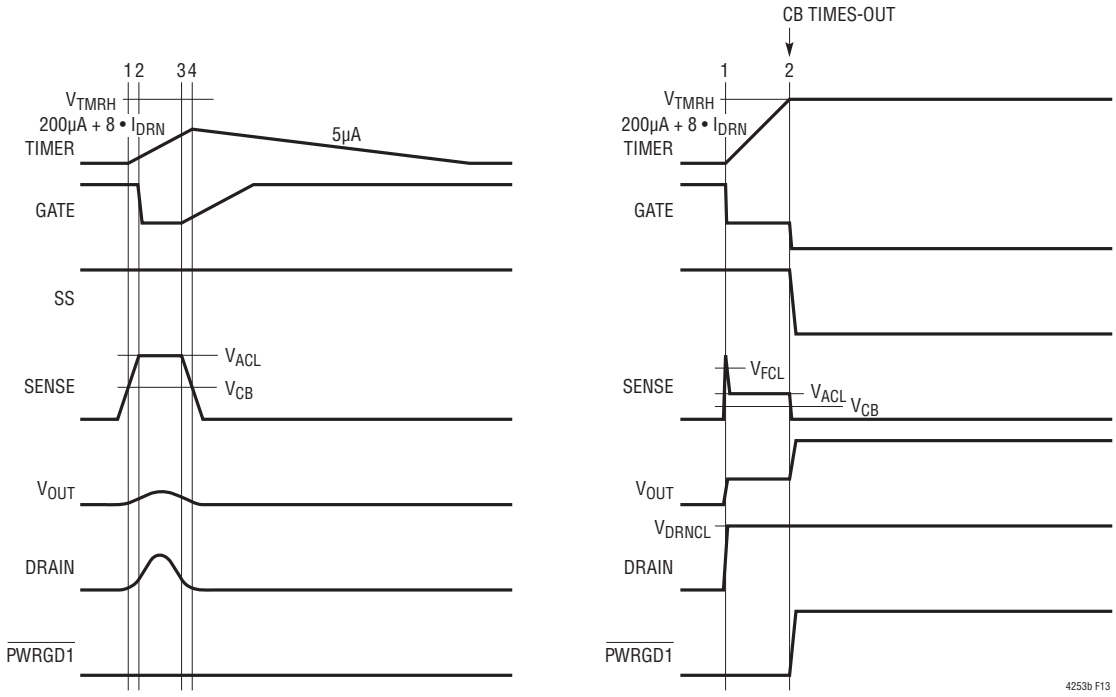
(12a) Reset Forcing Start-Up without Initial TIMER Cycle

(12b) Reset of the LTC4253B's Latched Fault

(12c) Reset as an ON/OFF Switch

Figure 12. Reset Functions (All Waveforms Are Referenced to V_{EE})

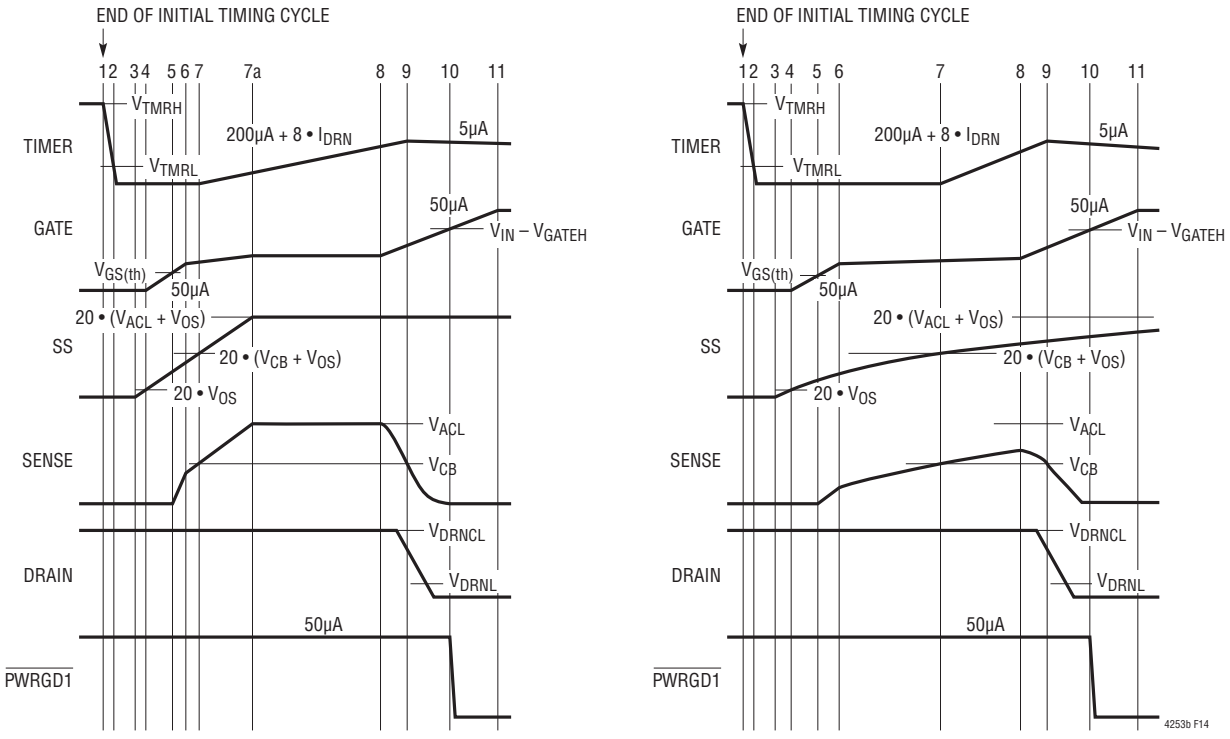
APPLICATIONS INFORMATION



(13a) Analog Current Limit Fault

(13b) Fast Current Limit Fault

Figure 13. Current Limit Behavior (All Waveforms Are Referenced to V_{EE})



(14a) Without External C_{SS}

(14b) With External C_{SS}

Figure 14. Soft-Start Timing (All Waveforms Are Referenced to V_{EE})

APPLICATIONS INFORMATION

Power Limit Circuit Breaker

Figure 15 shows the LTC4253B in a power limit circuit breaking application. The SENSE pin is modulated by board voltage V_{SUPPLY}. The D1 Zener voltage, V_Z, is set to be the same as the lowest operating voltage, $V_{SUPPLY(MIN)} = 43V$. If the goal is to have the high supply operating voltage, $V_{SUPPLY(MAX)} = 82V$ give the same power as available at $V_{SUPPLY(MIN)}$, then resistors R3 and R4 are selected by:

$$\frac{R4}{R3} = \frac{V_{CB}}{V_{SUPPLY(MAX)}} \quad (16)$$

If R4 is 22Ω, then R3 is 36.5k. The peak circuit breaker power limit is:

$$POWER(MAX) = \frac{\left(V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)}\right)^2}{4 \bullet V_{SUPPLY(MIN)} \bullet V_{SUPPLY(MAX)}} \quad (17)$$

$$\bullet POWER\ AT\ V_{SUPPLY(MIN)}$$

$$= 1.108V \bullet POWER\ AT\ V_{SUPPLY(MIN)}$$

when $V_{SUPPLY} = 0.5 \bullet (V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)})$
$= 62.5V$

The peak power at the fault current limit occurs at the supply overvoltage threshold. The fault current limited power is:

$$POWER(FAULT) = \frac{\left(V_{SUPPLY}\right)}{R_S} \bullet \left[V_{ACL} - (V_{SUPPLY} - V_Z) \bullet \frac{R4}{R3}\right] \quad (18)$$

Circuit Breaker with Foldback Current Limit

Figure 16 shows the LTC4253B in a foldback current limit application. When V_{OUT} is shorted to the –48V RTN supply, current flows through resistors R3 and R4. This results in a voltage drop across R4 and a corresponding reduction in voltage drop across the sense resistor, R_S, as the ACL amplifier servos the sense voltage between the SENSE and V_{EE} pins to about 100mV. The short-circuit current through RS reduces as the V_{OUT} voltage increases during an output short-circuit condition. Without foldback current limiting resistor R4, the current is limited to 5A during analog current limit. With R4, the short-circuit current is limited to 1.5A when V_{OUT} is shorted to 82V.

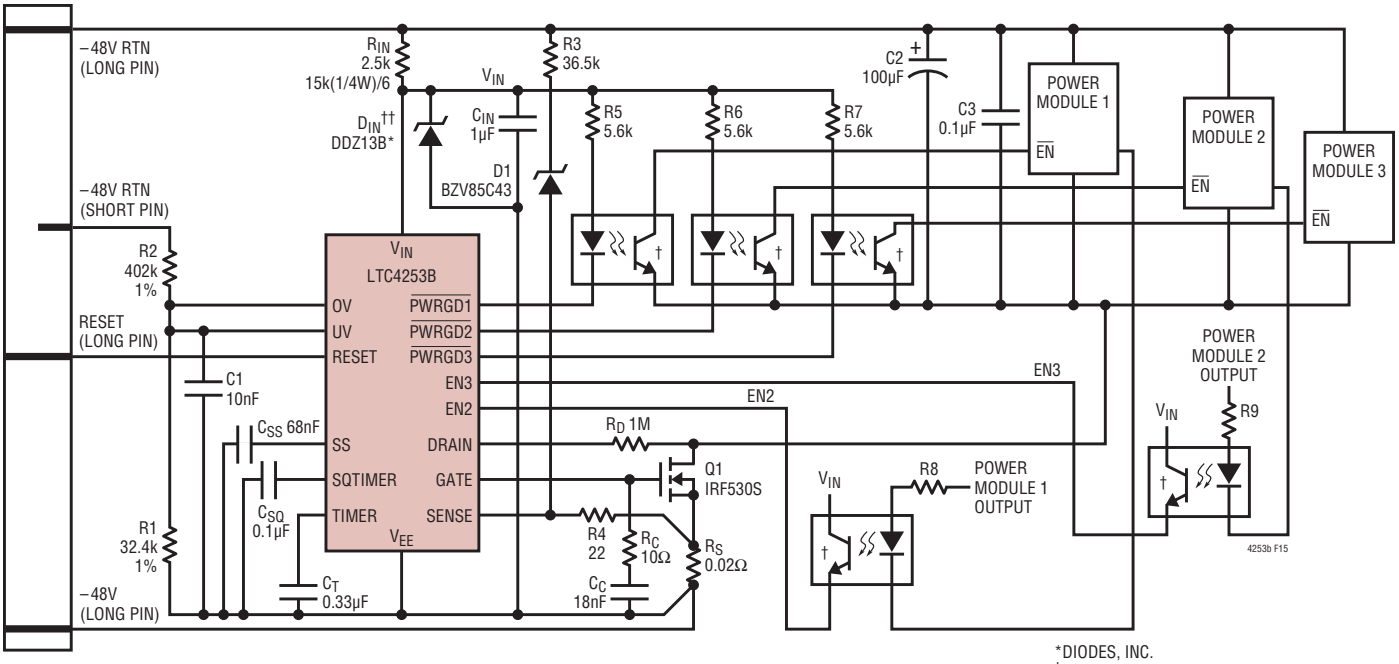
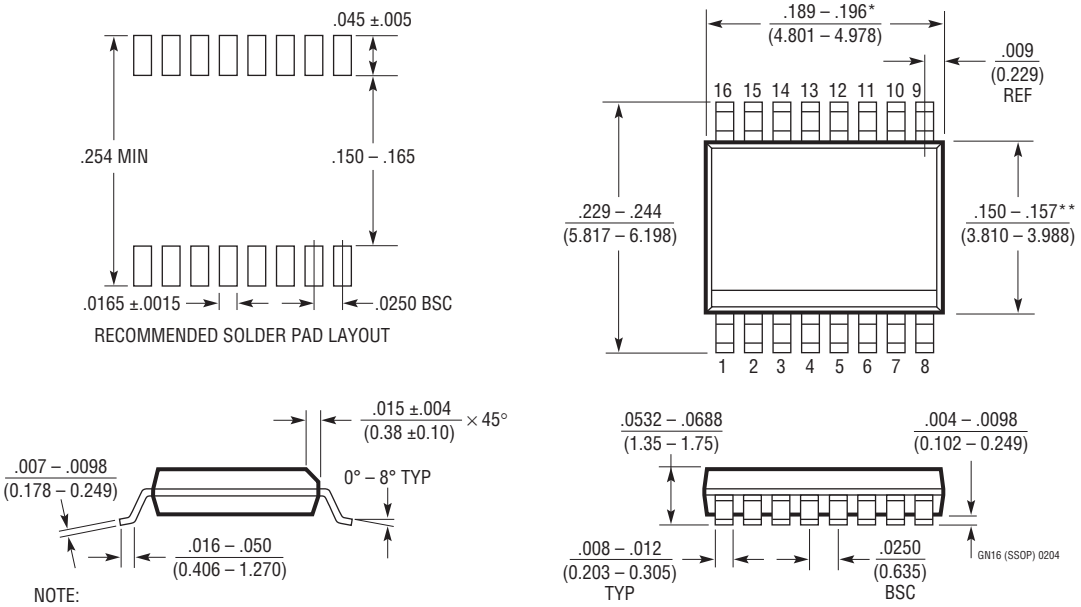


Figure 15. Power Limit Circuit Breaker Application

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

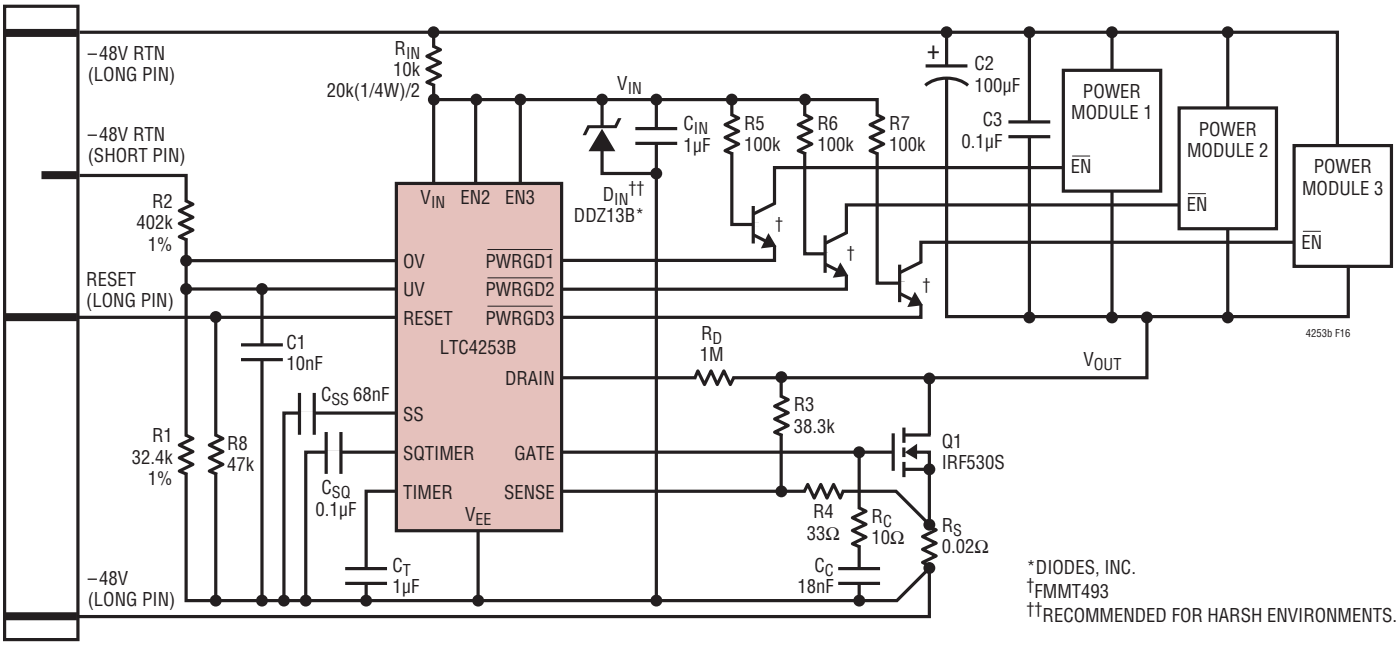


Figure 16. –48V/2.5A Application with Foldback Current Limiting and Transistor Enabled Sequencing without Feedback

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1640AH/LT1640AL	Negative High Voltage Hot Swap Controllers in SO-8	Negative High Voltage Supplies from –10V to –80V
LT1641-1/LT1641-2	Positive High Voltage Hot Swap Controllers in SO-8	Supplies from 9V to 80V, Auto-retry/Latched Off
LTC1642A	Fault Protected Hot Swap Controller	3V to 16.5V, Overvoltage Protection up to 33V
LT4250	–48V Hot Swap Controller	Active Current Limiting, Supplies from –20V to –80V
LTC4251B/LTC4251B-1/ LTC4251B-2	–48V Hot Swap Controllers in SOT-23	Fast Active Current Limiting, Supplies from –15V
LTC4252B-1/LTC4252B-2 LTC4252C-1/LTC4252C-2	–48V Hot Swap Controllers in MS8/MS10	Fast Active Current Limiting, Supplies from –15V, Drain Accelerated Response, 1% Accurate UV/OV Thresholds

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