74AXP1G57

Low-power configurable multiple function gate

Rev. 3 — 16 September 2015 — Product data sheet

1. General description

The 74AXP1G57 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer. All inputs can be connected directly to V_{CC} or GND.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.7 V to 2.75 V. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.7 V to 2.75 V
- Low input capacitance; C_I = 0.5 pF (typical)
- Low output capacitance; C_O = 1.0 pF (typical)
- Low dynamic power consumption; C_{PD} = 2.7 pF at V_{CC} = 1.2 V (typical)
- Low static power consumption; I_{CC} = 0.6 μA (85 °C maximum)
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-12A.01 (1.1 V to 1.3 V)
  - JESD8-11A.01 (1.4 V to 1.6 V)
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A.01 (2.3 V to 2.7 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM JESD22-C101E exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 2.75 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AXP1G57GM	–40 °C to +85 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AXP1G57GN	–40 °C to +85 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74AXP1G57GS	–40 °C to +85 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74AXP1G57GX	–40 °C to +85 °C	X2SON6	plastic thermal extremely thin small outline package; no leads; 6 terminals; body 1 × 0.8 × 0.35 mm	SOT1255

4. Marking

Table 2. Marking

Type number	Marking code[1]
74AXP1G57GM	RC
74AXP1G57GN	RC
74AXP1G57GS	RC
74AXP1G57GX	RC

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

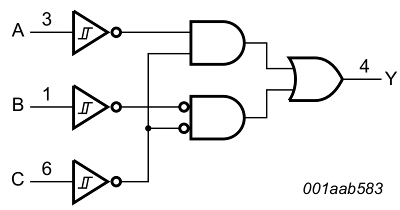
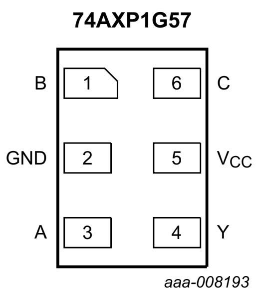


Fig 1. Logic symbol

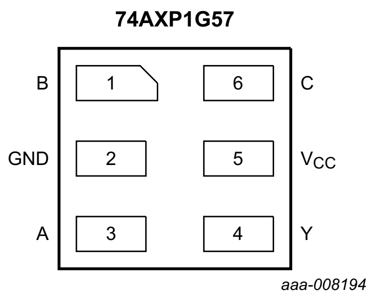
6. Pinning information

6.1 Pinning



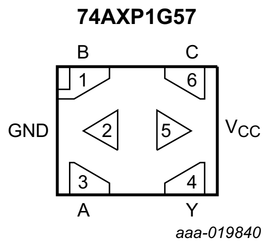
Transparent top view

Fig 2. Pin configuration SOT886



Transparent top view

Fig 3. Pin configuration SOT1115 and SOT1202



Transparent top view

Fig 4. Pin configuration SOT1255 (X2SON6)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V_{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table[1]

Input			Output
C	**B**	**A**	**Y**
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7.1 Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input AND	see Figure 5
2-input AND with both inputs inverted	see Figure 8
2-input NAND with inverted input	see Figure 6 and Figure 7
2-input OR with inverted input	see Figure 6 and Figure 7
2-input NOR	see Figure 8
2-input NOR with both inputs inverted	see Figure 5
2-input XNOR	see Figure 9
Inverter	see Figure 10
Buffer	see Figure 11

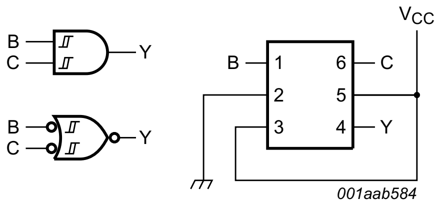


Fig 5. 2-input AND gate or 2-input NOR gate with both inputs inverted

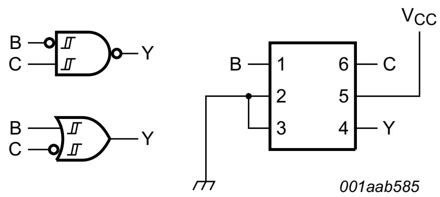


Fig 6. 2-input NAND gate with input B inverted or 2-input OR gate with inverted C input

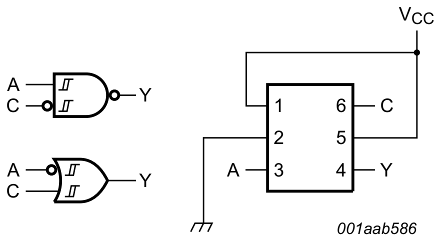


Fig 7. 2-input NAND gate with input C inverted or 2-input OR gate with inverted A input

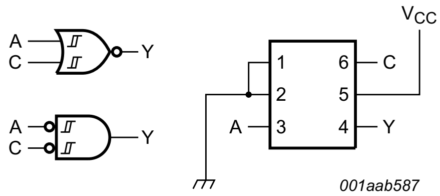


Fig 8. 2-input NOR gate or 2-input AND gate with both inputs inverted

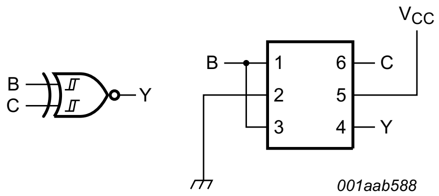


Fig 9. 2-input XNOR gate

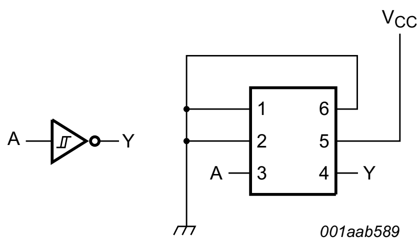


Fig 10. Inverter

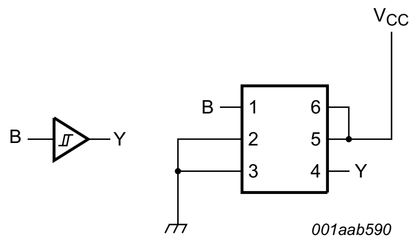


Fig 11. Buffer

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	3.3	V
I_{IK}	input clamping current	$V_I < 0$ V	–50	-	mA
V_I	input voltage	[1]	–0.5	3.3	V
I_{OK}	output clamping current	$V_O < 0$ V	–50	-	mA
V_O	output voltage	[1]	–0.5	3.3	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		–50	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.7	2.75	V
V_I	input voltage		0	2.75	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	2.75	V
T_{amb}	ambient temperature		–40	+85	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions, unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C				Unit
			Min	Typ 25 °C	Max 25 °C	Max 85 °C	
V_{T+}	positive-going threshold voltage	see Figure 12 and Figure 13					
		V_{CC} = 0.75 V to 0.85 V	$0.3V_{CC}$	-	$0.8V_{CC}$	$0.8V_{CC}$	V
		V_{CC} = 1.1 V to 1.95 V	$0.4V_{CC}$	-	$0.7V_{CC}$	$0.7V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	0.9	-	1.7	1.7	V
V_{T-}	negative-going threshold voltage	see Figure 12 and Figure 13					
		V_{CC} = 0.75 V to 0.85 V	$0.2V_{CC}$	-	$0.7V_{CC}$	$0.7V_{CC}$	V
		V_{CC} = 1.1 V to 1.95 V	$0.3V_{CC}$	-	$0.6V_{CC}$	$0.6V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	0.7	-	1.5	1.5	V
V_H	hysteresis voltage	see Figure 12 and Figure 13					
		V_{CC} = 0.75 V to 0.85 V	$0.06V_{CC}$	-	$0.5V_{CC}$	$0.5V_{CC}$	V
		V_{CC} = 1.1 V to 1.95 V	$0.1V_{CC}$	-	$0.4V_{CC}$	$0.4V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	0.2	-	1.0	1.0	V
V_{OH}	HIGH-level output voltage	I_O = –20 μA; V_{CC} = 0.7 V	-	0.69	-	-	V
		I_O = –100 μA; V_{CC} = 0.75 V	0.65	-	-	-	V
		I_O = –2 mA; V_{CC} = 1.1 V	0.825	-	-	-	V
		I_O = –3 mA; V_{CC} = 1.4 V	1.05	-	-	-	V
		I_O = –4.5 mA; V_{CC} = 1.65 V	1.2	-	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.7	-	-	-	V
V_{OL}	LOW-level output voltage	I_O = 20 μA; V_{CC} = 0.7 V	-	0.01	-	-	V
		I_O = 100 μA; V_{CC} = 0.75 V	-	-	0.1	0.1	V
		I_O = 2 mA; V_{CC} = 1.1 V	-	-	0.275	0.275	V
		I_O = 3 mA; V_{CC} = 1.4 V	-	-	0.35	0.35	V
		I_O = 4.5 mA; V_{CC} = 1.65 V	-	-	0.45	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.7	0.7	V
I_I	input leakage current	V_I = 0 V to 2.75 V; V_{CC} = 0 V to 2.75 V [1]	-	0.001	±0.1	±0.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 2.75 V; V_{CC} = 0 V [1]	-	0.01	±0.1	±0.5	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V or 2.75 V; V_{CC} = 0 V to 0.1 V [1]	-	0.02	±0.1	±0.5	μA
I_{CC}	supply current	V_I = 0 V or V_{CC}; I_O = 0 A [1]	-	0.01	0.3	0.6	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} – 0.5 V; I_O = 0 A; V_{CC} = 2.5 V	-	2	100	150	μA

[1] All typical values are measured at V_{CC} = 1.2 V.

10.1 Waveform transfer characteristics

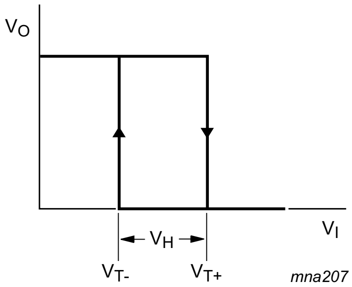


Fig 12. Transfer characteristic

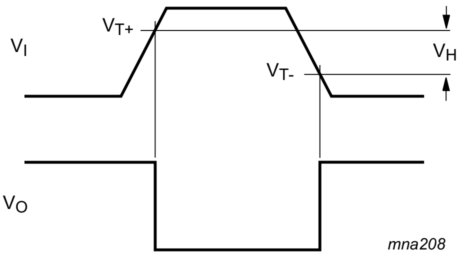


Fig 13. Definition of V_{T+}, V_{T-}, and V_H

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 20.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	A, B and C to Y; see Figure 14 [2][3]						
		V_{CC} = 0.75 V to 0.85 V	3.5	13	50	2.9	125	ns
		V_{CC} = 1.1 V to 1.3 V	1.8	5.0	8.4	1.6	8.4	ns
		V_{CC} = 1.4 V to 1.6 V	1.6	3.8	5.4	1.4	5.8	ns
		V_{CC} = 1.65 V to 1.95 V	1.3	3.2	4.4	1.2	4.8	ns
		V_{CC} = 2.3 V to 2.7 V	0.9	2.6	3.4	0.8	3.7	ns
t_t	transition time	V_{CC} = 2.7 V; see Figure 14 [4]	-	-	-	1.0	-	ns
C_I	input capacitance	V_I = 0 V or V_{CC}; V_{CC} = 0 V to 2.75 V	-	0.5	-	-	-	pF
C_O	output capacitance	V_O = 0 V; V_{CC} = 0 V	-	1.0	-	-	-	pF

Table 9. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 20.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = 0 V to V_{CC} [5]						
		V_{CC} = 0.75 V to 0.85 V	-	2.6	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	2.7	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	2.8	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	2.9	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	3.3	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] For additional propagation delay values at different load capacitances see Figure 15 to Figure 19.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + C_L \times V_{CC}^2 \times f_o$ where:

f_i = input frequency in MHz;

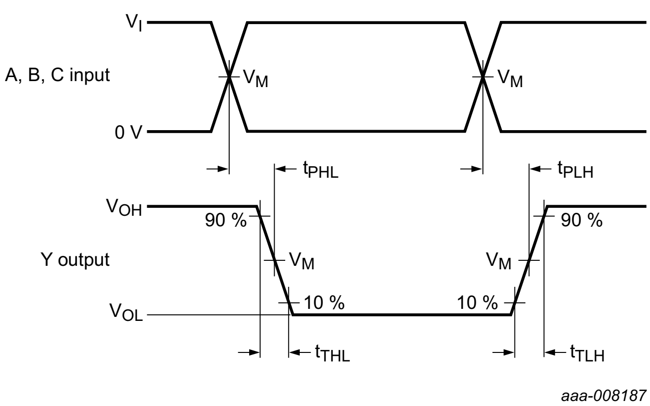
f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching.

11.1 Waveforms and graphs



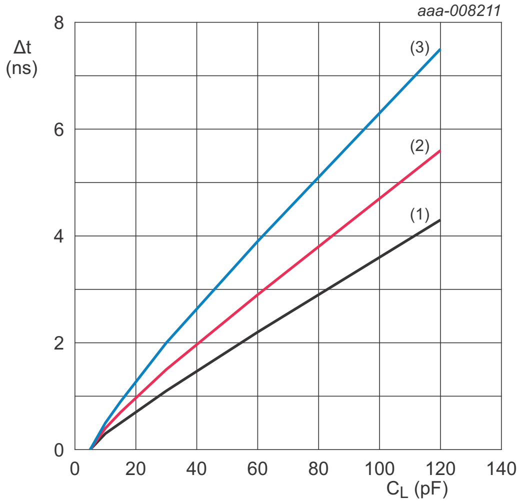
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. Input A, B and C to output Y propagation delay times and output transition times

Table 10. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.75 V to 2.7 V	0.5V_{CC}	0.5V_{CC}	V_{CC}	≤ 3.0 ns



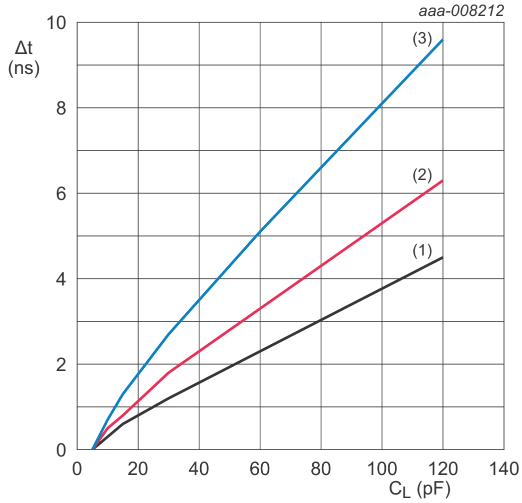
T_{amb} = –40 °C to +85 °C unless otherwise specified.

(1) Minimum: V_{CC} = 2.7 V

(2) Typical: T_{amb} = 25 °C; V_{CC} = 2.5 V

(3) Maximum: V_{CC} = 2.3 V

Fig 15. Additional t_{pd} versus load capacitance



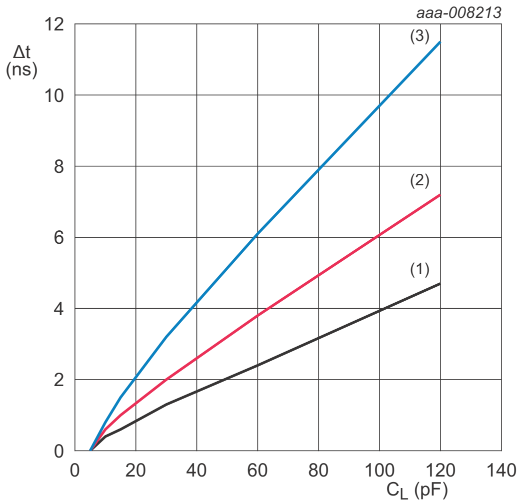
T_{amb} = –40 °C to +85 °C unless otherwise specified.

(1) Minimum: V_{CC} = 1.95 V

(2) Typical: T_{amb} = 25 °C; V_{CC} = 1.8 V

(3) Maximum: V_{CC} = 1.65 V

Fig 16. Additional t_{pd} versus load capacitance



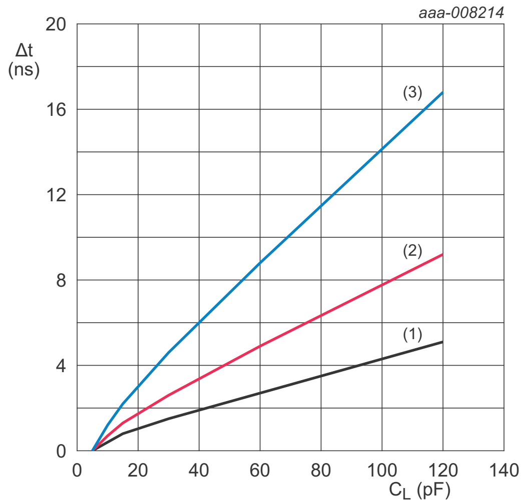
T_{amb} = –40 °C to +85 °C unless otherwise specified.

(1) Minimum: V_{CC} = 1.6 V

(2) Typical: T_{amb} = 25 °C; V_{CC} = 1.5 V

(3) Maximum: V_{CC} = 1.4 V

Fig 17. Additional t_{pd} versus load capacitance



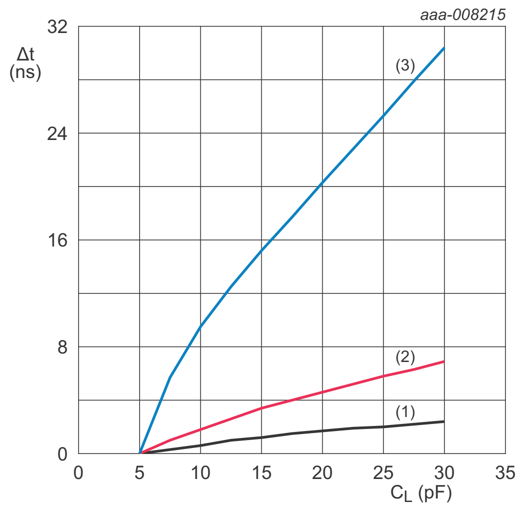
T_{amb} = –40 °C to +85 °C unless otherwise specified.

(1) Minimum: V_{CC} = 1.3 V

(2) Typical: T_{amb} = 25 °C; V_{CC} = 1.2 V

(3) Maximum: V_{CC} = 1.1 V

Fig 18. Additional t_{pd} versus load capacitance



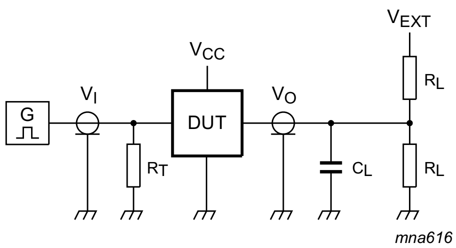
T_{amb} = −40 °C to +85 °C unless otherwise specified.

(1) Minimum: V_{CC} = 0.85 V

(2) Typical: T_{amb} = 25 °C; V_{CC} = 0.8 V

(3) Maximum: V_{CC} = 0.75 V

Fig 19. Additional t_{pd} versus load capacitance



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

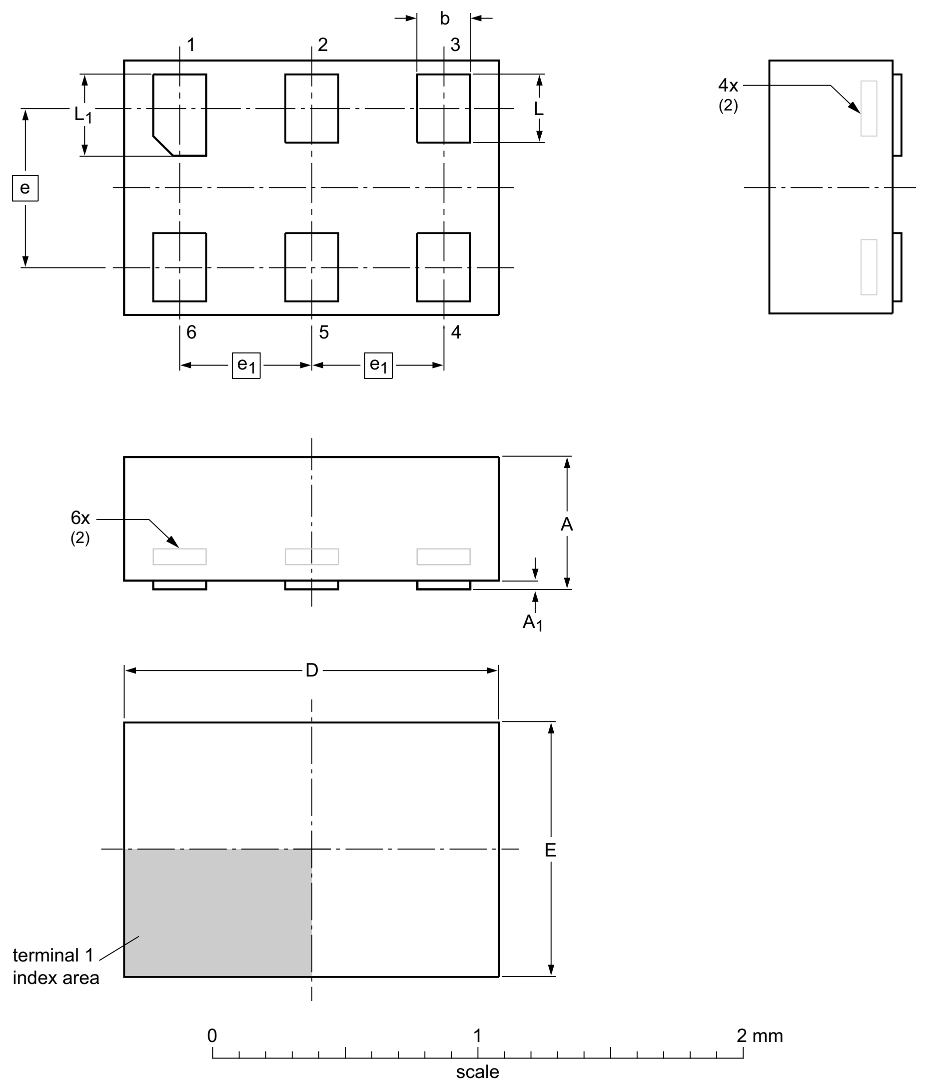
Fig 20. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.75 V to 2.7 V	5 pF	10 kΩ	0 V	0 V	2 × V_{CC}

12. Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

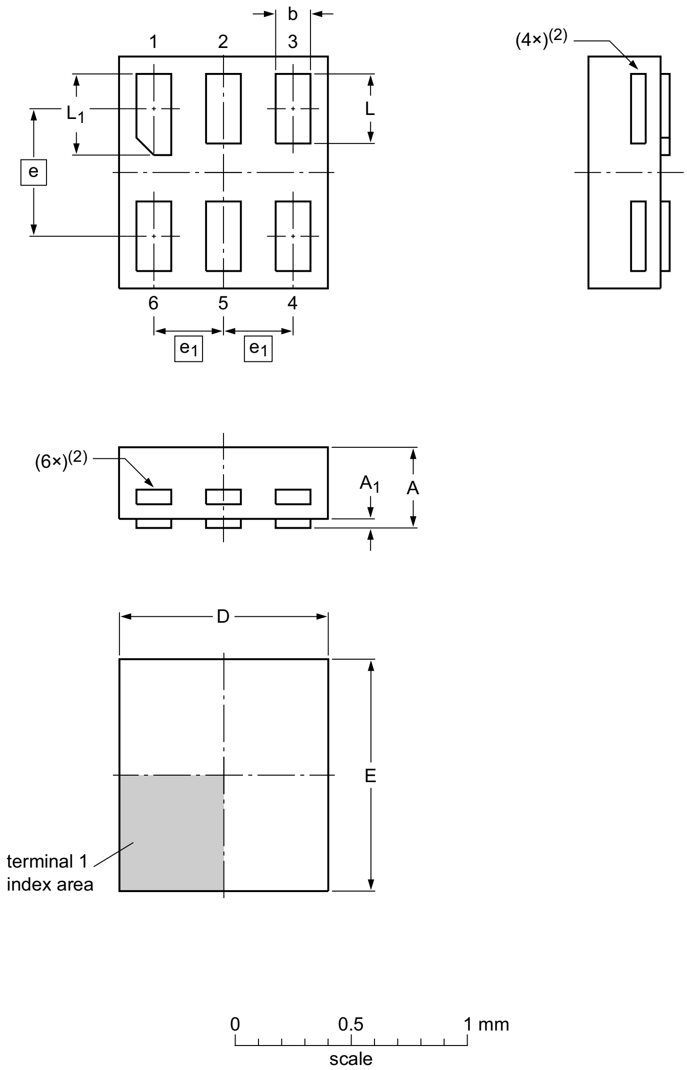
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig 21. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		A(1)	A1	b	D	E	e	e1	L	L1
mm	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

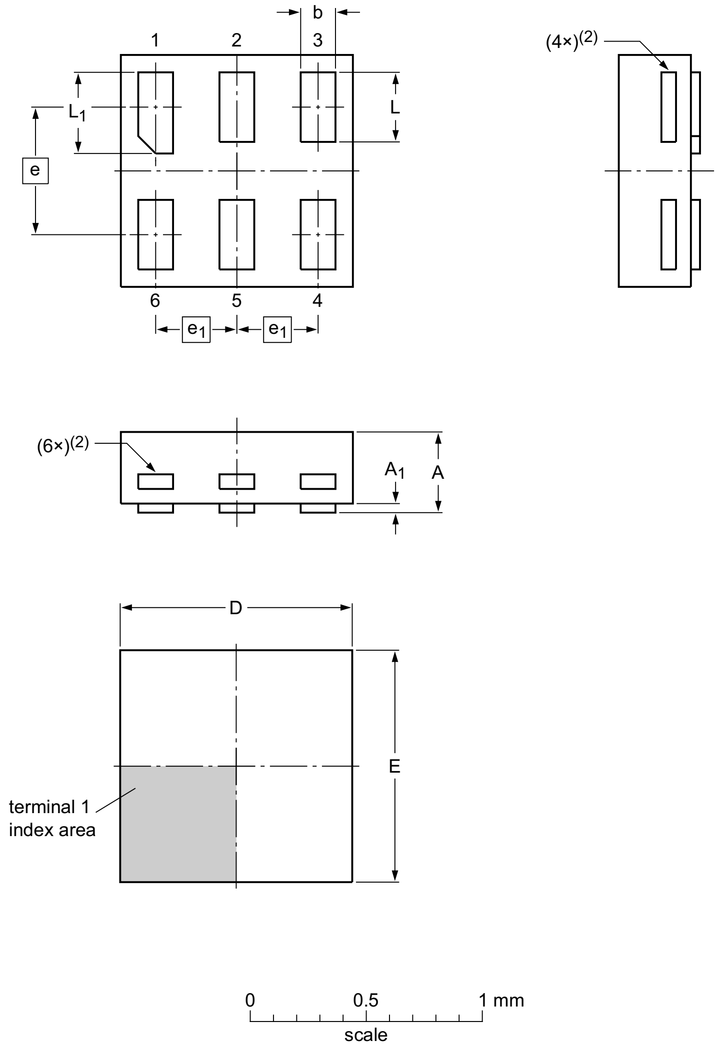
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						~~10-04-02~~ 10-04-07

Fig 22. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
mm	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

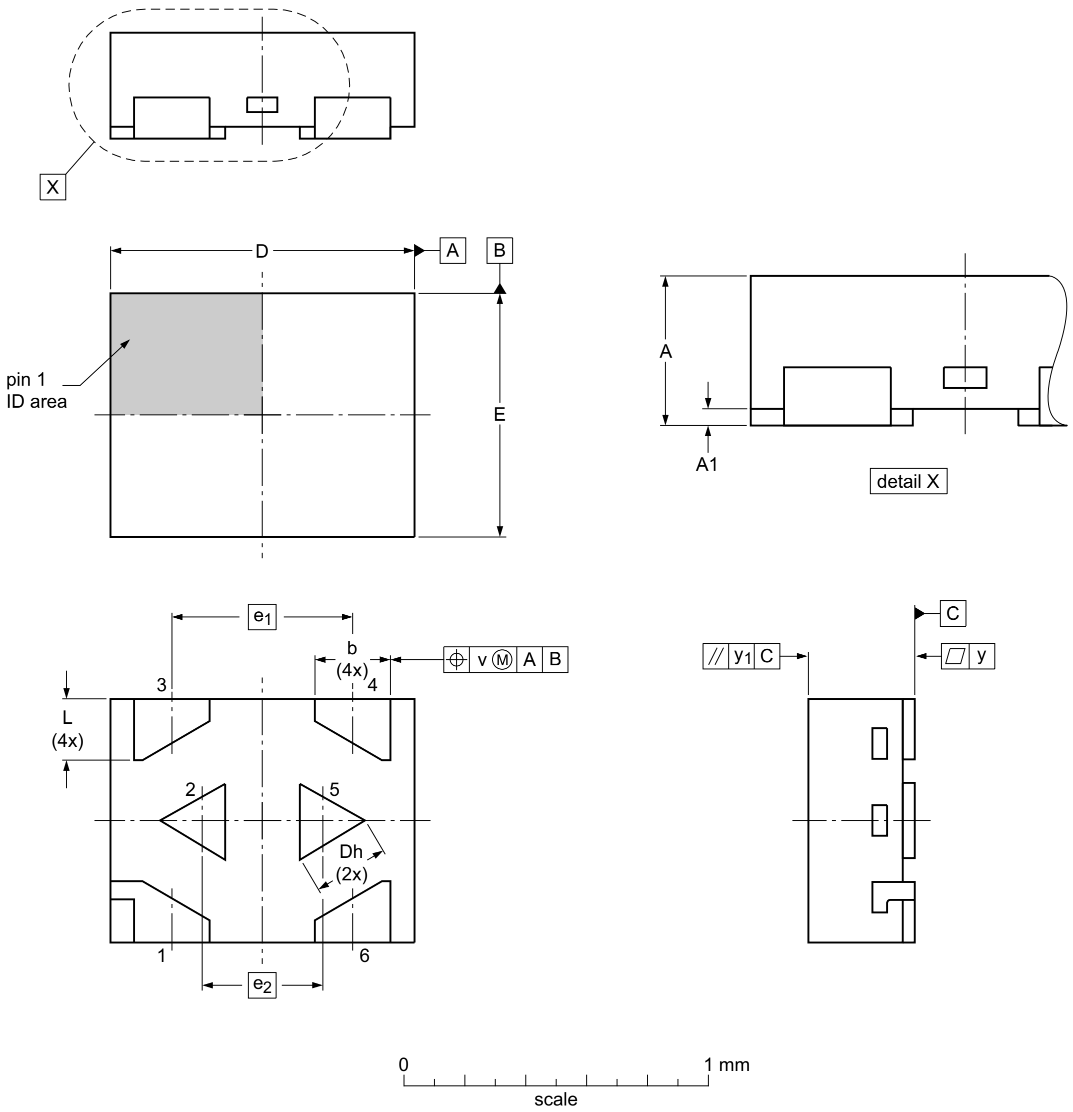
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig 23. Package outline SOT1202 (XSON6)

X2SON6: plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 x 0.8 x 0.35 mm **SOT1255**



Dimensions (mm are the original dimensions)

Unit		A	A_1	D	D_h	E	e_1	e_2	b	L	v	y	y_1
	max	0.35	0.04	1.05	0.30	0.85			0.30	0.25			
mm	nom	0.32	0.02	1.00	0.25	0.80	0.60	0.40	0.25	0.20	0.10	0.05	0.05
	min	0.30	0.00	0.95	0.22	0.75			0.22	0.17			

sot1255_po

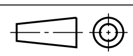
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1255						~~15-07-20~~ 15-07-22

Fig 24. Package outline SOT1255 (X2SON6)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AXP1G57 v.3	20150916	Product data sheet	-	74AXP1G57 v.2
Modifications:	• Added type number 74AXP1G57GX (SOT1255/X2SON6).			
74AXP1G57 v.2	20131212	Product data sheet	-	74AXP1G57 v.1
Modifications:	• Specification status changed to product data sheet.			
74AXP1G57 v.1	20130625	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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17. Contents

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