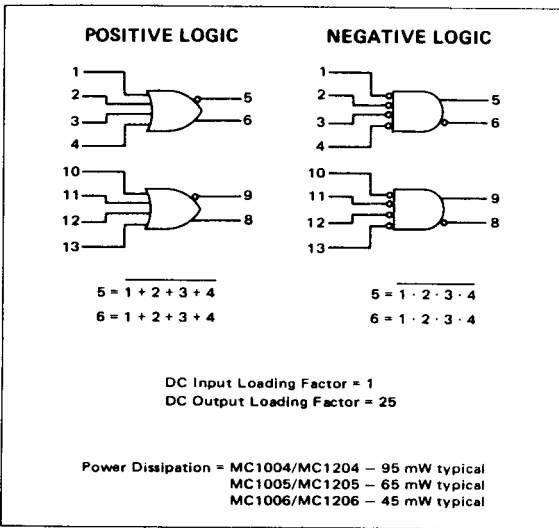


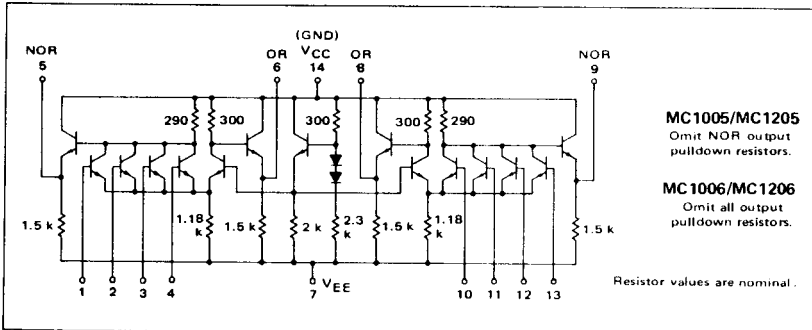
MC1004 thru MC1006
MC1204 thru MC1206

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



MC1004/MC1204 CIRCUIT SCHEMATIC

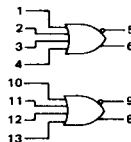


130

MC1004 thru MC1006, MC1204 thru MC1206 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 kΩ resistor to V_{EE}.



Characteristic	Symbol	Pin Under Test	MC1204-1206 Test Limits						MC1004-1006 Test Limits									
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Power Supply Drain Current MC1204, MC1004 MC1205, MC1005 MC1206, MC1006	I _E	7	-	-	-	26	-	-	mA _{dc}	-	-	-	26	-	-	mA _{dc}		
Input Current	I _{in}	1 2 3 4	-	-	-	100	-	-	μA _{dc}	-	-	-	100	-	-	μA _{dc}		
Input Leakage Current	I _R	Inputs*	-	-	-	0.2	-	1.0	μA _{dc}	-	-	-	0.2	-	1.0	μA _{dc}		
"NOR" Logical "1" Output Voltage	V _{OH1}	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	V _{dc}	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	V _{dc}		
"NOR" Logical "0" Output Voltage	V _{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.360	V _{dc}	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	V _{dc}		
"OR" Logical "1" Output Voltage	V _{OH1}	6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	V _{dc}	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	V _{dc}		
"OR" Logical "0" Output Voltage	V _{OL}	6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.360	V _{dc}	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	V _{dc}		
Switching Times Propagation Delay (Fan-Out = 3)	t ₁₋₅₋ t ₁₋₅₊ t ₁₋₆₊ t ₁₋₆₋	5 5 6 6	Typ	Max	Typ	Max	Typ	Max	ns	Typ	Max	Typ	Max	Typ	Max	ns		
			5	5.0	7.0	5.0	7.0	6.5		9.0	5.0	7.0	5.0	7.0	6.0		8.0	
			5	4.0	7.5	4.0	7.5	5.5		9.0	4.0	7.5	4.0	7.5	5.0		8.5	
			6	4.0	7.5	4.0	7.0	5.5		8.5	4.0	7.0	4.0	7.0	5.0		8.0	
			6	4.0	7.0	4.0	7.0	5.5		9.0	4.0	7.0	4.0	7.0	5.0		8.0	
			5	14	-	14	-	18		-	14	-	14	-	16		-	
	(Fan-Out = 15)	t ₁₋₅₊ t ₁₋₅₋ t ₁₋₆₊ t ₁₋₆₋	5 5 6 6	Typ	Max	Typ	Max	Typ	Max	ns	Typ	Max	Typ	Max	Typ	Max	ns	
				5	5.0	-	5.0	-	7.0		-	5.0	-	5.0	-	6.0		-
				6	6.0	-	6.0	-	8.0		-	6.0	-	6.0	-	7.0		-
				6	13	-	13	-	17		-	13	-	13	-	15		-
				5	5.0	7.5	5.0	7.5	6.0		9.0	5.0	7.5	5.0	7.5	5.0		8.0
				6	4.0	7.0	4.0	6.5	5.5		8.0	4.0	6.5	4.0	6.5	5.0		7.0
Rise Time (Fan-Out = 3)	t ₅₊ t ₆₊	5 6	Typ	Max	Typ	Max	Typ	Max	ns	Typ	Max	Typ	Max	Typ	Max	ns		
			5	5.0	7.5	5.0	7.5	6.0		9.0	5.0	7.5	5.0	7.5	5.0		8.0	
Fall Time (Fan-Out = 3)	t ₅₋ t ₆₋	5 6	Typ	Max	Typ	Max	Typ	Max	ns	Typ	Max	Typ	Max	Typ	Max	ns		
			5	5.0	8.5	5.0	8.0	6.0		10	5.0	8.0	5.0	8.0	5.5		9.0	
			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max			
			5	5.0	8.0	5.0	8.0	7.0	10	5.0	8.0	5.0	8.0	6.0	9.0			

* Individually test each input using the pin connections shown. † V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

131

@Test
 Temperature
 -55°C
 +25°C
 +125°C
 0°C
 +25°C
 +75°C

MC1204-1206
 MC1004-1006

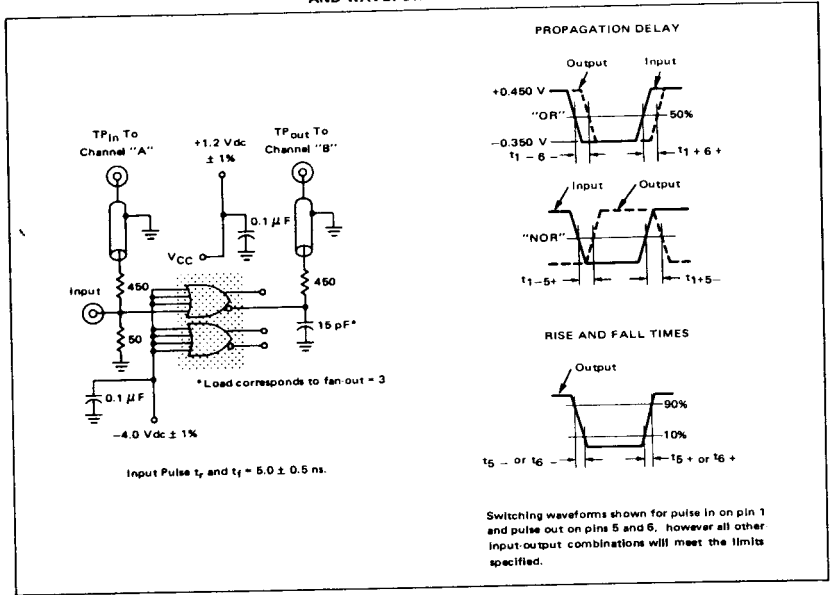
		TEST VOLTAGE/CURRENT VALUES					
		Vdc ± 1.0%					mAdc
		V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	
		-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5	
		-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
		-5.2 to -1.205	-0.875 to -0.550	-	-5.2	-2.5	
		-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5	
		-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
		-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5	

		TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					V _{CC} (Gnd)
Characteristic	Symbol	Pin Under Test	V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L
Power Supply Drain Current MC1204 MC1004 MC1205 MC1005 MC1206 MC1006	I _E	7 ↓	-	-	-	1 2 3 4 7 10 11 12 13	14 ↓
Input Current	I _{in}	1 2 3 4	-	-	1 2 3 4	2 3 4 7 10 11 12 13	14 ↓
Input Leakage Current	I _R	Inputs*	-	-	-	1 2 3 4 7 10 11 12 13	14 ↓
NOR* Logical "1" Output Voltage	V _{OH†}	5 ↓	1 2 3 4	-	-	2 3 4 7 10 11 12 13	14 ↓
NOR* Logical "0" Output Voltage	V _{OL}	5 ↓	-	1 2 3 4	-	2 3 4 7 10 11 12 13	14 ↓
OR* Logical "1" Output Voltage	V _{OH†}	6 ↓	-	1 2 3 4	-	2 3 4 7 10 11 12 13	14 ↓
OR* Logical "0" Output Voltage	V _{OL}	6 ↓	1 2 3 4	-	-	2 3 4 7 10 11 12 13	14 ↓
Switching Times Propagation Delay (Fan-Out = 3)			Pulse In	Pulse Out		V _{EE} = -4.0 Vdc	(+1.2 V)
	t ₁₊₅₋	5	1	5		2 3 4 7 10 11 12 13	14
	t ₁₋₅₊	5	↓	5			
	t ₁₊₆₋	6	↓	6			
	t ₁₋₆₊	6	↓	6			
(Fan-Out = 15)	t ₁₊₅₋	5	↓	5			
	t ₁₋₅₊	5	↓	5			
	t ₁₊₆₋	6	↓	6			
	t ₁₋₆₊	6	↓	6			
Rise Time (Fan-Out = 3)	t ₅₋	5	↓	5			
	t ₆₋	6	↓	6			
Fall Time (Fan-Out = 3)	t ₅₊	5	↓	5			
	t ₆₊	6	↓	6			

132

MC1004 thru MC1006, MC1204 thru MC1206 (continued)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

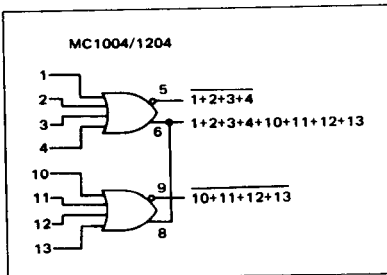


APPLICATIONS INFORMATION

The MC1004-1006/MC1204-1206 dual 4-input OR/NOR gates are very useful in generating system logic due to their flexibility. By employing negative logic on the inputs (low level of -1.6 V is considered true), the AND/NAND logic function is obtained from the basic gate. Since complementary inputs are available in MECL system, OR/NOR-AND/NAND logic may be employed, reducing the package count

in the system. An 8-input OR or AND gate is obtained by tying the OR outputs together and using positive or negative logic. The dual 4-input gate is also useful for driving two twisted pair lines where the lines must carry independent information. For a further discussion of twisted pair driving and receiving, refer to MC1020/MC1220 Line Receiver.

8-INPUT "OR" GATE (positive logic) or 8-INPUT "AND" GATE (negative logic)



DUAL 4-INPUT GATE USED TO DRIVE TWO BALANCED TWISTED PAIR LINES

