

# CD4000B, CD4001B, CD4002B, CD4025B Types

## COS/MOS NOR Gates

### Features:

- Propagation delay time = 60 ns (typ.) at  $C_L = 50 \text{ pF}$ ,  $V_{DD} = 10 \text{ V}$
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package-temperature range;  $100 \text{ nA}$  at 18 V and  $25^\circ\text{C}$
- Noise margin (over full package temperature range):

1 V at  $V_{DD} = 5 \text{ V}$   
 2 V at  $V_{DD} = 10 \text{ V}$   
 2.5 V at  $V_{DD} = 15 \text{ V}$

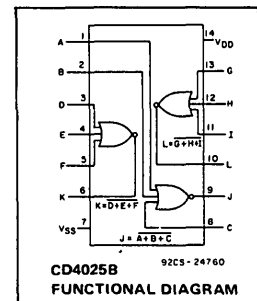
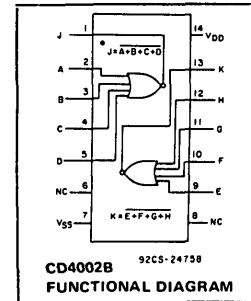
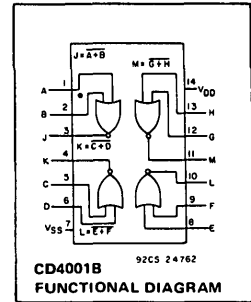
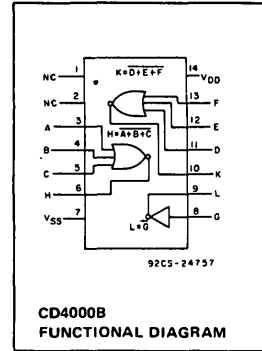
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"

High-Voltage Types (20-Volt Rating)

Dual 3 Input  
 plus Inverter – CD4000B  
 Quad 2 Input – CD4001B  
 Dual 4 Input – CD4002B  
 Triple 3 Input – CD4025B

RCA-CD4000B, CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

The CD4000B, CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ( $^\circ\text{C}$ )							UNITS
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	Values at $-55, +25, +125$ Apply to D,F,H Packages				Values at $-40, +25, +85$ Apply to E Package			
				$-55$	$-40$	$+85$	$+125$	$+25$			
								Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD}$ Max	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	$\mu\text{A}$
	-	0.10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0.15	15	1	1	30	30	-	0.01	1	
	-	0.20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current $I_{OL}$ Min	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	$\text{mA}$
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, $I_{OH}$ Min	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	$\text{mA}$
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage Low-Level, $V_{OL}$ Max	-	0.5	5	0.05			-	0	0.05	-	V
	-	0.10	10	0.05			-	0	0.05	-	
	-	0.15	15	0.05			-	0	0.05	-	
Output Voltage High-Level, $V_{OH}$ Min	-	0.5	5	4.95			4.95	5	-	-	V
	-	0.10	10	9.95			9.95	10	-	-	
	-	0.15	15	14.95			14.95	15	-	-	
Input Low Voltage, $V_{IL}$ Max	0.5, 4.5	-	5	1.5			-	-	1.5	-	V
	1.9	-	10	3			-	-	3	-	
	1.5, 13.5	-	15	4			-	-	4	-	
Input High Voltage, $V_{IH}$ Min	0.5	-	5	3.5			3.5	-	-	-	V
	1	-	10	7			7	-	-	-	
	1.5	-	15	11			11	-	-	-	
Input Current $I_{IN}$ Max		0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu\text{A}$

# CD4000B, CD4001B, CD4002B, CD4025B Types

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ = Full Package Temperature Range)	3	18	V

## MAXIMUM RATINGS, Absolute-Maximum Values

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ ) (Voltages referenced to $V_{SS}$ Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD}$ + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10$ mA
POWER DISSIPATION PER PACKAGE ( $P_D$ )	500 mW
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A$ = FULL PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ) PACKAGE TYPES D, F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79 mm) from case for 10 s max	$+265^\circ\text{C}$

## DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20$  ns,  $C_L = 50$  pF,  $R_L = 200$  k $\Omega$

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS	
		$V_{DD}$ VOLTS	TYP.		MAX.
Propagation Delay Time, $t_{PHL}, t_{PLH}$		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, $t_{THL}, t_{TLH}$		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, $C_{IN}$	Any Input	5	7.5	pF	

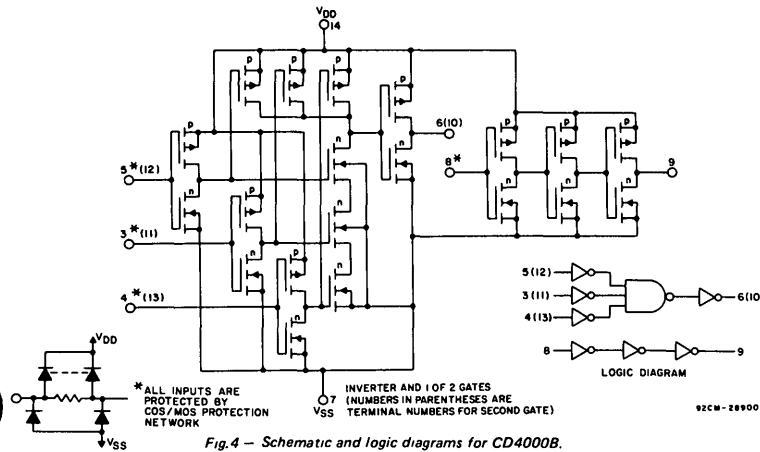


Fig. 4 - Schematic and logic diagrams for CD4000B.

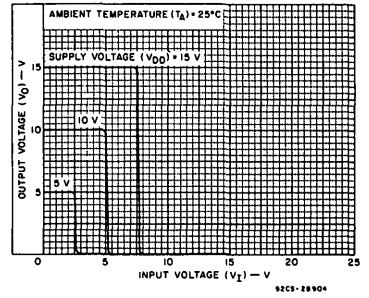


Fig. 1 - Typical voltage transfer characteristics.

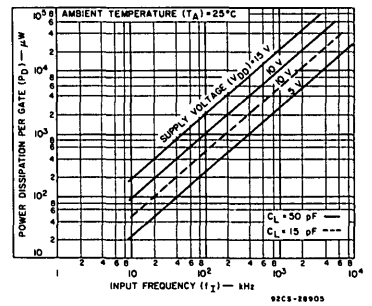


Fig. 2 - Typical power dissipation vs. frequency.

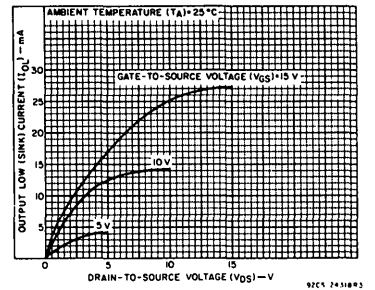


Fig. 3 - Typical output low (sink) current characteristics.

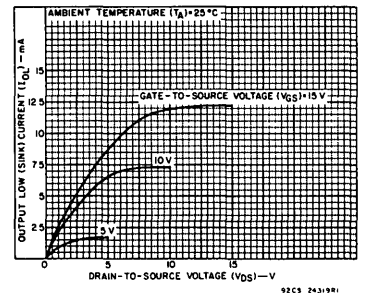


Fig. 5 - Minimum output low (sink) current characteristics

# CD4000B, CD4001B, CD4002B, CD4025B Typ s

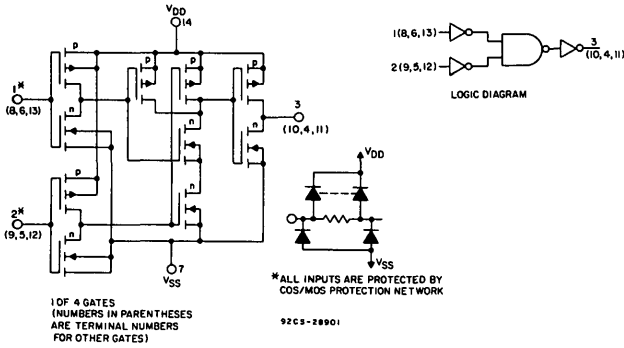


Fig.6 - Schematic and logic diagrams for CD4001B.

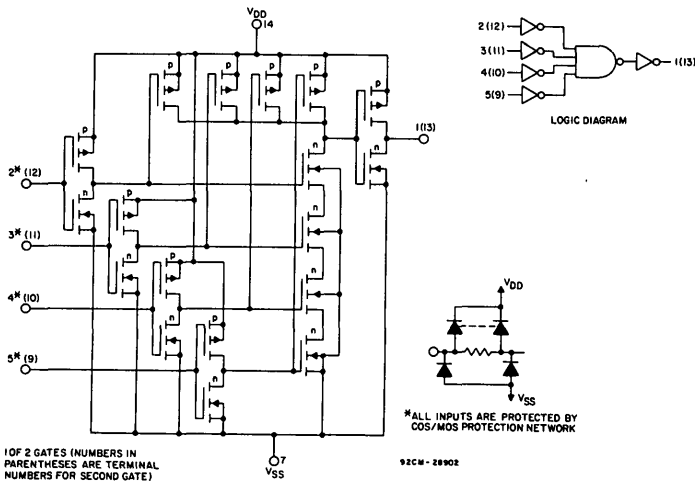


Fig.7 - Schematic and logic diagrams for CD4002B.

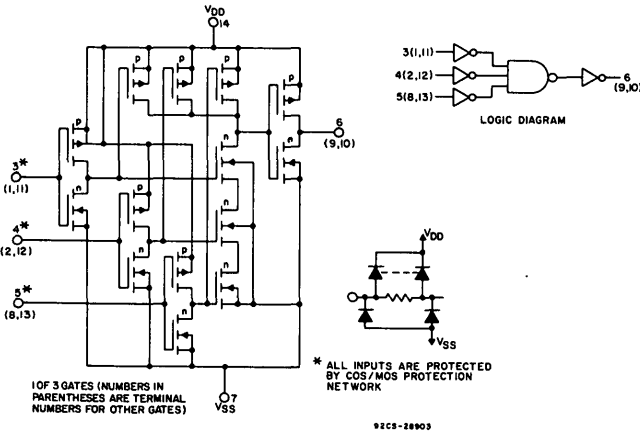


Fig.8 - Schematic and logic diagrams for CD4025B.

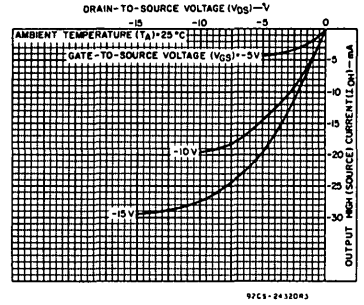


Fig.9 - Typical output high (source) current characteristics.

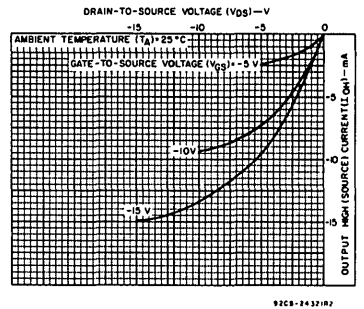


Fig.10 - Minimum output high (source) current characteristics.

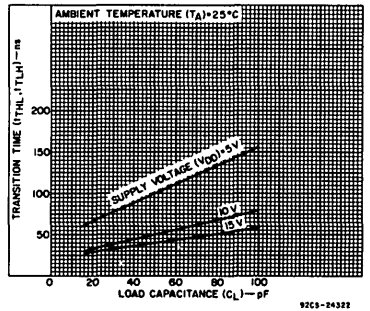


Fig.11 - Typical transition time vs. load capacitance.

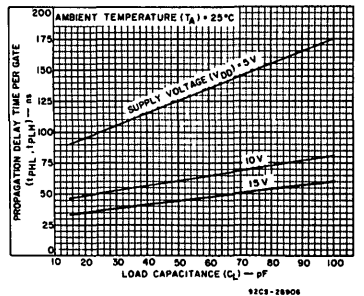


Fig.12 - Typical propagation delay time vs. load capacitance.

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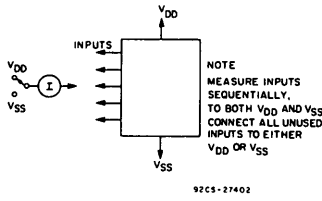


Fig. 13 - Input leakage current test circuit.

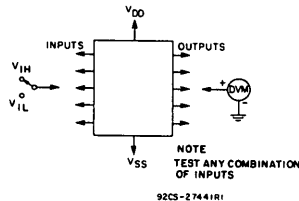


Fig. 14 - Input-voltage test circuit.

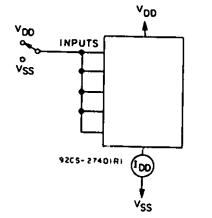
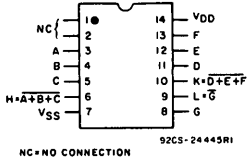
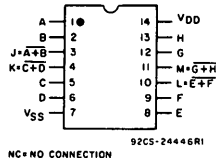


Fig. 15 - Quiescent-device current test circuit.

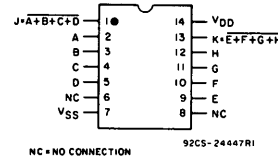
## TERMINAL ASSIGNMENTS (TOP VIEW)



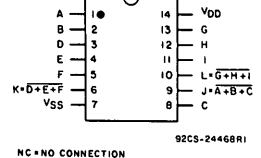
CD4000B



CD4001B

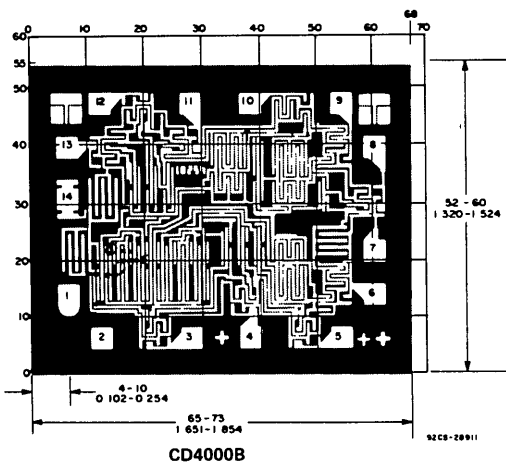


CD4002B

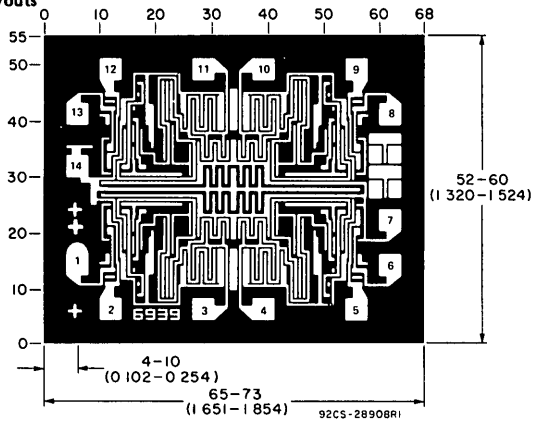


CD4025B

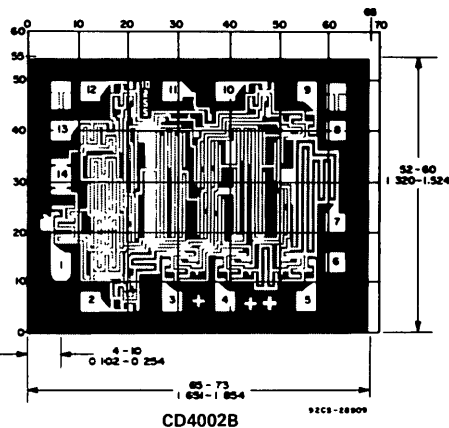
## CHIP PHOTOGRAPHS Dimensions and Pad Layouts



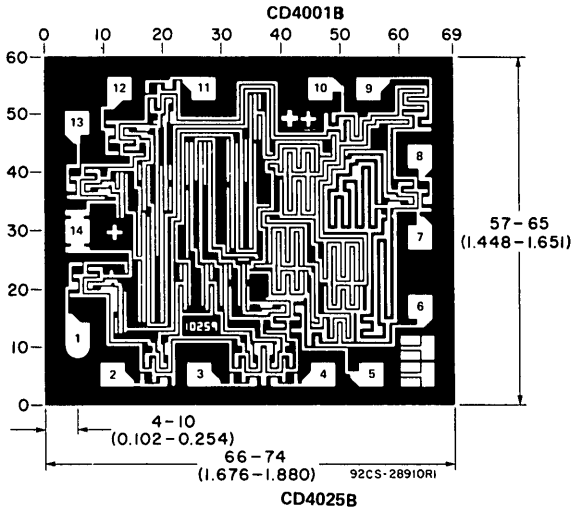
CD4000B



CD4002B



CD4001B



CD4025B